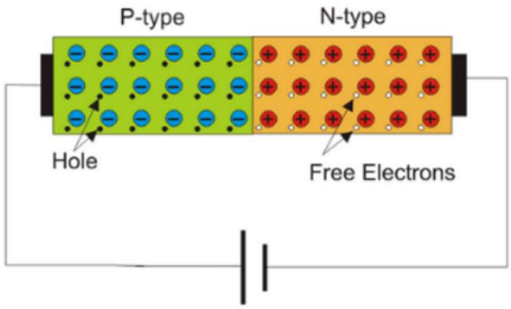
1. Explain VI characteristics PN Junction and write applications Forward Biased PN Junction



A PN junction is said to be forward-biased when the p-type region of a junction is connected to the positive terminal of a voltage source and the n-type region is connected to the voltage source's negative terminal.

In this forward-biased condition, due to the attraction of the positive terminal of the source, electrons that participated in covalent bond creation in the p-type material will be attracted towards the terminal.

As a result, the number of covalent bonds is broken and electrons are shifted towards the positive terminal. This results in the electrons' concentration in the crystal closer to the terminal to increase, and these electrons recombine with holes here. In this way, the number of holes increases in the portion of the p-type region away from the junction, and it is reduced in the portion of the p-type region nearer to the terminal as such holes are shifted from terminal to junction.

Due to the higher concentration of holes adjacent to the negative impurity ions layer, the electrons of negative ions come out and recombine with those holes and create new holes in the layer. Consequently, the width of this negative ions layer is reduced, and finally, this layer vanishes.

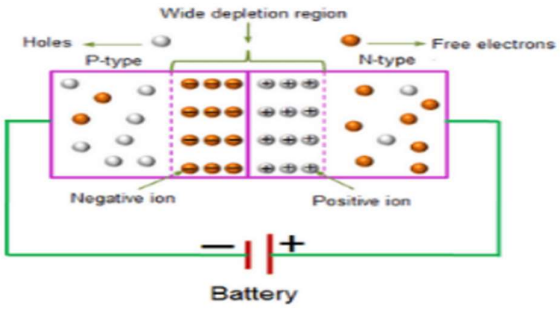
Similarly, due to the negative terminal of the source, the free electrons in the n-type region will repeal towards the junction where they will find the layer of positive impurity ions and start recombine with these ions and generate free electrons inside the layer. Consequently, the width of positive impurity ions is reduced, and finally, it vanishes.

In these ways, both layers of ions disappear, and there will be no more depletion layer. After the depletion layer disappeared, free electrons from the n-type region can easily drift to the p-type region and holes from the p-type region to the n-type region in the crystal. Hence, ideally, there will be no obstruction of flowing current, and the PN junction behaves as the short circuit.

Reverse Biased PN Junction

When the positive terminal of a voltage source is connected to the n-type region and the negative terminal of the source is connected to the p-type region. The PN junction is said to be in reverse biased condition.

When there is no voltage applied across the p n junction, the potential developed across the junction is 0.3 volts at 25ºC for germanium on the junction and 0.7 volts at 25ºC for silicon p n junction. The polarity of this potential barrier is the same as the voltage source's polarity applied during the reverse biased condition. If the reverse biased voltage across the PN junction is increased the barrier potential developed across the PN junction is also increased. Hence, the PN junction is widened.



Reverse bias

When positive terminal of the source is connected to the n-type region, the free electrons of that region are attracted towards the positive terminal of the source because of that more positive impurity ions are created in the depletion layer which makes the layer of positive impurity ions thicker .At the same time since the negative terminal of the source is connected to the p-type region of the junction, electrons are injected in this region.

Although this increment of barrier potential will continue up to applied reverse-biased voltage, if the applied reverse biased voltage is sufficiently high, then the depletion layer will disappear due to Zener breakdown and avalanche breakdowns.

It is also to be noted that after completion of reverse biased depletion layer there is no more drift of charge carriers (electrons and holes) through the junction as the potential barrier opposes the applied voltage which has the same value as the potential barrier.

Although tiny current flow from n-type region to p-type region due to minority carriers that are thermally generated electrons in p-type semiconductor and holes in an n-type semiconductor.

Forward Current in PN Junction:

When the battery voltage is applied across the forward bias junction, a current will flow continuously through this junction.

$$Forward\ biased\ current\ \ i_D = I_s\left(e^{\frac{v_D}{nV_T}} - 1\right)$$

I_S is Saturation Current (10^{-9} to 10^{-18} A)

V_T is Volt-equivalent temperature (= 26 mV at room temperature)

n is the Emission coefficient ($1 \leq n \leq 2$ for Si ICs)

Actually, this expression is approximated.

Reverse Current in PN Junction:

When a p-n junction is connected across a battery in such a manner that its n-type region is connected to the positive potency of the battery and the p-type region is connected to the negative potency of the battery the p n junction is said to be in reverse biased condition.

Ideally, there is no current flowing through the junction. But practically there will be a tiny reverse bias current i_D which is expressed as.

i_D drops to zero value or minimum value. i_D can be written as i_0.

$$Reverse\ biased\ current\ \ i_0 \approx I_s e^{\frac{V_D}{nV_T}}$$

I_S is Saturation Current (10^{-9} to 10^{-18} A)

V_T is Volt-equivalent temperature (= 26 mV at room temperature)

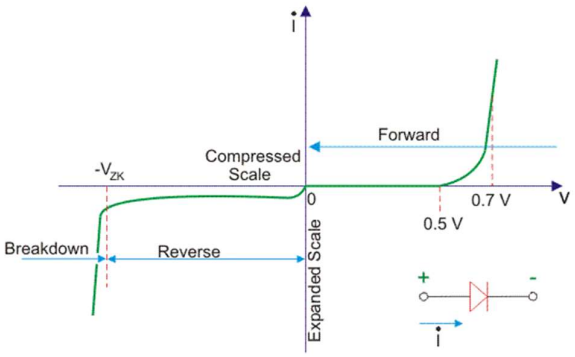
n is the Emission coefficient ($1 \leq n \leq 2$ for Si ICs)
Actually, this expression is approximated.

General Specification of PN Junction

A p-n junction is specified in four manners.

2. Average Forward Current (I_F): It is the forward-biased current due to the drift electron flow or the majority carriers. If the average forward current exceeds its value, the diode gets overheated and may be damaged.
3. Peak Reverse Voltage (V_R): The maximum reverse voltage across the diode at its reverse biased condition. Over this reverse voltage diode will go for breakdown due to its minority carriers.
4. Maximum Power Dissipation (P): It is the product of the forward current and the forward voltage.

V-I Characteristics of A PN Junction



In the forward bias, the operational region is in the first quadrant. The threshold voltage for Germanium is 0.3 V and for Silicon is 0.7 V. Beyond this threshold voltage, the graph goes upward in a non-linear manner. This graph is for the dynamic Resistance of the junction in the forward bias.

In the reverse bias the voltage increases in the reverse direction across the p-n junction, but no current due to the majority carriers, only a minimal leakage current flows. But at a certain reverse voltage p-n junction breaks in conduction.

It is only due to the minority carriers. This amount of voltage is sufficient for these minority carriers to break the depletion region. In this situation, a sharp current will flow through this junction. This breakdown of voltage is of two types.

- Avalanche Breakdown: it is not a sharp graph, rather inclined linear graph, i.e. after the break down a small increase in reverse voltage causes more sharp current gradually.
- Zener Breakdown: This breakdown is sharp and no need to increase reverse bias voltage to get more current, because current flows sharply.

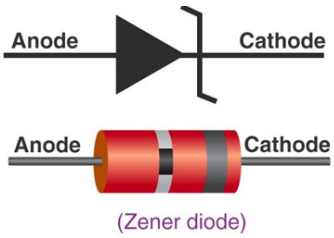
Applications of PN Junction Diode

- p-n junction diode can be used as a photodiode as the diode is sensitive to the light when the configuration of the diode is reverse-biased.
- It can be used as a solar cell.
- When the diode is forward-biased, it can be used in LED lighting applications.
- It is used as rectifiers in many electric circuits and as a voltage-controlled oscillator in varactors.

2. **Explain the working principle of Zener diode and also explain Avalanche Breakdown and Zener Breakdown**

Zener Diode

There are many ways in which a Zener diode is packaged. Some are used for high levels of power dissipation and the others are contained with surface mount formats. The most common type of Zener diode is contained within a small glass encapsulation. It has a band around one end marking the cathode side of the diode.



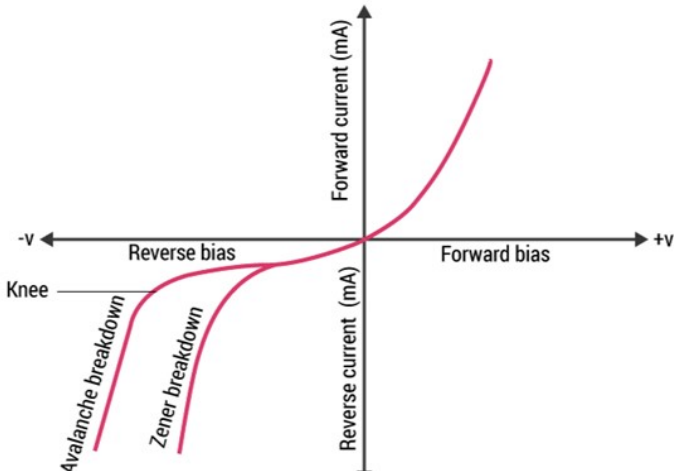
Zener diode symbol and package outlines

From the diagram, we can see that the band around the package corresponds to the line on the diode circuit symbol and this can be an easy way of remembering which end is for which.

The Zener diode circuit symbol places two tags at the end of the bar – one in the upward direction and the other in the lower direction as shown in the figure. This helps in distinguishing Zener diodes from other forms of diodes within the circuit.

V-I Characteristics of Zener Diode:

The diagram given below shows the V-I characteristics of the Zener diode.



When reverse-biased voltage is applied to a Zener diode, it allows only a small amount of leakage current until the voltage is less than Zener voltage.

The V-I characteristics of a Zener diode can be divided into two parts as follows:

(i) Forward Characteristics

(ii) Reverse Characteristics

Forward Characteristics of Zener Diode

The first quadrant in the graph represents the forward characteristics of a Zener diode. From the graph, we understand that it is almost identical to the forward characteristics of any other P-N junction diode.

Reverse Characteristics of Zener Diode

When a reverse voltage is applied to a Zener voltage, initially a small reverse saturation current Io flows across the diode. This current is due to thermally generated minority carriers. As the reverse voltage is increased, at a certain value of reverse voltage, the reverse current increases drastically and sharply. This is an indication that the breakdown has occurred. We call this voltage breakdown voltage or Zener voltage and it is denoted by Vz.

Zener Diode Specifications

Some commonly used specifications for Zener diodes are as follows:

- **Zener/Breakdown Voltage** – The Zener or the reverse breakdown voltage ranges from 2.4 V to 200 V, sometimes it can go up to 1 kV while the maximum for the surface-mounted device is 47 V.
- **Current Iz (max)** – It is the maximum current at the rated Zener Voltage (Vz – 200μA to 200 A)
- **Current Iz (min)** – It is the minimum value of current required for the diode to breakdown.
- **Power Rating** – It denotes the maximum power the Zener diode can dissipate. It is given by the product of the voltage of the diode and the current flowing through it.
- **Temperature Stability** – Diodes around 5 V have the best stability
- **Voltage Tolerance** – It is typically ±5%
- **Zener Resistance (Rz)** – It is the resistance to the Zener diode exhibits

Avalanche Breakdown in Zener Diode

Avalanche breakdown occurs both in normal diode and Zener Diode at high reverse voltage. When a high value of reverse voltage is applied to the PN junction, the free electrons gain sufficient energy and accelerate at high velocities. These free electrons moving at high velocity collides other atoms and knocks off more electrons. Due to this continuous collision, a large number of free electrons are generated as a result of electric current in the diode rapidly increases. This sudden increase in electric current may permanently destroy the normal diode, however, a Zener diode is designed to operate under avalanche breakdown and can sustain the sudden spike of current. Avalanche breakdown occurs in Zener diodes with Zener voltage (Vz) greater than 6V.

Zener Breakdown in Zener Diode

When the applied reverse bias voltage reaches closer to the Zener voltage, the electric field in the depletion region gets strong enough to pull electrons from their valence band. The valence electrons that gain sufficient energy from the strong electric field of the depletion region break free from the parent atom. At the Zener breakdown region, a small increase in the voltage results in the rapid increase of the electric current.

Avalanche Breakdown vs Zener Breakdown

- The Zener effect is dominant in voltages up to 5.6 volts and the avalanche effect takes over above that.
- They are both similar effects, the difference being that the Zener effect is a quantum phenomenon and the avalanche effect is the movement of electrons in the valence band like in any electric current.
- Avalanche effect also allows a larger current through the diode than what a Zener breakdown would allow.

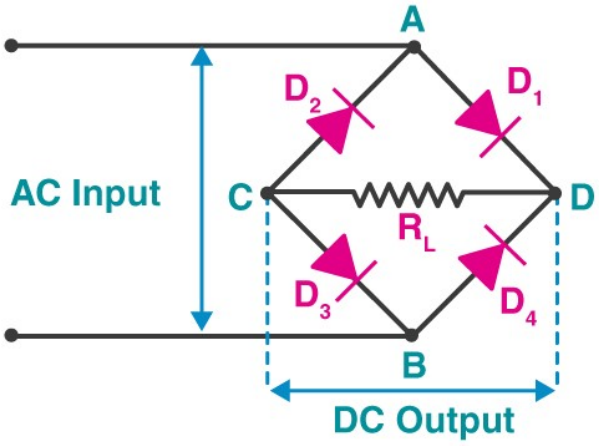
3. Explain the operation of full wave Rectifier and also obtain the expression RMS current ,RMS Voltage, PIV, TUF, Efficiency and Ripple factor?

Many electronic circuits require a rectified DC power supply to power various electronic basic components from the available AC mains supply. Rectifiers are used to convert an AC power to a DC power. Among the rectifiers, the bridge rectifier is the most efficient rectifier circuit.

We can define bridge rectifiers as a type of full-wave rectifier that uses four or more diodes in a bridge circuit configuration to efficiently convert alternating (AC) current to a direct (DC) current. In the next few sections, let us learn more about its construction, working, and more.

Construction

The construction of a bridge rectifier is shown in the figure below. The bridge rectifier circuit is made of four diodes D_1, D_2, D_3, D_4, and a load resistor R_L. The four diodes are connected in a closed-loop configuration to efficiently convert the alternating current (AC) into Direct Current (DC). The main advantage of this configuration is the absence of the expensive center-tapped transformer. Therefore, the size and cost are reduced.

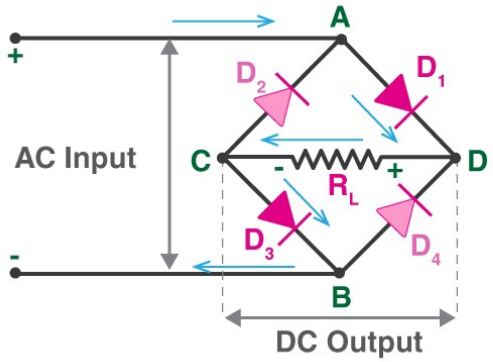


The input signal is applied across terminals A and B and the output DC signal is obtained across the load resistor R_L connected between terminals C and D. The four diodes are arranged in such a way that only two diodes conduct electricity during each half cycle. D_1 and D_3 are pairs that conduct electric current during the positive half cycle/. Likewise, diodes D_2 and D_4 conduct electric current during a negative half cycle.

Working

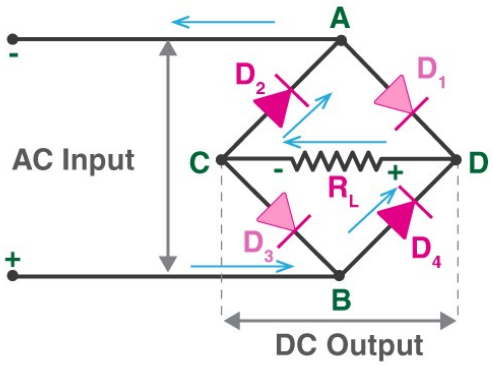
When an AC signal is applied across the bridge rectifier, during the positive half cycle, terminal A becomes positive while terminal B becomes negative. This results in diodes D_1 and D_3 to become forward biased while D_2 and D_4 become reverse biased.

The current flow during the positive half-cycle is shown in the figure below:



During the negative half-cycle, terminal B becomes positive while the terminal A becomes negative. This causes diodes D_2 and D_4 to become forward biased and diode D_1 and D_3 to be reverse biased.

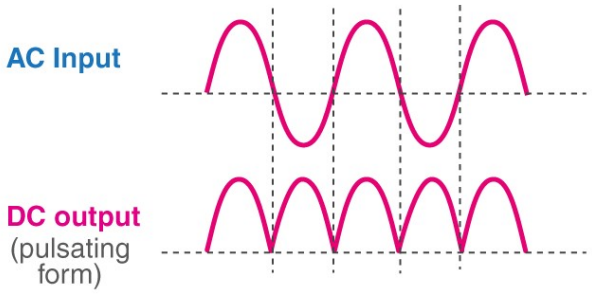
The current flow during the negative half cycle is shown in the figure below:



From the figures given above, we notice that the current flow across load resistor R_L is the same during the positive half cycle and the negative half cycles. The output DC signal polarity may be either completely positive or negative. In our case, it is completely positive. If the direction of diodes is reversed then we get a complete negative DC voltage.

Thus, a bridge rectifier allows electric current during both positive and negative half cycles of the input AC signal.

The output waveforms of the bridge rectifier are shown in the below figure.



$$Average\ Value = (\frac{1}{\pi}) \int_0^{\pi} Imsin\omega t d(wt)$$

$$= (\frac{Im}{\pi}) \int_0^{\pi} sin\omega t d(wt)$$

$$= \left(\frac{Im}{\pi}\right)[cos0 - cos\pi]$$

$$= (2\frac{Im}{\pi})$$

$$= 0.637Im$$

$$RMS\ Value = \sqrt{(\frac{1}{\pi}) \int_0^{\pi} (Imsin\omega t)^2 d(\omega t)}$$

$$= Im \sqrt{(\frac{1}{2\pi}) \int_0^{\pi} 2(sin\omega t)^2 d(\omega t)}$$

$$= Im \sqrt{(\frac{1}{2\pi}) \int_0^{\pi} (1 - cos\omega t) d(\omega t)}$$

$$= Im \sqrt{\left(\frac{1}{2\pi}\right)[\pi - 0]}$$

$$= \frac{Im}{\sqrt{2}}$$

$$Ripple\ Factor = \frac{\sqrt{(Irms)^2 - (Idc)^2}}{Idc}$$

$$= \frac{\sqrt{(0.707Im)^2 - (0.637Im)^2}}{(0.637Im)}$$

$$= \frac{\sqrt{(0.707Im)^2 - (0.637Im)^2}}{(0.637Im)}$$

$$= 0.482$$

Form Factor = RMS value / Average value

$$= (0.707I_m / 0.637I_m)$$

$$= 1.11$$

$$\Rightarrow \eta = \frac{P_{DC}}{P_{AC}}$$

$$\Rightarrow \eta = \frac{\frac{{V_{DC}}^2}{R_L}}{\frac{{V_{RMS}}^2}{R_L}} = \frac{{V_{DC}}^2}{{V_{RMS}}^2}$$

By putting value of V_{DC} and V_{RMS} we have,

$$\Rightarrow \eta = \frac{\left[2V_M/\pi\right]^2}{\left[V_M/\sqrt{2}\right]^2}$$

$$\Rightarrow \eta = \frac{8}{\pi^2} = 0.812$$

To calculate in percentage we just need to multiply by 100 so we have,

$$\Rightarrow \eta = 0.812 \times 100 = 81.2$$

$$\Rightarrow \eta = 81.2$$

The peak inverse voltage of diode in bridge rectifier is equal to the peak value of supply voltage

4. **Explain the operation of half wave Rectifier and also obtain the expression RMS current ,RMS Voltage, PIV, TUF, Efficiency and Ripple factor?**

Defining Half Wave Rectifier

Half-wave rectifiers transform AC voltage to DC voltage. A halfwave rectifier circuit uses only one diode for the transformation.

A halfwave rectifier is defined as a type of rectifier that allows only one-half cycle of an AC voltage waveform to pass while blocking the other half cycle.

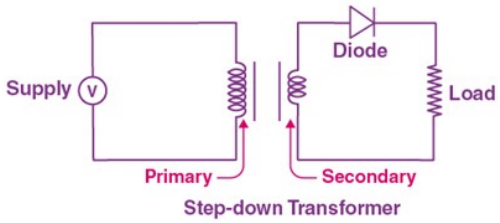
Half Wave Rectifier Circuit

A half-wave rectifier is the simplest form of the rectifier and requires only one diode for the construction of a halfwave rectifier circuit.

A halfwave rectifier circuit consists of three main components as follows:

- A diode
- A transformer
- A resistive load

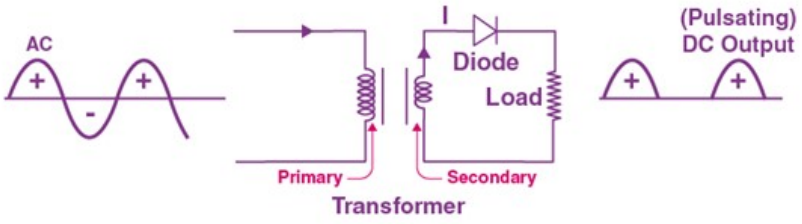
Given below is the half-wave rectifier diagram:



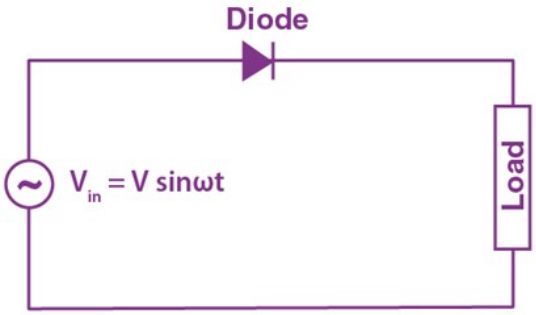
Working of Half Wave Rectifier

In this section, let us understand how a half-wave rectifier transforms AC into DC.

1. A high AC voltage is applied to the primary side of the step-down transformer. The obtained secondary low voltage is applied to the diode.
2. The diode is forward biased during the positive half cycle of the AC voltage and reverse biased during the negative half cycle.
3. The final output voltage waveform is as shown in the figure below:

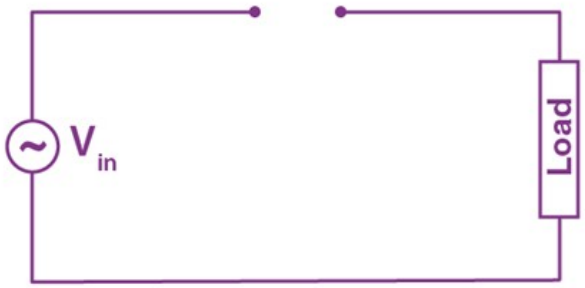


For better understanding, let us simplify the half-wave circuit by replacing the secondary transformer coils with a voltage source as shown below:



For the positive half cycle of the AC source voltage, the circuit effectively becomes as shown below in the diagram:

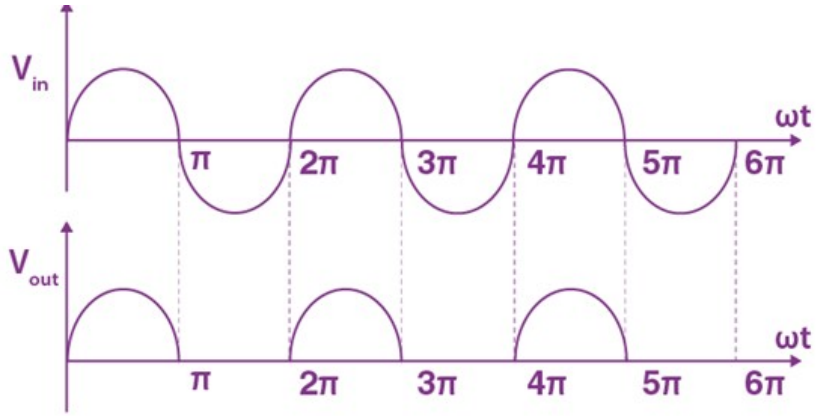
When the diode is forward biased, it acts as a closed switch. But, during the negative half cycle of the AC source voltage, the equivalent circuit becomes as shown in the figure below



When a diode is reverse biased, it acts as an open switch. Since no current can flow to the load, the output voltage is equal to zero.

Half Wave Rectifier Waveform

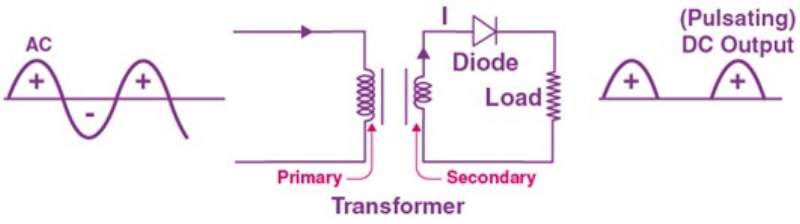
The halfwave rectifier waveform before and after rectification is shown below in the figure.



Half Wave Rectifier Capacitor Filter

The output waveform of a halfwave rectifier is a pulsating DC waveform. Filters in halfwave rectifiers are used to transform the pulsating waveform into constant DC waveforms. A capacitor or an inductor can be used as a filter.

The circuit diagram below shows how a capacitive filter is used with halfwave rectifier to smoothen out a pulsating DC waveform into a constant DC waveform.



$$Average\ Output\ Current$$

$$= \left(\frac{1}{2\pi}\right)\left[\int_0^{\pi} ImSin\omega td(wt) + \int_{\pi}^{2\pi} 0d(\omega t)\right]$$

$$= \left(\frac{1}{2\pi}\right)\int_0^{\pi} ImSin\omega td(wt)$$

$$= \left(\frac{Im}{2\pi}\right)\int_0^{\pi} Sin\omega td(wt)$$

$$= \left(\frac{-Im}{2\pi}\right)[cos\pi - cos0]$$

$$= \left(\frac{Im}{\pi}\right)$$

$$RMS\ Value = \sqrt{\left(\frac{1}{2\pi}\right)\int_0^{\pi}(Imsin\omega t)^2 d(\omega t) + \left(\frac{1}{2\pi}\right)\int_{\pi}^{2\pi} 0\, d\omega t}$$

$$= \sqrt{\left(\frac{Im^2}{2\pi}\right)\int_0^{\pi}(sin\omega t)^2 d(\omega t)}$$

$$= Im\sqrt{\left(\frac{1}{4\pi}\right)\int_0^{\pi}2(sin\omega t)^2\, d(\omega t)}$$

$$= \left(\frac{Im}{2}\right)\sqrt{\left(\frac{1}{\pi}\right)\int_0^{\pi}(1 - cos\omega t)\, d(\omega t)}$$

$$= \left(\frac{Im}{2}\right)\sqrt{\left(\frac{1}{\pi}\right)\left[\int_0^{\pi} 1 d(\omega t) - \int_0^{\pi} cos\omega t\, d(\omega t)\right]}$$

$$= \left(\frac{Im}{2}\right)\sqrt{\left(\frac{1}{\pi}\right)[\pi - 0)]}$$

$$= \frac{Im}{2}$$

$$\textbf{Ripple Factor}, \boldsymbol{\gamma} = \frac{\sqrt{(\boldsymbol{Irms})^2 - (\boldsymbol{Idc})^2}}{\boldsymbol{Idc}}$$

$$= \frac{\sqrt{(\boldsymbol{Vrms})^2 - (\boldsymbol{Vdc})^2}}{\boldsymbol{Vdc}}$$

$$Ripple\ Factor = \frac{\sqrt{(0.5Im)^2 - (0.318Im)^2}}{0.318Im}$$

$$= 1.21$$

$$\Rightarrow \eta\% = \frac{P_{DC}}{P_{AC}} \times 100$$

Putting the values of both the power terms in the above equation, we get:

$$\Rightarrow \eta\% = \frac{\left(\frac{\left(\frac{I_m}{\pi}\right)^2}{R}\right)}{\left(\frac{\left(\frac{I_m}{2}\right)^2}{R}\right)} \times 100$$

$$\Rightarrow \eta\% = \frac{4}{\pi^2} \times 100$$

Here, we can estimate the value of pi squared as 10. This will give us the efficiency as:

$$\Rightarrow \eta\% \approx \frac{4}{10} \times 100$$

$$\Rightarrow \eta\% \approx 40$$

$$\therefore \eta \approx 40\%$$

Hence, the efficiency of a half-wave rectifier is nearly 40%.

i.e. $$TUF = \frac{dc - power - delivered - the - load}{ac - rating - of - the - transformer - secondary} \quad .....(22)$$

Hence, $$TUF = \frac{P_{dc}}{P_{ac}(rating)} = \frac{(\frac{I_m}{\pi})^2 R_L}{(\frac{V_m}{\sqrt{2}})(\frac{I_m}{\sqrt{2}})} \quad .....(23)$$

But, $V_m = I_m(R_f + R_L)$

Hence, $$TUF = \frac{0.286 R_L}{R_f + R_L} \quad .....(24)$$

If $R_L \gg R_f, TUF = 0.286$

Half Wave Rectifier Formulae

Efficiency of HWR

The efficiency of HWR is defined as the ration output DC power to the input AC power.

$$\eta = \frac{P_{dc}}{P_{ac}}$$

The maximum efficiency of half wave rectifier is 40.6%.

Peak Inverse Voltage of HWR

The peak inverse voltage of a HWR is the maximum voltage that can a diode withstand without destruction when reverse bias is applied to it.

$$\text{PIV} = V_m$$

RMS Value of Load Current of HWR

$$I_{RMS} = \frac{I_m}{2}$$

Average Value of Load Current of HWR

$$I_{avg} = \frac{I_m}{\pi}$$

Form Factor of HWR

$$\text{Form Factor} = \frac{\text{RMS Value}}{\text{Avg. Value}} = \frac{V_{\text{rms}}}{V_{\text{avg}}}$$

For HWR the form factor equals to 1.57

Ripple Factor of HWR

Ripple Factor gives the information about how a HWR can transform input AC voltage to output DC voltage. It is given by

$$\text{Ripple Factor} = \sqrt{((\text{Form Factor})^2 - 1)}$$

The ripple factor for half wave rectifier is 1.21.

Application of Half Wave Rectifier

There are some applications of Half Wave Rectifier −

- They are used for rectification
- They are used for demodulation
- They are used for signal peak applications

Disadvantages of Half Wave Rectifier

- The AC supply delivers power only for the half cycle. Therefore, the output is low.
- The pulsating current in the load contains alternating current whose frequency is equal to supply frequency. Therefore, filtering is required to produce steady direct current.

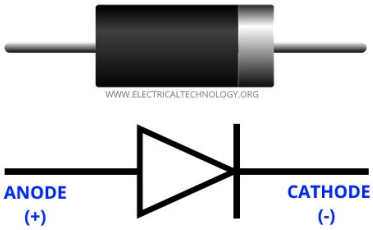
5. Explain the working principle of PN Junction diode and mention the application

"Di "= Two, *and "***Ode "= Electrodes** *i.e a device or component having two electrodes viz Anode "+" (P) and Cathode "-" (N).*

A diode is a two-terminal unidirectional power electronics device. The semiconductor diode is the first invention in a family of semiconductor electronics devices. After that many types of diodes are invented. But today also the most commonly used diode is a semiconductor diode. Generally, silicon is used to make a diode. But another semiconductor material like germanium or germanium arsenide is also used.

A diode allows current to flow only in one direction and it blocks the current in another direction. It offers low resistance (ideally zero) in one direction and it offers a high resistance (ideally infinite) in another direction.

Symbol of Diode



- **Related Post:** ***Different types of Diodes Symbols***

Construction of Diode

There are two types of semiconductor material; Intrinsic and Extrinsic semiconductor. An intrinsic semiconductor is a pure semiconductor in which hole and electrons are available in equal numbers at room temperature. In an extrinsic semiconductor, impurities are added to increase the number of holes or the number of electrons. These impurities are tri-valent (boron, indium, aluminum) or pentavalent (phosphorous, Arsenic, Antimony).

A semiconductor diode has two layers. One layer is made of a P-type semiconductor layer and the second layer is made of an N-type semiconductor layer.

If we add trivalent impurities in silicon or germanium, a greater number of holes are present and it is a positive charge. Hence, this layer is known as the P-type layer.

If we add pentavalent impurities in silicon or germanium, a greater number of electrons are present and it is a negative change. Hence, this layer is known as the N-type layer.

The diode is formed by joining both N-type and P-type semiconductors together. This device is a combination of P-type and N-type semiconductor material hence it is **also known as PN Junction Diode**.

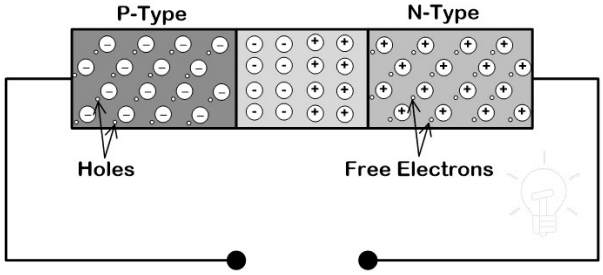
A junction is formed between the P-type and N-type layers. This junction is known as PN junction.

A diode has two terminals; one terminal is taken from the P-type layer and it is known as Anode. The second terminal is taken from the N-type material and it is known as Cathode.

The below figure shows the basic construction of the diode.

Working of Diode

In the N-type region, electrons are the majority charge carriers and holes are minority charge carriers. In the P-type region, the holes are majority charge carrier and the electrons are negative charge carriers. Because of the concentration difference, majority charge carriers diffuse and recombine with the opposite charge. It makes a positive or negative ion. These ions are collected at the junction. And this region is known as the depletion region.



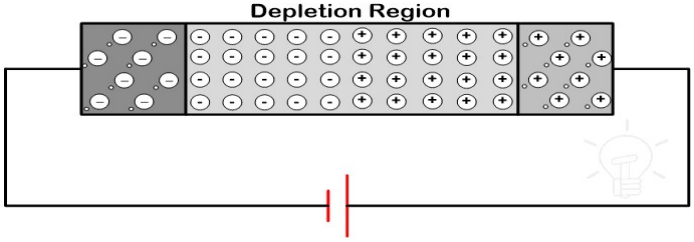
When anode terminal of diode is connected with a negative terminal and cathode is connected with the positive terminal of a battery, the diode is said to be connected in reverse bias.

Similarly, when anode terminal is connected with a positive terminal and cathode is connected with the negative terminal of the battery, the diode is said to be connected in forward bias.

Operation of Diode in Reverse Bias Condition

The diode is connected in reverse bias. In this condition, free electrons diffusing into the P-type regions and recombine with holes. It will create negative ions. Similarly, holes diffuse into the N-type region and recombine with electrons. It will create positive ions.

The connection diagram is as shown in the below figure.



When such voltage is applied to the circuit, immobile ions create a depletion region as shown in the above figure. The width of the depletion region is large. Hence, no more hole or electron crosses the junction.

It cannot create a flow of electrons or holes even if it is supplied at rated voltage. Hence, it is not possible to flow the current through the diode and it behaves as an open switch.

Here a very small amount of current will flow through the circuit. This current is known as reverse saturation current or reverses leakage current. This current flow due to the minority charge carriers. This current is not high enough to conduct the diode.

If we increase the voltage up to reverse breakover voltage, the minority charge carriers get high kinetic energy and collide with atoms. In this condition, the number of covalent bonds broken and a huge number of electrons-holes pair generates a huge amount of flow of current.

Due to this high amount of current, a diode may get damaged. Hence, in general condition, the diode is not connected in reverse bias.

Operation of Diode in Forward Bias Condition

When the anode is connected with the positive terminal of the battery and cathode is connected with a negative terminal of the battery, the anode is positive with respect to the cathode. And the diode is said to be connected in forward bias.

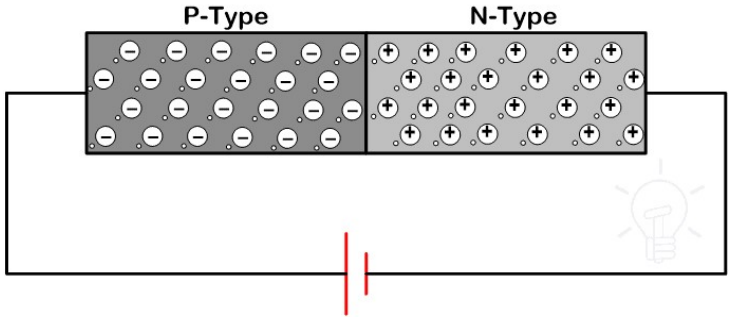
Now, we gradually increase the supply voltage. If we increase a small voltage, the majority charge carrier does not get sufficient energy to cross the depletion region.

In the forward bias conditions, the width of the depletion region is very small. If we increase the voltage more than forward breakover voltage, the majority charge carrier gets enough energy to cross the depletion region.

For silicon forward breakover voltage is 0.7V and for germanium forward breakover voltage is 0.3V.

When supply voltage increases more than this voltage, the majority charge carriers flowing through the circuit and it made the diode conducting.

In this mode of operation, a very small amount of drop occurs. This drop is known as an on-state voltage drop. The connection diagram of this mode is as shown in the below figure.



Applications of PN Junction Diode

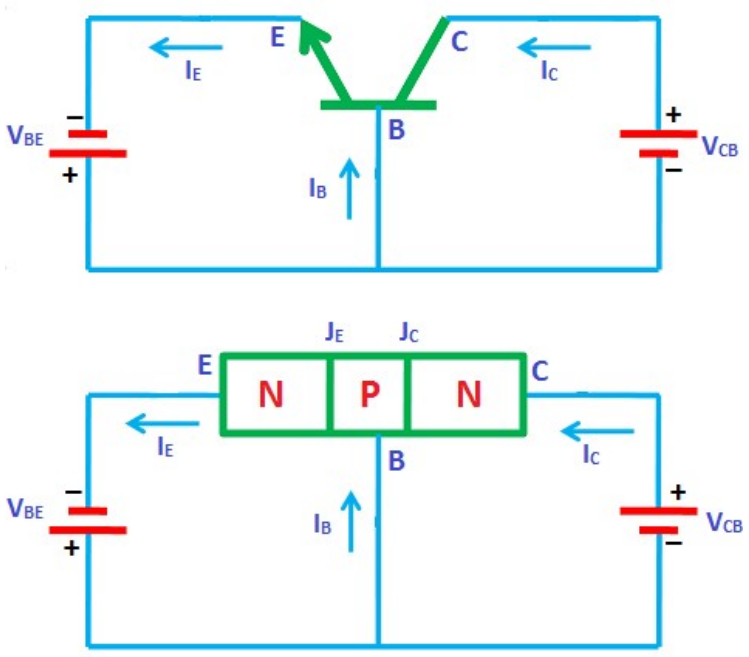
- p-n junction diode can be used as a photodiode as the diode is sensitive to the light when the configuration of the diode is reverse-biased.
- It can be used as a solar cell.
- When the diode is forward-biased, it can be used in LED lighting applications.
- It is used as rectifiers in many electric circuits and as a voltage-controlled oscillator in varactors.

6. Explain the working of Common Base Configuration of NPN Transistor

Common Base Configuration

In common base configuration, emitter is the input terminal, collector is the output terminal and base terminal is connected as a common terminal for both input and output. That means the emitter terminal and common base terminal are known as input terminals whereas the collector terminal and common base terminal are known as output terminals.

In common base configuration, the base terminal is grounded so the common base configuration is also known as grounded base configuration. Sometimes common base configuration is referred to as common base amplifier, CB amplifier, or CB configuration.



Common base configuration

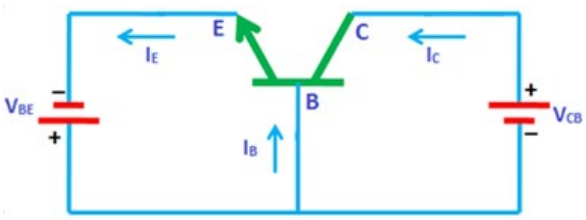
The input signal is applied between the emitter and base terminals while the corresponding output signal is taken across the collector and base terminals. Thus the base terminal of a

transistor is common for both input and output terminals and hence it is named as common base configuration.

The supply voltage between base and emitter is denoted by V_{BE} while the supply voltage between collector and base is denoted by V_{CB}.

As mentioned earlier, in every configuration, the base-emitter junction J_E is always forward biased and collector-base junction J_C is always reverse biased. Therefore, in common base configuration, the base-emitter junction J_E is forward biased and collector-base junction J_C is reverse biased.

The common base configuration for NPN is shown in the below figure.



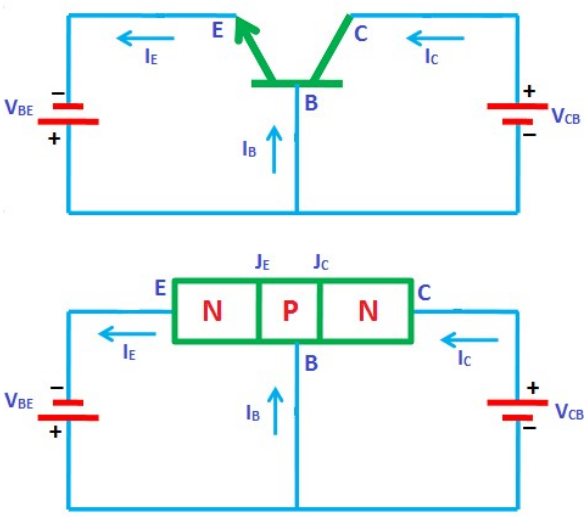
NPN Transistor

From the above circuit diagrams of npn transistors, it can be seen that for npn transistors, the input is applied to the emitter and the output is taken from the collector. The common terminal for both the circuits is the base.

Current flow in common base amplifier

For the sake of understanding, let us consider NPN transistor in common base configuration.

The npn transistor is formed when a single p-type semiconductor layer is sandwiched between two n-type semiconductor layers.

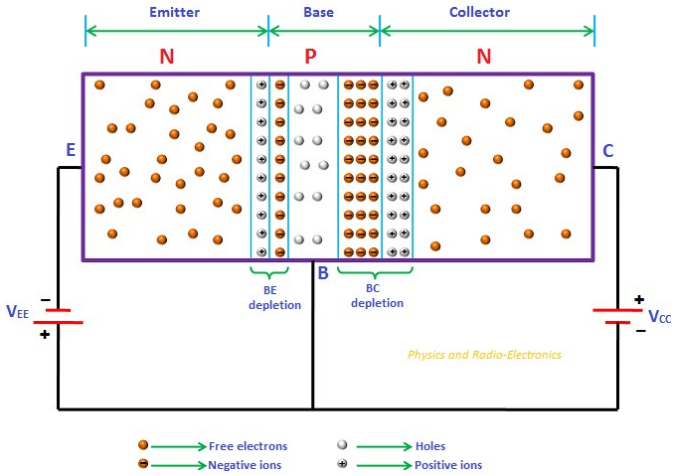


Common base configuration

The base-emitter junction J_E is forward biased by the supply voltage V_{BE} while the collector-base junction J_C is reverse biased by the supply voltage V_{CB}.

Due to the forward bias voltage V_{BE}, the free electrons (majority carriers) in the emitter region experience a repulsive force from the negative terminal of the battery similarly holes (majority carriers) in the base region experience a repulsive force from the positive terminal of the battery.

As a result, free electrons start flowing from emitter to base similarly holes start flowing from base to emitter. Thus free electrons which are flowing from emitter to base and holes which are flowing from base to emitter conducts electric current. The actual current is carried by free electrons which are flowing from emitter to base. However, we follow the conventional current direction which is from base to emitter. Thus electric current is produced at the base and emitter region.



The free electrons which are flowing from emitter to base will combine with the holes in the base region similarly the holes which are flowing from base to emitter will combine with the electrons in the emitter region.

From the above figure, it is seen that the width of the base region is very thin. Therefore, only a small percentage of free electrons from emitter region will combine with the holes in the base region and the remaining large number of free electrons cross the base region and enters into the collector region. A large number of free electrons which entered into the collector region will experience an attractive force from the positive terminal of the battery. Therefore, the free electrons in the collector region will flow towards the positive terminal of the battery. Thus, electric current is produced in the collector region.

The electric current produced at the collector region is primarily due to the free electrons from the emitter region similarly the electric current produced at the base region is also primarily due to the free electrons from emitter region. Therefore, the emitter current is greater than the base current and collector current. The emitter current is the sum of base current and collector current.

$$I_E = I_B + I_C$$

We know that emitter current is the input current and collector current is the output current.

The output collector current is less than the input emitter current, so the current gain of this amplifier is actually less than 1. In other words, the common base amplifier attenuates the electric current rather than amplifying it.

The base-emitter junction J_E at input side acts as a forward biased diode. So the common base amplifier has a low input impedance (low opposition to incoming current). On the other hand, the collector-base junction J_C at output side acts somewhat like a reverse biased diode. So the common base amplifier has high output impedance.

Therefore, the common base amplifier provides a low input impedance and high output impedance. Transistors with low input impedance and high output impedance provide a high voltage gain. Even though the voltage gain is high, the current gain is very low and the overall power gain of the common base amplifier is low as compared to the other transistor amplifier configurations.

The common base transistor amplifiers are primarily used in the applications where low input impedance is required. The common base amplifier is mainly used as a voltage amplifier or current buffer. This type of transistor arrangement is not very common and is not as widely used as the other two transistor configurations.

The working principle of pnp transistor with CB configuration is same as the npn transistor with CB configuration. The only difference is in npn transistor free electrons conduct most of the current whereas in pnp transistor the holes conduct most of the current.

Total collector current,

$$I_C = \alpha I_E + I_{leakage}$$

The above expression shows that if $I_E = 0$ (when the emitter circuit is open) then still a small current flow in the collector circuit called leakage current. This leakage current is represented by as I_{CBO}, i.e., collector-base current with emitter circuit is open.

$$I_C = \alpha I_E + I_{CBO}$$

The leakage current is also abbreviated as I_{CO} i.e., the collector current with emitter circuit open.

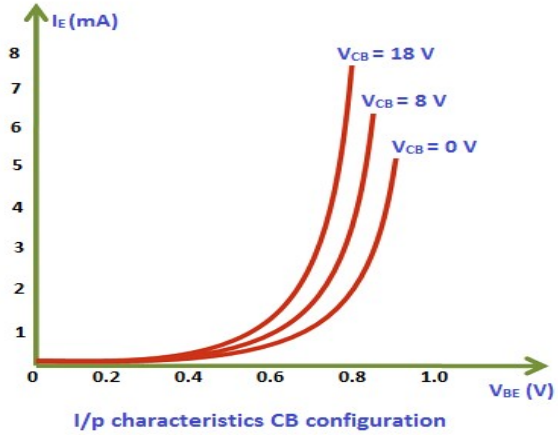
To fully describe the behavior of a transistor with CB configuration, we need two set of characteristics: they are

- Input characteristics
- Output characteristics.

Input characteristics

The input characteristics describe the relationship between input current (I_E) and the input voltage (V_{BE}).First, draw a vertical line and horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The input current or emitter current (I_E) is taken along the y-axis (vertical line) and the input voltage (V_{BE}) is taken along the x-axis (horizontal line).

To determine the input characteristics, the output voltage V_{CB} (collector-base voltage) is kept constant at zero volts and the input voltage V_{BE} is increased from zero volts to different voltage levels. For each voltage level of the input voltage (V_{BE}), the input current (I_E) is recorded on a paper or in any other form.A curve is then drawn between input current I_E and input voltage V_{BE} at constant output voltage V_{CB} (0 volts).



I/p characteristics CB configuration

Next, the output voltage (V_{CB}) is increased from zero volts to a certain voltage level (8 volts) and kept constant at 8 volts. While increasing the output voltage (V_{CB}), the input voltage (V_{BE}) is kept constant at zero volts. After we kept the output voltage (V_{CB}) constant at 8 volts, the input voltage V_{BE} is increased from zero volts to different voltage levels. For each voltage level of the input voltage (V_{BE}), the input current (I_E) is recorded on a paper or in any other form.A curve is then drawn between input current I_E and input voltage V_{BE} at constant output voltage V_{CB} (8 volts).This is repeated for higher fixed values of the output voltage (V_{CB}).

When output voltage (V_{CB}) is at zero volts and emitter-base junction J_E is forward biased by the input voltage (V_{BE}), the emitter-base junction acts like a normal p-n junction diode. So the input characteristics are same as the forward characteristics of a normal pn junction diode.

The cut in voltage of a silicon transistor is 0.7 volts and germanium transistor is 0.3 volts. In our case, it is a silicon transistor. So from the above graph, we can see that after 0.7 volts, a small increase in input voltage (V_{BE}) will rapidly increase the input current (I_E).

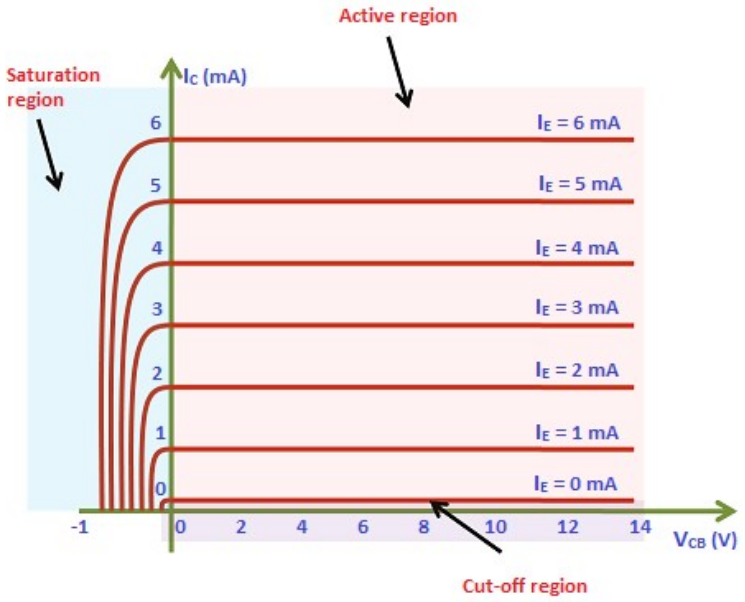
When the output voltage (V_{CB}) is increased from zero volts to a certain voltage level (8 volts), the emitter current flow will be increased which in turn reduces the depletion region width at emitter-base junction. As a result, the cut in voltage will be reduced. Therefore, the curves shifted towards the left side for higher values of output voltage V_{CB}.

Output characteristics

The output characteristics describe the relationship between output current (I_C) and the output voltage (V_{CB}).First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The output current or collector current (I_C) is taken along the y-axis (vertical line) and the output voltage (V_{CB}) is taken along the x-axis (horizontal line).

To determine the output characteristics, the input current or emitter current I_E is kept constant at zero mA and the output voltage V_{CB} is increased from zero volts to different voltage levels. For each voltage level of the output voltage V_{CB}, the output current (I_C) is recorded.

A curve is then drawn between output current I_C and output voltage V_{CB} at constant input current I_E (0 mA). When the emitter current or input current I_E is equal to 0 mA, the transistor operates in the cut-off region.



O/P characteristics CB configuration

Next, the input current (I_E) is increased from 0 mA to 1 mA by adjusting the input voltage V_{BE} and the input current I_E is kept constant at 1 mA. While increasing the input current I_E, the output voltage V_{CB} is kept constant.

After we kept the input current (I_E) constant at 1 mA, the output voltage (V_{CB}) is increased from zero volts to different voltage levels. For each voltage level of the output voltage (V_{CB}), the output current (I_C) is recorded. A curve is then drawn between output current I_C and output voltage V_{CB} at constant input current I_E (1 mA). This region is known as the active region of a transistor. This is repeated for higher fixed values of input current I_E (I.e. 2 mA, 3 mA, 4 mA and so on).

From the above characteristics, we can see that for a constant input current I_E, when the output voltage V_{CB} is increased, the output current I_C remains constant.At saturation region, both emitter-base junction J_E and collector-base junction J_C are forward biased. From the above graph, we can see that a sudden increase in the collector current when the output voltage V_{CB} makes the collector-base junction J_C forward biased.

Early effect

Due to forward bias, the base-emitter junction J_E acts as a forward biased diode and due to reverse bias, the collector-base junction J_C acts as a reverse biased diode.

Therefore, the width of the depletion region at the base-emitter junction J_E is very small whereas the width of the depletion region at the collector-base junction J_C is very large.

If the output voltage V_{CB} applied to the collector-base junction J_C is further increased, the depletion region width further increases. The base region is lightly doped as compared to the collector region. So the depletion region penetrates more into the base region and less into the collector region. As a result, the width of the base region decreases. This dependency of base width on the output voltage (V_{CB}) is known as an early effect.

If the output voltage V_{CB} applied to the collector-base junction J_C is highly increased, the base width may be reduced to zero and causes a voltage breakdown in the transistor. This phenomenon is known as punch through.

Transistor parameters

Dynamic input resistance (r_i)

Dynamic input resistance is defined as the ratio of change in input voltage or emitter voltage (V_{BE}) to the corresponding change in input current or emitter current (I_E), with the output voltage or collector voltage (V_{CB}) kept at constant.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_E}, \qquad V_{CB} = \text{constant}$$

The input resistance of common base amplifier is very low.

Dynamic output resistance (r_o)

Dynamic output resistance is defined as the ratio of change in output voltage or collector voltage (V_{CB}) to the corresponding change in output current or collector current (I_C), with the input current or emitter current (I_E) kept at constant.

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C}, \qquad I_E = \text{constant}$$

The output resistance of common base amplifier is very high.

Current gain (α)

The current gain of a transistor in CB configuration is defined as the ratio of output current or collector current (I_C) to the input current or emitter current (I_E).

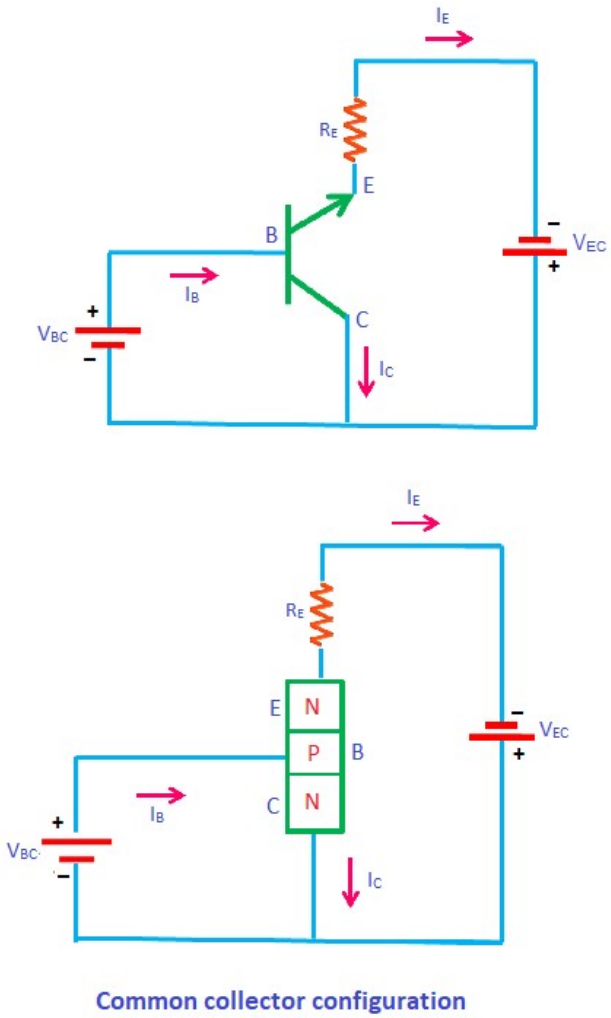
$$\alpha = \frac{I_C}{I_E}$$

The current gain of a transistor in CB configuration is less than unity. The typical current gain of a common base amplifier is 0.98.

7. Explain the working of Common Collector Configuration of NPN Transistor

Common Collector Configuration

In this configuration, the base terminal of the transistor serves as the input, the emitter terminal is the output and the collector terminal is common for both input and output. Hence, it is named as common collector configuration. The input is applied between the base and collector while the output is taken from the emitter and collector. In common collector configuration, the collector terminal is grounded so the common collector configuration is also known as grounded collector configuration.



Common collector configuration

Sometimes common collector configuration is also referred to as emitter follower, voltage follower, common collector amplifier, CC amplifier, or CC configuration. This configuration is mostly used as a voltage buffer.

The input supply voltage between base and collector is denoted by V_{BC} while the output voltage between emitter and collector is denoted by V_{EC}.In this configuration, input current or base current is denoted by I_B and output current or emitter current is denoted by I_E.The common collector amplifier has high input impedance and low output impedance. It has low voltage gain and high current gain.

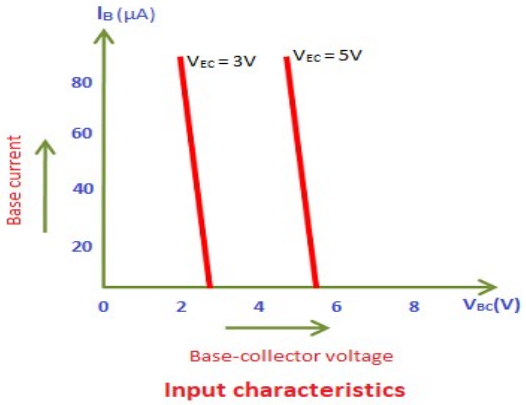
The power gain of the common collector amplifier is medium. To fully describe the behavior of a transistor with CC configuration, we need two set of characteristics - input characteristics and output characteristics.

Input characteristics

The input characteristics describe the relationship between input current or base current (I_B) and input voltage or base-collector voltage (V_{BC}).First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis

The input current or base current (I_B) is taken along y-axis (vertical line) and the input voltage or base-collector voltage (V_{BC}) is taken along x-axis (horizontal line).

To determine the input characteristics, the output voltage V_{EC} is kept constant at 3V and the input voltage V_{BC} is increased from zero volts to different voltage levels. For each level of input voltage $V_{BC,}$ the corresponding input current I_B is noted. A curve is then drawn between input current I_B and input voltage V_{BC} at constant output voltage V_{EC} (3V).



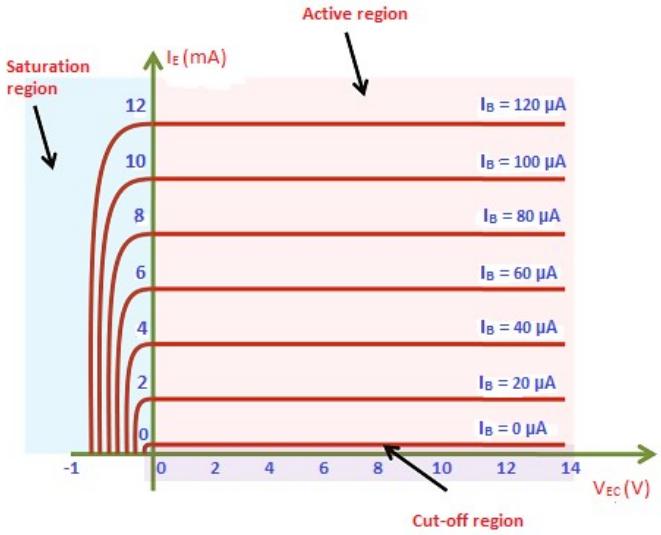
Input characteristics

Next, the output voltage V_{EC} is increased from 3V to different voltage level, say for example 5V and then kept constant at 5V. While increasing the output voltage V_{EC}, the input voltage V_{BC} is kept constant at zero volts.
After we kept the output voltage V_{EC} constant at 5V, the input voltage V_{BC} is increased from zero volts to different voltage levels. For each level of input voltage V_{BC}, the corresponding input current I_B is noted. A curve is then drawn between input current I_B and input voltage V_{BC} at constant output voltage V_{EC} (5V).
This process is repeated for higher fixed values of output voltage (V_{EC}).

Output characteristics

The output characteristics describe the relationship between output current or emitter current (I_E) and output voltage or emitter-collector voltage (V_{EC}).First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis.
The output current or emitter current (I_E) is taken along y-axis (vertical line) and the output voltage or emitter-collector voltage (V_{EC}) is taken along x-axis (horizontal line).

To determine the output characteristics, the input current I_B is kept constant at zero micro amperes and the output voltage V_{EC} is increased from zero volts to different voltage levels. For each level of output voltage V_{EC}, the corresponding output current I_E is noted. A curve is then drawn between output current I_E and output voltage V_{EC} at constant input current I_B (0 μA).



Output characteristics

Next, the input current (I_B) is increased from 0 µA to 20 µA and then kept constant at 20 µA. While increasing the input current (I_B), the output voltage (V_{EC}) is kept constant at 0 volts. After we kept the input current (I_B) constant at 20 µA, the output voltage (V_{EC}) is increased from zero volts to different voltage levels. For each level of output voltage (V_{EC}), the corresponding output current (I_E) is recorded. A curve is then drawn between output current I_E and output voltage V_{EC} at constant input current I_B (20µA). This region is known as the active region of a transistor.

This process is repeated for higher fixed values of input current I_B (I.e. 40 µA, 60 µA, 80 µA and so on).In common collector configuration, if the input current or base current is zero then the output current or emitter current is also zero. As a result, no current flows through the transistor. So the transistor will be in the cutoff region. If the base current is slightly increased then the output current or emitter current also increases. So the transistor falls into the active region. If the base current is heavily increased then the current flowing through the transistor also heavily increases. As a result, the transistor falls into the saturation region.

Transistor parameters

Dynamic input resistance (r_i)

Dynamic input resistance is defined as the ratio of change in input voltage or base voltage (V_{BC}) to the corresponding change in input current or base current (I_B), with the output voltage or emitter voltage (V_{EC}) kept at constant.

$$r_i = \frac{\Delta V_{BC}}{\Delta I_B}, \qquad V_{EC} = \text{constant}$$

The input resistance of common collector amplifier is high.

Dynamic output resistance (r_o)

Dynamic output resistance is defined as the ratio of change in output voltage or emitter voltage (V_{EC}) to the corresponding change in output current or emitter current (I_E), with the input current or base current (I_B) kept at constant. The output resistance of common collector amplifier is low.

$$r_o = \frac{\Delta V_{EC}}{\Delta I_E}, \quad I_B = \text{constant}$$

Current amplification factor (γ)

The current amplification factor is defined as the ratio of change in output current or emitter current I_E to the change in input current or base current I_B. It is expressed by **γ.**

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

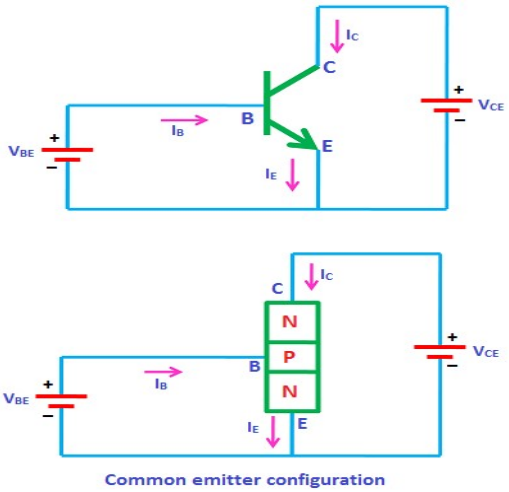
The current gain of a common collector amplifier is high.

8. **Explain the working of Common Emitter Configuration of NPN Transistor**

Common Emitter Configuration

In common emitter configuration, base is the input terminal, collector is the output terminal and emitter is the common terminal for both input and output. That means the base terminal and common emitter terminal are known as input terminals whereas collector terminal and common emitter terminal are known as output terminals.

In common emitter configuration, the emitter terminal is grounded so the common emitter configuration is also known as grounded emitter configuration. Sometimes common emitter configuration is also referred to as CE configuration, common emitter amplifier, or CE amplifier. The common emitter (CE) configuration is the most widely used transistor configuration.



Common emitter configuration

The common emitter (CE) amplifiers are used when large current gain is needed.The input signal is applied between the base and emitter terminals while the output signal is taken between the collector and emitter terminals. Thus, the emitter terminal of a transistor is common for both input and output and hence it is named as common emitter configuration.

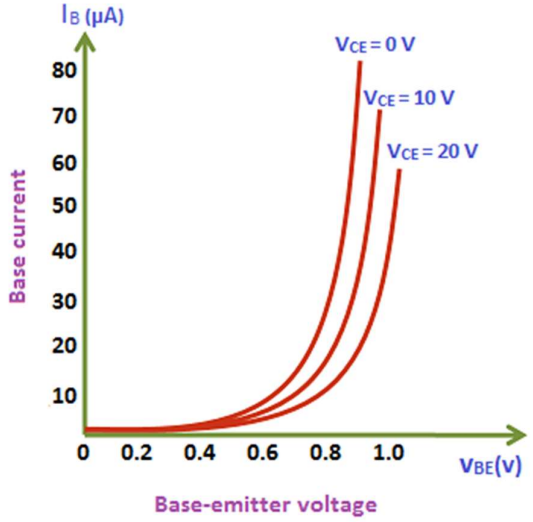
The supply voltage between base and emitter is denoted by V_{BE} while the supply voltage between collector and emitter is denoted by V_{CE}.In common emitter (CE) configuration, input current or base current is denoted by I_B and output current or collector current is denoted by I_C.

The common emitter amplifier has medium input and output impedance levels. So the current gain and voltage gain of the common emitter amplifier is medium. However, the power gain is high.To fully describe the behavior of a transistor with CE configuration, we need two set of characteristics – input characteristics and output characteristics.

Input characteristics

The input characteristics describe the relationship between input current or base current (I_B) and input voltage or base-emitter voltage (V_{BE}).First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The input current or base current (I_B) is taken along y-axis (vertical line) and the input voltage (V_{BE}) is taken along x-axis (horizontal line).

To determine the input characteristics, the output voltage V_{CE} is kept constant at zero volts and the input voltage V_{BE} is increased from zero volts to different voltage levels. For each voltage level of input voltage (V_{BE}), the corresponding input current (I_B) is recorded.



I/P characteristics CE configuration

A curve is then drawn between input current I_B and input voltage V_{BE} at constant output voltage V_{CE} (0 volts).Next, the output voltage (V_{CE}) is increased from zero volts to certain voltage level (10 volts) and the output voltage (V_{CE}) is kept constant at 10 volts. While increasing the output voltage (V_{CE}), the input voltage (V_{BE}) is kept constant at zero volts. After we kept the output voltage (V_{CE}) constant at 10 volts, the input voltage V_{BE} is increased from zero volts to different voltage levels. For each voltage level of input voltage (V_{BE}), the corresponding input current (I_B) is recorded.A curve is then drawn between input current I_B and input voltage V_{BE} at constant output voltage V_{CE} (10 volts).This process is repeated for higher fixed values of output voltage (V_{CE}).

When output voltage (V_{CE}) is at zero volts and emitter-base junction is forward biased by input voltage (V_{BE}), the emitter-base junction acts like a normal p-n junction diode. So the input characteristics of the CE configuration is same as the characteristics of a normal pn junction diode.

The cut in voltage of a silicon transistor is 0.7 volts and germanium transistor is 0.3 volts. In our case, it is a silicon transistor. So from the above graph, we can see that after 0.7 volts, a small increase in input voltage (V_{BE}) will rapidly increases the input current (I_B).

In common emitter (CE) configuration, the input current (I_B) is very small as compared to the input current (I_E) in common base (CB) configuration. The input current in CE configuration is measured in microamperes (μA) whereas the input current in CB configuration is measured in milliamperes (mA).

In common emitter (CE) configuration, the input current (I_B) is produced in the base region which is lightly doped and has small width. So the base region produces only a small input current (I_B). On the other hand, in common base (CB) configuration, the input current (I_E) is produced in the emitter region which is heavily doped and has large width. So the emitter region produces a large input current (I_E). Therefore, the input current (I_B) produced in the common emitter (CE) configuration is small as compared to the common base (CB) configuration.

Due to forward bias, the emitter-base junction acts as a forward biased diode and due to reverse bias, the collector-base junction acts as a reverse biased diode.Therefore, the width of the depletion region at the emitter-base junction is very small whereas the width of the depletion region at the collector-base junction is very large.

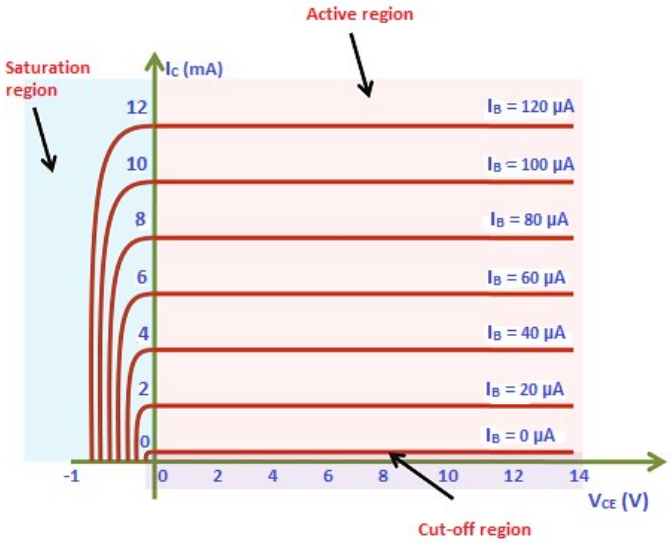
If the output voltage V_{CE} applied to the collector-base junction is further increased, the depletion region width further increases. The base region is lightly doped as compared to the collector region. So the depletion region penetrates more into the base region and less into the collector region. As a result, the width of the base region decreases which in turn reduces the input current (I_B) produced in the base region.

From the above characteristics, we can see that for higher fixed values of output voltage V_{CE}, the curve shifts to the right side. This is because for higher fixed values of output voltage, the cut in voltage is increased above 0.7 volts. Therefore, to overcome this cut in voltage, more input voltage V_{BE} is needed than previous case.

Output characteristics

The output characteristics describe the relationship between output current (I_C) and output voltage (V_{CE}).First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The output current or collector current (I_C) is taken along y-axis (vertical line) and the output voltage (V_{CE}) is taken along x-axis (horizontal line).

To determine the output characteristics, the input current or base current I_B is kept constant at 0 μA and the output voltage V_{CE} is increased from zero volts to different voltage levels. For each level of output voltage, the corresponding output current (I_C) is recorded.



O/P Characteristics CE Configuration

A curve is then drawn between output current I_C and output voltage V_{CE} at constant input current I_B (0 µA).When the base current or input current I_B = 0 µA, the transistor operates in the cut-off region. In this region, both junctions are reverse biased.

Next, the input current (I_B) is increased from 0 µA to 20 µA by adjusting the input voltage (V_{BE}). The input current (I_B) is kept constant at 20 µA.While increasing the input current (I_B), the output voltage (V_{CE}) is kept constant at 0 volts.

After we kept the input current (I_B) constant at 20 µA, the output voltage (V_{CE}) is increased from zero volts to different voltage levels. For each voltage level of output voltage (V_{CE}), the corresponding output current (I_C) is recorded.A curve is then drawn between output current I_C and output voltage V_{CE} at constant input current I_B (20 µA). This region is known as the active region of a transistor. In this region, emitter-base junction is forward biased and the collector-base junction is reverse biased.

This steps are repeated for higher fixed values of input current I_B (I.e. 40 µA, 60 µA, 80 µA and so on).When output voltage V_{CE} is reduced to a small value (0.2 V), the collector-base junction becomes forward biased. This is because the output voltage V_{CE} has less effect on collector-base junction than input voltage V_{BE}.

As we know that the emitter-base junction is already forward biased. Therefore, when both the junctions are forward biased, the transistor operates in the saturation region. In this region, a small increase in output voltage V_{CE} will rapidly increases the output current I_C.

Collector current:

$$I_E = I_C + I_B$$

$$\Delta I_E = \Delta I_C + \Delta I_B$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

Substituting the value of ΔI_E in equation (1), we get,

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C}$$

$$\beta = \frac{\frac{\Delta I_C}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{\alpha}{1-\alpha}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$I_E = I_C + I_B \ldots\ldots (1)$$

$$I_C = \alpha I_E + I_{CBO} \ldots\ldots (2)$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C(1-\alpha) = \alpha(I_B) + I_{CBO}$$

$$I_C = \frac{\alpha}{(1-\alpha)}(I_B) + \frac{1}{(1-\alpha)} I_{CBO} \ldots\ldots\ldots (3)$$

Transistor parameters

Dynamic input resistance (r_i)

Dynamic input resistance is defined as the ratio of change in input voltage or base voltage (V_{BE}) to the corresponding change in input current or base current (I_B), with the output voltage or collector voltage (V_{CE}) kept at constant.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B}, \qquad V_{CE} = \text{constant}$$

In CE configuration, the input resistance is very low.

Dynamic output resistance (r_o)

Dynamic output resistance is defined as the ratio of change in output voltage or collector voltage (V_{CE}) to the corresponding change in output current or collector current (I_C), with the input current or base current (I_B) kept at constant.

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C}, \qquad I_B = \text{constant}$$

In CE configuration, the output resistance is high.

Current gain (α)

The current gain of a transistor in CE configuration is defined as the ratio of output current or collector current (I_C) to the input current or base current (I_B).

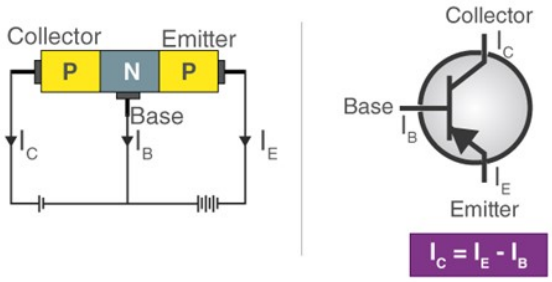
$$\alpha = \frac{I_C}{I_B}$$

The current gain of a transistor in CE configuration is high. Therefore, the transistor in CE configuration is used for amplifying the current.

9. Explain with neat diagram construction and operation of PNP transistor

PNP Transistors

PNP transistors representation is as shown in the figure below.



This bipolar PNP junction transistor is formed with three layers of semiconductor material, with two P-type regions and one N-type region. It includes three terminals:

- Emitter
- Collector
- Base

Emitter – emitter part in a transistor lets it supply majority charge carriers. The emitter is always forward biased with respect to the base. Hence the majority of charge carriers are supplied to the base. The emitter of a transistor is heavily doped and moderate in size.

Collector – the majority of the charge carrier supplied by the emitter is collected by the collector. The collector-base junction is always reverse biased. The collector area is moderately doped and has the capacity to collect the charge carrier supplied by the emitter.

Base – The centre section of the transistor is known as the base. The base forms two circuits, the input circuit with the emitter and the output circuit with the collector. The emitter-base is forward biased and offers low resistance to the circuit. The collector-base junction is in reverse bias and offers higher resistance to the circuit. The base of a transistor is lightly doped and very thin, due to which it offers the majority charge carrier to the base.

Depletion region –The depletion regions are formed at the emitter-base junction and the base-collector junction.

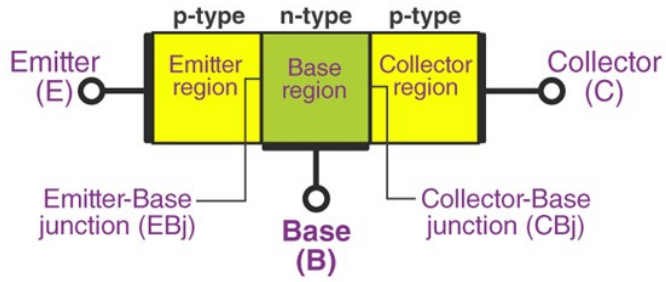
Construction Of PNP Transistor

P-type semiconductors, which represent the emitter and collector, are doped heavily than N-type semiconductors, which represent the base. Hence, the depletion region at both junctions penetrates towards the N-type layer.

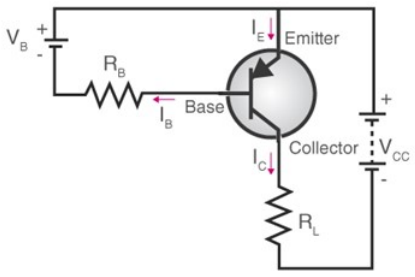
In PNP transistors, in this type of transistor, majority charge carriers are holes, and minority charge carriers are electrons. The emitter emits holes and is collected at the collector.

In a PNP transistor, the base current which enters into the collector is amplified. The flow of current is typically controlled by the base. Current flows in the opposite direction in the base. In a PNP transistor, the emitter emits “holes”, and these holes are collected by the collector.

The base region features a large number of free electrons. But, the width of the middle layer is very small and is lightly doped. So significantly less free electrons are present in the base region.



Working of PNP Transistor



Emitter current is created when the emitter-base junction is forward biased, the emitter pushes the holes towards the base region. When electrons move into the N-type semiconductor or base, they combine with the holes. The base is lightly doped and is comparatively thin. Hence only

a few holes are combined with the electrons and the remaining are moved towards the collector space charge layer. This phenomenon generates the base current. The current is carried by holes in p-n-p transistors.

10. Write neat diagram describe how a voltage regulator circuits aids the output voltage under the following condition

A zener diode can be used as a voltage regulator or voltage stabilizer, to provide a constant voltage from a source whose voltage may vary over a particular range.

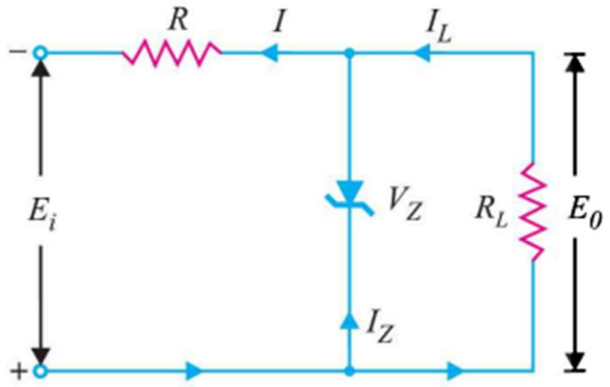


Fig.1

The circuit connection is shown in Fig.1 .
The zener diode of zener voltage V_Z is connected reversely across the load resistance R_L across which constant output voltage E_O is required.The series resistance R is used to absorb the output voltage fluctuations, so as to maintain constant output voltage across R_L .When the circuit is properly designed, the output voltage E_O remains constant even though the input voltage E_i and load resistance R_L may vary over a wide range.
Case 1: E_i Variable and R_L constant

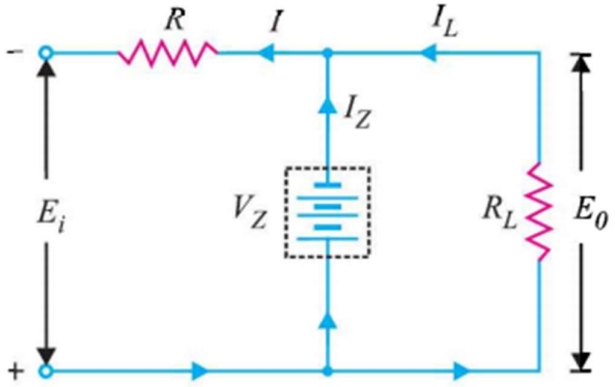


Fig.2

Suppose the input voltage E_i increases, since the zener is in the breakdown region, the zener diode is equivalent to a battery of voltage V_Z as shown in Fig.2 and the output voltage remains constant at V_Z ($E_O = V_Z$).
The excess voltage is dropped across R. This will cause an increase in the value of total current I. The zener will conduct the increase of current in I, while the load current remains constant.

Hence the output voltage remains constant irrespective of the change in input voltage E_i

Summary(Case 1)

Suppose E_i increases Since zener is in breakdown region, V_Z remains constant $E_O = V_Z$ So E_O remains constant Excess voltage drops across R So I increases, since I_L remains constant, I_Z increases $\uparrow I = \uparrow I_Z + I_L$ (constant)

So the excess current is conducted by the zener diode and E_O remains constant irrespective of the change in E_i

Case 2: E_i Constant and R_L Vaiable

Now suppose the input voltage E_i is constant but R_L decreases

Since the zener diode is in breakdown region , voltage across it will remain constant at V_Z.

As the output voltage E_O is equal to the zener voltage, So E_O will also remain constant at V_Z.

When R_L decreases ,in order to maintain E_O constant, current through the load resistance I_L will increase. Since E_i is constant, total current I is also constant. So the increase in load current I_L will come from a decrease in zener current I_Z .

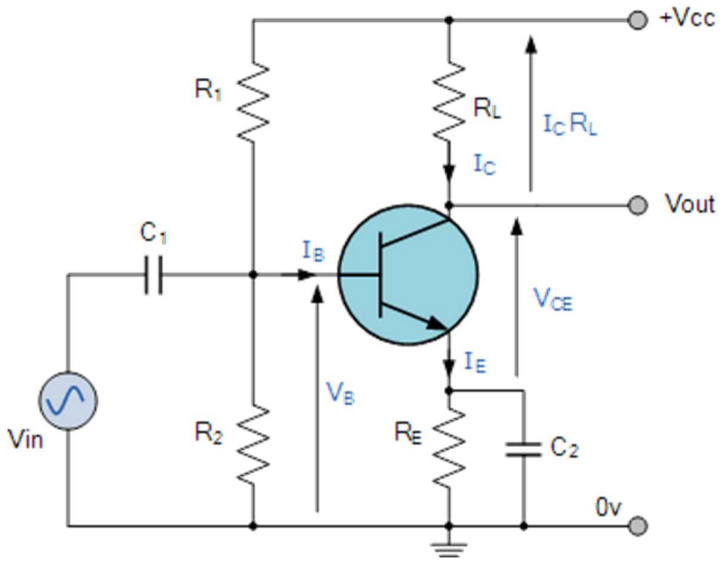
$I(\text{constant}) = \uparrow I_L + \downarrow I_Z$

Voltage drop across R = $E_i - E_O$

Current through R , $I = I_Z + I_L$

11. Explain the elementary treatment of small signalamplifier

Typical Single Stage Amplifier Circuit



Small Signal Amplifiers

- Small Signal Amplifiers are also known as **Voltage Amplifiers**.
- Voltage Amplifiers have 3 main properties, **Input Resistance**, **Output Resistance** and **Gain**.
- The Gain of a small signal amplifier is the amount by which the amplifier "Amplifies" the input signal.
- Gain is a ratio of output divided by input, therefore it has no units but is given the symbol (A) with the most common types of transistor gain being, **Voltage Gain (Av), Current Gain (Ai)** and **Power Gain (Ap)**
- The power Gain of the amplifier can also be expressed in **Decibels** or simply **dB**.
- In order to amplify all of the input signal distortion free in a Class A type amplifier, DC Base Biasing is required.
- DC Bias sets the Q-point of the amplifier half way along the load line.
- This DC Base biasing means that the amplifier consumes power even if there is no input signal present.
- The transistor amplifier is non-linear and an incorrect bias setting will produce large amounts of distortion to the output waveform.
- Too large an input signal will produce large amounts of distortion due to clipping, which is also a form of amplitude distortion.
- Incorrect positioning of the Q-point on the load line will produce either **Saturation Clipping** or **Cut-off Clipping**.
- The **Common Emitter Amplifier** configuration is the most common form of all the general purpose voltage amplifier circuit using a Bipolar Junction Transistor.
- The **Common Source Amplifier** configuration is the most common form of all the general purpose voltage amplifier circuit using a Junction Field Effect Transistor.

12. Problem

Changes in bases current= 150 μA-100 μA

= 50 μA

Changes in collector current=7.5 mA – 5mA

= 2.5mA

Current Gain β $= \Delta I_C/\Delta I_B$

$=2.5mA/50\ \mu A$

$= 50$