UNIT 4 QUESTION BANK ANSWERS

PART A

1. Define Flip flop. What are the different types of flip Flop?

A flip-flop or latch is **a circuit that has two stable states and can be used to store state information** – a bistable multivibrator. ... A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero".

Types of flip flops:

SR Flip Flop

JK Flip Flop

D Flip Flop

T Flip Flop

2. Which gates are called as Universal gates? What are its advantages?

The NAND and NOR gates are universal gates. **because they can be combined to produce any of the other gates like OR, AND, and NOT gates**.

3. Name two types of D/ A & A/D converter.

Types of ADC

- Successive Approximation (SAR) ADC.
- Dual Slope ADC.
- Flash ADC.

Types of DAC

- Weighted Resistor DAC.
- R-2R Ladder DAC

4.What is a decade counter?

A decade counter is **one that counts in decimal digits, rather than binary**. A decade counter may have each (that is, it may count in binary-coded decimal, as the 7490 integrated circuit did) or other binary encodings. A decade counter is a binary counter that is designed to count to 1001 (decimal 9).

5. What are the basic properties of Boolean algebra?

Commutative Property

Associative Property

Distributive Property

6. State and prove Distributive law.

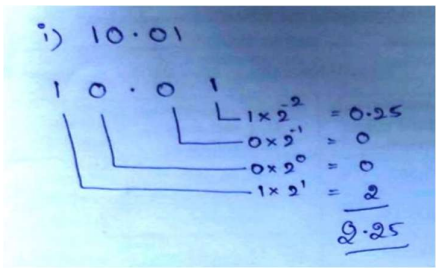
$$A(B + C) = A.B + A.C$$

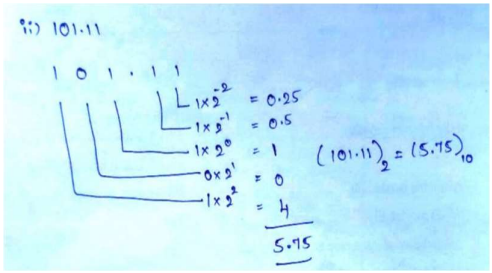
$$A + BC = (A + B).(A + C)$$

A	B	C	B+C	A.(B+C)	A.B	A.C	A.B+A.C
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

A	B	C	BC	A+BC	A+B	A+C	(A+B).(A+C)
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

7. Demonstrate the given binary numbers in its equivalent Decimal numbers with steps.





8. Illustrate the excitation table of J-K flip flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation table of JK flip flop

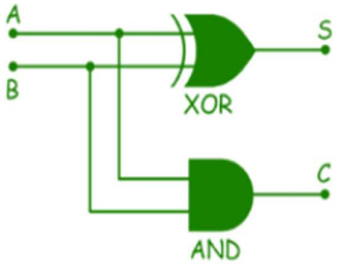
9. Give the truth table of XOR gate

XOR

X	Y	X ⊕ Y
0	0	0
0	1	1
1	0	1
1	1	0

XOR Symbol

10. Show the logic diagram and truth table for a half adder

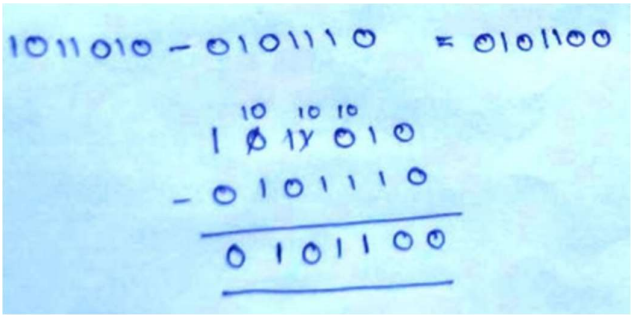


Half Adder

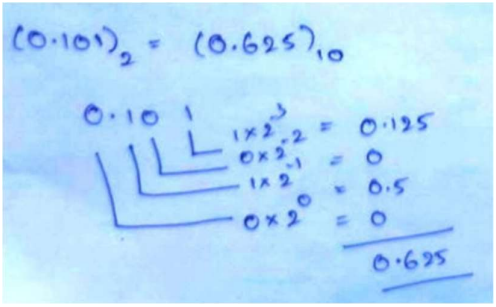
Inputs		Outputs	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Table 3.6 Truth table for half-adder

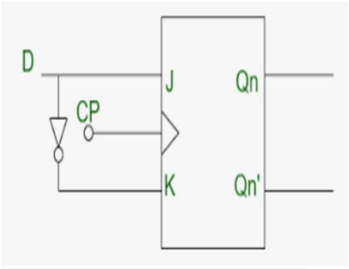
11. Solve for the following binary difference: 1011010-0101110

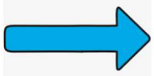


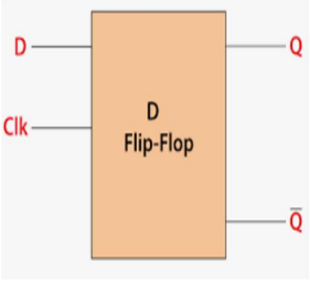
12. Identify the decimal equivalent of binary fraction 0.101



13. Construct D Flip-flop from JK flip-flop







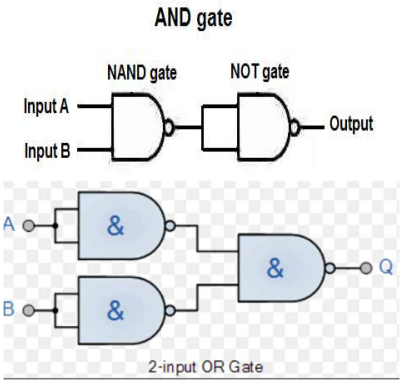
14. Distinguish between combinational logic and sequential Logic.

Combinational	Sequential
output depends only upon present input	output depends upon present as well as past input
Elementary building blocks: Logic gates	Elementary building blocks: Flip-flops
circuits don't have clock, they don't require triggering.	circuits are clock dependent they need triggering.
Used for arithmetic as well as Boolean operations.	Mainly used for storing data.

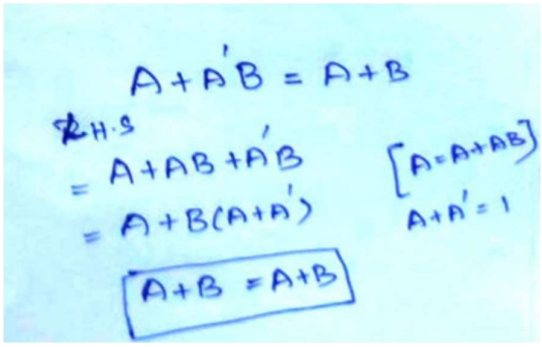
15. Compare asynchronous and synchronous counters.

Asynchronous Counter	Synchronous Counter
1) Clock input is applied to LSB flip-flop. The output of first flip-flop is connected as clock to next FF.	1) Clock input is common to all flip-flop.
2) All Flip-Flops are toggle flip-flop.	2) Any flip-flop can be used.
3) Speed depends on no. of flip-flop used for n bit .	3) Speed is independent of no. of flip-flop used.
4) No extra Logic Gates are required.	4) Logic Gates are required based on design.
5) Cost is less.	5) Cost is more.

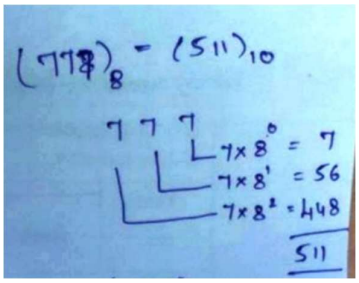
16. Construct AND and OR gates using NAND gates.



17. Prove that A + A'B = A+B



18. Convert (777)8 to decimal.



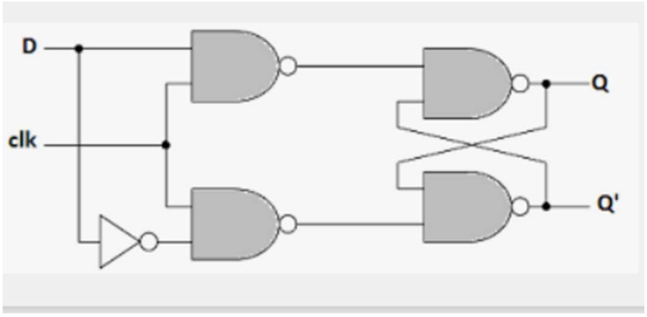
19. State De Morgan's theorems

DeMorgan's Theorem states that inverting the output of any gate results in same function as opposite type of gate (AND vs. OR) with two inverted variables A and B.

$$\overline{A\,B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A}\,\overline{B}$$

20. Design' D' Latch using NAND gates.

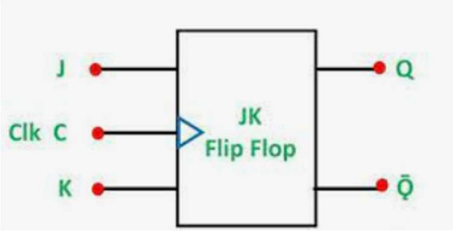


PART B

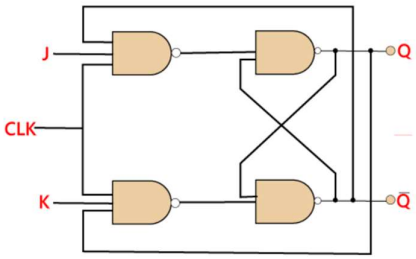
(ii) Explain the working of JK and D flip flops.

JK FLIP FLOP

Symbol:



Logic Diagram



Truth Table:

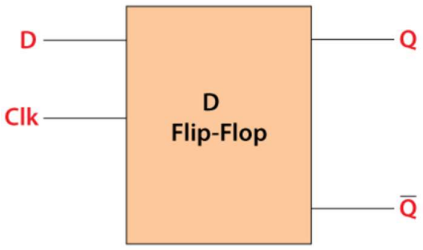
J	K	$Q_{(t+1)}$	
0	0	$Q_{(t)}$	*unchanged*
0	1	0	*reset*
1	0	1	*set*
1	1	$\overline{Q}_{(t)}$	*output inversion*

The JK flip flop is used to remove the drawback of the S-R flip flop, i.e., undefined states. The JK flip flop is formed by doing modification in the SR flip flop. The S-R flip flop is improved in order to construct the J-K flip flop. When S and R input is set to true, the SR flip flop gives an inaccurate result. But in the case of JK flip flop, it gives the correct output.

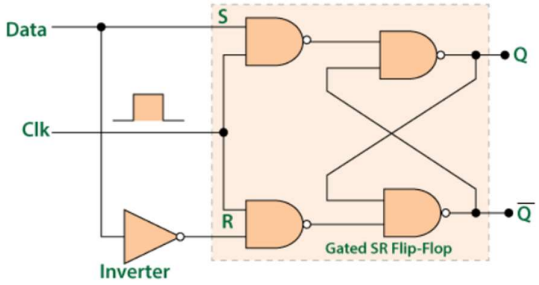
D FLIP FLOP

In D flip flop, the single input "D" is referred to as the "Data" input. When the data input is set to 1, the flip flop would be set, and when it is set to 0, the flip flop would change and become reset.

Symbol:



Logic diagram:



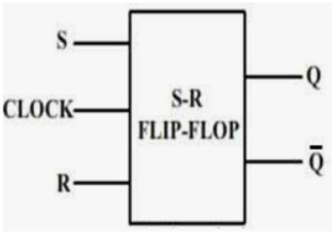
Truth Table:

Input D_n	Output Q_{n+1}
0	0
1	1

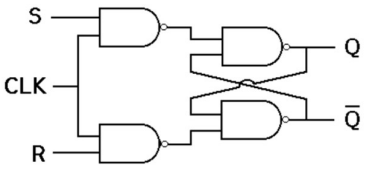
2. Write short notes on the following flip flops:

A) RS- Flip flop

Symbol:



Logic Diagram



Truth Table:

Inputs		*Output*
S_n	R_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	–

Characteristics Table of SR Flip Flop:

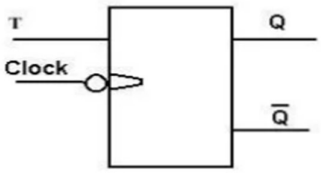
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	×
1	1	1	×

The S-R flip flop is the most common flip flop used in the digital system. In SR flip flop, when the set input "S" is true, the output Y will be high, and Y' will be low.

b) Toggle flip flop

The T flip-flop is obtained from a JK flip-flop when inputs J and K are connected to provide a single input designated by T.

The flip-flop thus has only two conditions.

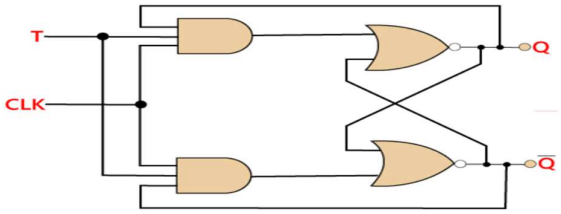


Graphic Symbol

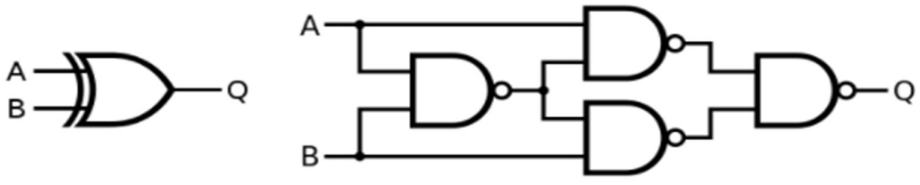
(d) *T* Flip-Flop

T	$Q(t+1)$	Operation
0	$Q(t)$	No change
1	$\overline{Q}(t)$	Complement

Truth Table



4.(i) How can you implement XOR gate using NAND Gates.



EXOR GATE **EXOR USING NAND GATES**

Q = **A** XOR **B**

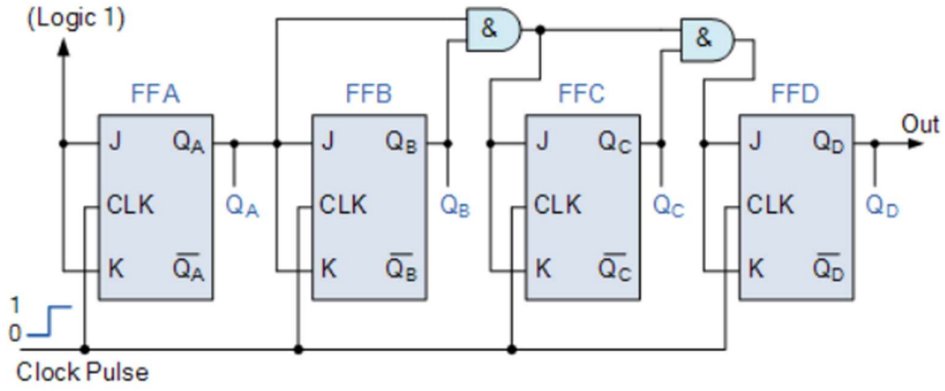
= [**A** NAND (**A** NAND **B**)] NAND[**B** NAND (**A** NAND **B**)]

Truth Table

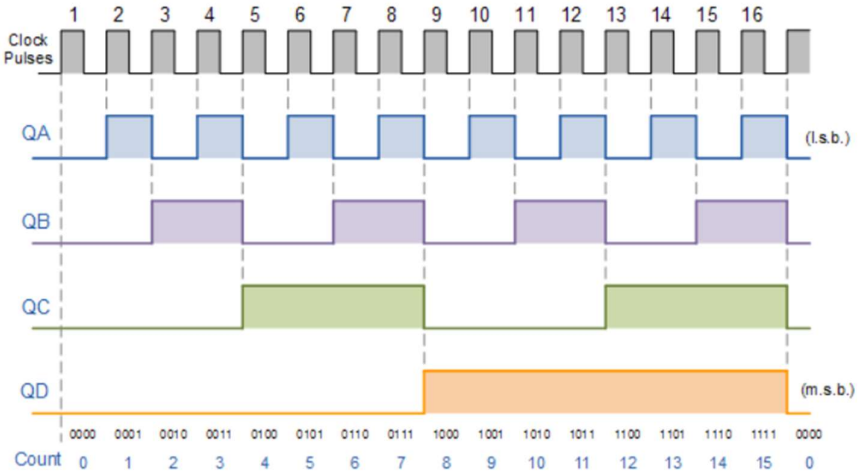
Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	0

(ii) Show the operation of 4-bit synchronous UP counter with its timing diagram and its design.

An external CLK signal is given to all four flip-flops in parallel. This counter includes 16 output states where it counts from 0000 to 1111.

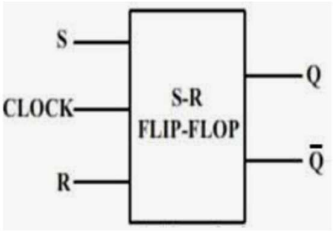


4-bit Synchronous Counter Waveform Timing Diagram

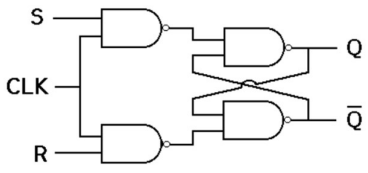


5. Demonstrate the different states of SR flip flop for Various input with logic diagram. Show its characteristics table.

Symbol:



Logic Diagram



Truth Table:

Inputs		*Output*
S_n	R_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	–

Characteristics Table of SR Flip Flop:

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	×
1	1	1	×

The S-R flip flop is the most common flip flop used in the digital system. In SR flip flop, when the set input "S" is true, the output Y will be high, and Y' will be low.

6. Demonstrate various Boolean laws with its truth table.

Commutative law

A + B = B + A Additive and Multiplicative A·B = B·A

A	B	A+B	A·B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

Table 1

B	A	B+A	B·A
0	0	0	0
1	0	1	0
0	1	1	0
1	1	1	1

Table 2

From table 1 and table 2

A + B = B + A and A·B = B·A

Associative law

(A+B)+C=A+(B+C)

(A.B).C=A.(B.C)

Proof:

A	B	C	A + B	(A + B) + C	B + C	A + (B + C)
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	1	1	0	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

From the above tables,

(A+B)+C=A+(B+C)

Similarly, we can prove,

A.(B.C)=(A.B).C

A	B	C	B.C	A.(B.C)	A.B	(A.B).C
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	0	1	0
1	1	1	1	1	1	1

Distributive law

1. A(B + C) = A.B + A.C
2. A + BC = (A + B).(A + C)

Truth Table of first law

A	B	C	B+C	A.(B+C)	A.B	A.C	A.B+A.C
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

Truth Table of second law

A	B	C	BC	A+BC	A+B	A+C	(A+B).(A+C)
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

AND & OR law

AND Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

INVERSION law

NOT Truth Table

A	B
0	1
1	0

De – morgan's law

$\overline{A.B} = \overline{A} + \overline{B}$

A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A} + \overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

$\overline{A + B} = \overline{A}.\overline{B}$

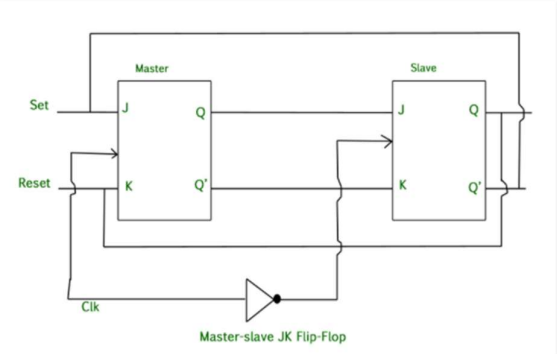
A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

7. (i) Draw the logic diagram of clocked Master – slave JK Flip flop and explain its working.

Race Around Condition In JK Flip-flop – For J-K flip-flop, if J=K=1, and if clk=1 for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop. This problem (Race Around Condition) can be avoided by ensuring that the clock input is at logic "1" only for a very short time. This introduced the concept of **Master Slave JK** flip flop.

Master Slave JK flip flop –

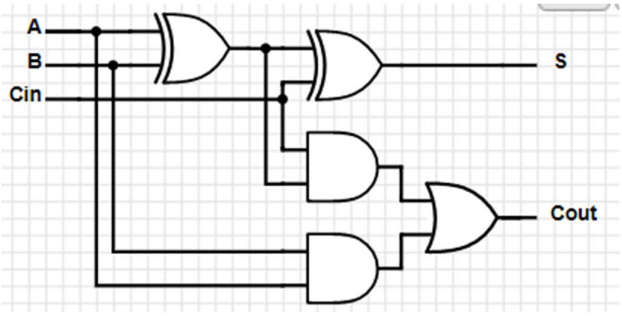
The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the **"master"** and the other as a **"slave"**. The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.



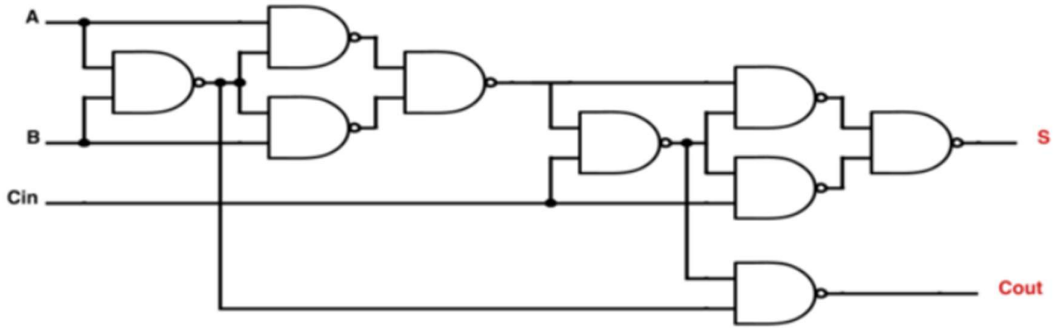
(ii) Show how a full adder can be implemented using NAND gate.

A Full-adder circuit adds three one-bit binary numbers (A, B, Cin) and outputs two one-bit binary numbers, a Sum (S) and a carry (Cout).

Full Adder Equivalent



Full-Adder NAND Equivalent



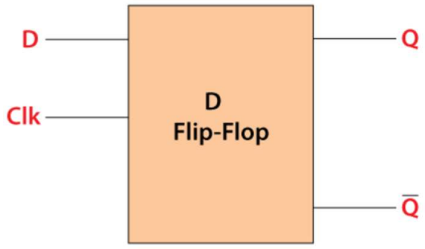
9. Develop the following flip flops and explain its operations

(i) D flip flop using NAND gates

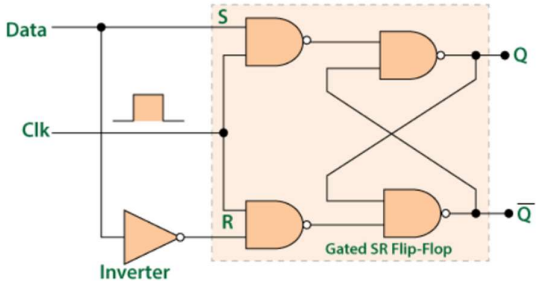
D FLIP FLOP

In D flip flop, the single input "D" is referred to as the "Data" input. When the data input is set to 1, the flip flop would be set, and when it is set to 0, the flip flop would change and become reset.

Symbol:

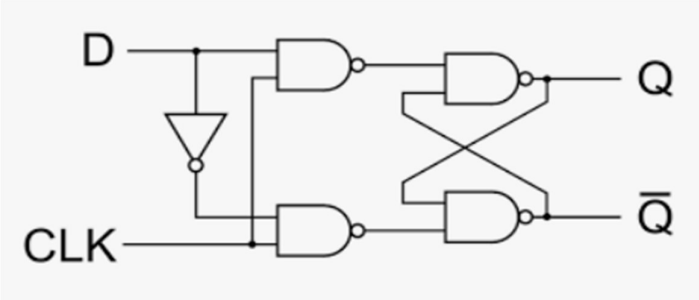


Logic diagram:



Truth Table:

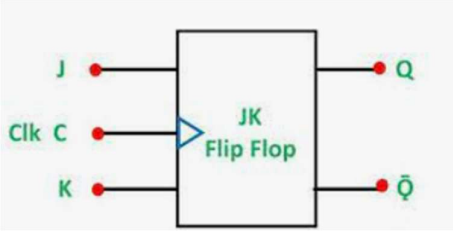
Input D_n	Output Q_{n+1}
0	0
1	1



(ii) JK flip flop using NAND gates

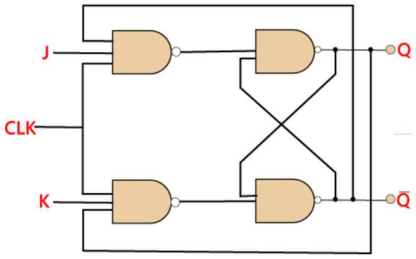
JK FLIP FLOP

Symbol:



Logic Diagram

Truth Table:



J	K	$Q_{(t+1)}$	
0	0	$Q_{(t)}$	*unchanged*
0	1	0	*reset*
1	0	1	*set*
1	1	$\overline{Q}_{(t)}$	*output inversion*

The JK flip flop is used to remove the drawback of the S-R flip flop, i.e., undefined states. The JK flip flop is formed by doing modification in the SR flip flop. The S-R flip flop is improved in order to construct the J-K flip flop. When S and R input is set to true, the SR flip flop gives an inaccurate result. But in the case of JK flip flop, it gives the correct output.

10. Classify the types of D/A and A/D converters .Also Explain the working principle of any one type in each converter.

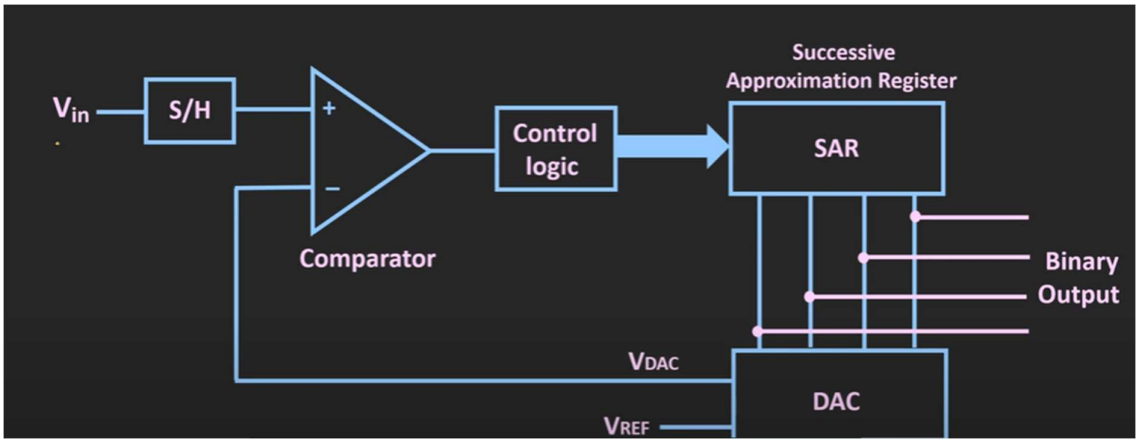
Types of ADC

- Successive Approximation (SAR) ADC.
- Dual Slope ADC.
- Flash ADC.

Types of DAC

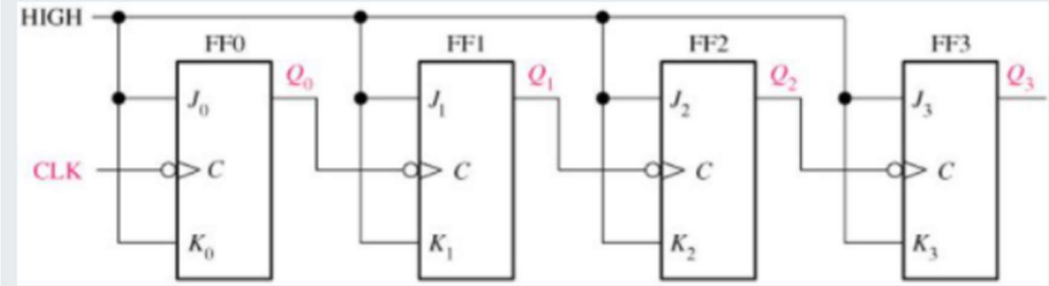
- Weighted Resistor DAC.
- R-2R Ladder DAC

Successive Approximation (SAR) ADC



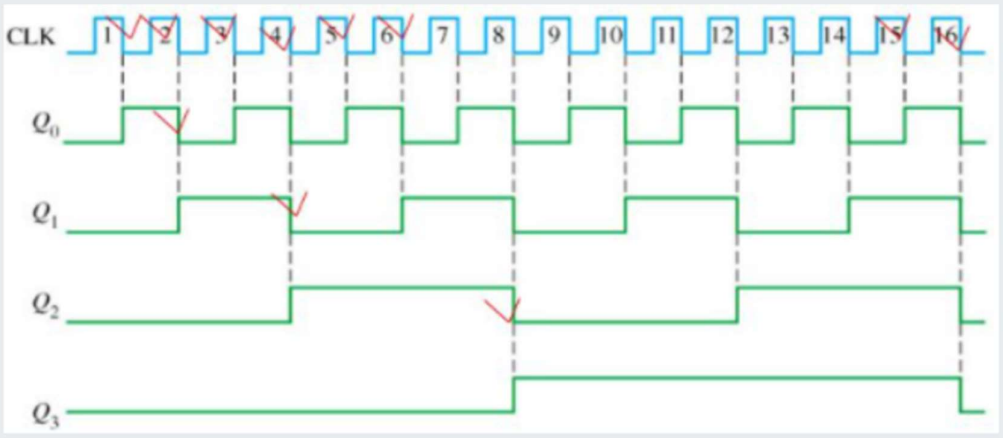
11.With a neat diagram explain the working of 4bit binary ripple counter

A binary ripple counter consists of a series connection of complementing flip-flops (T or JK type), with the output of each flip-flop connected to the Clock Pulse input of the next higher-order flip-flop. The flip-flop holding the least significant bit receives the incoming count pulses. The diagram of a 4-bit binary ripple counter is shown in Fig. below. All J and K inputs are equal to 1



The small circle in the CP input indicates that the flip-flop complements during a negative-going transition or when the output to which it is connected goes from 1 to 0. The lowest-order bit Q_0 must be complemented with each count pulse. Every time Q_0 goes from 1 to 0, it complements Q_1. Every time Q_1 goes from 1 to 0, it complements Q_2, and so on.

Timing Diagram:



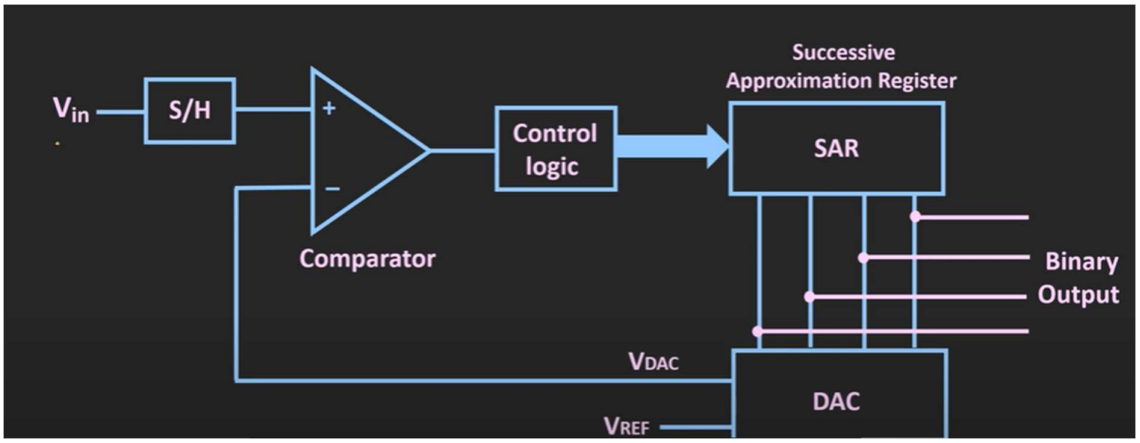
In timing diagram Q_0 is changing as soon as the negative edge of clock pulse is encountered, Q1 is changing when negative edge of Q_0 is encountered (because Q_0 is like clock pulse for second flip flop) and so on.

12. Compare the performance features of different types of ADC and DAC.

TABLE 1: COMPARISON OF PERFORMANCE CHARACTERISTICS FOR DIFFERENT ADC ARCHITECTURES			
Architecture	**Advantages**	**Disadvantages**	**Applications**
Flash	• Ultra-high-speed sample rates	• Sparkle codes • Metastability • Component matching limits resolution to 8 bits • High power consumption • Large size • Expensive	• Wireless communications • Optical communications
Pipeline	• High-speed sample rates • Good resolution • Increased throughput • Small form factor • High SFDR • Low THD • Fewer sparkle codes	• Parallelism causes greater power consumption and latency • Requires digital error correction	• High-speed cellular base stations • Telecommunications • Satellite base stations • Radar
Delta-sigma	• Low-to-medium sample rate • High resolution (up to 31 bits) • Low cost • Low power consumption	• Complexity of circuitry due to oversampling • Limited bandwidths • No need for anti-aliasing filters	• Digital audio applications • Process control • Temperature measurements
SAR	• Low power consumption • High resolution and accuracy	• Limited speed • May require anti-aliasing filter	• Data acquisition for medical imaging • Industrial process control • Optical communications

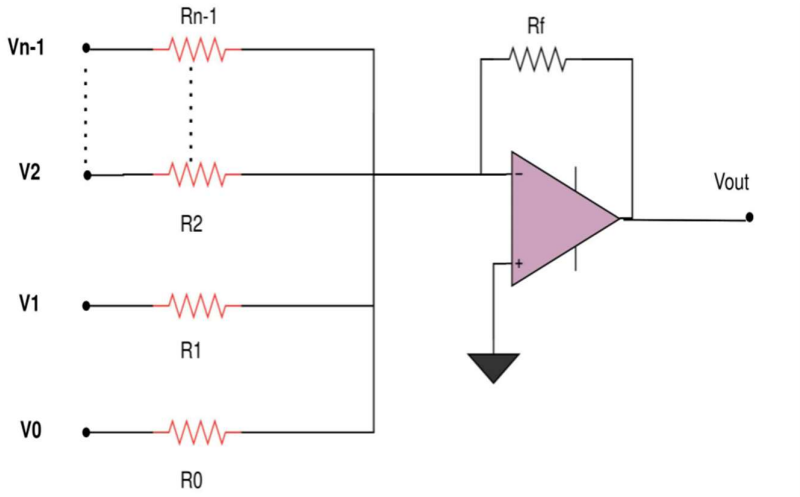
TABLE 2: COMPARISON OF PERFORMANCE CHARACTERISTICS FOR DIFFERENT DAC ARCHITECTURES			
Architecture	**Advantages**	**Disadvantages**	**Application**
String resistor	• Fast sample input rate • Low power • Monotonicity • Low glitch energy	• High element count (2N resistors/bits for N bits) • High settling time • Gain/offset error • High noise	• Portable instrumentation • Process control • Data-acquisition systems
R-2R	• High voltage output • High resolution • High accuracy	• Binary-weighted resistors generally require expensive op amps • Switching delay • Gain/offset error • Low sampling rate	• Industrial applications
Interleaved and pipelined	• High bandwidth • High resolution • Extremely fast data input rate • Low power • Fast settling time	• High cost • Integral nonlinearity • Gain error at analog output	• Radar/jammers • Test and measurement • Satellite communications • Multiband base stations

13. (i) Explain the operation of successive approximation Type ADC with a neat sketch.



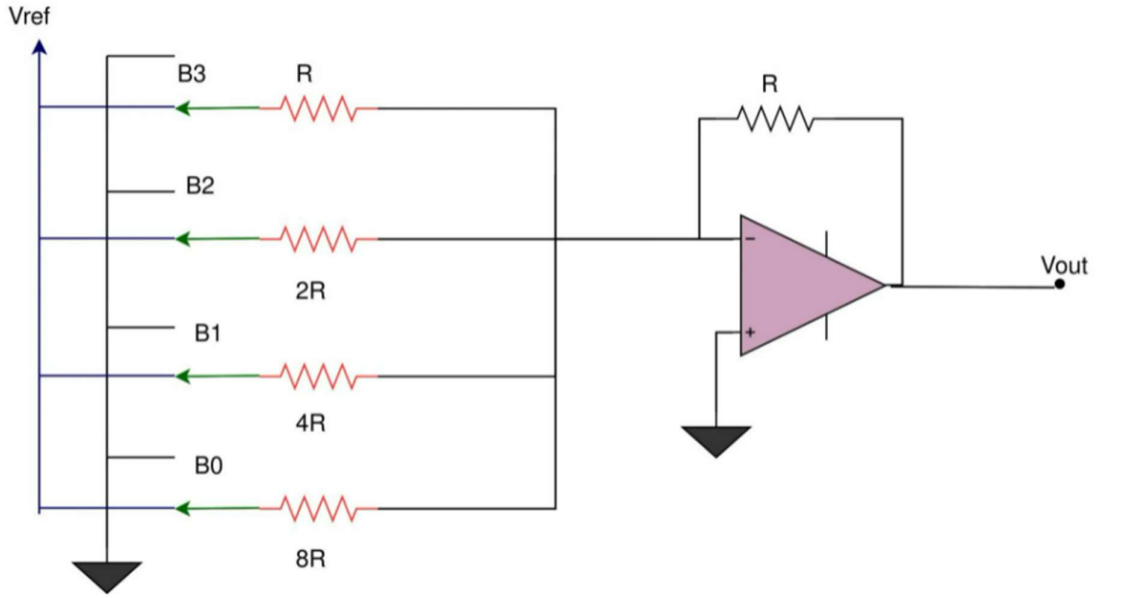
(ii) Draw the circuit of Binary weighted resistor Digital to analog Converter and Explain its operation.

It is the type of DAC that transforms a particular binary code into an equivalent analog signal. This type consists of weighted resistors whose values are kept as the multiples of two and an inverted summing operational amplifier which results in an output signal with 180 degrees phase shift. The reference voltage is either generated internally or is provided to the DAC converter to decide the maximum output voltage of the converter.



$$V_{out} = -\{(R_f/R_0)V_0 + (R_f/R_1)V_1 + (R_f/R_2)V_2 + \ldots + (R_f/R_{n-1})V_{n-1}\}$$

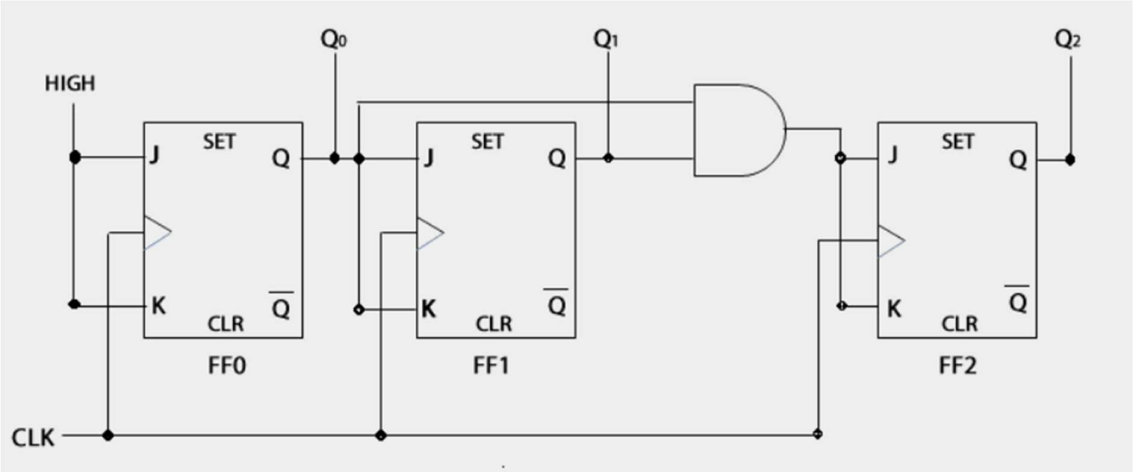
Assuming Vref = 5 V and code as 1011, the weighted output voltage is



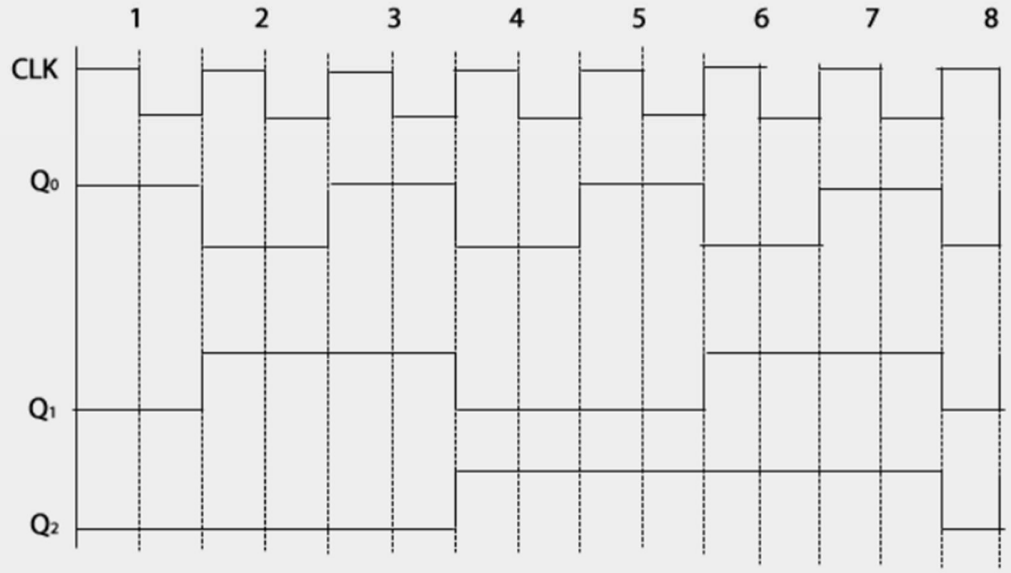
14. Design a 3 bit asynchronous UP counter.

Synchronous counters are designed in such a way that the clock pulses are applied to the CP inputs of all the flip-flops. The common pulse triggers all the flip-flops simultaneously, rather than one at a time in succesion.

In the 3-bit synchronous counter, we have used three j-k flip-flops. As in the diagram, The J and K inputs of FF0 are connected to HIGH. The inputs J and K of FF1 are connected to the output of FF0, and the J and K inputs of FF2 are connected to the output of an AND gate, which is fed by the outputs of FF0 and FF1.



Timing Diagram



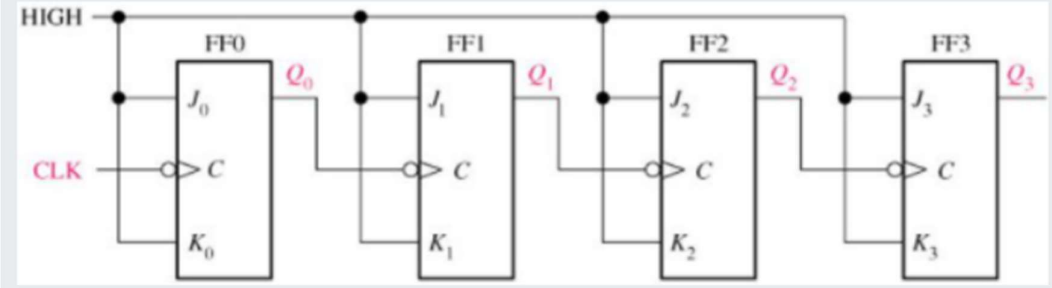
Binary state sequence

FF2	FF1	FF0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

PART C

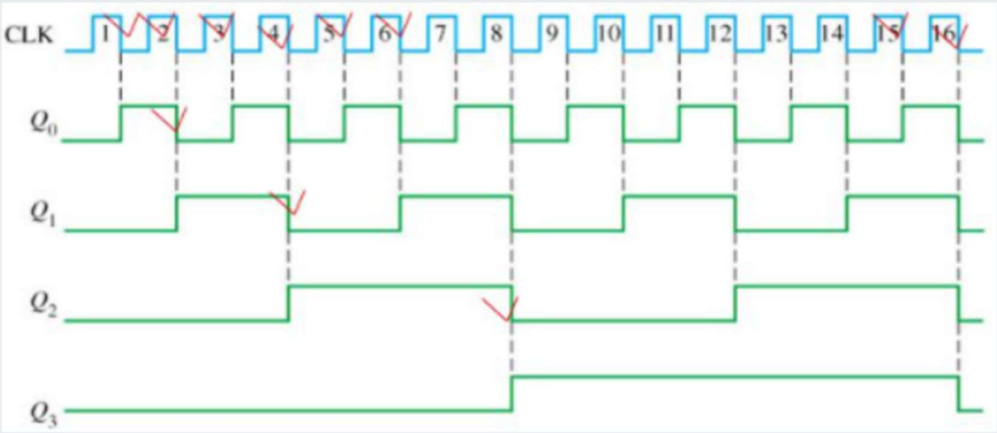
2. Explain the operation of ripple counter.

A binary ripple counter consists of a series connection of complementing flip-flops (T or JK type), with the output of each flip-flop connected to the Clock Pulse input of the next higher-order flip-flop. The flip-flop holding the least significant bit receives the incoming count pulses. The diagram of a 4-bit binary ripple counter is shown in Fig. below. All J and K inputs are equal to 1



The small circle in the CP input indicates that the flip-flop complements during a negative-going transition or when the output to which it is connected goes from 1 to 0. The lowest-order bit Q_0 must be complemented with each count pulse. Every time Q_0 goes from 1 to 0, it complements Q_1. Every time Q_1 goes from 1 to 0, it complements Q_2, and so on.

Timing Diagram:



In timing diagram Q_0 is changing as soon as the negative edge of clock pulse is encountered, Q1 is changing when negative edge of Q_0 is encountered (because Q_0 is like clock pulse for second flip flop) and so on.

3. Prepare neat sketch for working of binary ladder network for digital to analog conversion.

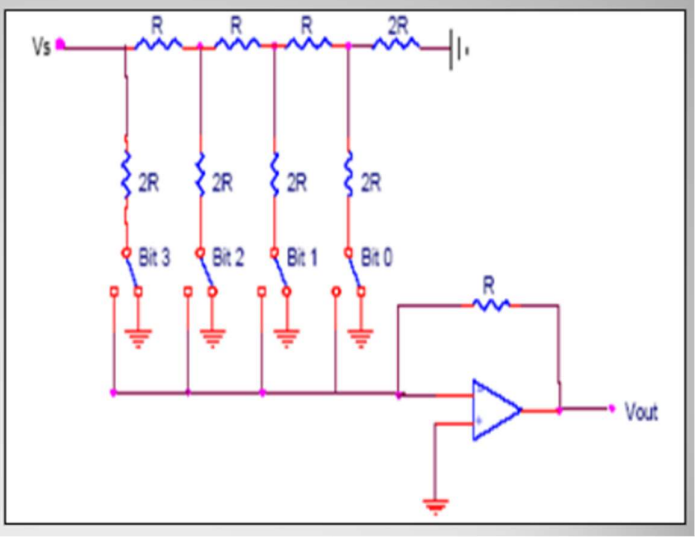
A digital to analog converter (DAC) is a device that converts digital numbers (binary) into an analog voltage or current output.

R-2R Ladder

Each bit corresponds to a switch:

If the bit is high, the corresponding switch is connected to the inverting input of the op-amp.

If the bit is low, the corresponding switch is connected to ground.



R-2R Ladder

For a 4-Bit R-2R Ladder

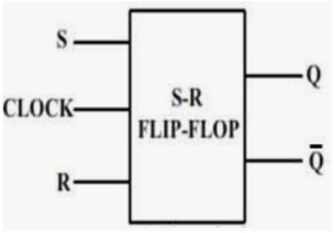
$$V_{out} = -V_{ref}\left(b_3\frac{1}{2} + b_2\frac{1}{4} + b_1\frac{1}{8} + b_0\frac{1}{16}\right)$$

For general n-Bit R-2R Ladder or Binary Weighted Resister DAC

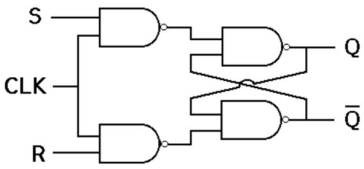
$$V_{out} = -V_{ref}\sum_{i=1}^{n} b_{n-i}\frac{1}{2^i}$$

4. Develop neat diagram operation of RS flip-flop with truth table and waveforms.

Symbol:



Logic Diagram



Truth Table:

Inputs		*Output*
S_n	R_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	–

Characteristics Table of SR Flip Flop:

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	×
1	1	1	×

The S-R flip flop is the most common flip flop used in the digital system. In SR flip flop, when the set input "S" is true, the output Y will be high, and Y' will be low.