# Homework 7

## Systolic Architecture Design

*(Deadline : 2022/12/15)*

**Implementation part**：

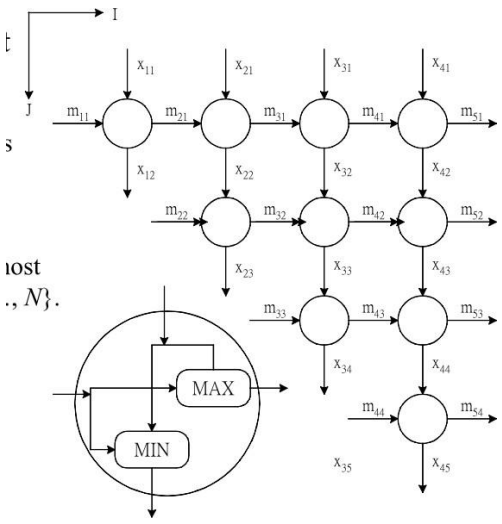
In computer and electronic engineering, bubble sorting is a common approach in sorting existing elements from high to low or low to high orientation. The method is popular because the original design is simple and efficient. The sort starts from the beginning of the element by swapping adjacent elements if the adjacent value order is not correct. After swapping every element in the array for several times, the low to high or high to low element array is detected. The pseudo-code for this algorithm is as follows :

(from wiki, http://en.wikipedia.org/wiki/Bubble_sort)

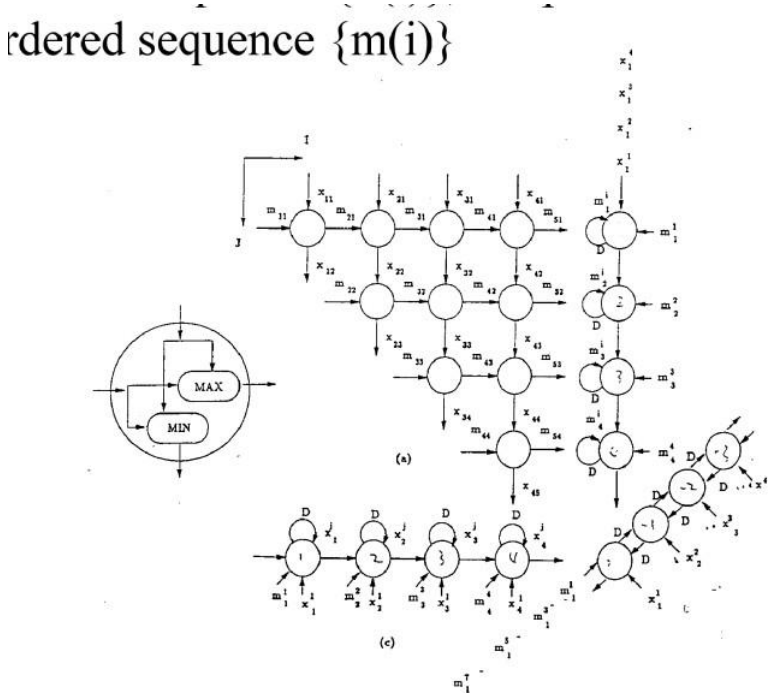
```
procedure bubbleSort( A : list of sortable items )
  n = length(A)
  do
    newn = 0
    for (i = 0; i < n-1; i++) do:
      if A[i] > A[i+1] then
        swap(A[i], A[i+1])
        newn = i + 1
      end if
    end for
    n = newn
  while n > 1
end procedure
```

Based on the algorithm, the DG and SG diagram is as follows：

DG:



SG:




Based on the three selected vectors, there are three implementations based on three vectors {0,1}, {1,0}, {1,1} with respect of {I,j} notation.

1. (50%)Please implement the original SG bubble sorting design and three projected SG designs. That is, please implement four different design of bubble sorting including original SG, and three projection vector {1,0},{0,1},{1,1}. Verify the behavior model.
2. (20%) Synthesize the designs and give the results from the synthesis. The synthesized waveform should also be provided, providing that the difference between the synthesized waveform and behavior model should be differentiated.
3. (30%) Compare the results. It is better to compare the results with “meaningful” explanation or theorem.
4. (15%, Additional) From the results above, what is the effect of different vectors, based on the theoretical algorithm’s perspective? For example, what are the efficiencies for different motion vectors? (This is an additional item, not necessary. The two items above are required, be aware please.)

此次作業需繳交：

1. RTL code(Verilog)
2. Top module testbench
3. Testbench 需加入 dump fsdb 或 vcd 指令
4. 書面紙本、書面電子檔(doc)、報告電子檔(ppt)
5. 檔名為：學號_VDSP111_HW7(ex: 111521001_VDSP111_HW7.rar)

6. 檔名為：學號_VDSP111_HW7 (ex: 111521001_VDSP111_HW7.rar)
7. 壓縮檔-檔案結構：

RTL(資料夾)：include RTL code
sim(資料夾)：include testbench
學號_VDSP111_HW7.ppt
學號_VDSP111_HW7.doc

如有任何疑問，可至 E1-410 詢問助教，或透過以下信箱
詢問 助教信箱: 110521027@cc.ncu.edu.tw