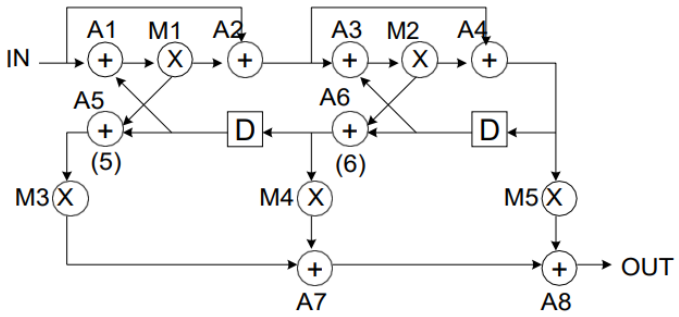
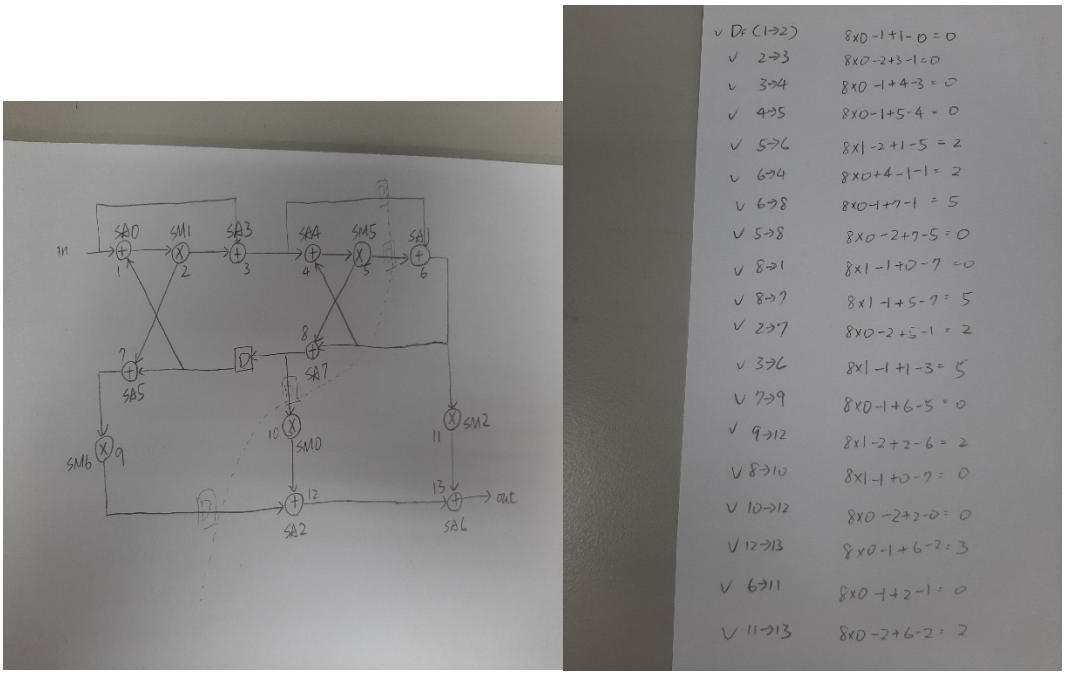
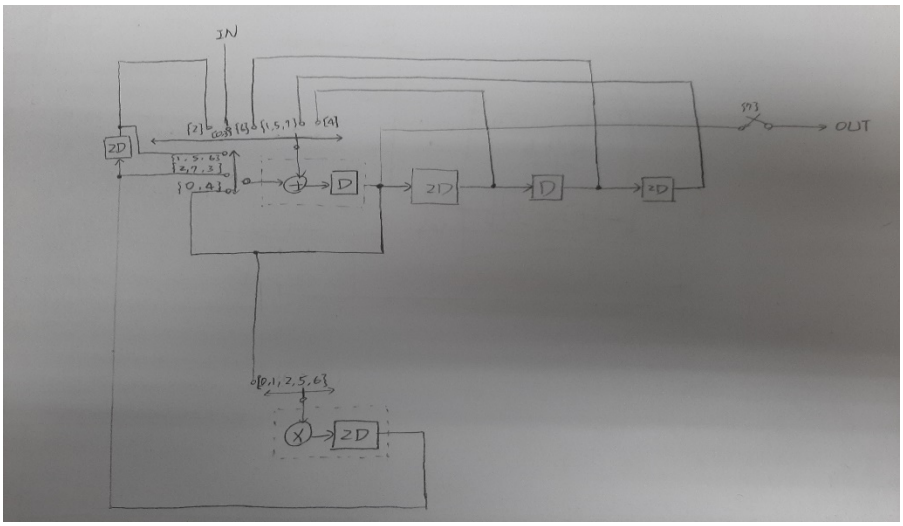
1.



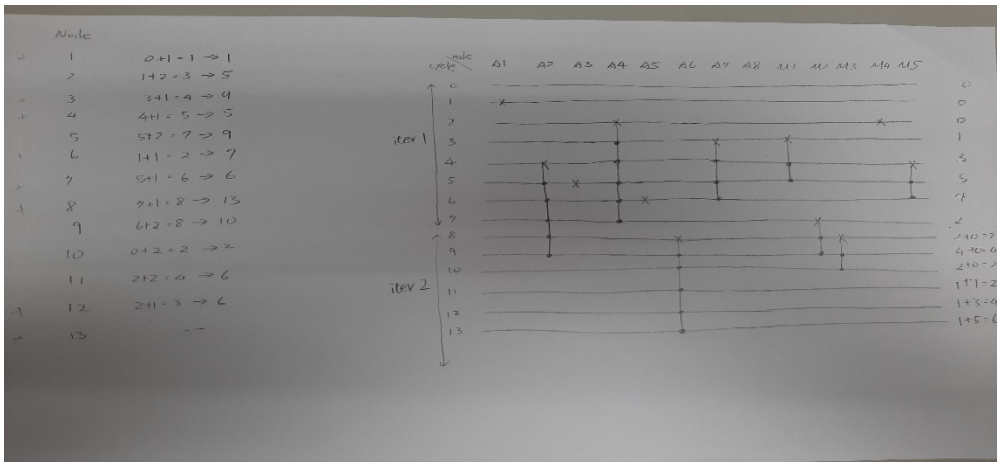
(a)

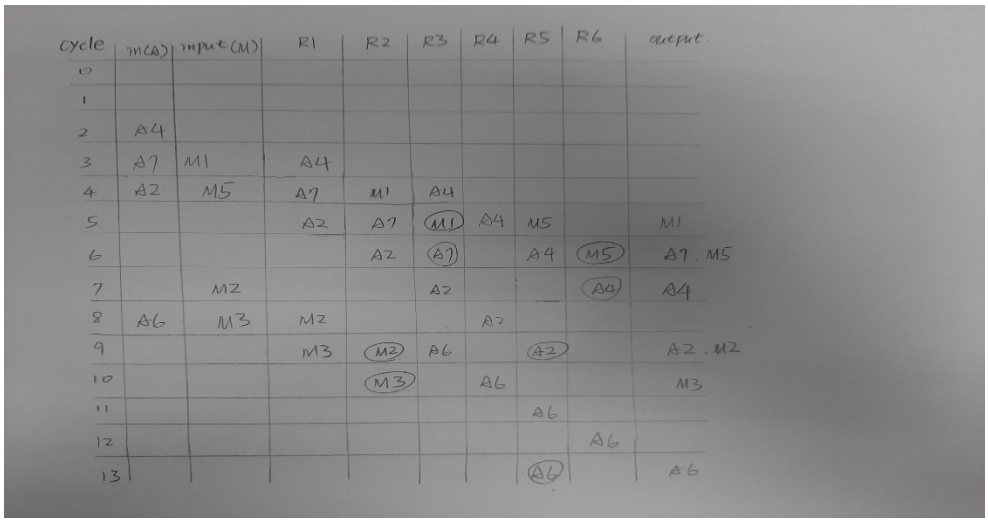


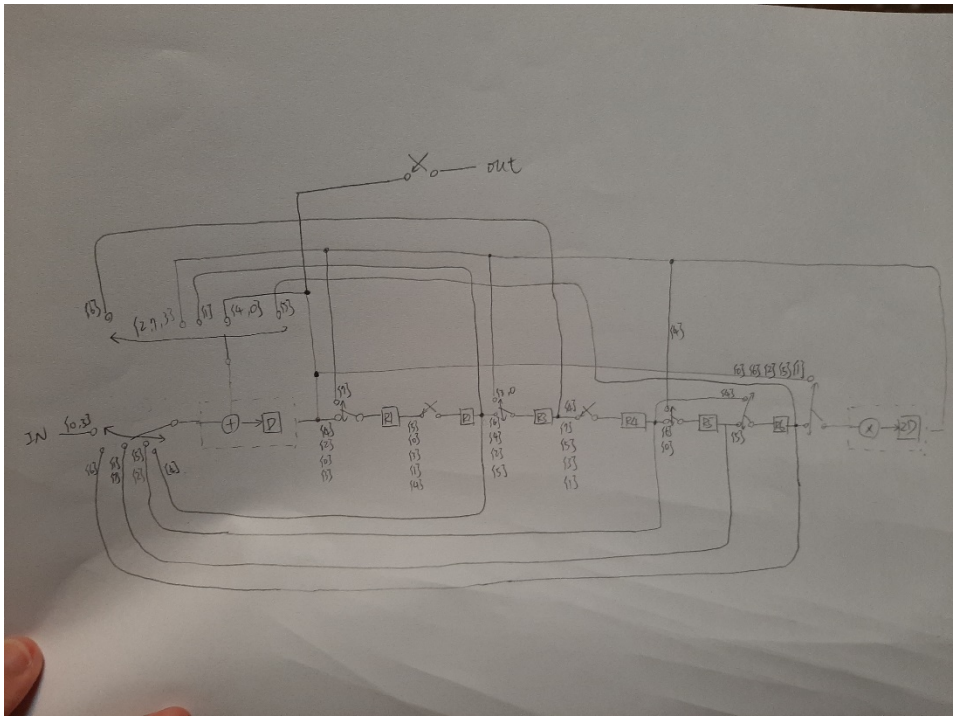
(b)



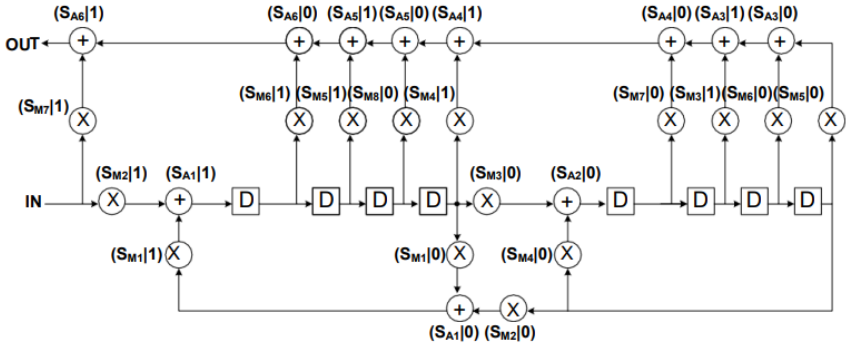
(c)


Node
cycle
node
iter 1
iter 2


cycle
input(A)
input(M)
R1
R2
R3
R4
R5
R6
output

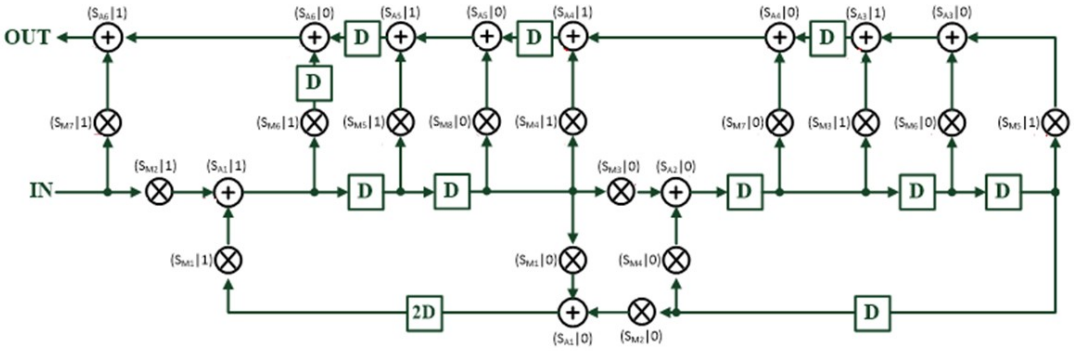

out
IN

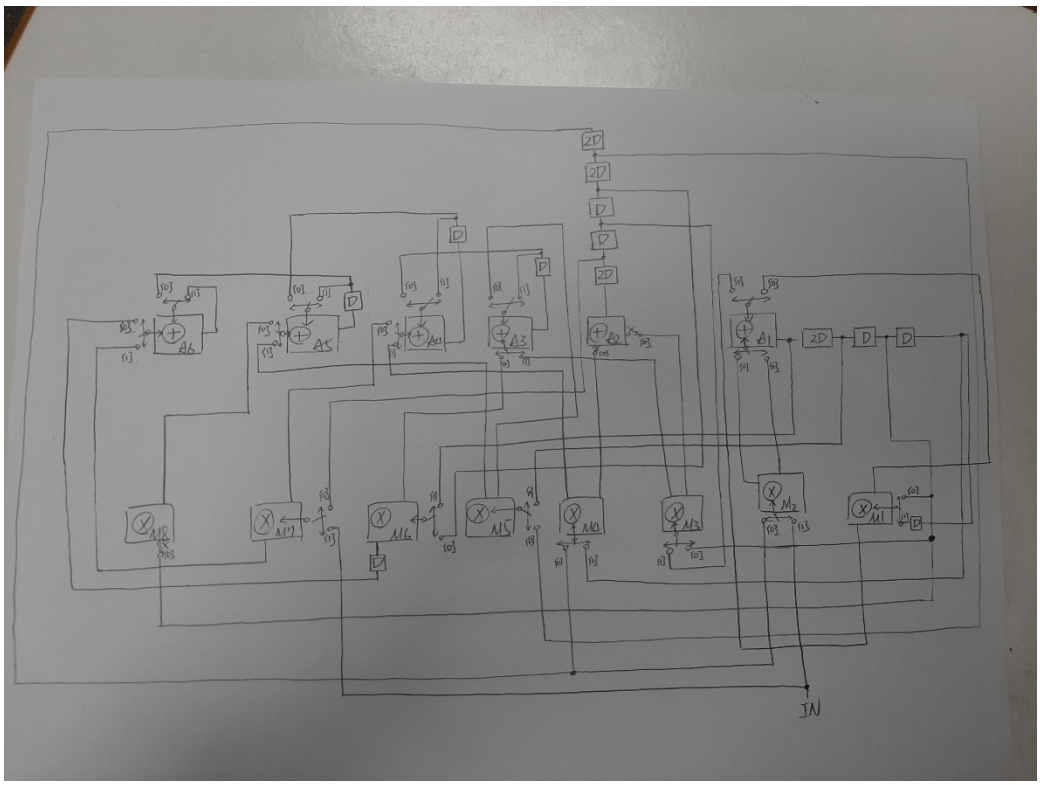
2.



Fold the lattice filter shown in Fig. 6.34 using folding factor *N*=2.

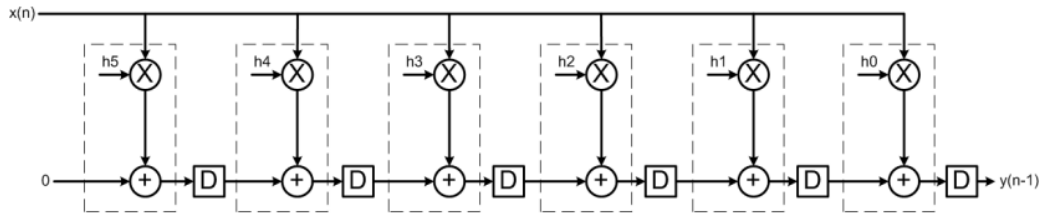
Perform retiming for folding if necessary.



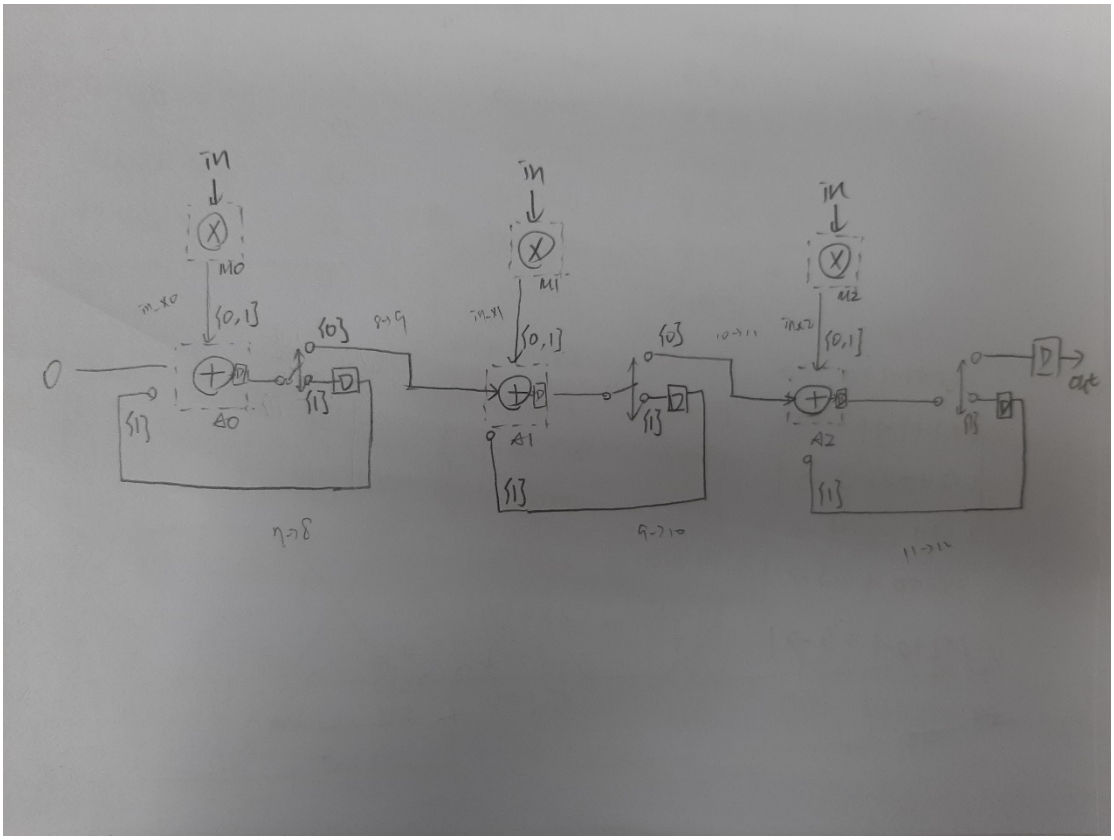


3.

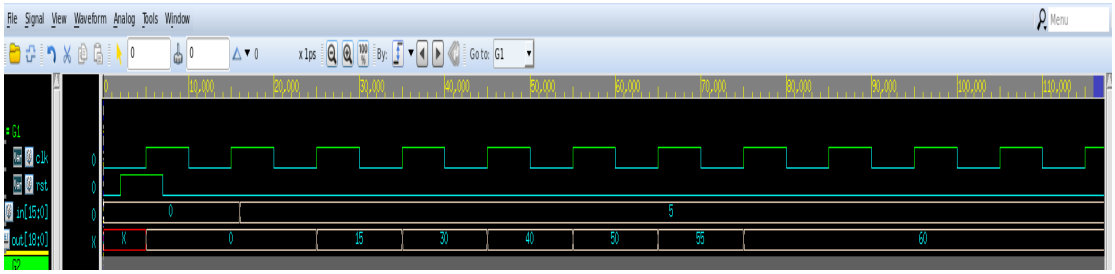
如下圖所示之 6-tap data-broadcast FIR filter，以 folding factors 2 和來實現 folding 電路。

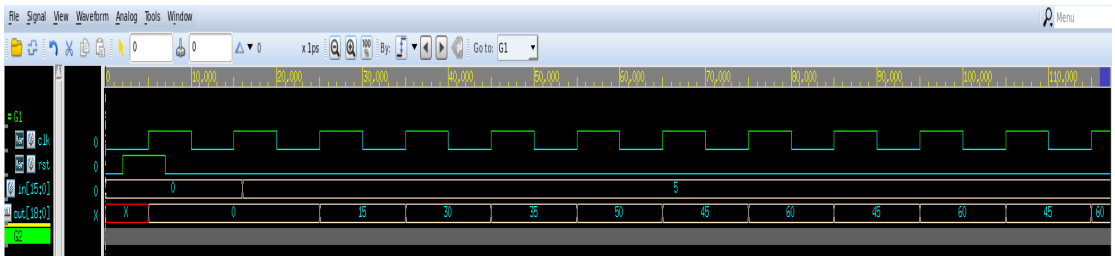


經過 folding 後的結構如下圖：



waveform(original vs folding)





area(original vs folding)

```
Report : area
Design : top
Version: R-2020.09
Date   : Wed Dec  7 21:15:49 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                         1429
Number of nets:                          3758
Number of cells:                         2311
Number of combinational cells:           2159
Number of sequential cells:               114
Number of macros/black boxes:               0
Number of buf/inv:                        476
Number of references:                      23

Combinational area:          19380.913141
Buf/Inv area:                 1928.246364
Noncombinational area:        3413.471436
Macro/Black Box area:            0.000000
Net Interconnect area:     undefined  (No wire load specified)

Total cell area:             22794.384577
Total area:                undefined
```

```
Report : area
Design : top
Version: R-2020.09
Date   : Wed Dec  7 21:20:49 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          613
Number of nets:                          2086
Number of cells:                         1484
Number of combinational cells:           1382
Number of sequential cells:                77
Number of macros/black boxes:               0
Number of buf/inv:                        305
Number of references:                      45

Combinational area:          12292.570731
Buf/Inv area:                 1184.785178
Noncombinational area:        2464.624828
Macro/Black Box area:            0.000000
Net Interconnect area:     undefined  (No wire load specified)

Total cell area:             14757.195559
Total area:                undefined
```

timing(original vs folding)

```
clock clk (rise edge)                                   2.50       2.50
clock network delay (ideal)                             0.50       3.00
clock uncertainty                                      -0.10       2.90
D4/q_reg[17]/CK (DFFTRX4)                               0.00       2.90 r
library setup time                                     -0.15       2.75
data required time                                                 2.75
--------------------------------------------------------------------------
data required time                                                 2.75
data arrival time                                                 -2.75
--------------------------------------------------------------------------
slack (MET)                                                        0.00
```

```
clock clk (rise edge)                                   2.60       2.60
clock network delay (ideal)                             0.50       3.10
clock uncertainty                                      -0.10       3.00
in_y2_reg[17]/CK (DFFRX4)                               0.00       3.00 r
library setup time                                     -0.17       2.83
data required time                                                 2.83
--------------------------------------------------------------------------
data required time                                                 2.83
data arrival time                                                 -2.83
--------------------------------------------------------------------------
slack (MET)                                                        0.00
```

power(original vs folding)

```
                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register           1.1919        9.6388e-02          3.4148e+06            1.2918  (  58.38%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational      0.5288           0.3777          1.4463e+07             0.9210  (  41.62%)
--------------------------------------------------------------------------------------------------
Total              1.7207 mW        0.4741 mW       1.7878e+07 pW          2.2127 mW
```

```
                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register           0.9307        8.9064e-02          2.4279e+06            1.0222  (  57.35%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational      0.4311           0.3198          9.2555e+06             0.7602  (  42.65%)
--------------------------------------------------------------------------------------------------
Total              1.3618 mW        0.4089 mW       1.1683e+07 pW          1.7824 mW
```

4. 結論

	Area(um^2)	Time(ns)	Power(mW)
Original	22794.384577	2.75	2.2127
2-folding	14757.195559	2.83	1.7824

經過 folding 折疊後，會根據 folding factor 而使面積越來越小
折疊後 D-flip flop 數量從 6 變成 4，另外還會額外多出 counter 的組合邏輯面積

時間的部分，因為折疊後需要 N 次 interation 才能完成原本一次 iteration 的計算量，所以 throughput 下降很多