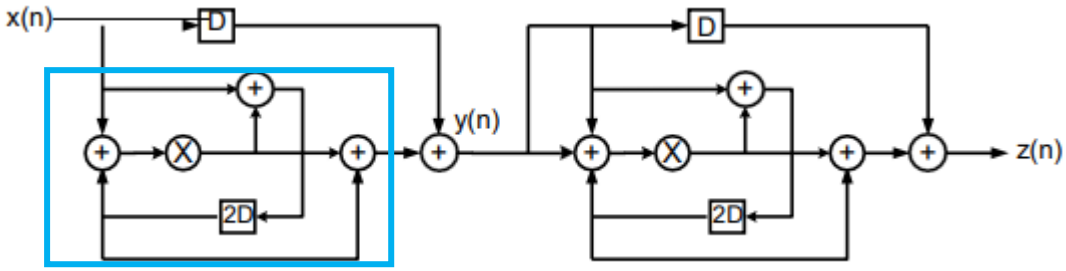
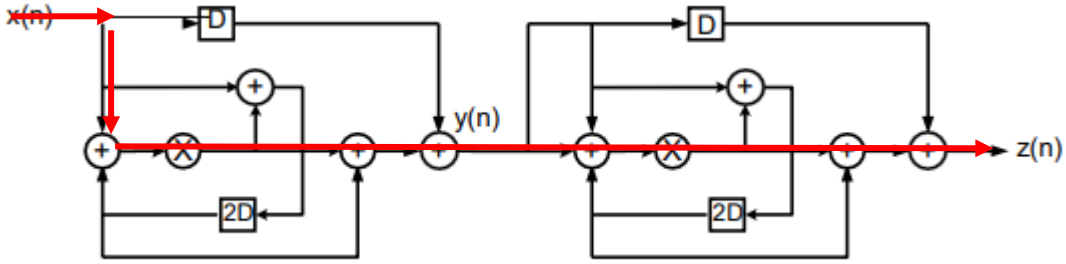
1.

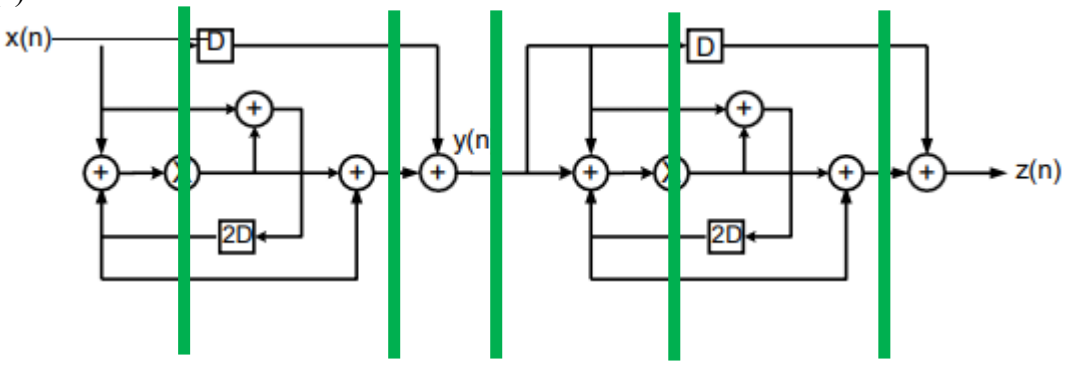
(a) iteration bound = 36/2 = 18ns



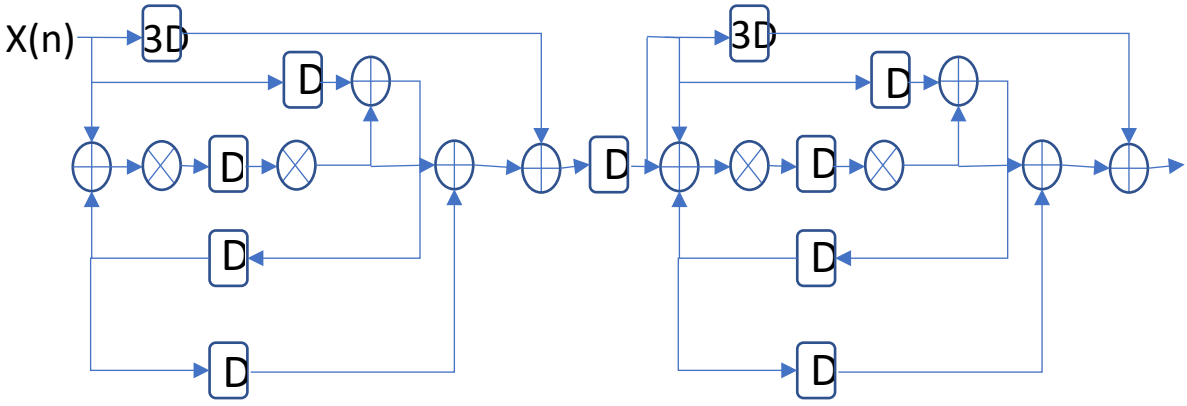
(b) critical path = 88ns



(c)



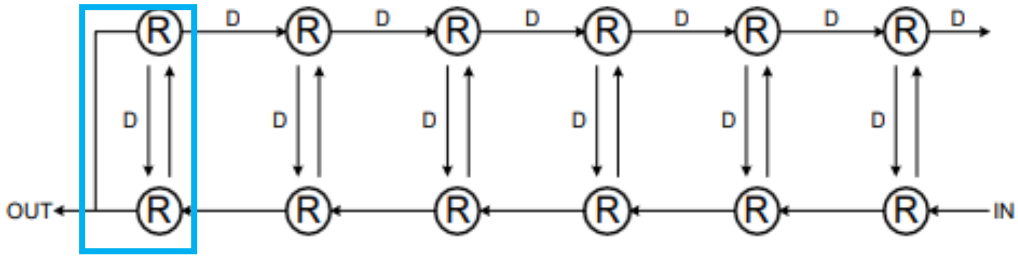
pipeline and retime :



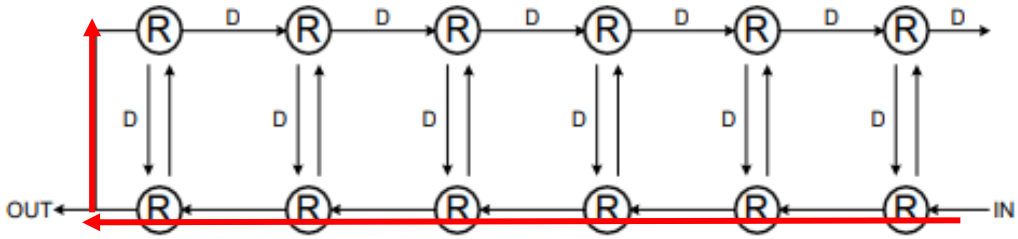
critical path = 18ns

2.

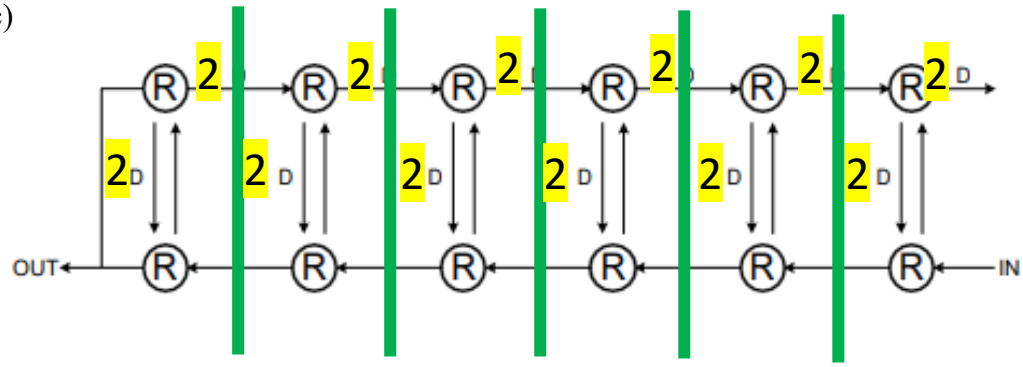
(a) iteration bound = 2T ns



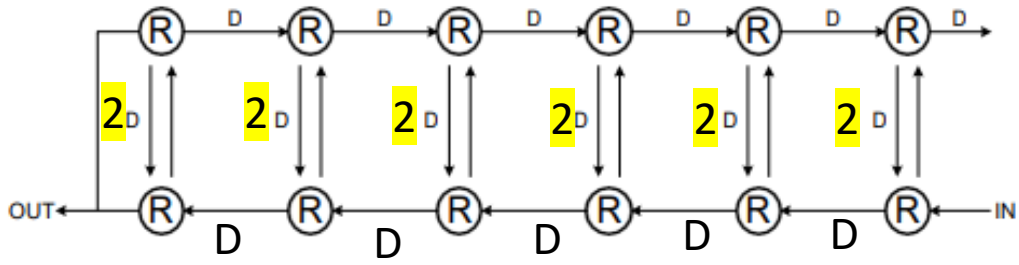
(b) critical path = 7T ns



(c)



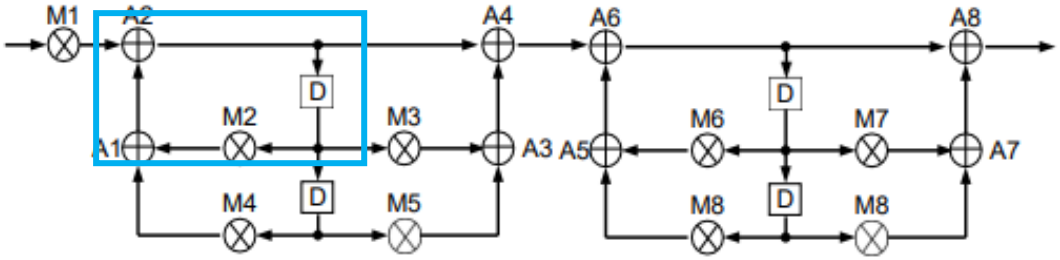
pipeline and retiming :



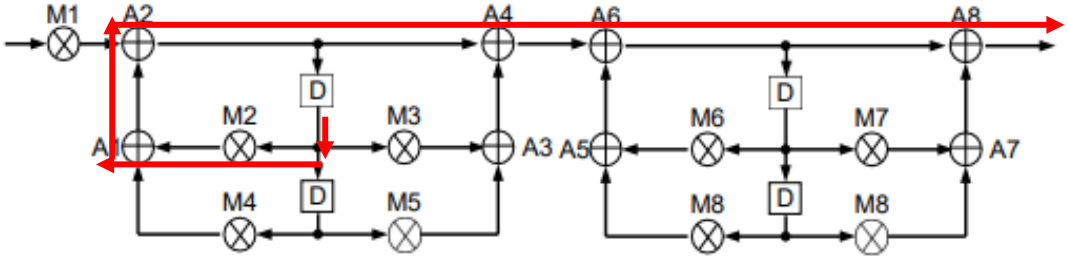
critical path = 2T ns

3.

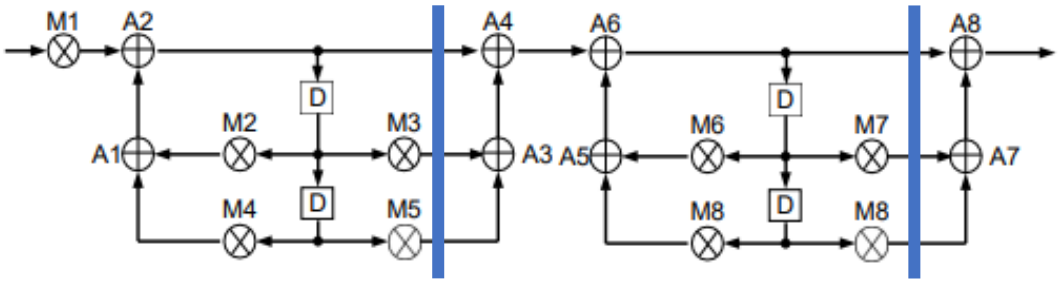
(a) iteration bound = 4



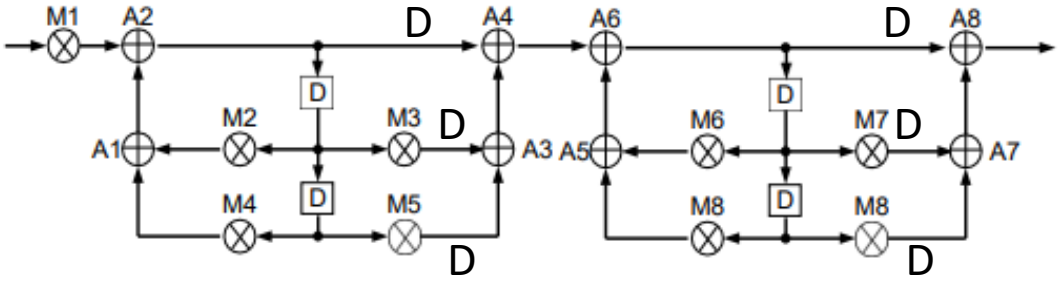
(b) critical path = 7



(c)



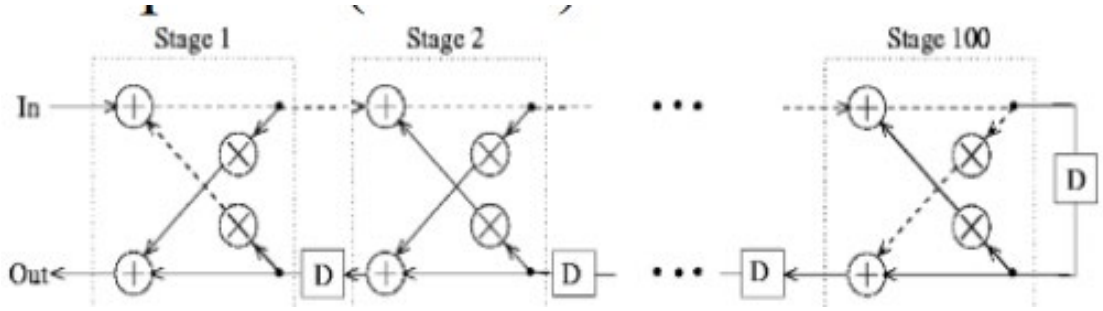
pipeline and retiming :



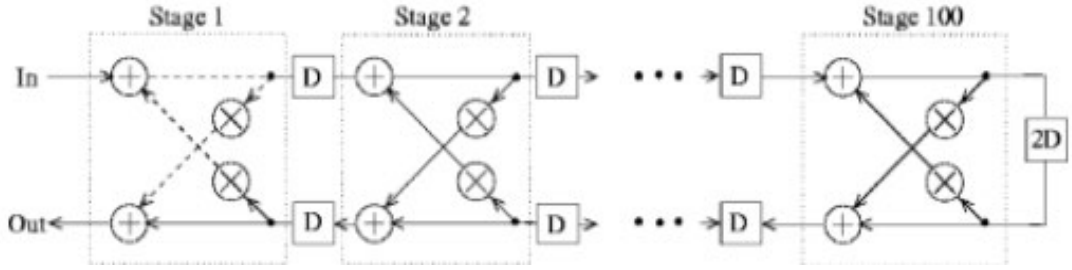
critical path = 4

4. 10-stage lattice filter

(A)



(C)



(A)是原本的架構 (C)為經過 2-slow version 的 retiming 架構

(A)波型 vs (C)波型：

(A)時間 vs (C)時間

```
clock clk (rise edge)                                   6.80       6.80
clock network delay (ideal)                             0.50       7.30
clock uncertainty                                      -0.10       7.20
D1/q_reg[19]/CK (DFFTRX4)                               0.00       7.20 r
library setup time                                     -0.14       7.06
data required time                                                 7.06
--------------------------------------------------------------------------
data required time                                                 7.06
data arrival time                                                 -7.06
--------------------------------------------------------------------------
slack (MET)                                                        0.00
```

```
clock clk (rise edge)                                   4.75       4.75
clock network delay (ideal)                             0.50       5.25
clock uncertainty                                      -0.10       5.15
D16/q_reg[19]/CK (DFFTRX4)                              0.00       5.15 r
library setup time                                     -0.16       4.99
data required time                                                 4.99
--------------------------------------------------------------------------
data required time                                                 4.99
data arrival time                                                 -4.99
--------------------------------------------------------------------------
slack (MET)                                                        0.00
```

(A)面積 vs (C)面積

```
Combinational area:              28735.284497
Buf/Inv area:                     3313.324739
Noncombinational area:            5864.517105
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 34599.801602
Total area:                 undefined
```

```
Number of ports:                          2908
Number of nets:                           4973
Number of cells:                          1979
Number of combinational cells:            1506
Number of sequential cells:                400
Number of macros/black boxes:                0
Number of buf/inv:                         267
Number of references:                       33

Combinational area:              26246.895966
Buf/Inv area:                     1890.903569
Noncombinational area:           11871.615778
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 38118.511744
Total area:                 undefined
```

(A)功率 vs (C)功率

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	0.7306	7.9714e-02	5.9181e+06	0.8163	(44.95%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	0.5394	0.4369	2.3380e+07	0.9997	(55.05%)	
Total	1.2701 mW	0.5166 mW	2.9298e+07 pW	1.8160 mW		

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	1.9581	9.5838e-02	1.2112e+07	2.0661	(78.54%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	0.3656	0.1692	2.9840e+07	0.5646	(21.46%)	
Total	2.3237 mW	0.2650 mW	4.1952e+07 pW	2.6307 mW		

5. 結論

	Area(um^2)	Time(ns)	Power(mW)
Original	34599.801602	7.06	1.8160
2-slow retiming	38118.511744	4.99	2.6307