Homework 4

Retiming

(Due : 2022/11/10)

1. Consider the wave digital filter shown in Fig. 4.15. Assume that each multiply operation requires 20 nsec and each add operation requires 8 nsec.

(a) Calculate the iteration period bound of this filter by inspection.

(b) What is the circuit path?

(c) Manually pipeline and/or retime this filter to achieve a critical path equal to iteration period bound.

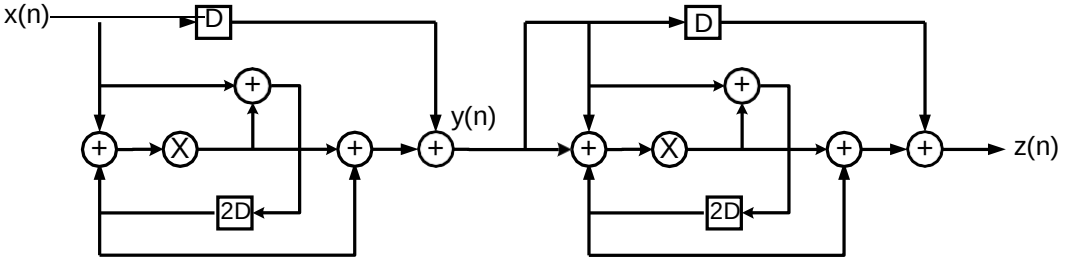


Fig 4.15 The wave digital filter structure in Problem 1.

2. Consider the 6th-order orthogonal filter structure shown in Fig. 4.18. All operations in this structure are CORDIC (coordinate rotation digital computer) rotation operations, which are orthogonal. Assume that each CORDIC rotation operation requires T nsec.

   What is the iteration bound of this filter? What is the critical path of this filter? Manually pipeline and/or retime the filter structure to achieve a critical path of computation 2T nsec. Show all the cutest locations used for retiming explicitly.

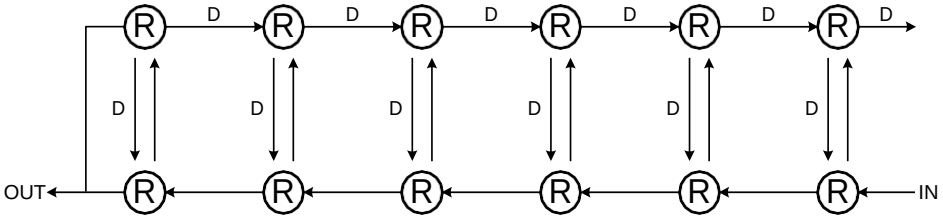
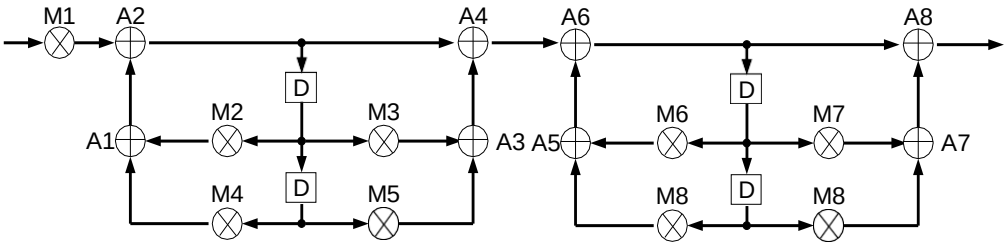


Fig. 4.18 The DFG for the 4th-order IIR filter in Problem 2.

3. The DFG shown in Fig. 4.19 describes a 4th-order IIR digital filter implemented as cascade of 2 2nd-order sections. Assume each multiply requires 2 u.t. and add requires 1 u.t. .

(a) What is the critical path of this DFG? What is the iteration bound of this DFG?

(b) Manually retime and pipeline the DFG to minimize the clock period. What is the minimum achievable clock period obtained with pipelining and retiming?



4. Verilog-HDL Design:

在課本第 4 章 Fig. 4.7 中，圖(a)與(c)分別為 100-stage lattice filter 與 retiming 之後的 100 stage lattice filter。請實現圖(a)與(c)的電路，其中 stage 請自選 10~100。

作業要求：

原始電路與 parallel 電路的 RTL-level function 驗證無誤並比較兩者之間的差異性。

以 Design Compiler 合成後，gate-level function 驗證無誤。

比較合成之後，兩者的面積(area)、速度(timing)與功率消耗(power consumption)。

此次作業需繳交：

1. RTL code(Verilog)
2. Top module testbench
3. Testbench 需加入 dump fsdb 或 vcd 指令
4. 書面紙本、書面電子檔(doc)、報告電子檔(ppt)
5. 檔名為：學號_VDSP111_HW4 (ex: 111521001_VDSP111_HW4.rar)
6. 檔名為：學號_VDSP111_HW4 (ex: 111521001_VDSP111_HW4.rar)
7. 請註明使用 NCVerilog 或 VCS 做 function 模擬，並以文字檔(sim_cmd.txt)附上模擬時所下的指令
8. 壓縮檔-檔案結構：

RTL(資料夾)：include RTL code

sim(資料夾)：include testbench and sim_cmd.txt

學號_VDSP111_HW4.ppt

學號_VDSP111_HW4.doc

如有任何疑問，可至 E1-410 詢問助教，或透過以下信箱

詢問 助教信箱: 110521027@cc.ncu.edu.tw