Homework 6

Folding

(Due : 2022/12/08)

1. For the lattice filter in Fig. 6.33, let the folding factor be *N*=8 and the folding sets be

$$S_A = \{A_1, A_4, A_7, A_2, A_3, A_5, A_8, A_6\}$$
$$S_M = \{M_4, M_1, M_5, \emptyset, \emptyset, M_2, M_3, \emptyset\}$$

Assume that addition and multiplication require 1 and 2 units of time, respectively.

(a) Perform retiming for folding so that all folded edges contain nonnegative delays.

(b) Synthesize the folded architecture for this system.

(c) Using lifetime analysis, minimize the number of delay elements used in this architecture. Allocate the variables to the minimum number of delay elements using forward-backward allocation. Redraw the folded synthesized architecture.

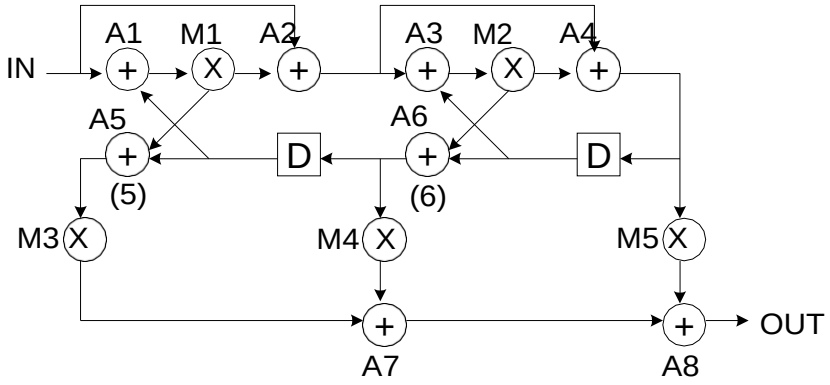


Fig. 6.33 The lattice filter

2. Fold the lattice filter shown in Fig. 6.34 using folding factor *N*=2.
   Perform retiming for folding if necessary.

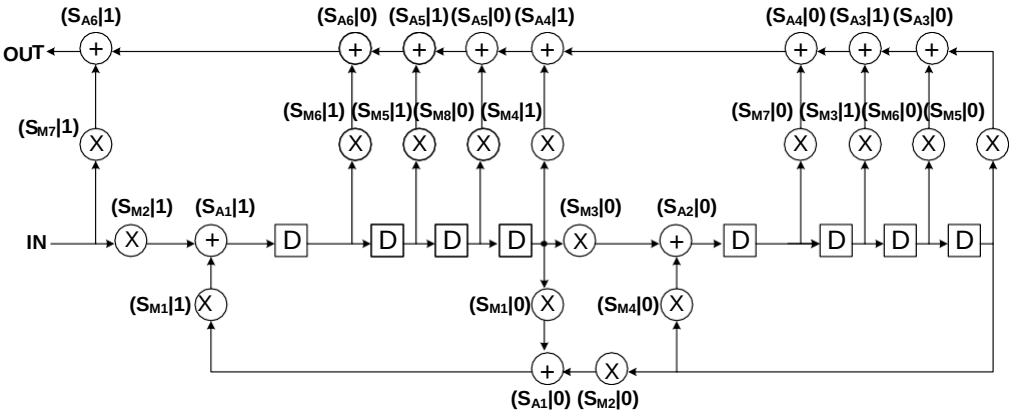
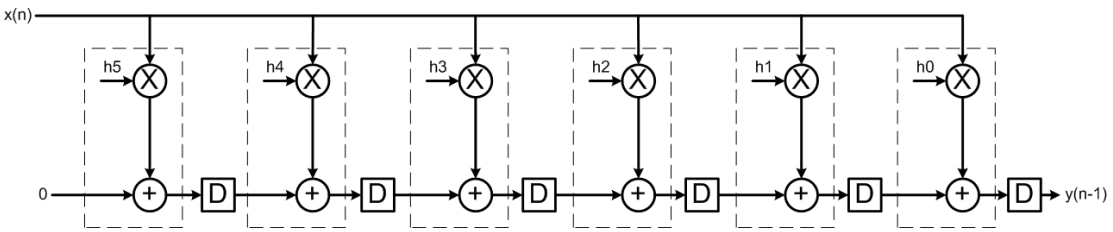


Fig. 6.34 The normalized lattice filter

3. Verilog-HDL Design:

如下圖所示之 6-tap data-broadcast FIR filter，以 folding factors 2 和來實現 folding 電路。



作業要求：

(1) 電路的 RTL-level function 驗證無誤

(2) 比較原始電路與 folding 之後電路的差異。

(3) 以 Design Compiler 合成後，gate-level function 驗證無誤。

(4) 比較合成之後，面積(area)、速度(timing)與功率消耗(power consumption)。

此次作業需繳交：

1. RTL code(Verilog)

2. Top module testbench

3. 書面紙本、書面電子檔(doc)、報告電子檔(ppt)

4. 檔名為：學號_VDSP111_HW6(ex: 111521001_VDSP111_HW6.rar)

5. 壓縮檔-檔案結構：

RTL(資料夾)：include RTL code
sim(資料夾)：include testbench
學號_VDSP111_HW6.ppt
學號_VDSP111_HW6.doc

如有任何疑問，可至 E1-410 詢問助教，或透過以下信箱
詢問 助教信箱: 110521027@cc.ncu.edu.tw