Homework 5

Unfolding

(Due : 2021/11/17)

1. Unfold the DFG in Fig. 5.21 using unfolding factors 2 and 5

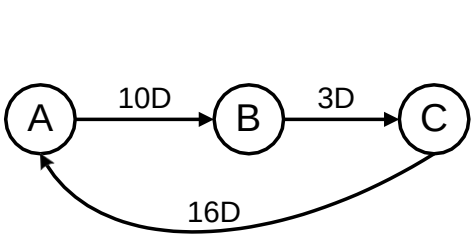


Fig. 5.21(a)

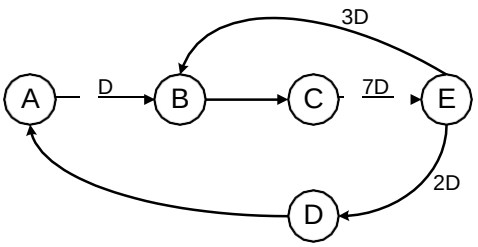


Fig. 5.21 (b)

2. For the DFG in Fig. 5.25, find the minimum unfolding factor J such that the J-unfolded DFG can retimed so that the critical path of this unfolded and retimed DFG is JT_{∞}. Assume that addition and multiplication require 1 and 2 u.t., respectively.

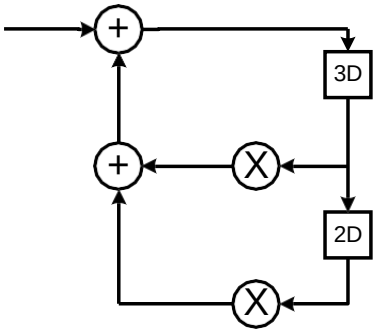


Fig. 5.25

3. This problem address loop unfolding (unrolling) in software in order to maximize the hardware utilization efficiency for fixed hardware structure, and a given algorithm (program). It exploits unfolding for parallel computation for a problemmable DSP (PDSP) with three MAC (multiply-accumulate) units. Our objective is to use unfolding to maximize the hardware utilization in parallel FIR filtering applications with the PDSP architecture in Fig 5.27. This PDSP has a data bottleneck, i.e., we can fetch only one input operand in each clock cycle from the random access memory (RAM) representing the inputs. Assume that only the input data need to be fetched through this data bus, which creates the bottleneck, while filter coefficients are stored in other local memory units(s) and can be accessed by each MAC unit freely during the clock cycle. Draw a schedule

for a 7-tap FIR filter computation with appropriate unfolding factor so that hardware utilization efficiency is maximized.

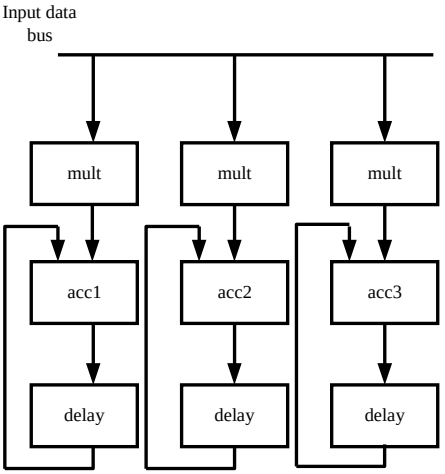
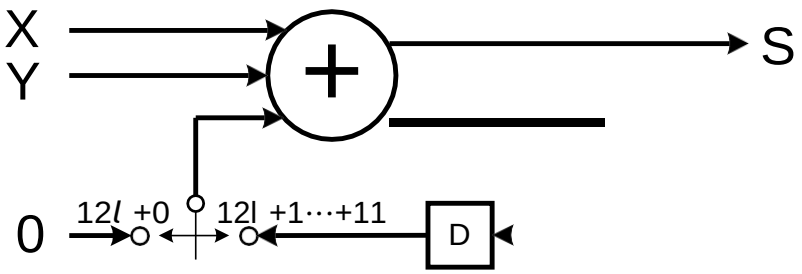


Fig 5.27 The PDSP architecture

4. Verilog-HDL Design:

如下圖所示之 bit-serial adder，以 unfolding factors 4 和 5 來實現其 digit-serial adders，其 word-length 為 12 bits。



作業要求：

(1) 電路的 RTL-level function 驗證無誤

(2) 比較原始電路與 unfold 之後電路的差異。

(3) 以 Design Compiler 合成後，gate-level function 驗證無誤。

(4) 比較合成之後，面積(area)、速度(timing)與功率消耗(power consumption)。

此次作業需繳交：

1. RTL code(Verilog)
2. Top module testbench
3. 書面紙本、書面電子檔(doc)、報告電子檔(ppt)
4. 檔名為：學號_VDSP111_HW5 (ex: 111521001_VDSP111_HW5.rar)
5. 檔名為：學號_VDSP111_HW5 (ex: 111521001_VDSP111_HW5.rar)
6. 壓縮檔-檔案結構：

RTL(資料夾)：include RTL code

sim(資料夾)：include testbench
學號_VDSP111_HW5.ppt
學號_VDSP111_HW5.doc

如有任何疑問，可至 E1-410 詢問助教，或透過以下信箱
詢問 助教信箱: 110521027@cc.ncu.edu.tw