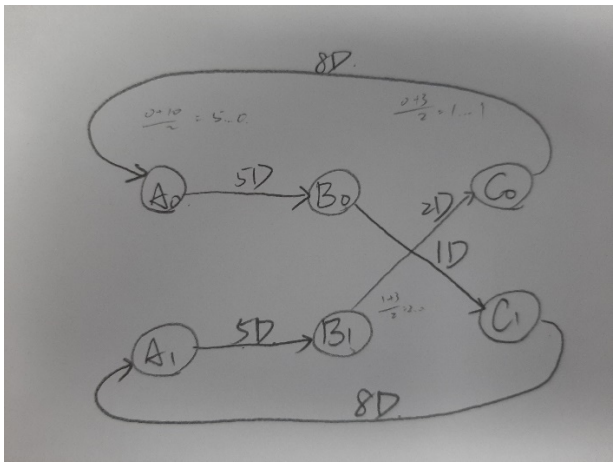
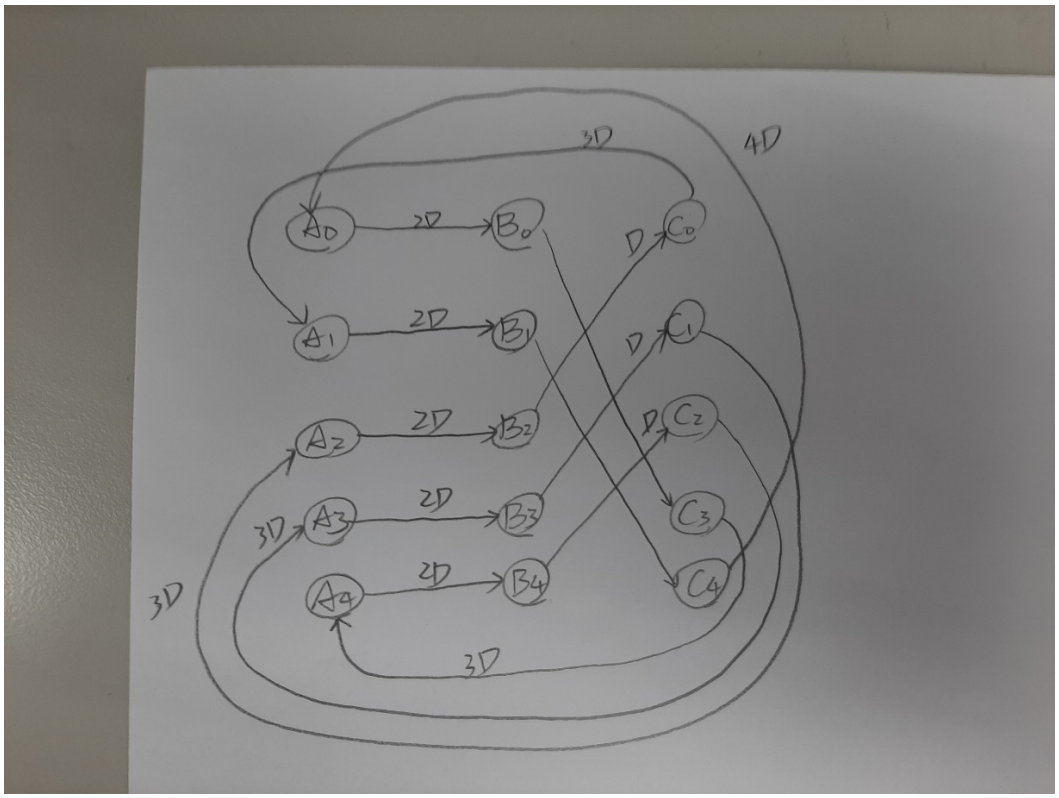
1.

(a)

factor = 2

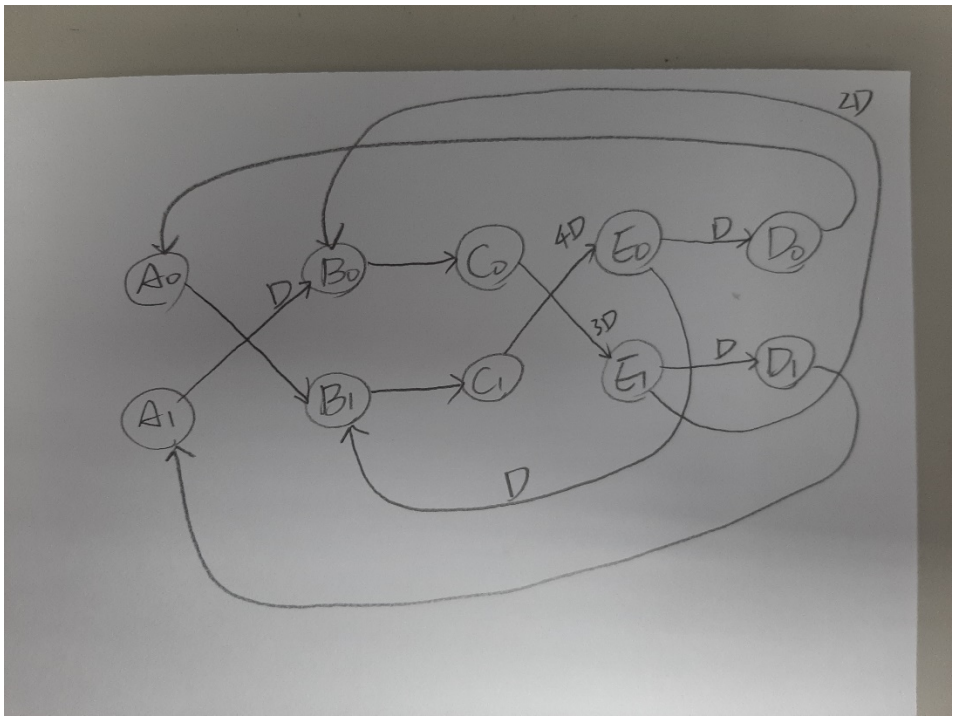


factor = 5

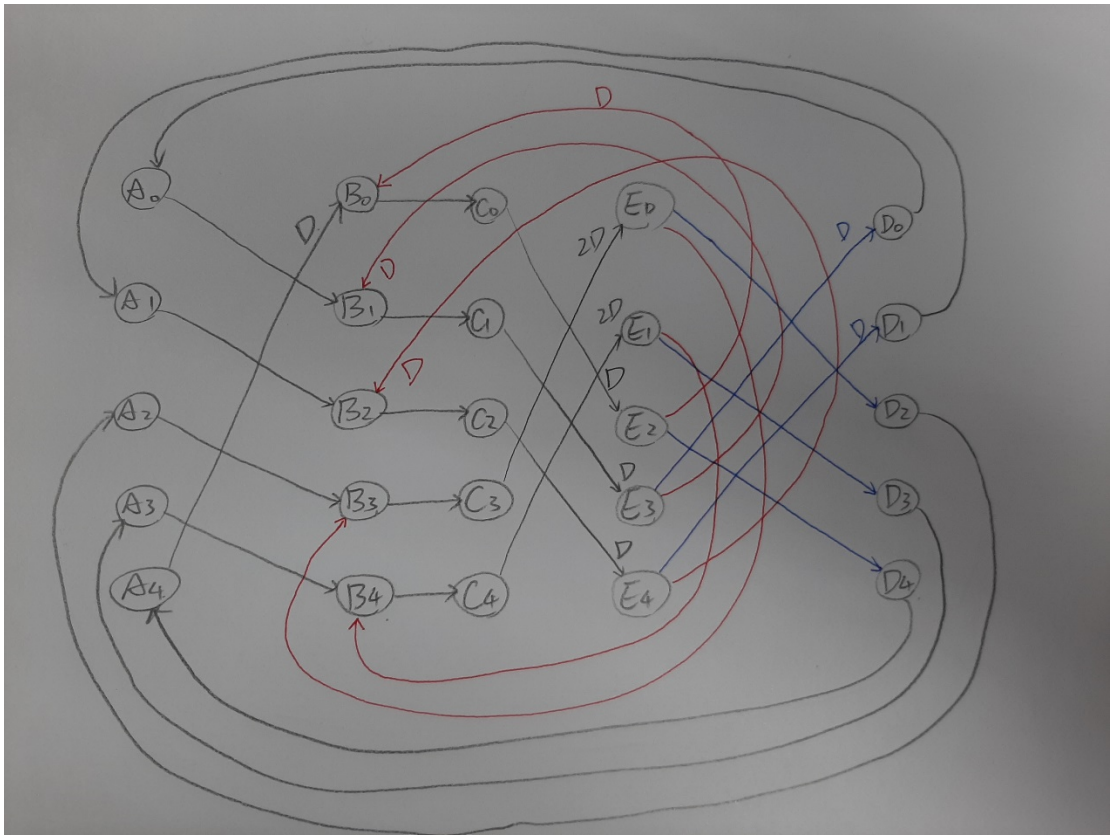


(b)

factor = 2



factor = 5



2.

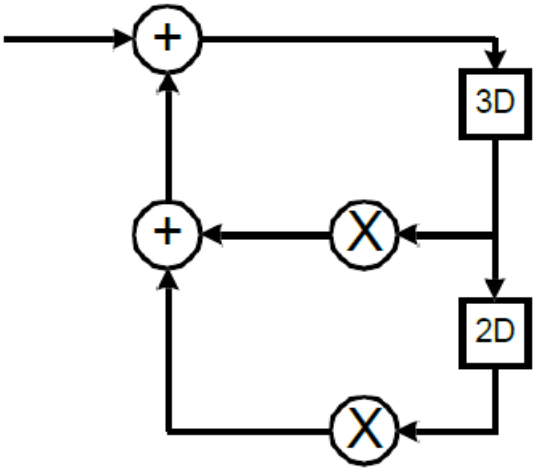


Fig. 5.25

max{4/3,4/5} = 4/3

分母即為要取的 unfolding factor

3-unfolding

3.

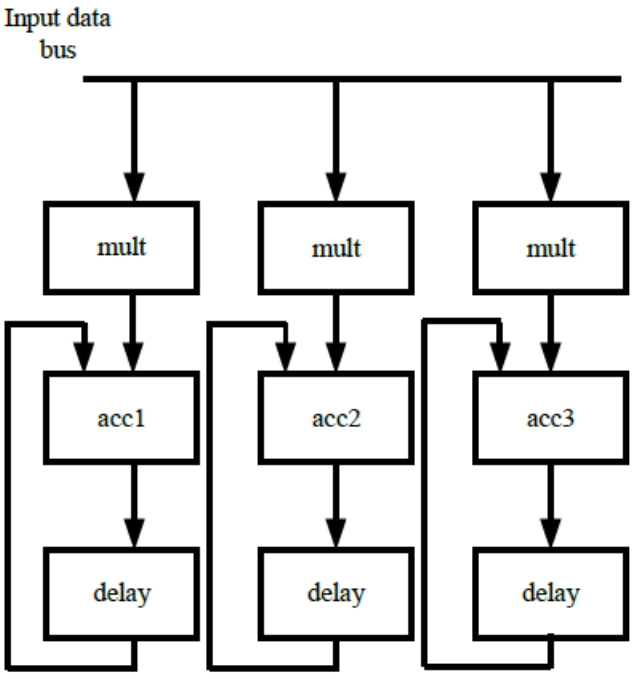
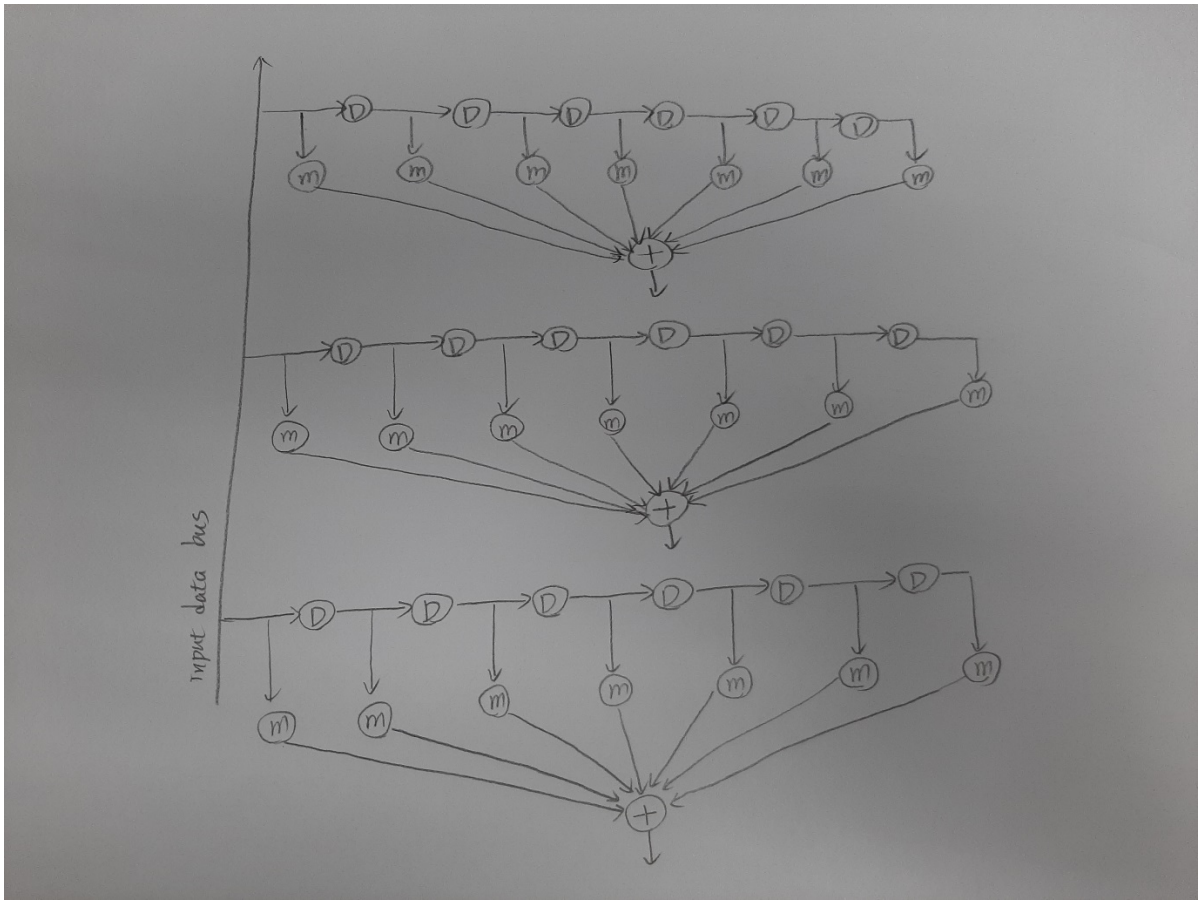


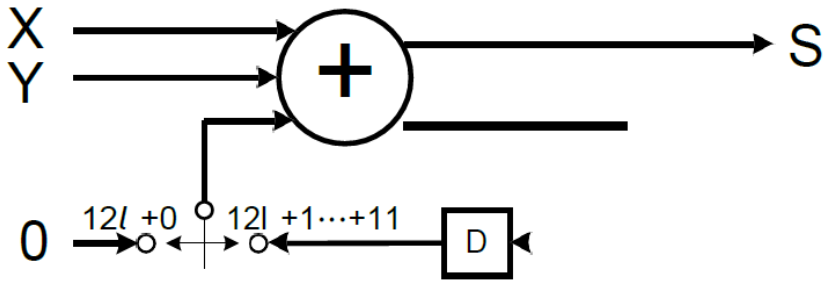
Fig 5.27 The PDSP architecture

For a 7-tap FIR filter computation with 7-unfolding :

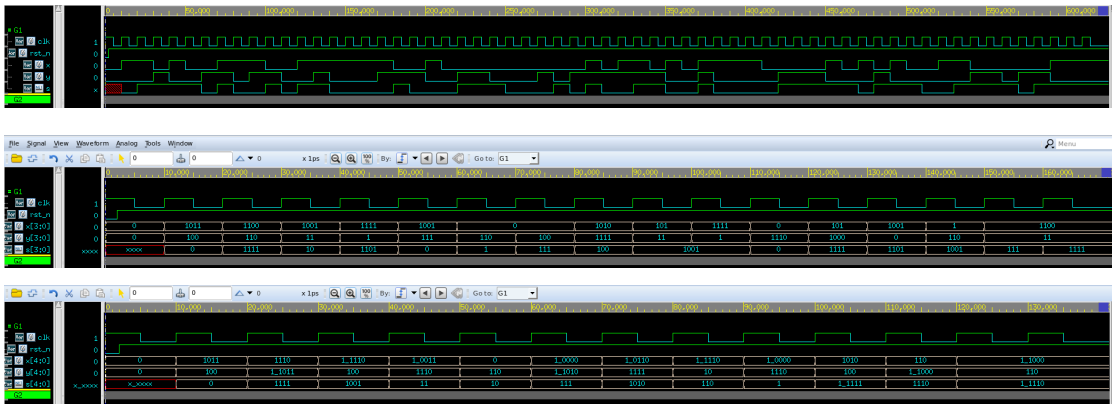


4.

如下圖所示之 bit-serial adder，以 unfolding factors 4 和 5 來實現其 digit-serial adders，其 word-length 為 12 bits。



waveform (original vs 4-unfolding vs 5-unfolding):



timing (original vs 4-unfolding vs 5-unfolding):

```
Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (ideal)              0.50       0.50
in_c_reg/CK (DFFRX1)                     0.00       0.50 r
in_c_reg/Q (DFFRX1)                      0.52       1.02 f
F0/cin (fa)                              0.00       1.02 f
F0/U2/Y (XOR2X1)                         0.15       1.17 f
F0/U1/Y (AO22X1)                         0.59       1.76 f
F0/cout (fa)                             0.00       1.76 f
c (out)                                  0.00       1.76 f
data arrival time                                   1.76

clock clk (rise edge)                    8.00       8.00
clock network delay (ideal)              0.50       8.50
clock uncertainty                       -0.10       8.40
output external delay                   -0.50       7.90
data required time                                  7.90
-----------------------------------------------------------
data required time                                  7.90
data arrival time                                  -1.76
-----------------------------------------------------------
slack (MET)                                         6.14
```

```
clock clk (rise edge)                          0.00       0.00
clock network delay (ideal)                    0.50       0.50
in_c_reg/CK (DFFRX1)                           0.00       0.50 r
in_c_reg/Q (DFFRX1)                            0.52       1.02 f
f0/cin (fa_3)                                  0.00       1.02 f
f0/U2/Y (XOR2X1)                               0.15       1.17 f
f0/U1/Y (AO22X1)                               0.34       1.51 f
f0/c (fa_3)                                    0.00       1.51 f
f1/cin (fa_2)                                  0.00       1.51 f
f1/U2/Y (XOR2X1)                               0.16       1.67 f
f1/U1/Y (AO22X1)                               0.34       2.01 f
f1/c (fa_2)                                    0.00       2.01 f
f2/cin (fa_1)                                  0.00       2.01 f
f2/U2/Y (XOR2X1)                               0.16       2.17 f
f2/U1/Y (AO22X1)                               0.34       2.51 f
f2/c (fa_1)                                    0.00       2.51 f
f3/cin (fa_0)                                  0.00       2.51 f
f3/U2/Y (XOR2X1)                               0.16       2.67 f
f3/U1/Y (AO22X1)                               0.59       3.26 f
f3/c (fa_0)                                    0.00       3.26 f
c (out)                                        0.00       3.26 f
data arrival time                                         3.26

clock clk (rise edge)                          8.00       8.00
clock network delay (ideal)                    0.50       8.50
clock uncertainty                             -0.10       8.40
output external delay                         -0.50       7.90
data required time                                       7.90
-----------------------------------------------------------------
data required time                                       7.90
data arrival time                                       -3.26
-----------------------------------------------------------------
slack (MET)                                              4.64
```

```
clock clk (rise edge)                          8.00       8.00
clock network delay (ideal)                    0.50       8.50
clock uncertainty                             -0.10       8.40
output external delay                         -0.50       7.90
data required time                                       7.90
-----------------------------------------------------------------
data required time                                       7.90
data arrival time                                       -3.76
-----------------------------------------------------------------
slack (MET)                                              4.14
```

area (original vs 4-unfolding vs 5-unfolding):

```
Number of ports:                           13
Number of nets:                            41
Number of cells:                           27
Number of combinational cells:             17
Number of sequential cells:                 9
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       9

Combinational area:                186.713998
Buf/Inv area:                        0.000000
Noncombinational area:             297.044994
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                   483.758993
Total area:                 undefined
```

```
Report : area
Design : top
Version: R-2020.09
Date   : Thu Nov 17 18:48:01 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           40
Number of nets:                            69
Number of cells:                           40
Number of combinational cells:             23
Number of sequential cells:                13
Number of macros/black boxes:               0
Number of buf/inv:                          1
Number of references:                      16

Combinational area:               220.661997
Buf/Inv area:                       3.394800
Noncombinational area:            446.416203
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  667.078199
Total area:                 undefined
```

```
Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           49
Number of nets:                            81
Number of cells:                           46
Number of combinational cells:             26
Number of sequential cells:                15
Number of macros/black boxes:               0
Number of buf/inv:                          1
Number of references:                      17

Combinational area:               254.609996
Buf/Inv area:                       3.394800
Noncombinational area:            517.707005
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  772.317000
```

power (original vs 4-unfolding vs 5-unfolding):

```
                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register       2.4435e-02       3.2644e-04          2.5684e+05         2.5018e-02  (  92.29%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational  1.0323e-03       8.5173e-04          2.0509e+05         2.0891e-03  (   7.71%)
--------------------------------------------------------------------------------------------------
Total          2.5467e-02 mW     1.1782e-03 mW     4.6193e+05 pW      2.7107e-02 mW
```

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	3.6306e-02	5.9708e-04	3.4464e+05	3.7247e-02	(88.27%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	1.7354e-03	2.9790e-03	2.3500e+05	4.9495e-03	(11.73%)	
Total	3.8041e-02 mW	3.5761e-03 mW	5.7963e+05 pW	4.2197e-02 mW		

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	4.1925e-02	6.1741e-04	3.9369e+05	4.2936e-02	(88.10%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	1.9923e-03	3.5284e-03	2.7903e+05	5.7997e-03	(11.90%)	
Total	4.3918e-02 mW	4.1458e-03 mW	6.7272e+05 pW	4.8736e-02 mW		

5. 結論

	Area(um^2)	Time(ns)	Power(mW)
Original	483.75	1.76	0.027107
4-unfolding	667.08	3.26	0.042197
5-unfolding	772.32	3.76	0.048736

經過 unfolding 展開後，會根據 unfolding factor 而使面積越來越大

雖然時間看似越來越長，但各個架構處理 word-length = 12 所需乘上的倍數不同

original : 1.76*12 = 21.12

4-unfolding : 3.26*3 = 9.78

5-unfolding : 3.76*2.4 = 9.024

所以展開後的 throughput 會變大

功率和面積相同，會隨著 unfolding factor 而越來越大