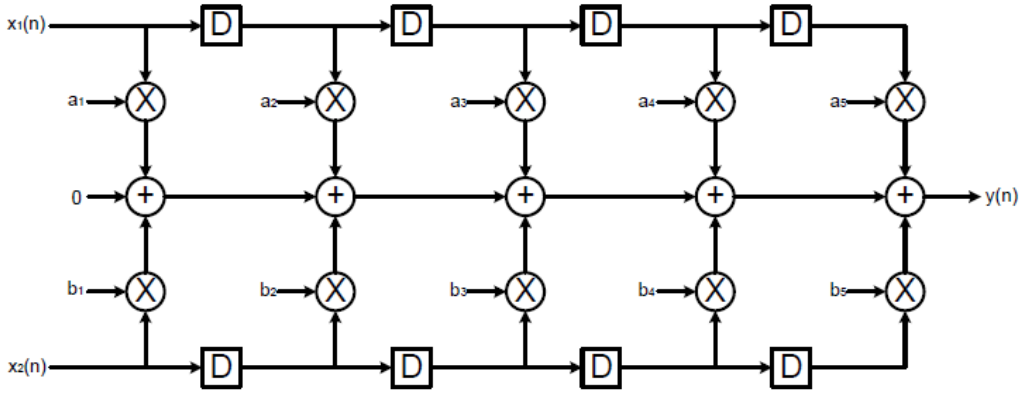
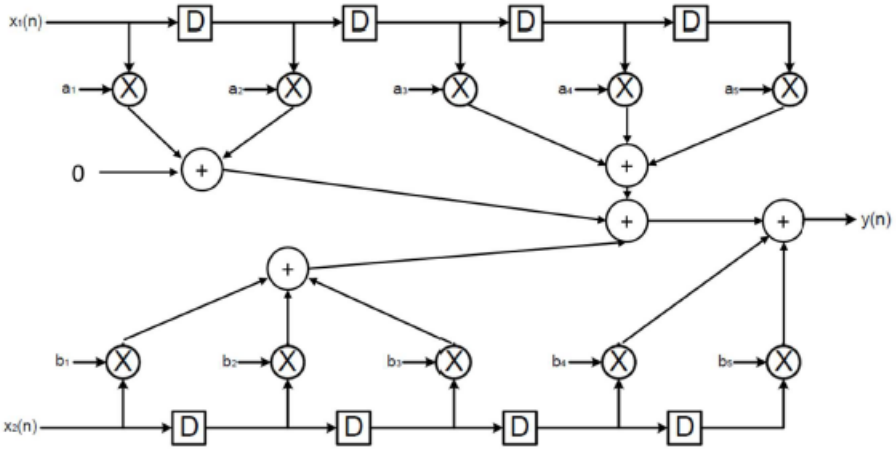
1.

Consider the nonrecursive signal processing structure shown in Fig.3.22. Find an equivalent data-broadcast implementation of this algorithm to improve the speed of the system. Do not use any additional latches. Calculate the throughput or sample speed of the broadcast architecture.(Hint Transpose operation is not applicable to the 2-input 1-output system in Fig.3.22.)





sample period = Tm+3Ta

2.

It is necessary to reduce the power consumption of a system by at least 5 times using pipeline. For the threshold voltage of 0.4V and initial supply voltage of 5V, at what level should the system be pipeline? What is the supply voltage of the pipelined system?

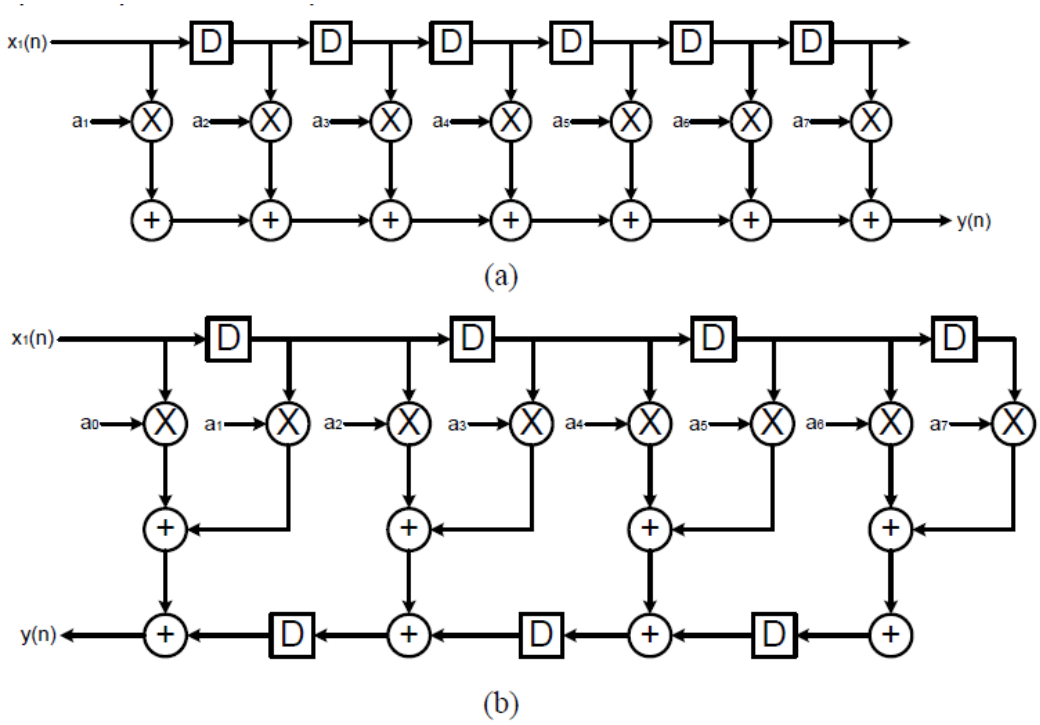
$\beta = \text{sqrt}(1/5) = 0.4472$

$\beta(Vo-Vt)^2 = M(\beta Vo-Vt)^2, M=3$

supply voltage = $\beta Vo = 0.4472*5 =$ 2.236V

pipeline level = 3

3.



total capacitance ： Cm = 10Ca

charging capacitance ： Cm=2Ca

for(b), m = Ctotal/Ccharge = 12/4 = 3

β(Vo-Vt)^2 = M(βVo-Vt)^2 , β = 0.472

minimum supply: Vpip = βVo = 0.472*4 = 1.888V

power reduction: (1-β^2)*100% = 77.72%

4. 環境設置：

TSMC13

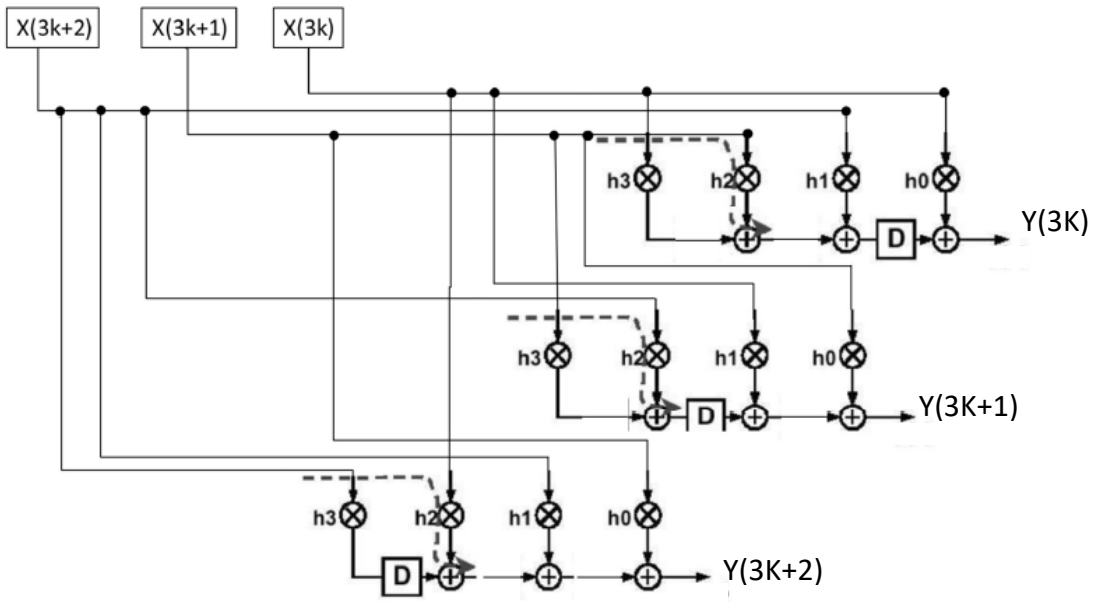
set cycle 8.2

input delay 0.5*cycle

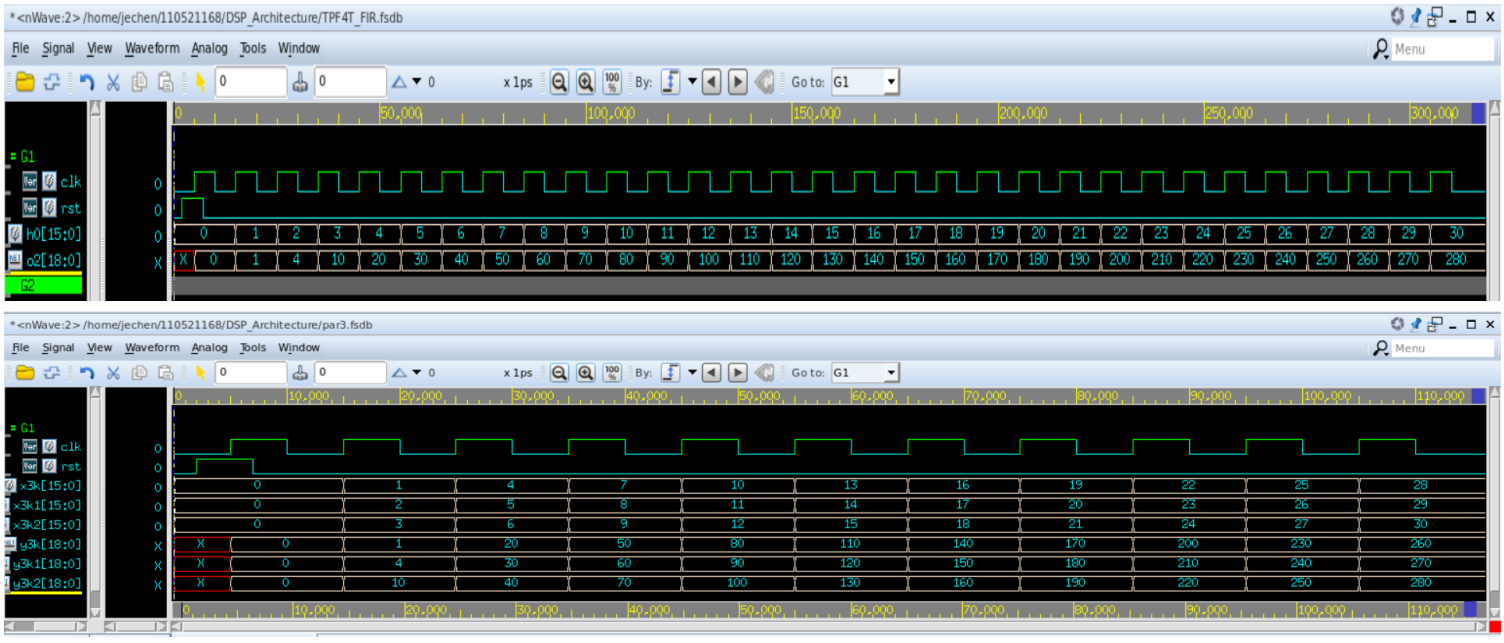
output delay 0.5*cycle

output load 0.05pf

Parallel Transposed Form FIR



RTL waveform (serial vs parallel)



Timing (serial vs parallel)

```
clock clk (rise edge)                                   8.20       8.20
clock network delay (ideal)                             0.50       8.70
clock uncertainty                                      -0.10       8.60
D2_reg[17]/CK (DFFTRX1)                                 0.00       8.60 r
library setup time                                     -0.22       8.38
data required time                                                 8.38
-------------------------------------------------------------------------
data required time                                                 8.38
data arrival time                                                 -7.76
-------------------------------------------------------------------------
slack (MET)                                                        0.62
```

```
clock clk (rise edge)                                  24.60      24.60
clock network delay (ideal)                             0.50      25.10
clock uncertainty                                      -0.10      25.00
y3k2_reg[18]/CK (DFFTRX1)                               0.00      25.00 r
library setup time                                     -0.23      24.77
data required time                                                24.77
-------------------------------------------------------------------------
data required time                                                24.77
data arrival time                                                 -8.65
-------------------------------------------------------------------------
slack (MET)                                                       16.11
```

Area (serial vs parallel)

```
Combinational area:               2235.475906
Buf/Inv area:                       64.501199
Noncombinational area:            2106.473446
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  4341.949352
```

```
Combinational area:               6648.716123
Buf/Inv area:                      171.437397
Noncombinational area:            3202.993870
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  9851.709993
```

Power (serial vs parallel)

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	0.2118	1.6114e-02	2.1210e+06	0.2300	(84.23%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	3.5155e-02	5.4796e-03	2.4381e+06	4.3073e-02	(15.77%)	
Total	0.2469 mW	2.1593e-02 mW	4.5591e+06 pW	0.2731 mW		

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	0.1109	1.5008e-02	3.2251e+06	0.1292	(70.13%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	4.1296e-02	6.5372e-03	7.1908e+06	5.5024e-02	(29.87%)	
Total	0.1522 mW	2.1545e-02 mW	1.0416e+07 pW	0.1842 mW		

5. 結論

	Area(um^2)	Time(ns)	Power(mW)
Serial	4341.949352	7.76	0.2731
Parallel	9851.709993	8.65	0.1842

因為 parallel 會讓硬體放大 3 倍但是 delay element 數量不變，所以只有 conbitational area 的部分會變 3 倍左右

將 transposed form FIR 改為 parallel 時，因為無法發揮將 output 路徑上的 delay 切開的效果，所以 timing 並不會變好。

因為經過 3 倍平行處理，變成一個 clk 就能有 3 個輸出，所以將 clk 放慢三倍讓電容的充電時間變長，降低 supply voltage，就能達到 low power 的效果。