Homework 3

Pipelining and Parallel Processing

(Due: 2022/10/27)

1. Consider the nonrecursive signal processing structure shown in Fig.3.22. Find an equivalent data-broadcast implementation of this algorithm to improve the speed of the system. Do not use any additional latches. Calculate the throughput or sample speed of the broadcast architecture.(Hint Transpose operation is not applicable to the 2-input 1-output system in Fig.3.22.)

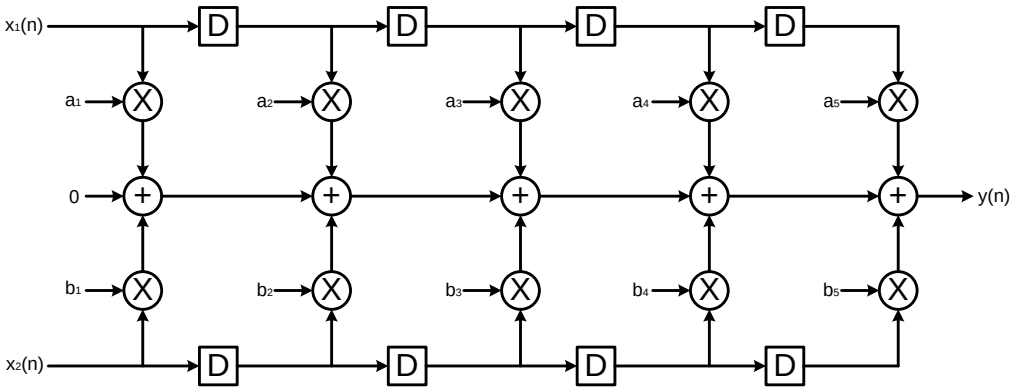
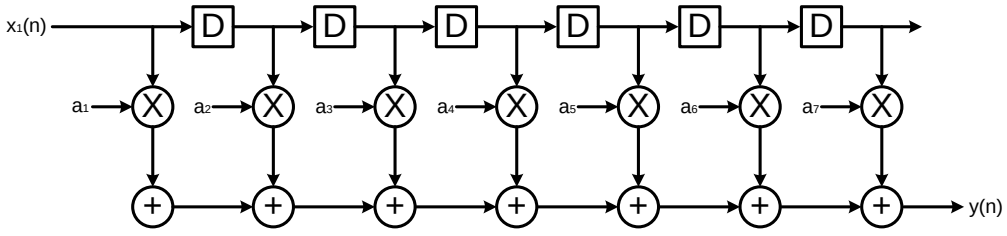


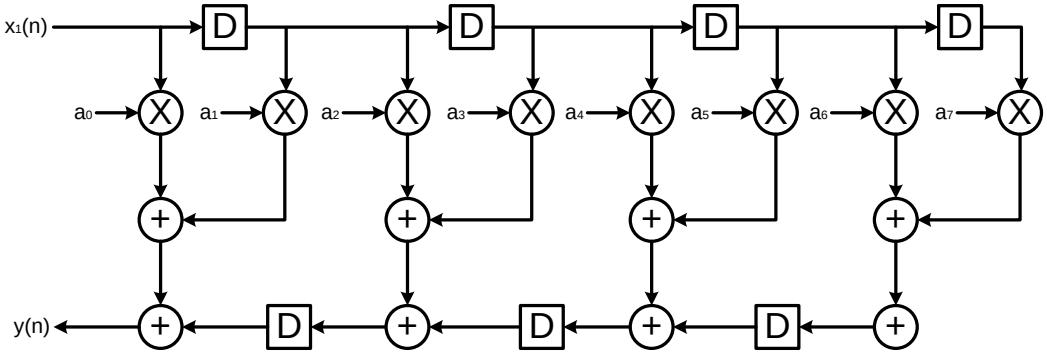
Fig. 3.22 Data-flow graph for Problem 1

2. It is necessary to reduce the power consumption of a system by at least 5 times using pipeline. For the threshold voltage of 0.4V and initial supply voltage of 5V, at what level should the system be pipeline? What is the supply voltage of the pipelined system?
3. Two implementations of an 8-tap FIR filter are shown in Fig. 3.24.Assume the critical path (or the propagation delay) of a multiplier to be twice that of an adder, i.e., Tm=2Ta. Therefore, the charging capacitance of a multiplier is twice that of an adder. Further assume that the total capacitance of a multiplier is 10 times that of an adder, i.e., Cm=10Ca.The structure in Fig.3.24(b) can be operated with a lower supply voltage to meet the clock period or sampling period constraint of 9Ta.Thus, the structure in Fig.3.24(b) can be used to reduce the power consumption. Assume that the structure in Fig.3.24 (a) is operated with a supply voltage of 4V.Assume the technology threshold voltage to be 0.5V.The supply voltage must be greater than 1.2V to achieve the acceptable noise margin. What is the minimum supply voltage at which the structure shown in Fig.3.24 (b) can be operated to achieve the desired sampling period of 9Ta? Calculate the percentage of reduction in power consumption for the

structure in Fig.3.24 (b) as compared with that in Fig.3.24(a). Neglect the propagation delay and capacitance of delay elements in calculation of critical path or power consumption



(a)



(b)

Fig. 3.24 Two implementations of an 8-tap FIR filter in Problem 3

4. Verilog-HDL Design：

請從第一章中所學到的Transposed Form FIR filter ，以 parallel 技巧實現 3 倍 parallel 電路。

作業要求：

原始電路與 parallel 電路的 RTL-level function 驗證無誤並比較兩者之間的差異性。以 Design Compiler 合成後，gate-level function 驗證無誤。

比較合成之後，兩者的面積(area)、速度(timing)與功率消耗(power consumption)。**此次作業需繳交：**

1. RTL code(Verilog)
2. Top module testbench
3. 書面紙本、書面電子檔(doc)、報告電子檔(ppt)
4. 檔名為：學號_VDSP111_HW3 (ex: 111521001_VDSP111_HW3.rar)
5. 檔名為：學號_VDSP111_HW3 (ex: 111521001_VDSP111_HW3.rar)
6. 壓縮檔-檔案結構：

RTL(資料夾)：include RTL code

sim(資料夾)：include testbench and sim_cmd.txt

學號_VDSP111_HW3.ppt
學號_VDSP111_HW3.doc

如有任何疑問，可至 E1-410 詢問助教，或透過以下信箱詢問助教信箱: 110521027@cc.ncu.edu.tw