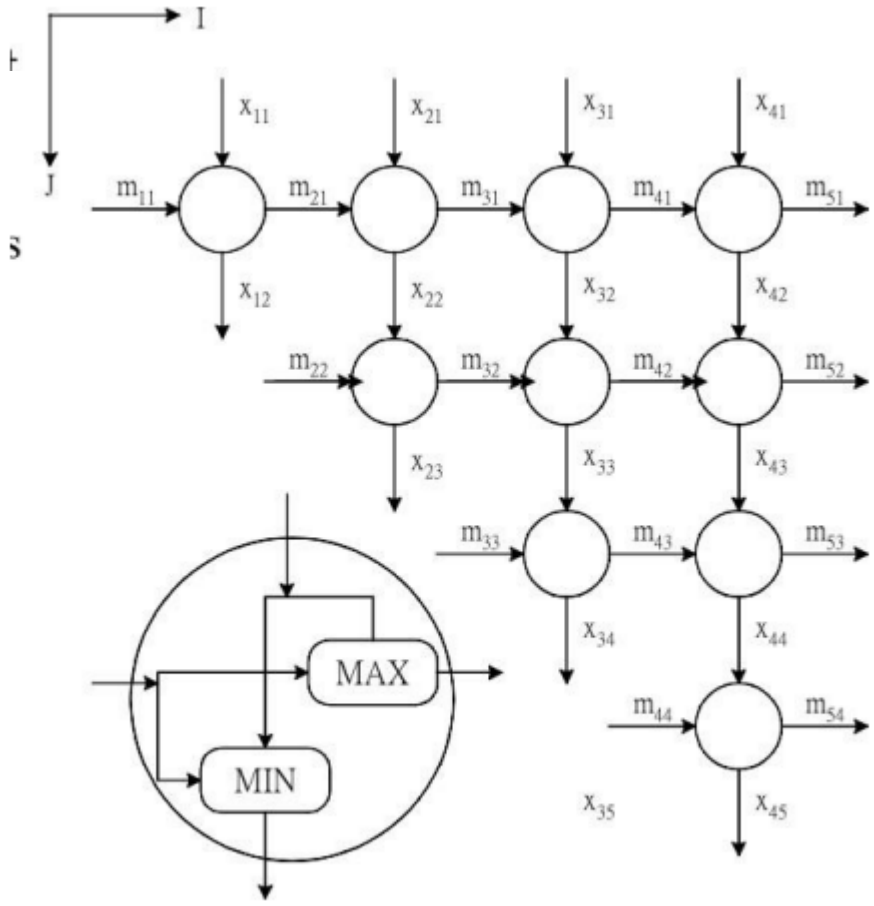
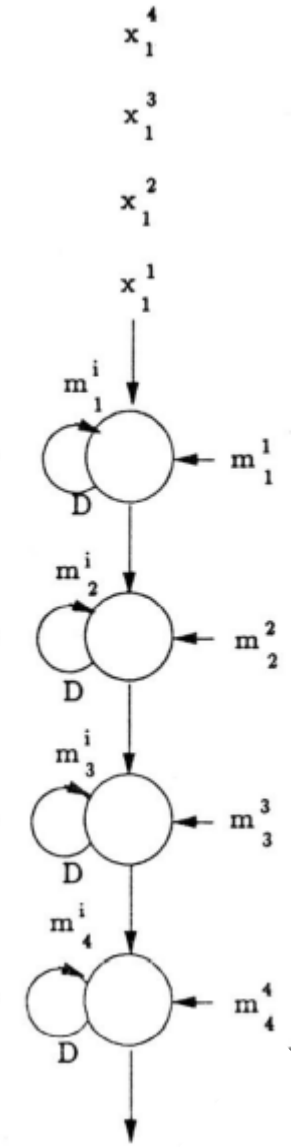
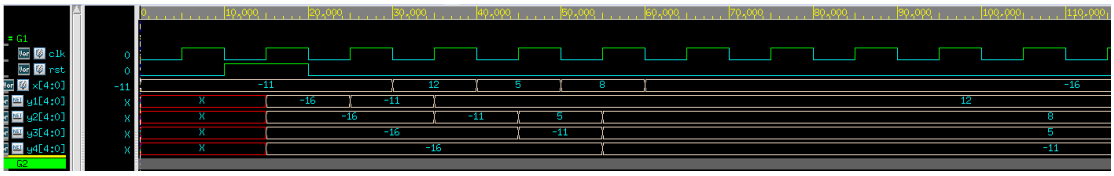
1. **Implement following architecture based on three vector{0,1}, {1,0}, {1,1}**



2. **For vector{1,0}, it is insertion sort**






```
Report : area
Design : top
Version: R-2020.09
Date   : Thu Dec 15 05:15:42 2022
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Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           27
Number of nets:                           120
Number of cells:                           94
Number of combinational cells:             74
Number of sequential cells:                20
Number of macros/black boxes:               0
Number of buf/inv:                         23
Number of references:                      17

Combinational area:                527.891400
Buf/Inv area:                       78.080399
Noncombinational area:             714.605402
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  1242.496802
```
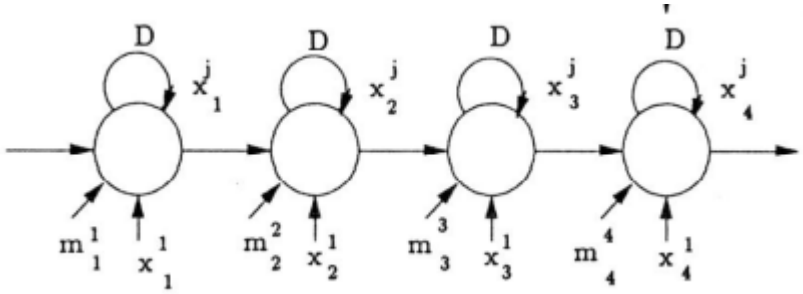
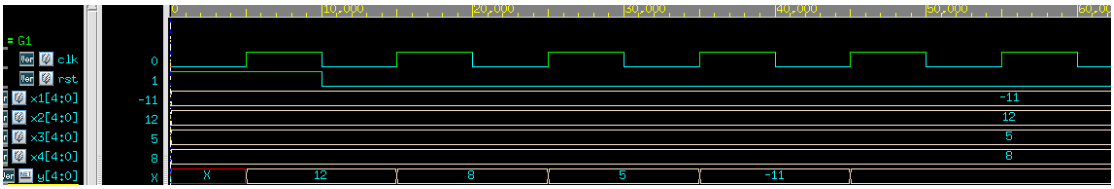

```
clock clk (rise edge)                          10.00      10.00
clock network delay (ideal)                     0.50      10.50
clock uncertainty                              -0.10      10.40
d4_reg[0]/CK (EDFFTRX1)                         0.00      10.40 r
library setup time                             -0.72       9.68
data required time                                         9.68
-----------------------------------------------------------------
data required time                                         9.68
data arrival time                                         -7.21
-----------------------------------------------------------------
slack (MET)                                                2.47
```

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	4.4869e-02	3.8830e-03	4.7574e+05	4.9228e-02	(90.09%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	2.4747e-03	2.6767e-03	2.6604e+05	5.4175e-03	(9.91%)	
Total	4.7344e-02 mW	6.5598e-03 mW	7.4179e+05 pW	5.4646e-02 mW		

3. **For vector{0,1}, it is selection sort**






```
Report : area
Design : top
Version: R-2020.09
Date   : Thu Dec 15 05:48:45 2022
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Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          27
Number of nets:                          190
Number of cells:                         154
Number of combinational cells:           134
Number of sequential cells:               20
Number of macros/black boxes:              0
Number of buf/inv:                        23
Number of references:                     26

Combinational area:               979.399788
Buf/Inv area:                      84.869999
Noncombinational area:            543.167997
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 1522.567786
```
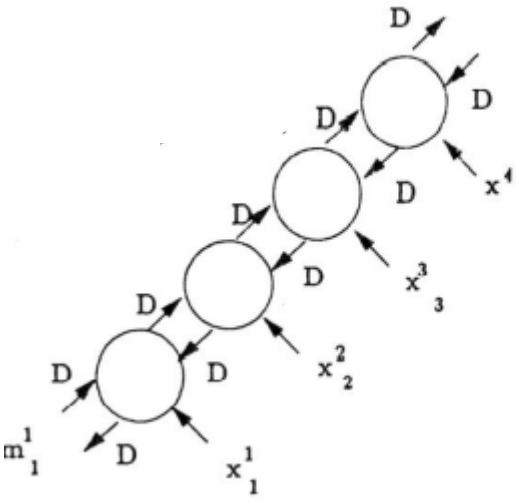
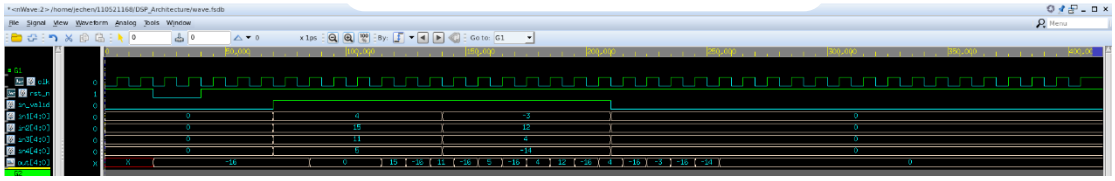

```
  clock clk (rise edge)                    10.00      10.00
  clock network delay (ideal)               0.50      10.50
  clock uncertainty                        -0.10      10.40
  output external delay                    -0.50       9.90
  data required time                                   9.90
  ---------------------------------------------------------
  data required time                                   9.90
  data arrival time                                   -6.90
  ---------------------------------------------------------
  slack (MET)                                          3.00
```

```
                 Internal         Switching          Leakage            Total
Power Group      Power            Power              Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000             0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000             0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000             0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000             0.0000             0.0000  (   0.00%)
register       3.6412e-02       1.0490e-03         3.7322e+05         3.7834e-02  (  76.45%)
sequential         0.0000           0.0000             0.0000             0.0000  (   0.00%)
combinational  4.7415e-03       6.4006e-03         5.1381e+05         1.1656e-02  (  23.55%)
--------------------------------------------------------------------------------------------------
Total          4.1154e-02 mW     7.4495e-03 mW     8.8703e+05 pW      4.9490e-02 mW
```

4. **For vector{1,1}, it is bubble sort**



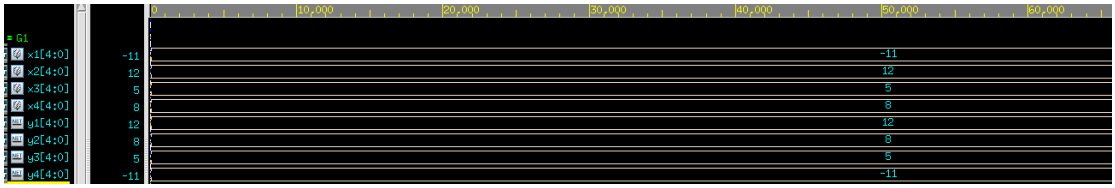


```
Report : area
Design : top
Version: R-2020.09
Date   : Thu Dec 15 04:33:31 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          108
Number of nets:                           312
Number of cells:                          215
Number of combinational cells:            166
Number of sequential cells:                43
Number of macros/black boxes:               0
Number of buf/inv:                         65
Number of references:                      19

Combinational area:              1169.508603
Buf/Inv area:                     288.557996
Noncombinational area:           1373.196560
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 2542.705163
```

```
  clock clk (rise edge)                    10.00      10.00
  clock network delay (ideal)               0.50      10.50
  clock uncertainty                        -0.10      10.40
  in2_reg_reg[1]/CK (DFFRX1)                0.00      10.40 r
  library setup time                       -0.21      10.19
  data required time                                  10.19
  ---------------------------------------------------------
  data required time                                  10.19
  data arrival time                                   -2.54
  ---------------------------------------------------------
  slack (MET)                                          7.65
```

```
                 Internal         Switching          Leakage            Total
Power Group      Power            Power              Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000             0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000             0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000             0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000             0.0000             0.0000  (   0.00%)
register       9.3336e-02       3.6519e-03         1.2790e+06         9.8267e-02  (  88.24%)
sequential         0.0000           0.0000             0.0000             0.0000  (   0.00%)
combinational  6.7747e-03       5.6767e-03         6.4204e+05         1.3093e-02  (  11.76%)
--------------------------------------------------------------------------------------------------
Total              0.1001 mW     9.3285e-03 mW     1.9210e+06 pW         0.1114 mW
```

5. Original DG




```
Report : area
Design : top
Version: R-2020.09
Date   : Thu Dec 15 06:16:56 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          240
Number of nets:                           472
Number of cells:                          282
Number of combinational cells:            270
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                        100
Number of references:                      10

Combinational area:               2053.853970
Buf/Inv area:                      339.479995
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  2053.853970
```

```
  s44/U20/Y (OAI22XL)                     0.13       8.32 f
  s44/U16/Y (OAI2BB1X1)                   0.18       8.50 f
  s44/U15/Y (OAI221XL)                    0.10       8.60 r
  s44/U14/Y (OAI221XL)                    0.16       8.76 f
  s44/U13/Y (OAI2BB1X1)                   0.34       9.10 r
  s44/U9/Y (MXI2X1)                       0.75       9.84 r
  s44/max[3] (sort_0)                     0.00       9.84 r
  y4[3] (out)                             0.00       9.84 r
  data arrival time                                  9.84
```

```
                 Internal         Switching          Leakage            Total
Power Group      Power            Power              Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad           0.0000           0.0000             0.0000             0.0000  (   0.00%)
memory           0.0000           0.0000             0.0000             0.0000  (   0.00%)
black_box        0.0000           0.0000             0.0000             0.0000  (   0.00%)
clock_network    0.0000           0.0000             0.0000             0.0000  (   0.00%)
register         0.0000           0.0000             0.0000             0.0000  (   0.00%)
sequential       0.0000           0.0000             0.0000             0.0000  (   0.00%)
combinational    0.1200           0.2336         1.9345e+06             0.3555  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total            0.1200 mW        0.2336 mW      1.9345e+06 pW          0.3555 mW
```

6. Conclusion

	Area(um^2)	Time(ns)	Power(mW)
Original	2053.85	9.84	0.3555
Insertion	1242.49	7.21	0.0546
Selection	1522.56	6.90	0.0494
Bubble	2542.71	2.54	0.1114

Bubble sort 每兩個 clk 才會有一個輸出，中間使用到的 D flip-flop 比其他三種架構還要多，所以面積最大

Original 要一個一個比較，需要等待的時間較長，所以速度慢；
Insertion 和 Selection 的架構類似，只是往後送跟留在迴圈內的值相反，所以兩者速度差不多；
Bubble 雖然每兩個 clk 才會有一次輸出，但在每個時間點都可以兩兩比較排序，速度是所有方法中最快的

Original 全部由 combinational circuit 組成需要的功耗相當大
Bubble 因為使用的 D flip-flop 數量是另外兩個的 2 倍以上，所以在 register 的部分的功耗偏大