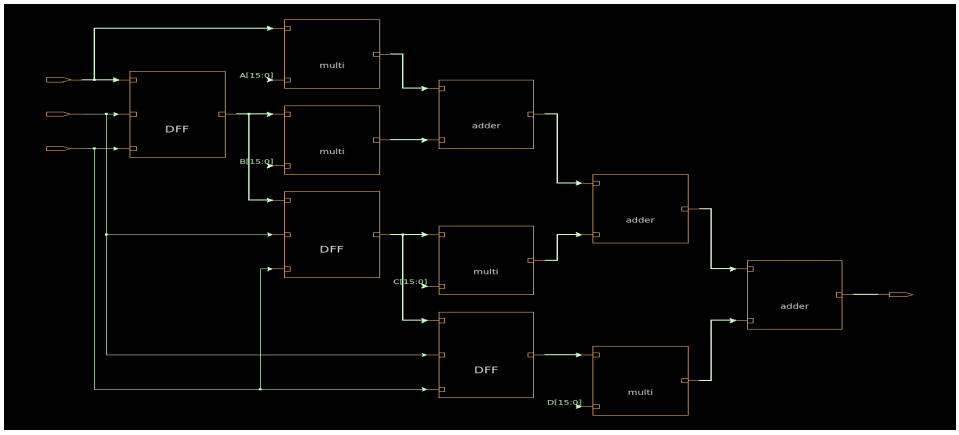
環境設置：

```
set target_library      "slow.db"
set link_library         "* $target_library dw_foundation.sldb"
set symbol_library      "tsmc13.sdb generic.sdb"
set synthetic_library "dw_foundation.sldb"
set_clock_uncertainty    0.1    [get_clocks clk]
set_clock_latency          0.5    [get_clocks clk]
set_input_delay    5       -clock clk [remove_from_collection [all_inputs]
[get_ports clk]]
set_output_delay 0.5       -clock clk [all_outputs]
```

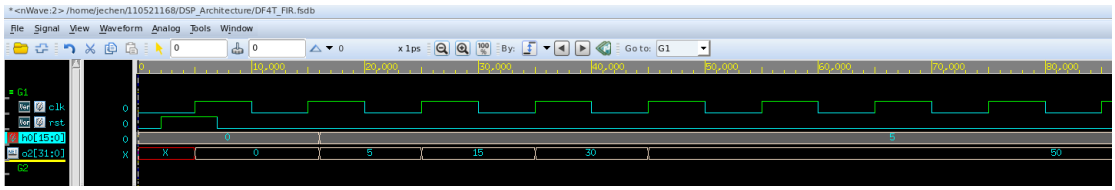
1. Direct Form 4-tap FIR

以 Verdi 顯示電路 schematic 架構



利用 testbench 驗證其正確性

(當輸入為 5 時，3 個 clk 後輸出應為 50)



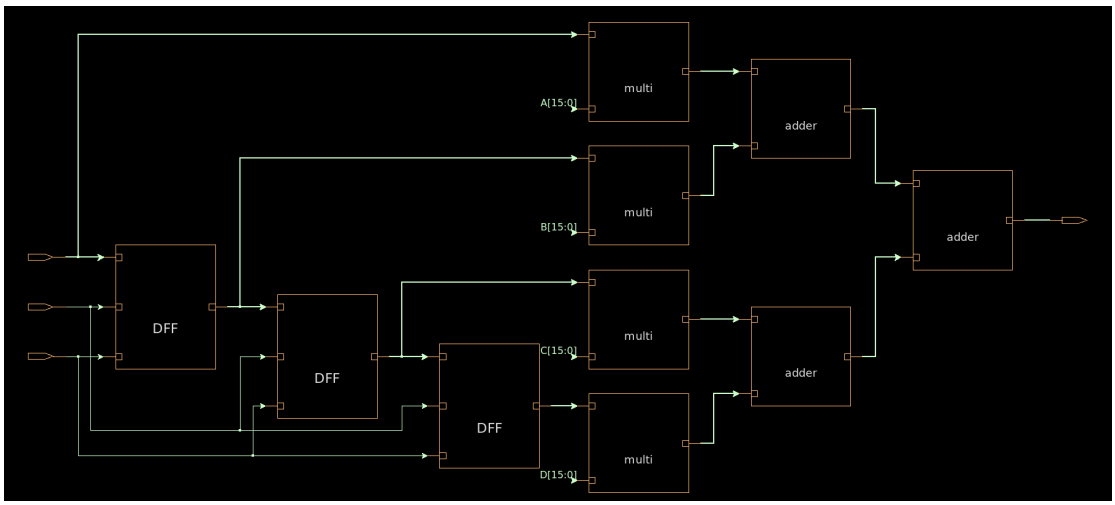
在 design compiler 的 tcl 檔裡面設定其 clk 週期為 9.5，並記錄 area 和 timing　　(set cycle 9.5)

```
****************************************
Report : area
Design : DF4T_FIR
Version: R-2020.09
Date   : Thu Oct  6 15:42:36 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          791
Number of nets:                          2243
Number of cells:                         1471
Number of combinational cells:           1401
Number of sequential cells:                48
Number of macros/black boxes:               0
Number of buf/inv:                        347
Number of references:                      16

Combinational area:              16371.422952
Buf/Inv area:                     2518.941595
Noncombinational area:            1385.078430
Macro/Black Box area:                0.000000
Net Interconnect area:          140000.700043

Total cell area:                 17756.501382
Total area:                     157757.201425
```

```
clock clk (rise edge)                                    9.50       9.50
clock network delay (ideal)                              0.50      10.00
clock uncertainty                                       -0.10       9.90
output external delay                                   -0.50       9.40
data required time                                                  9.40
-------------------------------------------------------------------------
data required time                                                  9.40
data arrival time                                                  -9.40
-------------------------------------------------------------------------
slack (VIOLATED: increase significant digits)                       0.00
```

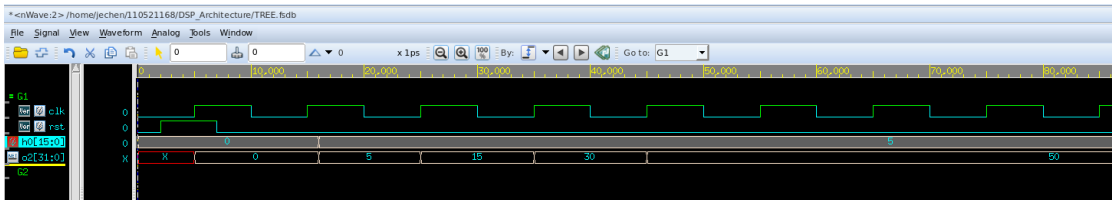
2. Direct Form 4-tap FIR with Adder Tree

以 Verdi 顯示電路 schematic 架構



利用 testbench 驗證其正確性

(當輸入為 5 時，3 個 clk 後輸出應為 50)



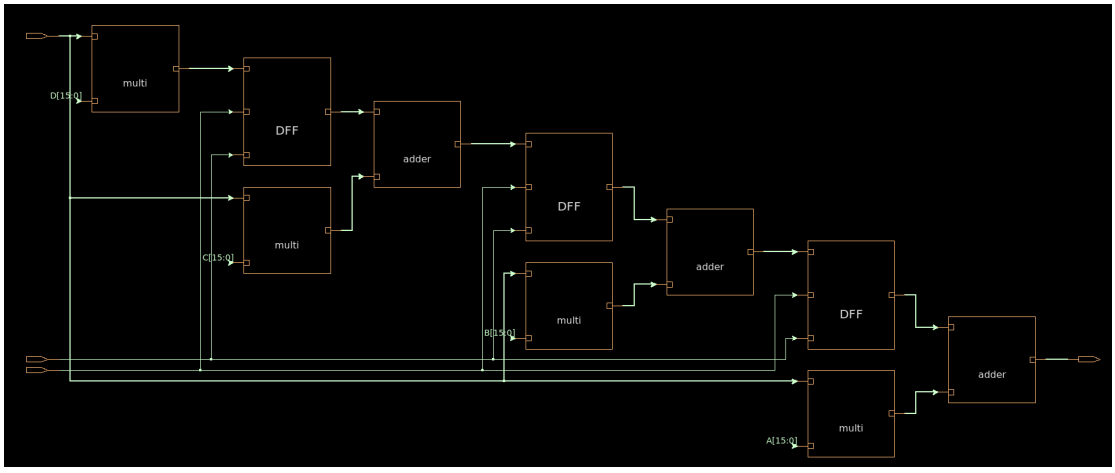
在 design compiler 的 tcl 檔裡面設定其 clk 週期為 8.8，並記錄 area 和 timing　(set cycle 8.8)

```
****************************************
Report : area
Design : ADDER_TREE
Version: R-2020.09
Date   : Wed Oct  5 21:06:29 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          791
Number of nets:                          2209
Number of cells:                         1435
Number of combinational cells:           1365
Number of sequential cells:                48
Number of macros/black boxes:               0
Number of buf/inv:                        371
Number of references:                      20

Combinational area:              15344.495984
Buf/Inv area:                     2729.419206
Noncombinational area:            1383.381029
Macro/Black Box area:                0.000000
Net Interconnect area:          134774.006775

Total cell area:                 16727.877013
Total area:                     151501.883788
```

```
clock clk (rise edge)                                    8.80       8.80
clock network delay (ideal)                              0.50       9.30
clock uncertainty                                       -0.10       9.20
output external delay                                   -0.50       8.70
data required time                                                  8.70
--------------------------------------------------------------------------
data required time                                                  8.70
data arrival time                                                  -8.70
--------------------------------------------------------------------------
slack (MET)                                                         0.00
```

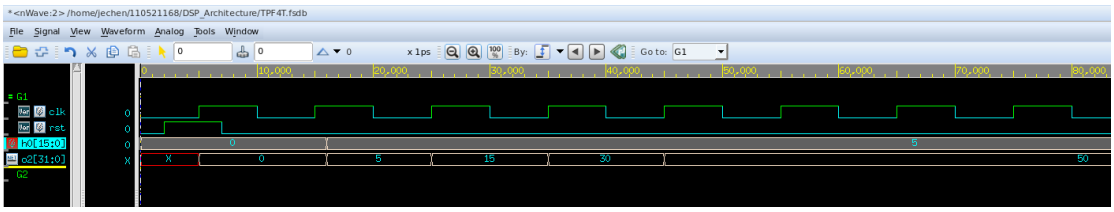
3. Transposed Form 4-tap FIR

以 Verdi 顯示電路 schematic 架構



利用 testbench 驗證其正確性

(當輸入為 5 時，3 個 clk 後輸出應為 50)



在 design compiler 的 tcl 檔裡面設定其 clk 週期為 8.0，並記錄 area 和 timing　(set cycle 8.0)

```
****************************************
Report : area
Design : TPF4T_FIR
Version: R-2020.09
Date   : Wed Oct  5 20:54:33 2022
****************************************

Library(s) Used:

    slow (File: /cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          809
Number of nets:                          2306
Number of cells:                         1493
Number of combinational cells:           1414
Number of sequential cells:                57
Number of macros/black boxes:               0
Number of buf/inv:                        372
Number of references:                      26

Combinational area:              18011.111335
Buf/Inv area:                     2888.974804
Noncombinational area:            1685.518227
Macro/Black Box area:                0.000000
Net Interconnect area:          140094.032745

Total cell area:                 19696.629562
Total area:                     159790.662307
```

```
  clock clk (rise edge)                                   8.00       8.00
  clock network delay (ideal)                             0.50       8.50
  clock uncertainty                                      -0.10       8.40
  output external delay                                  -0.50       7.90
  data required time                                                 7.90
  --------------------------------------------------------------------------
  data required time                                                 7.90
  data arrival time                                                 -7.90
  --------------------------------------------------------------------------
  slack (MET)                                                        0.00
```

結果

	Area(um^2)	Time(ns)
DF4T FIR	17756.501382	9.4
ADDER_TREE	16727.877013	8.7
TPF4T FIR	19696.629562	7.9

結論

根據合成結果顯示，三種濾波器的速度由快到慢是 3→2→1，以此次給定 N=4 的條件，帶入下圖中所提供的 critical path timing 公式中，可以得知此次結果符合預期。

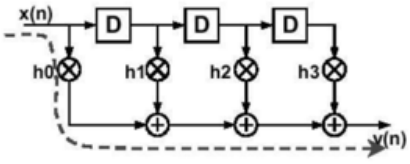


Fig.1.1 Direct Form 4-tap FIR

$T_{Critical} = T_M + (N-1)T_A$

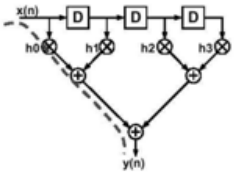


Fig.1.2 Direct Form 4-tap FIR with Adder Tree

$T_{Critical} = T_M + (\log_2 N)T_A$

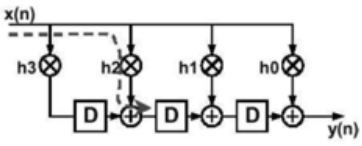


Fig.1.3 Transposed Form 4-tap FIR

$T_{Critical} = T_M + T_A$