Min Si

Assistant Computer Scientist
Mathematics and Computer Science Division
Argonne National Laboratory

9700 South Cass Avenue, Bldg. 240, Lemont, IL 60439, USA
(Office) +1 630-252-4249, (Mobile) +1 630-880-4388
(Argonne) msi@anl.gov, (Other) minsi.atwork@gmail.com
Linkedin: `https://www.linkedin.com/in/min-si-b871a490/`
Website: `http://www.mcs.anl.gov/~minsi/`

Research Interests

Parallel programming models and runtime systems, heterogeneous computing, data analytics in high performance computing.

Education

Ph.D. in Computer Science 2012/10 – 2016/03
Department of Computer Science Tokyo, Japan
Graduate School of Information Science and Technology
The University of Tokyo

Master of Science 2010/10 – 2012/09
Department of Computer Science Tokyo, Japan
Graduate School of Information Science and Technology
The University of Tokyo

Bachelor of Arts 2003/09 – 2007/07
Department of Japanese Language and Culture Chongqing, China
College of Oriental Languages
Sichuan International Studies University

Professional Experience

Assistant Computer Scientist 2018/05 – Current
Argonne National Laboratory, IL, USA
- OpenSHMEM implementation over MPI (Tech Lead).
- High performance MPI implementation (Co-PI).

Enrico Fermi Postdoctoral Scholar 2016/10 – 2018/04
Argonne National Laboratory, IL, USA
- Dynamic execution runtime (PI).
- High performance MPI implementation (Co-PI).

Postdoctoral Appointee 2016/05 – 2016/09
Argonne National Laboratory, IL, USA
- High performance MPI implementation.

Guest Graduate Student 2014/05 – 2016/03
Argonne National Laboratory, IL, USA
- MPI optimization on massively parallel multi-/many-core architectures.

Research Aide 2013/05 – 2013/09
Argonne National Laboratory, IL, USA
- Multithreaded MPI for many-core environments.

Summer Internship 2011/08 – 2011/11

NEC Corp, Tokyo, Japan
- InfiniBand driver modification for direct data transfer from/to FPGA board.

Other Programming Experience

Part-time Programmer 2010/12 – 2011/12
Secioss Corp, Tokyo, Japan
- E-commerce web system development using PHP.

Full-time Engineer 2008/07 – 2010/09
Kinotrope Inc, Tokyo, Japan
- Web system (CMS, E-commerce, Auto-test) development using PHP.

Full-time Engineer 2007/07 – 2008/04
DGT Information Systems Ltd, Shanghai, China
- Credit card member management system development using Java.

Project Management

- *OpenSHMEM over MPI: Analyzing and Improving the Suitability of MPI as an OpenSHMEM Runtime.*
  OpenSHMEM is a Partitioned Global Address Space (PGAS) library that provides targeted and specialized functionality for high performance communication, while MPI is a low-level communication library focusing on completeness of features and generalization. This project aims to analyze and optimize the OpenSHMEM implementation on top of MPI from both performance and semantics aspects.
  Role: Technical Lead and Core Developer. *Period*: 08/2018 to present.
  Project website: `http://www.mcs.anl.gov/project/oshmpi`
  Software: `https://github.com/pmodels/oshmpi`
- *MPICH: A high-performance, portable implementation of the Message Passing Interface (MPI).*
  MPICH and its derivatives form the most widely used implementations of MPI in the world. My interests especially focus on the research and development of MPI one-sided communication model.
  Role: Co-PI and Core Developer. *Period*: 10/2016 to present.
  Project website: `http://www.mpich.org`
  Software: `https://github.com/pmodels/mpich`
- *Beehive: A Dynamic Execution Environment for Performance, Power, and Resilience on Extreme-Scale Computing Systems.*
  Beehive is a dynamic execution environment for supporting irregular MPI applications. It focuses on adaptive MPI progress management, dynamic computation load balancing and communication overlapping, as well as lightweight checkpointing and migration for power management and resilience.
  Role: PI and Core Developer. *Period*: 10/2016 to 03/2020.
  Subproject Website: `http://www.mcs.anl.gov/project/casper`
  Software: `https://github.com/pmodels/casper`

Honors and Awards

Impact Argonne Award for Extraordinary Effort 2020/08
Argonne National Laboratory, USA

IEEE-CS Technical Consortium on High Performance Computing (TCHPC) *2018/11*
Early Career Researchers Award for Excellence in High Performance Computing
SC 2018, USA

Best Paper Award at the 27th ACM International Symposium on High-Performance Parallel and Distributed Computing (Top 1/112) *2018/06*
HPDC 2018, USA

Enrico Fermi Fellowship for Postdoctoral Scientists 2016 – 2018
Argonne National Laboratory, USA

2016 NERSC Award for Innovative Use of HPC in the Early Career Category 2016/03

National Energy Research Scientific Computing Center, USA

Dean's Award for Outstanding Achievement Doctoral Course 2016/03
The University of Tokyo, Japan

Fellowship Special Scholarship Program for International Students 2012 – 2015
The University of Tokyo, Japan

Finalist of the 8th IEEE International Scalable Computing Challenge (*Top 5/15*) 2015/05
Co-located with the IEEE/ACM CCGrid 2015, China

Finalist of the ACM Student Research Competition 2012/11
SC 2012, USA

Computer Science Research Award for Young Scientists 2012
Information Processing Society of Japan (IPSJ), Japan

Research Grants

- *Senior Personnel* (PI: Geoffrey Fox, Indiana University): FAIR Surrogate Benchmarks Supporting AI and Simulation Research (SBI). Department of Energy (DOE), Advanced Scientific Computing Research (ASCR). Period: 09/01/2020 – 08/31/2023. Argonne amount (collaborative grant): $562,500 (total: $2,245,582).
- *Senior Personnel* (PI: Ian Foster, Argonne National Laboratory): Braid: Data Flow Automation for Scalable and FAIR Science. Department of Energy (DOE), Advanced Scientific Computing Research (ASCR). Period: 10/01/2020 – 09/30/2023. Amount (single institute grant): $2,700,000.
- *Tech Lead* (PI: Pavan Balaji, Argonne National Laboratory): Analyzing and Improving the Suitability of MPI as an OpenSHMEM Runtime. Department of Defense (DOD). Period: 08/01/2018 to 09/30/2021. Amount (single institute grant): $1,200,000.
- *PI*: Beehive: A Dynamic Execution Environment for Performance, Power, and Resilience on Extreme-Scale Computing Systems. Argonne National Laboratory, Laboratory Directed Research and Development (LDRD) program. Period: 10/01/2016 to 03/31/2020. Amount (single institute grant): FY 2017: $178,000, FY 2018: $182,200, FY 2019: $35,000, FY 2020: $69,000.
- *Co-PI* (PI: Pavan Balaji, Argonne National Laboratory): Exascale MPI. Department of Energy (DOE), Advanced Scientific Computing Research (ASCR), Exascale Computing Project (ECP). Period: 10/01/2016 to 09/30/2024. Amount (single institute grant): $13,599,984.78.

Computing Resource Awards

- *Co-PI* (PI: Pavan Balaji, Argonne National Laboratory): Scalable Deep Learning (SDL). Argonne Laboratory Computing Resource Center Allocation. Period: 2018/10 to 2020/09. Core-hours: 2,400,000.
- *PI*: Scalable Deep Learning (SDL). Argonne Leadership Computing Facility Director's Discretionary Allocation. Period: 2019/02 to 2020/03. Core-hours: 2,000,000.
- *PI*: MPI one-sided communication: optimization and applications. National Energy Research Scientific Computing Center Allocation. Period: 2018/10 to 2021/01. Core-hours: 1,295,174.

Publications and Presentations

Refereed Journal Articles

1. Sarunya Pumma, **Min Si**, Wu-chun Feng, and Pavan Balaji. Scalable Deep Learning via I/O Analysis and Optimization. In *ACM Transactions on Parallel Computing (TOPC)*, vol. 6, no. 2, pp. 1–34. June, 2019.
2. **Min Si**, Antonio J. Peña, Jeff Hammond, Pavan Balaji, Masamichi Takagi, and Yutaka Ishikawa. Dynamic Adaptable Asynchronous Progress Model for MPI RMA Multiphase Applications. In *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 29, no. 9, pp. 1975–1989. September, 2018.

Research Papers in Refereed Conferences (peer-reviewed)

1. Kaiming Ouyang, **Min Si**, Atsushi Hori, Zizhong Chen, and Pavan Balaji. CAB-MPI: Exploring Interprocess Work-Stealing toward Balanced MPI Communication. In *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis (SC 2020)*. November 2020 (Accepted).
2. Abdelhalim Amer, Charles Archer, Michael Blocksome, Chongxiao Cao, Michael Chuvelev, Hajime Fujita, Maria Garzaran, Yanfei Guo, Jeff R. Hammond, Shintaro Iwasaki, Kenneth J. Raffenetti, Mikhail Shiryaev, **Min Si**, Kenjiro Taura, Sagar Thapaliya, and Pavan Balaji. Software Combining to Mitigate Multithreaded MPI Contention. In *Proceedings of the 33rd ACM International Conference on Supercomputing (ICS 2019)*, pages 367–379. June 2019. (*Acceptance Rate: 23%*)
3. Atsushi Hori, **Min Si (Joint First Co-Author)**, Balazs Gerofi, Masamichi Takagi, Jai Dayal, Pavan Balaji, and Yutaka Ishikawa. Process-in-Process: Techniques for Practical Address-Space Sharing. In *Proceedings of the 27th International Symposium on High-Performance Parallel and Distributed Computing (HPDC 2018)*, pages 131–143. June 2018. **Best Paper Award**. (*Acceptance Rate: 19.6%*)
4. Sarunya Pumma, **Min Si**, Wu-Chun Feng, and Pavan Balaji. Parallel I/O Optimizations for Scalable Deep Learning. In *Proceedings of 2017 IEEE 23rd International Conference on Parallel and Distributed Systems (ICPADS 2017)*, pages 720–729. December 2017.
5. **Min Si** and Pavan Balaji. Process-based Asynchronous Progress Model for MPI Point-To-Point Communication. In *Proceedings of 2017 IEEE 19th International Conference on High Performance Computing and Communications (HPCC 2017)*, pages 206–214. December 2017. (*Acceptance Rate: 38%*)
6. Sarunya Pumma, **Min Si**, Wu-Chun Feng, and Pavan Balaji. Towards Scalable Deep Learning via I/O Analysis and Optimization. In *Proceedings of 2017 IEEE 19th International Conference on High Performance Computing and Communications (HPCC 2017)*, pages 223–230. December 2017. (*Acceptance Rate: 38%*)
7. Kenneth J. Raffenetti, Abdelhalim Amer, Lena Oden, Charles Archer, Wesley Bland, Hajime Fujita, Yanfei Guo, Tomislav Janjusic, Dmitry Durnov, Michael Blocksome, **Min Si**, Sangmin Seo, Akhil Langer, Gengbin Zheng, Masamichi Takagi, Paul Coffman, Jithin Jose, Sayantan Sur, Alexander Sannikov, Sergey Oblomov, Michael Chuvelev, Masayuki Hatanaka, Xin Zhao, Paul Fischer, Thilina Rathnayake, Matt Otten, Misun Min, and Pavan Balaji. Why is MPI so Slow? Analyzing the Fundamental Limits in Implementing MPI-3.1. In *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis (SC 2017)*, pages 62:1–62:12. November 2017. (*Acceptance Rate: 18%*)
8. **Min Si**, Antonio J Peña, Jeff Hammond, Pavan Balaji, Masamichi Takagi, and Yutaka Ishikawa. Casper: An Asynchronous Progress Model for MPI RMA on Many-Core Architectures. In *Proceedings of the IEEE/ACM International Parallel and Distributed Processing Symposium (IPDPS 2015)*, pages 665–676, May 2015. (*Acceptance Rate: 21.8%*)
9. **Min Si**, Antonio J Peña, Jeff Hammond, Pavan Balaji, and Yutaka Ishikawa. Scaling NWChem with Efficient and Portable Asynchronous Communication in MPI RMA. In *Proceedings of 8th IEEE International Scalable Computing Challenge - Colocated with IEEE/ACM CCGrid 2015*, pages 811–816, May 2015. (*Acceptance Rate: 33%*)
10. **Min Si**, Antonio J. Peña, Pavan Balaji, Masamichi Takagi, and Yutaka Ishikawa. MT-MPI: Multithreaded MPI for Many-core Environments. In *Proceedings of the 28th ACM International Conference on Supercomputing (ICS 2014)*, pages 125–134. May 2014. (*Acceptance Rate: 21%*)

Research Papers in Refereed Workshops (peer-reviewed)

1. **Min Si**, Yutaka Ishikawa, and Masamichi Tatagi. Direct MPI Library for Intel Xeon Phi Co-Processors. In *Proceedings of the 2013 IEEE 27th International Parallel and Distributed Processing Symposium Workshops - PhD Forum (IPDPSW)*, pages 816-–824, May 2013.
2. **Min Si** and Yutaka Ishikawa. Design of Direct Communication Facility for Many-Core Based Accelerators. In *Proceedings of the 2012 IEEE 26th International Parallel and Distributed Processing Symposium Workshops - PhD Forum (IPDPSW)*, pages 924-–929, May 2012.

Abstracts and Posters in Peer-Reviewed Conferences and Workshops

1. Kaiming Ouyang, **Min Si**, and Zizhong Chen. Exploring Interprocess Work Stealing for Balanced MPI Communication. Accepted by the *SC19 research posters program*, November 2019.
2. **Min Si**, Antonio J Peña, Jeff Hammond, Masamichi Takagi, Pavan Balaji, and Yutaka Ishikawa. Accelerating the Global Arrays PGAS Model with Dynamic Adaptable Asynchronous Communication in MPI RMA. In *SC17 PGAS booth*, November 2017.
3. **Min Si**, Antonio J Peña, Jeff Hammond, Masamichi Takagi, Pavan Balaji, and Yutaka Ishikawa. Accelerating the Global Arrays PGAS Model with Efficient and Portable Asynchronous Communication in MPI RMA. In *SC16 PGAS booth*, November 2016.
4. **Min Si**, Pavan Balaji (Co-advisor), and Yutaka Ishikawa (Advisor). Techniques for Enabling Highly Efficient Message Passing on Many-Core Architectures. In *Proceedings of the 15th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid 2015)*, pages 697—700, May 2015.
5. **Min Si**, Yutaka Ishikawa (Advisor), and Pavan Balaji (Co-advisor). Optimizing MPI Implementation on Massively Parallel Many-Core Architectures. In *SC13 Doctoral Showcase - Early Research Showcase*, November 2013.
6. **Min Si** and Yutaka Ishikawa. Abstract: An MPI Library implementing Direct Communication for Many-Core Based Accelerators. In *High Performance Computing, Networking, Storage and Analysis (SCC), 2012 SC Companion*, pages 1527-–1528, November 2012. (*ACM Student Research Competition Final List*)

Thesis

1. **Min Si**. Techniques For Enabling Highly Efficient Message Passing on Many-Core Architectures. Dissertation. Department of Computer Science, Graduate School of Information Science and Technology, The University of Tokyo, Japan. March 2016.
2. **Min Si**. Communication Facility in Manycore-based Cluster System. Master Thesis. Department of Computer Science, Graduate School of Information Science and Technology, The University of Tokyo, Japan. September 2012.

Technical Talks and Invited Seminars

1. OpenSHMEM over MPI: Capabilities and Challenges. Invited talk at *State of the Union Birds of a Feather at SC19*, November 2019.
2. AI@Edge: Software System Implications. Invited talk of Microelectronics Workshop at *Argonne National Laboratory*, October 2019.
3. Beehive: A Dynamic Execution Environment for Performance, Power, and Resilience on Extreme-Scale Computing Systems. Invited talk of Argonne Named Fellows Mid-Year MiniSymposium at *Argonne National Laboratory*, June 2020.
4. Performance Analysis of MPI RMA in Supporting OpenSHMEM Runtime. Invited talk at *OpenSHMEM in the Era of Exascale Birds of a Feather at SC18*, November 2018.
5. Towards Dynamic Communication Runtime for Scalable Irregular Parallel Computing. Invited talk at *Florida State University*, December 2018.
6. Designing Dynamic Communication Infrastructure for Scalable Irregular Parallel Computing. LDRD seminar at *Argonne National Laboratory*, May 2018.
7. OpenSHMEM over Portable MPI RMA with Asynchronous Progress Support. Invited talk at *OpenSHMEM in the Era of Exascale Birds of a Feather at SC17*, November 2017.
8. Casper: Portable and Adaptable Asynchronous Progress Model for MPI Communication. Invited talk at *PCCluster Booth at SC17*, November 2017.
9. Towards Portable and Adaptable Asynchronous Communication for One-Sided Applications. Invited talk at *Tenth International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2 2017)*, August 2017.
10. Data Locality Challenges in Irregular Applications for Exascale Programing. Invited talk at *Fourth Workshop on Programming Abstractions for Data Locality (PADAL 2017)*, August 2017.

11. Scaling NWChem with Efficient and Portable Asynchronous Communication on NERSC Edison Supercomputer. Invited talk at *National Energy Research Scientific Computing Center*, March 2016.
12. Techniques for Enabling Highly Efficient Message Passing on Many-Core Architectures. Seminar at *Argonne National Laboratory*, October 2015.
13. Casper: An Asynchronous Progress Model for MPI RMA on Many-core Architectures. Seminar at *Argonne National Laboratory*, April 2015.
14. Casper: An Asynchronous Progress Model for MPI RMA on Many-core Architectures. Invited talk at *the 2ed Workshop of INRIA-ILLINOIS-ANL-BSC Joint Laboratory on Extreme Scale Computing*, November 2014.
15. MT-MPI: Multi-threaded MPI for Many-core Environments. Seminar at *Argonne National Laboratory*, September 2013.

Invited Panel

1. Panelist at *PGAS Applications Workshop held in conjunction with SC 2016*, November 2016.

Professional Services and Activities

Editorial Affiliations

1. *Co-Editor* of the IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS) Special Section on Parallel and Distributed Computing Techniques for AI, ML and DL. 2020.
2. *Guest Co-Editor* of the Special Issue on Programming Models and Applications for Multicores and Manycores (PMAM) of the International Journal of Concurrency and Computation: Practice and Experience (CCPE). 2021, 2020, 2019.
3. *Guest Co-Editor* of the Special Issue on Parallel Programming Models and Systems Software (P2S2) of the International Journal of Concurrency and Computation: Practice and Experience (CCPE). 2020.
4. *Guest Co-Editor* of the Special Issue on Applications and System Software for Hybrid Exascale Systems (AsHES) of the Elsevier International Journal of Parallel Computing (PARCO). 2019, 2018.
5. *Guest Co-Editor* of the Special Issue on Parallel Programming Models and Systems Software (P2S2) of the Elsevier International Journal of Parallel Computing (PARCO). 2019, 2018.
6. *Guest Co-Editor* of the Special Issue on Programming Models and Applications for Multicores and Manycores (PMAM 2018) of the Elsevier International Journal of Parallel Computing (PARCO). 2018.

Chair and Co-Chair - Conferences / Workshops

1. *General Chair* of the 11th International Workshop on Accelerators and Hybrid Emerging Systems (AsHES 2021), to be held in conjunction with the 35th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2021). May 2021, Portland, Oregon, USA.
2. *Financial Chair* of the 24th IEEE International Conference on Cluster Computing (Cluster 2022). September 2022, Heidelberg, Germany.
3. *Virtual Arrangements Co-Chair* of the 23th IEEE International Conference on Cluster Computing (Cluster 2021). September 2021, Portland, Oregon, USA.
4. *Track Co-Chair* of the Programming Models and System Software track at International Conference on High Performance Computing in Asia-Pacific Region (HPC Asia 2021). January 2021, Jeju, Korea.
5. *Program Co-Chair* of the 13th International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2 2020), to be held in conjunction with the 49th International Conference on Parallel Processing (ICPP 2020). Edmonton, AB, Canada.
6. *General Chair* of the 10th International Workshop on Accelerators and Hybrid Exascale Systems (AsHES 2020), to be held in conjunction with the 34th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2020). May 2020, New Orleans, Louisiana, USA.

7. *Program Co-Chair* of the 11th International Workshop on Programming Models and Applications for Multicores and Manycores (PMAM 2020), to be held in conjunction with Principles and Practice of Parallel Programming 2020 (PPoPP 2020). February 2020, San Diego, California, USA.
8. *Financial Chair* of the 27th European MPI Users Group Meeting (EuroMPI 2020). September 2020, Austin, Texas, USA.
9. *Panels Vice-Chair* of the 2019 International Conference for High Performance Computing, Networking, Storage, and Analysis (SC19). November 2019, Dallas, Texas, USA.
10. *Program Co-Chair* of the 12th International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2 2019), to be held in conjunction with the 48th International Conference on Parallel Processing (ICPP 2019). Kyoto, Japan.
11. *Program Co-Chair* of the 9th International Workshop on Accelerators and Hybrid Exascale Systems (AsHES 2019), to be held in conjunction with the 33rd IEEE International Parallel and Distributed Processing Symposium (IPDPS 2019). May 2019, Rio de Janeiro, Copacabana, Brazil.
12. *Program Co-Chair* of the 10th International Workshop on Programming Models and Applications for Multicores and Manycores (PMAM 2019), to be held in conjunction with Principles and Practice of Parallel Programming 2019 (PPoPP 2019). February 2019, Washington, DC, USA.
13. *Program Co-Chair* of the 11th International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2 2018), to be held in conjunction with the 47th International Conference on Parallel Processing (ICPP 2018). Portland, Oregon, USA.
14. *Program Co-Chair* of the 8th International Workshop on Accelerators and Hybrid Exascale Systems (AsHES 2018), to be held in conjunction with the 32nd IEEE International Parallel and Distributed Processing Symposium (IPDPS 2018). May 2018, Vancouver, Canada.
15. *Web Co-Chair* of the 25th European MPI Users Group Meeting (EuroMPI 2018). Barcelona, Spain.
16. *Financial Co-Chair* of the 24th European MPI Users Group Meeting (EuroMPI 2017). September 2017, Chicago, USA.
17. *Publicity Chair* of the 9th International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2 2016), to be held in conjunction with the 45th International Conference on Parallel Processing (ICPP 2016). August 2016, Philadelphia, PA, USA.
18. *Postdoc-Ph.D.-Student Evening Meeting Co-chair* of the 2ed INRIA-ILLINOIS-ANL-BSC Joint Laboratory on Extreme Scale Computing workshop (JLESC). November 2014, Chicago, IL, USA.

Committee Member - Conferences / Workshops

1. *Technical Program Committee Member* of the Multidisciplinary track at the 35th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2021). May 2021, Portland, Oregon, USA.
2. *Technical Program Committee Member* of the Programming Systems track at International Conference for High Performance Computing, Networking, Storage and Analysis (SC 2021). November 2021, St Louis, MO, USA.
3. *External Review Committee Member* of the 26th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP 2021). February 2021, Seoul, South Korea.
4. *Technical Program Committee Member* of the State of the Practice track at International Conference for High Performance Computing, Networking, Storage and Analysis (SC 2020). November 2020, Atlanta, GA, USA.
5. *Technical Program Committee Member* of the 34th ACM International Conference on Supercomputing (ICS 2020). June 2020, Barcelona, Spain.
6. *External Review Committee Member* of the 25th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP 2020). February 2020, San Diego, CA, USA.
7. *Technical Program Committee Member* of the International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD) 2019. October 2019, Campo Grande, Brazil
8. *Technical Program Committee Member* of the 26th European MPI Users Group Meeting (EuroMPI 2019). September 2019, Zurich, Switzerland.
9. *External Review Committee Member* of the 33rd ACM International Conference on Supercomputing (ICS 2019). June 2019, Phoenix, AZ, USA.

10. *Technical Program Committee Member* of the 48th International Conference on Parallel Processing (ICPP 2019). August 2019, Kyoto, Japan.
11. *Technical Program Committee Member* of the 19th IEEE/ACM International Symposium on Cluster,Cloud and Grid Computing (CCGrid 2019). May 2019, Larnaca, Cyprus.
12. *Technical Program Committee Member* of the 2019 Supercomputing Asia conference (SCA 2019). March 2019, Singapore.
13. *Technical Program Committee Member* of the 20th IEEE International Conference on Cluster Computing (Cluster 2018). September 2018, Belfast, UK.
14. *Technical Program Committee Member* of the 25th European MPI Users Group Meeting (EuroMPI 2018). September 2018, Barcelona, Spain.
15. *Technical Program Committee Member* of the 5th workshop on OpenSHMEM and Related Technologies (OpenSHMEM 2018). August 2018, Baltimore, MD, USA.
16. *Technical Program Committee Member* of the 32nd ACM International Conference on Supercomputing (ICS 2018). June 2018, Beijing, China.
17. *Technical Program Committee Member* of the 18th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid 2018). May 2018, Washington, DC, USA.
18. *Workshops Committee Member* of the 32nd IEEE International Parallel & Distributed Processing Symposium (IPDPS 2018). May 2018, Vancouver, Canada.
19. *Technical Program Committee Member* of the 2018 Supercomputing Asia conference (SCA 2018). March 2018, Singapore.
20. *Technical Program Committee Member* of the 23rd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP 2018). February 2018, Vienna, Austria.
21. *Technical Program Committee Member* of the 9th International Workshop on Programming Models and Applications for Multicores and Manycores (PMAM 2018), held in conjunction with the 23rd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP 2018). February 2018, Vienna, Austria.
22. *Technical Program Committee Member* of the 19th IEEE International Conference on High Performance Computing and Communications (HPCC 2017). December 2017, Bangkok, Thailand.
23. *Technical Program Committee Member* of the PGAS Applications Workshop, held in conjunction with the IEEE/ACM International Conference for High Performance Computing, Networking, Storage, and Analysis (SC). November 2017, Denver, CO, USA.
24. *Technical Program Committee Member* of the 11th International Conference on Advanced Engineering Computing and Applications in Sciences (ADVCOMP 2017). November 2017, Barcelona, Spain.
25. *Technical Program Committee Member* of the 19th IEEE International Conference on Cluster Computing (Cluster 2017). September 2017, Honolulu, Hawaii, USA.
26. *Technical Program Committee Member* of the 10th International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2 2017), held in conjunction with the 46th International Conference on Parallel Processing (ICPP 2018). August 2017, Bristol, UK.
27. *Technical Program Committee Member* of the 4th workshop on OpenSHMEM and Related Technologies (OpenSHMEM 2017). August 2017, Annapolis, MD, USA.
28. *Technical Program Committee Member* of the 25th International Symposium on High Performance Interconnects (HOTI 2017). August 2017, Santa Clara, CA, USA.
29. *Technical Program Committee Member* of the 7th International Workshop on Accelerators and Hybrid Exascale Systems (AsHES 2017), held in conjunction with the 31st IEEE International Parallel and Distributed Processing Symposium (IPDPS 2017). May 2017, Orlando, FL, USA.
30. *Technical Program Committee Member* of the 17th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid 2017). May 2017, Madrid, Spain.
31. *Technical Program Committee Member* of the 24th European MPI Users Group Meeting (EuroMPI 2017). September 2017, Chicago, USA.
32. *Workshops Committee Member* of the 31st IEEE International Parallel & Distributed Processing Symposium (IPDPS 2017). May 2017, Orlando, FL, USA.

33. *Technical Program Committee Member* of the 7th International Workshop on Data-Intensive Computing in the Clouds (DataCloud 2016), held in conjunction with the IEEE/ACM International Conference for High Performance Computing, Networking, Storage, and Analysis (SC). November 2016, Salt Lack City, UT, USA.
34. *Technical Program Committee Member* of the workshop on Exascale MPI (ExaMPI 2016), held in conjunction with the IEEE/ACM International Conference for High Performance Computing, Networking, Storage, and Analysis (SC). November 2016, Salt Lack City, UT, USA.

Reviewer - Conference / Workshops

IPDPS 2017, 2016
IEEE International Parallel & Distributed Processing Symposium

ICS 2016
ACM International Conference on Supercomputing

NPC 2016
IFIP International Conference on Network and Parallel Computing

HOTI 2016
IEEE International Symposium on High Performance Interconnects

ESPM2 2016
International Workshop on Extreme Scale Programming Models and Middleware

Euro-Par 2015
International European Conference on Parallel and Distributed Computing

AsHES 2014
International Workshop on Accelerators and Hybrid Exascale Systems

Journal Referee

TPDS 2020, 2019, 2018, 2017, 2014
IEEE Transactions on Parallel and Distributed Systems

TC 2020, 2019
IEEE Transactions on Computers

TCC 2017
IEEE Transactions on Cloud Computing

TMSCS 2018, 2017
IEEE Transactions on Multi-Scale Computing Systems

JPDC 2020, 2019, 2018, 2017, 2016, 2015
Journal of Parallel and Distributed Computing

CPE 2017, 2016
Concurrency and Computation: Practice and Experience

PARCO 2018, 2017, 2016
Elsevier International Journal of Parallel Computing

IJPP 2018, 2016
International Journal of Parallel Programming

Other Technical Referee

- *Award Selection Committee Member* of 2019 IEEE Computer Society TCHPC Early Career Researchers Award for Excellence in High Performance Computing.
- *Review Committee Member* of the ACM SIGHPC/Intel Computational and Data Science Fellowships Program. April, 2018.
- *External Reviewer* of doctoral dissertation for a PhD candidate (Sergio Iserte) from Jaume I University, Spain. July, 2018.

Tutorials

- **Min Si**. Parallel Programming with MPI. Invited lecture in the CS546 Parallel and Distributed Processing course at Illinois Institute of Technology. September 2019, IL, USA.

- **Min Si**. Parallel Programming with MPI. Invited lecture in the CS546 Parallel and Distributed Processing course at Illinois Institute of Technology. September 2018, IL, USA.
- Pavan Balaji, Rajeev Thakur, Ken Raffenetti, Antonio J Peña, and **Min Si**. Parallel Programming with MPI. Full-day tutorial at Argonne National Laboratory. June 2015, IL, USA.

Professional Affiliations

- ACM Professional Member.

Team Leadership

Staff Supervision

- *Huansong Fu*:
  Postdoctoral Research Associate, Argonne National Laboratory. Period: 03/2019 to 08/2019.
  Predoctoral Research Associate, Argonne National Laboratory. Period: 08/2018 to 12/2018.

Students Supervision

- *Michael Wilkins*: Ph.D. student, Department of Computer Engineering, Northwestern University, USA. Optimizing MPI communication by leveraging data analytics techniques. Period: 8/2020 to 11/2020.
- *Li Cao*: Master student, Physical Science Division, University of Chicago, USA. Exploring accurate and high-performance scientific data analytics. Period: 8/2020 to 12/2020.
- *Subhadeep Bhattacharya*: Ph.D. student, Department of Computer Science, Florida State University, USA. Exploring GPU-aware Reduction Offloading inside MPI Library on Heterogeneous Clusters. Period: 05/2019 to 08/2019.
- *Kaiming Ouyang*: Ph.D. student, Department of Computer Science, University of California, Riverside, USA. Leveraging Shared Memory Techniques in MPI Communication Runtime System. Period: 10/2018 to present.
- *Yanhao Chen*: Ph.D. student, Department of Computer Science, Rutgers University, USA. Exploiting Dynamic Communication Runtime for Irregular MPI Applications. Period: 05/2018 to 08/2018.
- *Huansong Fu*: Ph.D. student, Department of Computer Science, Florida State University, USA. Analyzing and Improving Portable OpenSHMEM Runtime Implementation over MPI. Period: 05/2018 to 08/2018.

Students Mentoring

- *Sarunya Pumma*: Ph.D. student, Department of Computer Science, Virginia Tech, USA. Scaling Machine Learning Algorithms on Large Supercomputing Systems. Period: 08/2016 to 01/2017.