MINSIK KIM

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RESEARCH INTERESTS

Domain-Specific Architecture / Reconfigurable Computing / Hardware Design Framework

EDUCATION

Seoul National University Mar. 2017 - Present
Undergraduate Student *Seoul, Korea*

- B.S. in Electrical and Computer Engineering (expected graduation: Feb. 2023)
- Overall GPA: 4.09 / 4.30, Major GPA: 4.19 / 4.30

RESEARCH EXPERIENCE

VLSI Lab, SNU Jul. 2022 - Present
Research Intern (Advisor: Professor Jae-Joon Kim) *Seoul, Korea*

- Led project of implementing variable bit-precision CNN accelerator on FPGA, and proposed to apply early computation termination on same architecture

Computer Architecture and Parallel Processing Lab, SNU Jan. 2022 - Jun. 2022
Bachelor Thesis (Advisor: Professors Hyuk-Jae Lee, Xuan Truong Nguyen) *Seoul, Korea*

- Led design and implementation of YOLOv3-tiny accelerator on Nexys A7-100T FPGA
- Quantized model and extracted intermediate feature maps for debugging by modifying darknet code
- Proposed, implemented, and validated dynamic data reuse scheme, spatially-banked feature map buffer, MAC units with configurable adder tree
- Submitted designed accelerator to Deep Learning Design Contest, won 1st place, gave English oral presentation in AICAS 2022 design contest session, and wrote paper describing its design ideas and implementation

Music and Audio Research Group, SNU Jul. 2021 - Aug. 2021
Research Intern (Advisor: Professor Kyogu Lee) *Suwon, Korea*

- Proposed and led project of implementing deep learning-based automatic differentiable mixing console

AWARDS & RECOGNITION

1st Place, Deep Learning Hardware Design Contest, POLARIS Jun. 2022
5,000,000 KRW (3.8K USD)

1st Place, AI OCR Hackathon, National Information Society Agency Dec. 2021
7,000,000 KRW (5.3K USD)

SNU ECE Aid Foundation Scholarship, SNU ECE Aid Foundation Fall 2021
2,500,000 KRW (1.8K USD)

Gwansa Foundation Scholarship, Gwansa Foundation Fall 2021
3,000,000 KRW (2.3K USD)

Merit-based Scholarship, SNU 2017 - 2018, 2020 - 2022
19,500,000 KRW in total (14.6K USD)

MANUSCRIPT IN PROGRESS

<u>Minsik Kim</u>[1], Hojin Seo[1], Kyoungseok Oh[1], Youngmock Cho[1], Xuan Truong Nguyen, and Hyuk-Jae Lee. "A Low-latency FPGA Accelerator for YOLOv3-tiny with Flexible Layerwise Mapping and Dataflow," **Under review** in *IEEE Transactions on Circuits and Systems for Video Technology.* [pdf]

TEACHING EXPERIENCE

Digital Logic Design and Lab, SNU   Fall 2022
Teaching Assistant   *Seoul, Korea*

- Ran lab sessions covering gate-level circuit design and Verilog coding every week, answered questions in person, marked assignments

AI Hardware System Design Project, SNU   Spring 2022
Teaching Assistant   *Seoul, Korea*

- Covered RISC-V CPU architecture and CNN accelerator design
- Ran lab sessions covering C, Verilog, and Matlab coding every week, answered questions in person, marked assignments and final project, proctored exam

Digital Systems Design and Experiments, SNU   Fall 2021
Tutor of Peer-tutoring Program   *Seoul, Korea*

- Gave supplementary lecture to assigned peer tutee via Zoom every week, answered questions relating to theory and lab sessions via Zoom and email

Digital Logic Design and Lab, SNU   Fall 2020
Tutor of Peer-tutoring Program   *Seoul, Korea*

- Ran open Zoom session for students every week, answered questions relating to theory and lab sessions via Zoom and email

INTERNSHIP

Hardware Design Group, Samsung Electronics   Jan. 2021 - Feb. 2021
Intern   *Suwon, Korea*

- Implemented Viterbi decoder based on published design methodology and proposed method to improve its latency, selected as one of top 5 intern projects among over 40 projects

TECHNICAL SKILLS

Programming Languages	C/C++, Python, Matlab, Java, Assembly Language (RISC-V, X86-64)
Hardware Tools	Verilog, Vitis HLS, Chisel

LANGUAGE PROFICIENCY

Fluent in English, Native in Korean

- **GRE** - Verbal: 170, 99%, Quantitative: 170, 96%, Writing: 5.0, 91%
- **IBT TOEFL** - 117 (Reading: 30, Listening: 29, Speaking: 29, Writing: 29)

MILITARY SERVICE

ROK Army English Interpreter   Jan. 2019 - Aug. 2020
Honorable Discharge   *Anyang, Korea*

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[1]Equal contribution