**Homework 10: Sliding window, CNN Accelerator top file**

**Issued:** May 16 (Tuesday.), 2023 **Due:** May 22 (Monday.), 2023

**What to turn in**: **Copy the text from your MODIFIED codes and paste it into a document**. If a question asks you to plot or display something to the screen, also include the plot and screen output your code generates. Submit either a \*.doc or \*.pdf file.

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**Problem 1 (10p): Sliding window**

Implement a sliding window algorithm in Verilog. Please see the description in lecture 11 for details.

What you have to do:

1. Complete the missing codes to generate din in first\_layer\_tb.v.
2. Do a simulation with time = 400 us and capture the waveform.
3. Use check\_hardware\_results.m to verify the output images generated by the H/W simulation.

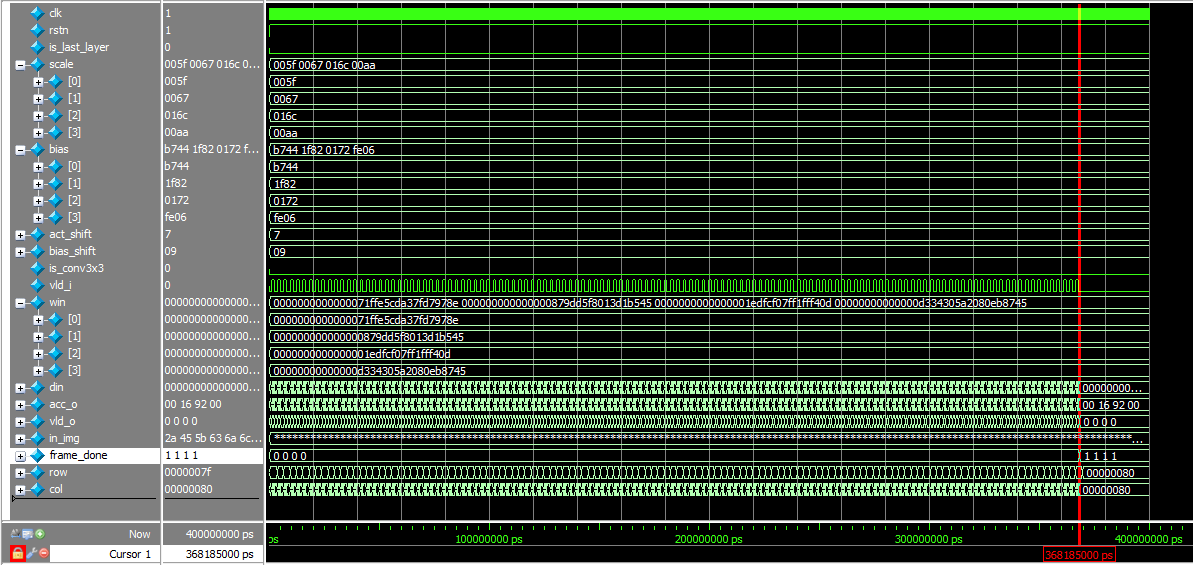
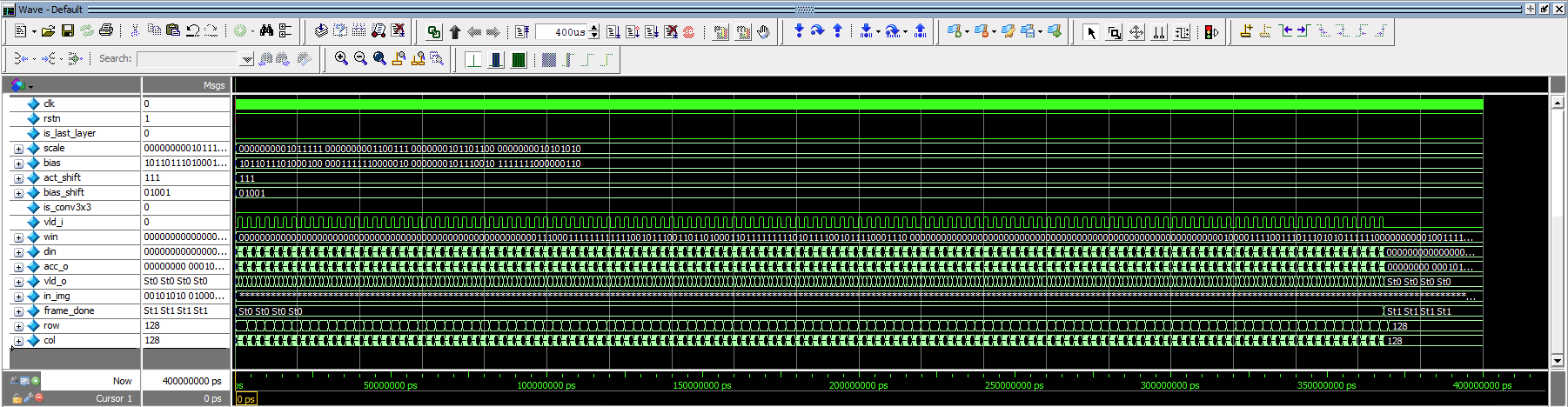
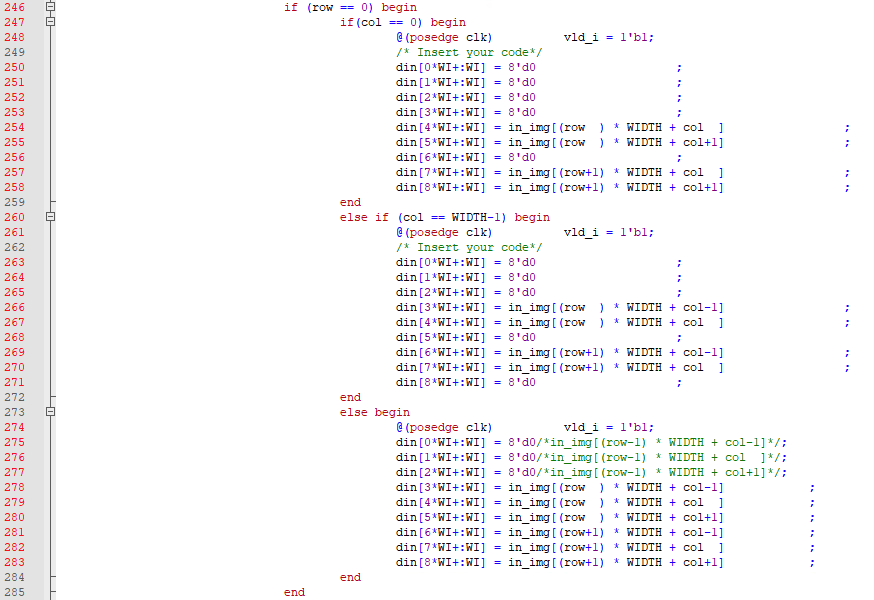
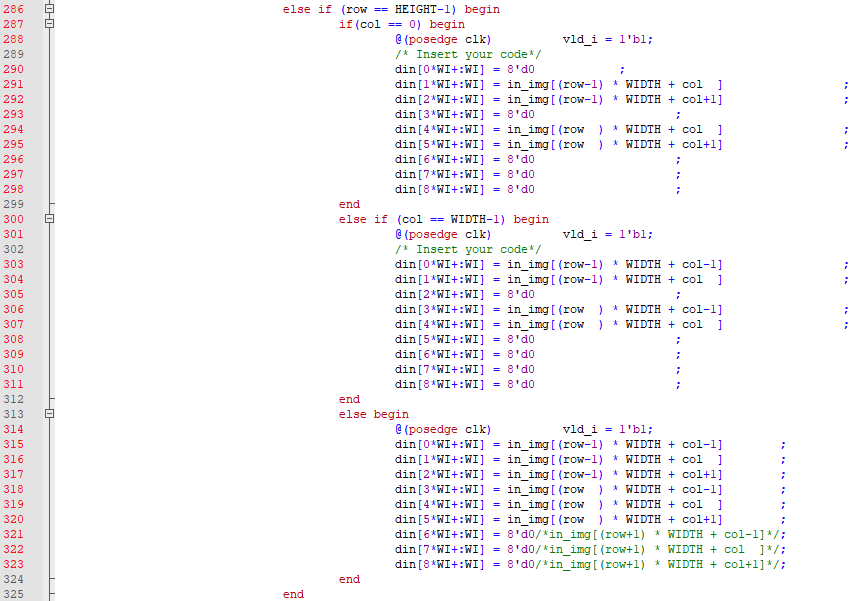


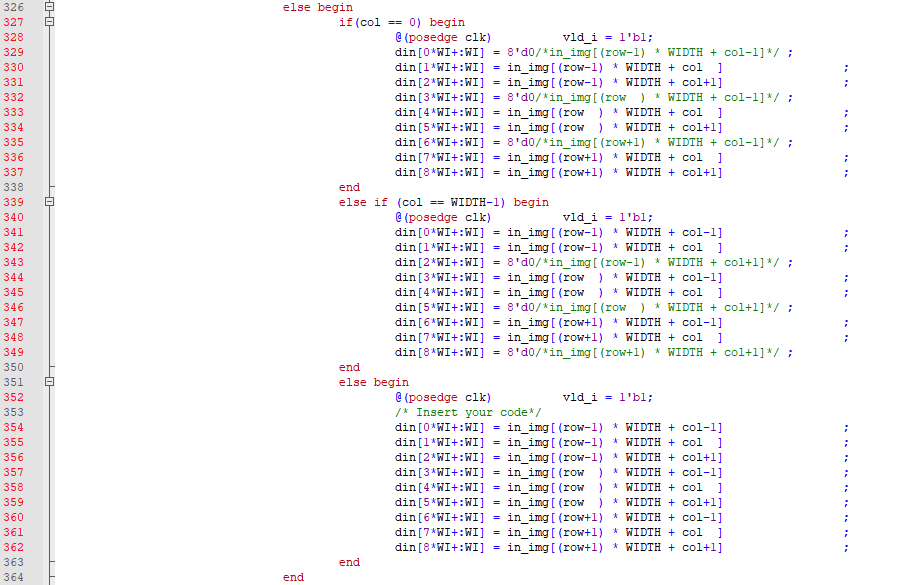
Fig. 1-1: A captured waveform of first\_layer\_tb.

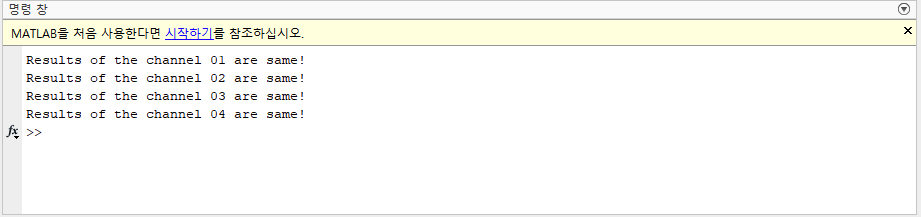
**Solution 1: Sliding Window**

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**Problem 2 (10p): AHB interface, CNN Controller**

Implement an AHB interface and a controller, i.e. finite state machine (FSM), for a CNN accelerator IP in Verilog. Please see the description in the lecture note for details.

What you have to do:

1. Complete the missing codes in cnn\_accel.v and cnn\_fsm.v.
2. Do a simulation with time = 400us and capture the waveform.

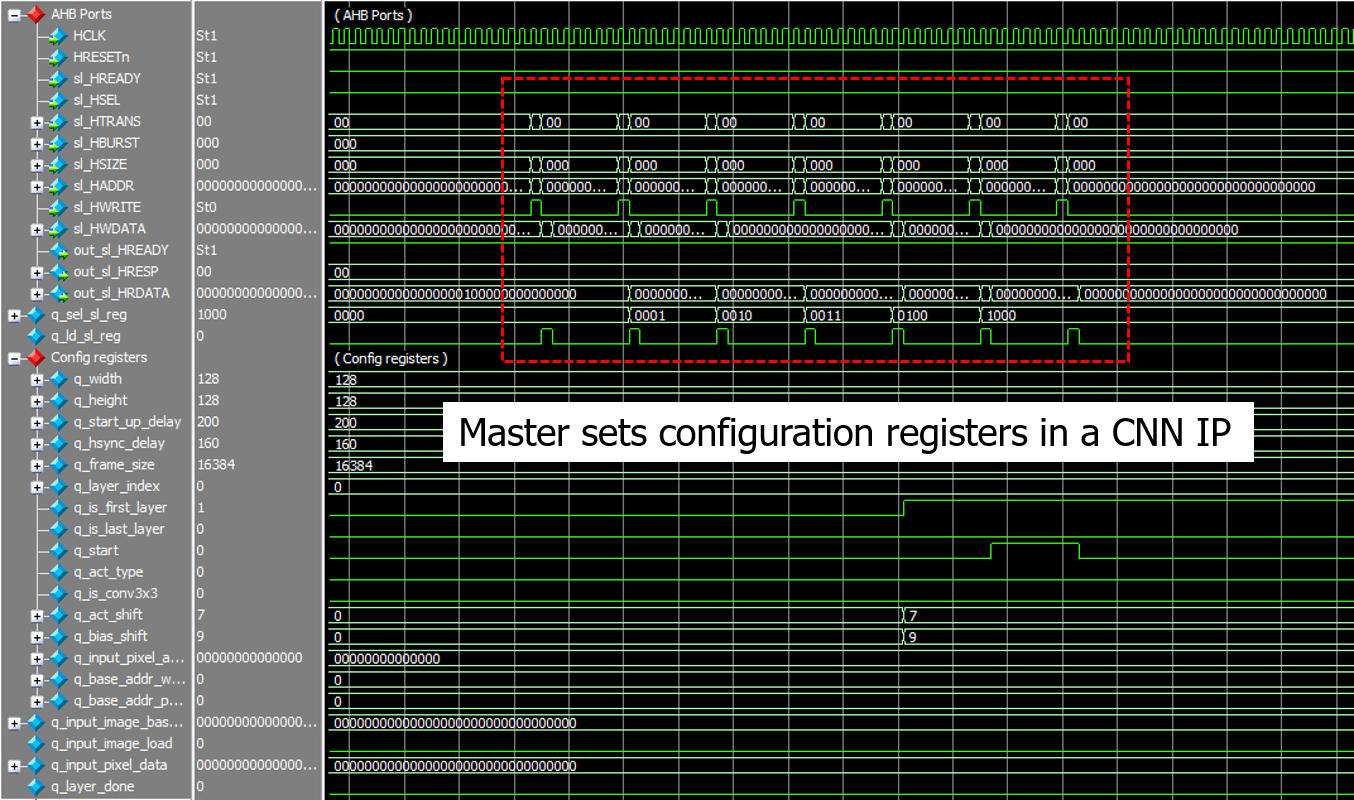


Fig. 2-1: A captured waveform of the AHB slave interface in cnn\_fsm.v.

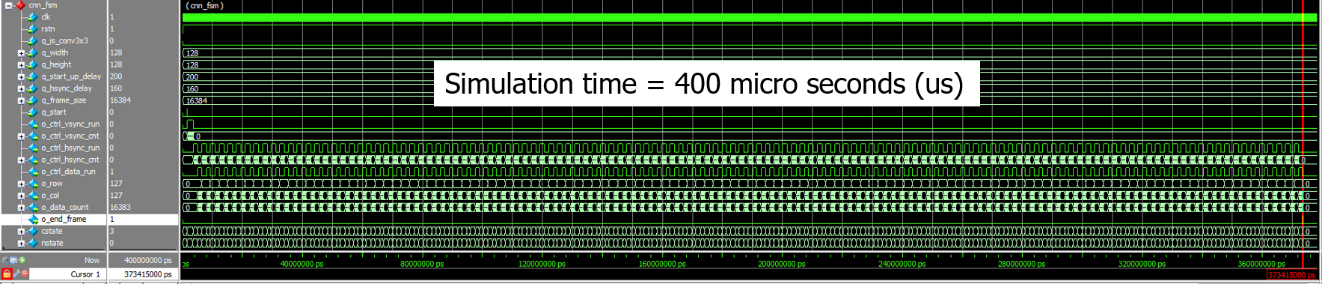
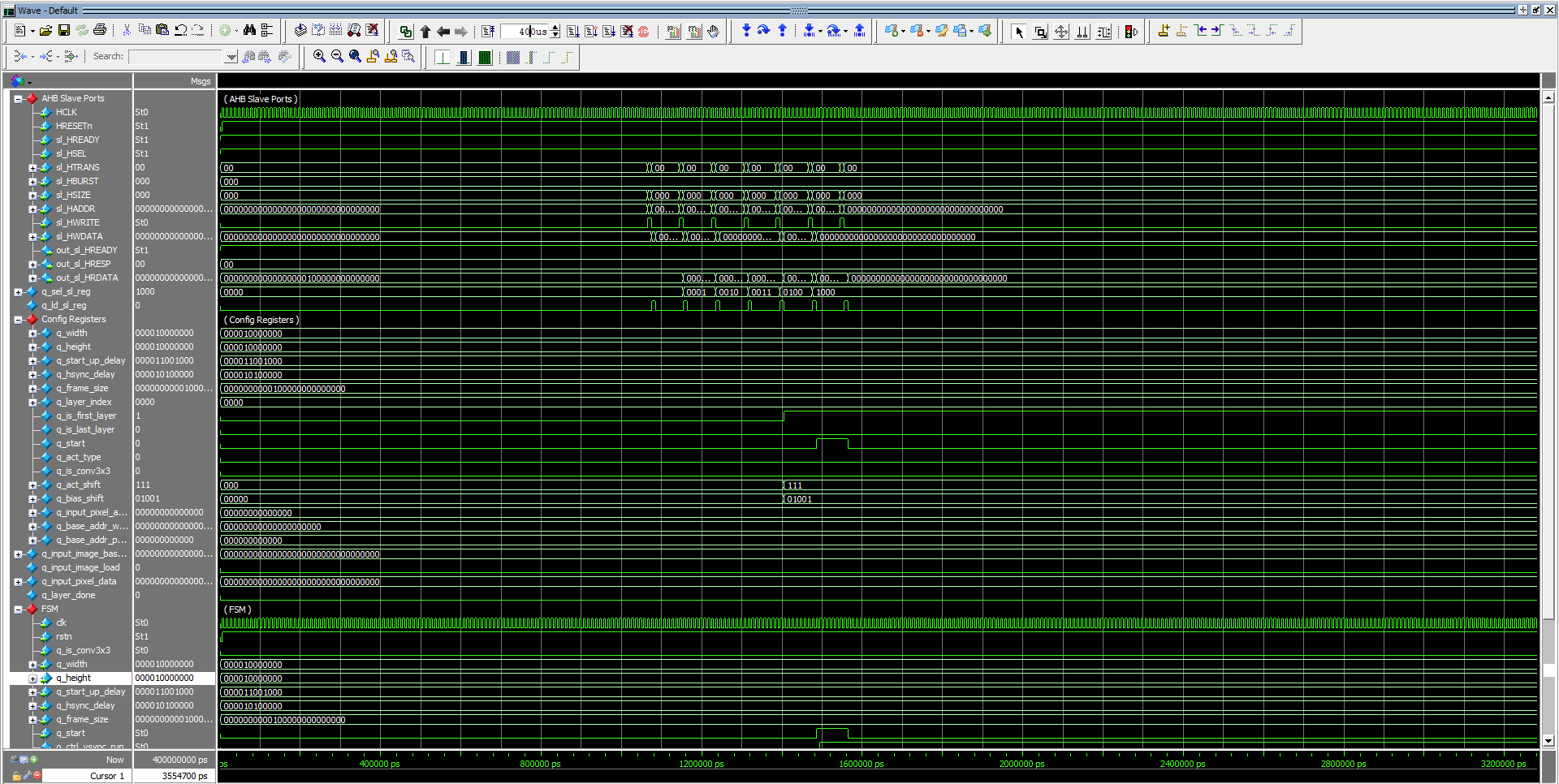
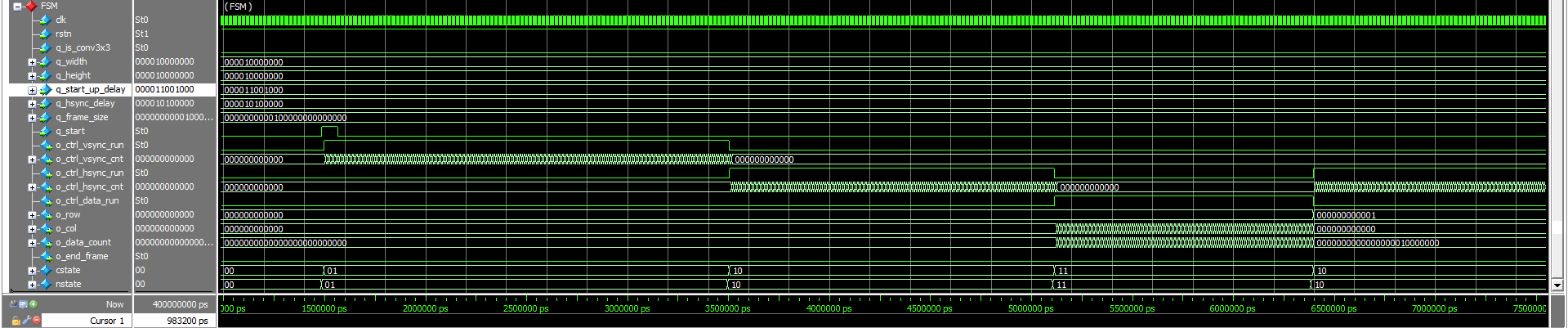
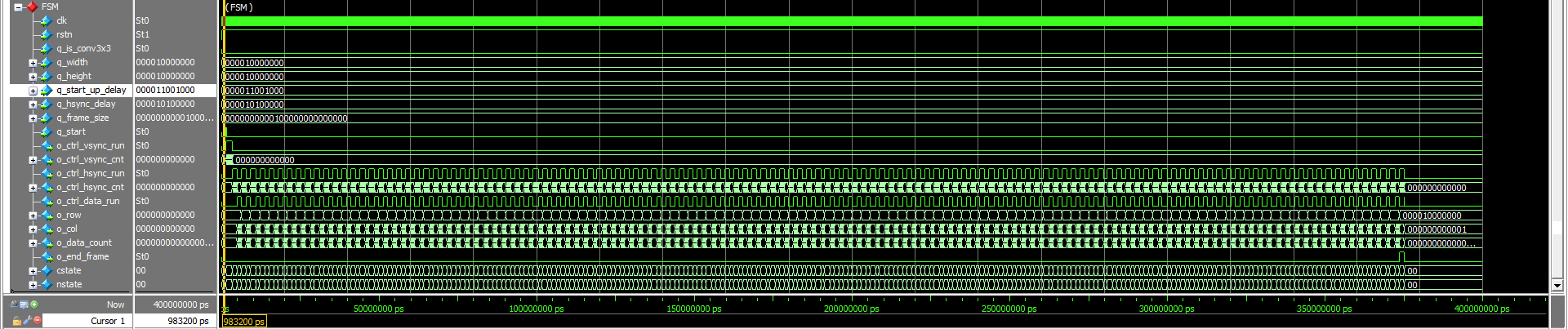


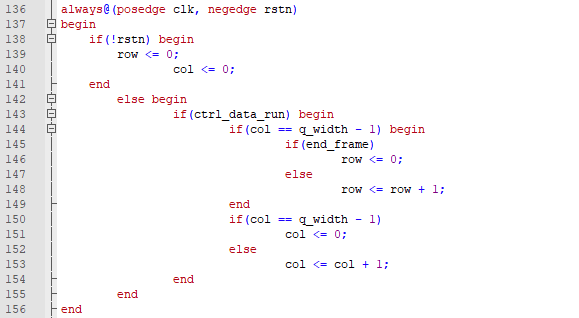
Fig. 2-2: A captured waveform of FSM in cnn\_fsm.v

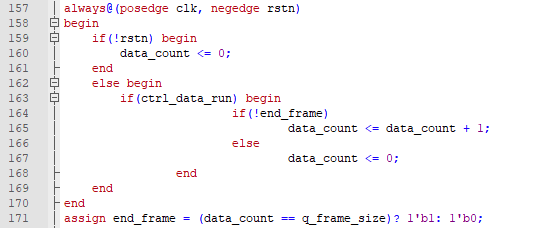
**Solution 2: AHB Interface, CNN Controller**

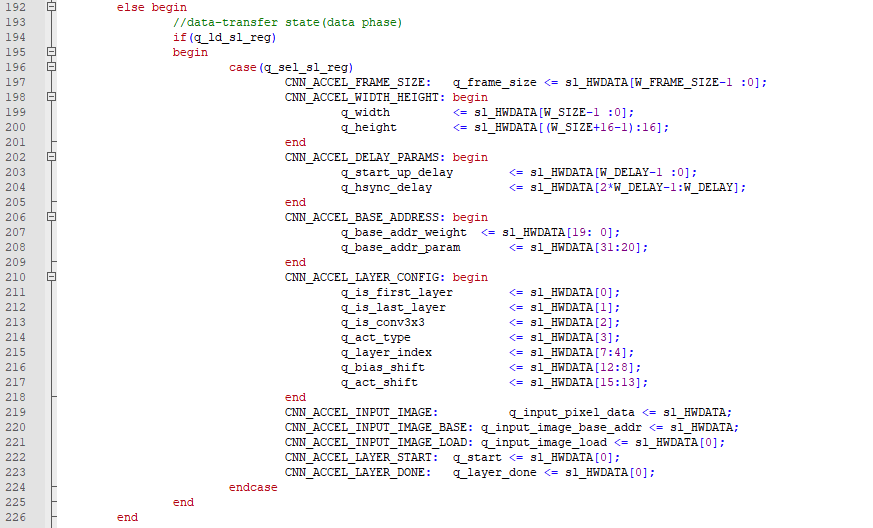
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**Problem 3 (10p): Simplified CNN Accelerator IP**

Implement a CNN top file in Verilog. Please see the description in lecture 11 for details.

What you have to do:

1. Reuse cnn\_fsm.v in Problem 2.
2. Complete the missing codes in cnn\_accel.v.

* Reuse code to set configuration registers in Lab 2
* Add filters for the output channel 3
* Generate din, vld\_i

1. Do a simulation with time = 400us and capture the waveform.
2. Use check\_hardware\_results.m to verify the output images generated by the H/W simulation.

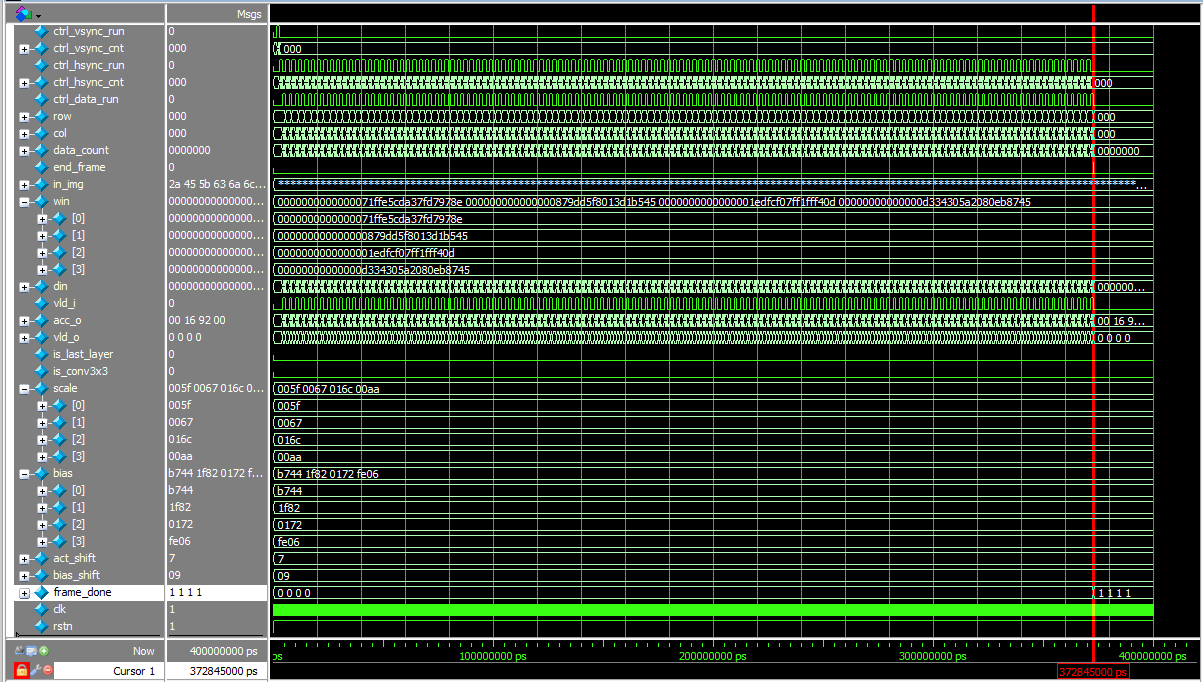
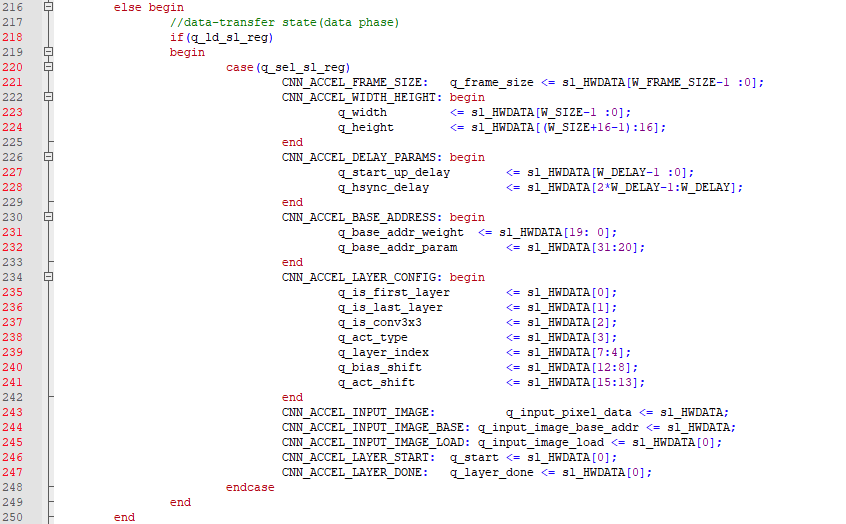
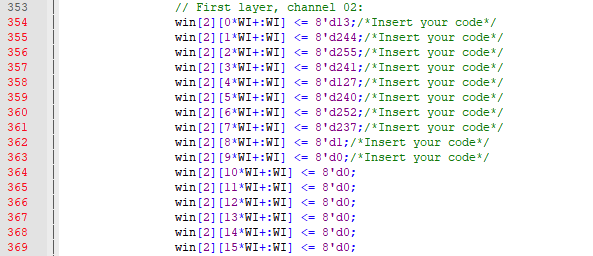
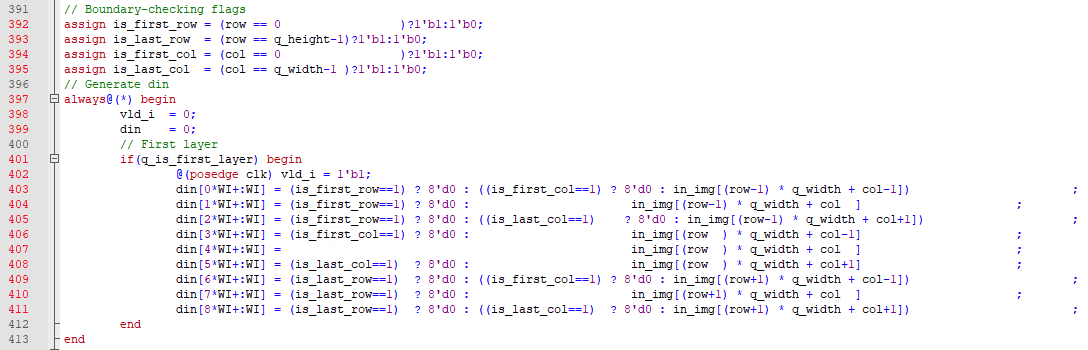
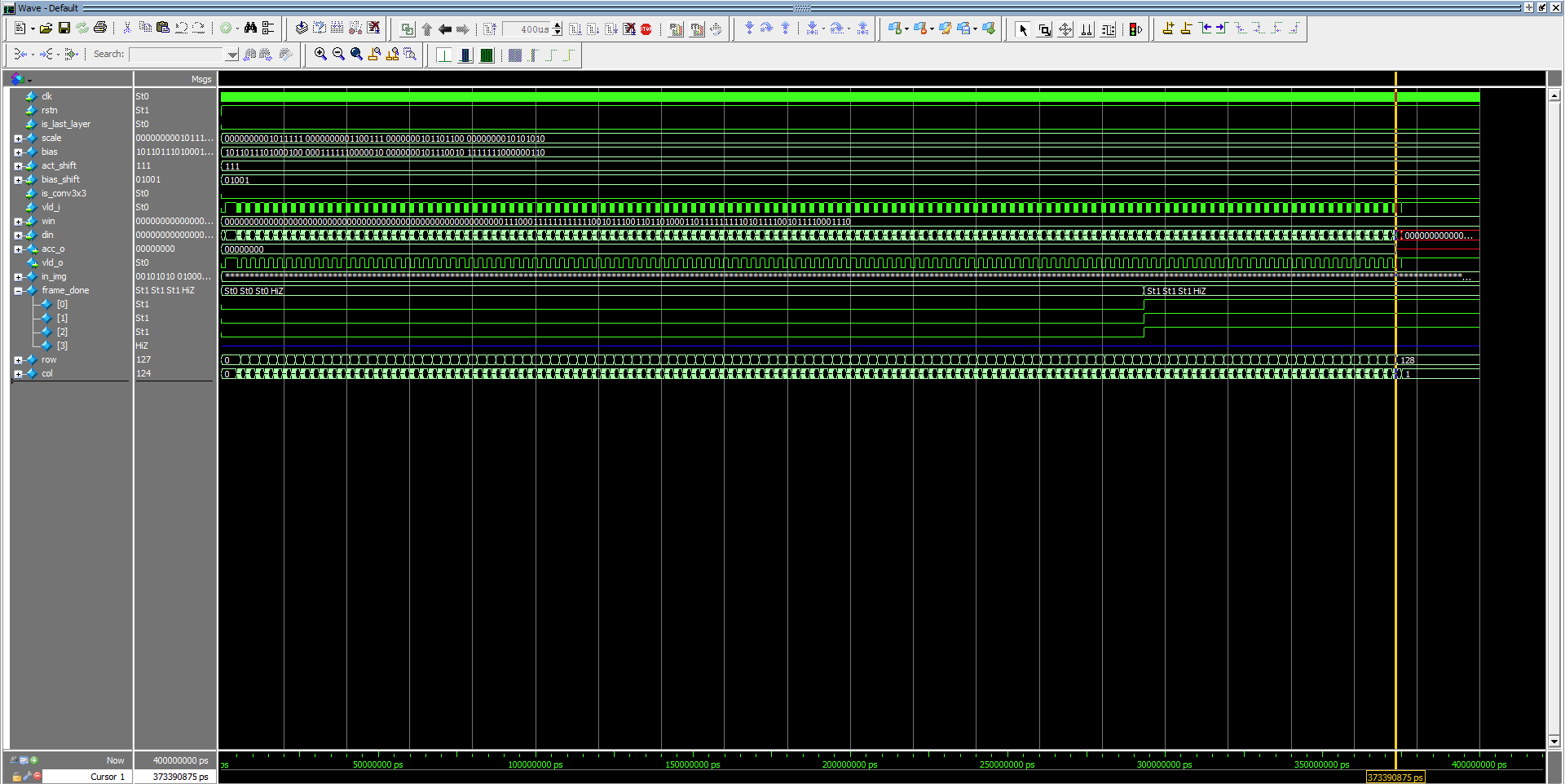


Fig. 3-1: Simulation results.

**Problem 3: Simplified CNN Accelerator IP**

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**Problem 4: (Optional)**

1. (1p) Briefly explain FSM’s states in the CNN accelerator in Problem 3. (Hint: You can change START\_UP\_DELAY and HSYNC\_DELAY in the testbench (cnn\_accel\_tb.v), do simulation, and check how the result is changed).
2. (1p) In Problems 1 and 3, it is costly to use multiplication for indexes in a sliding window (Fig.4-1). Modify the code to remove all multiplication operations for indexes here.

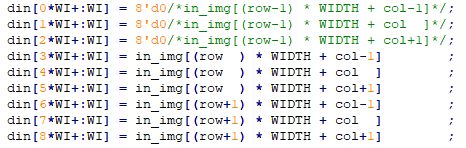


Fig. 4-1: Using multiplication to access image pixels in a sliding window.