

Lab Report for EESM5060 LAB6

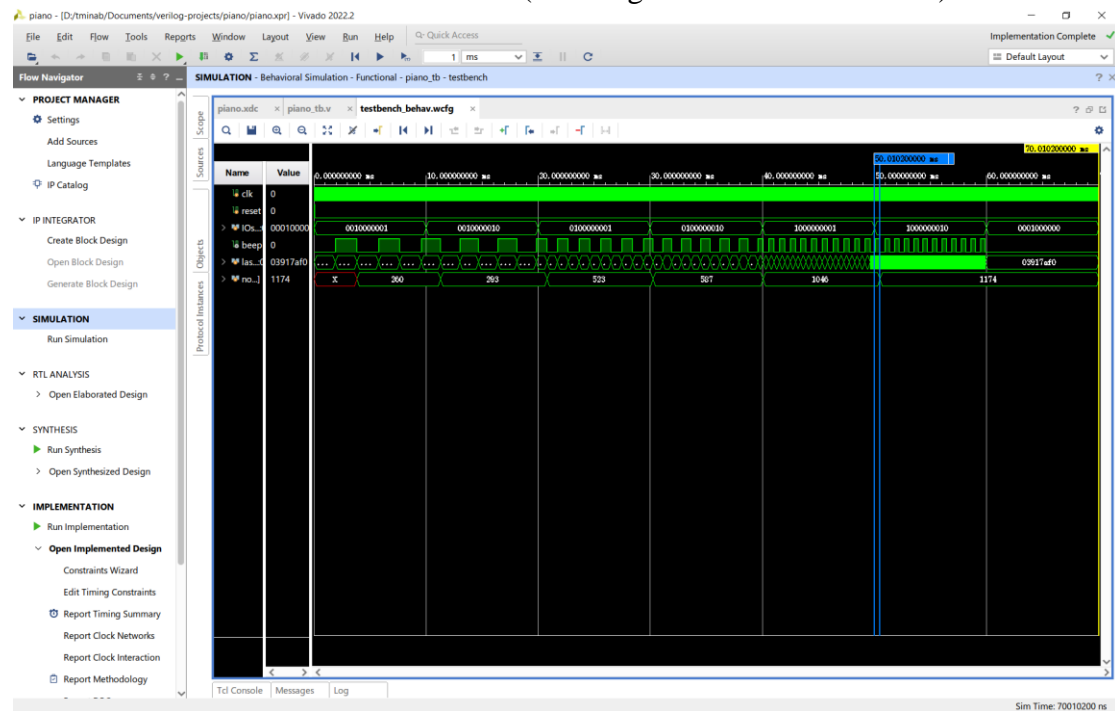
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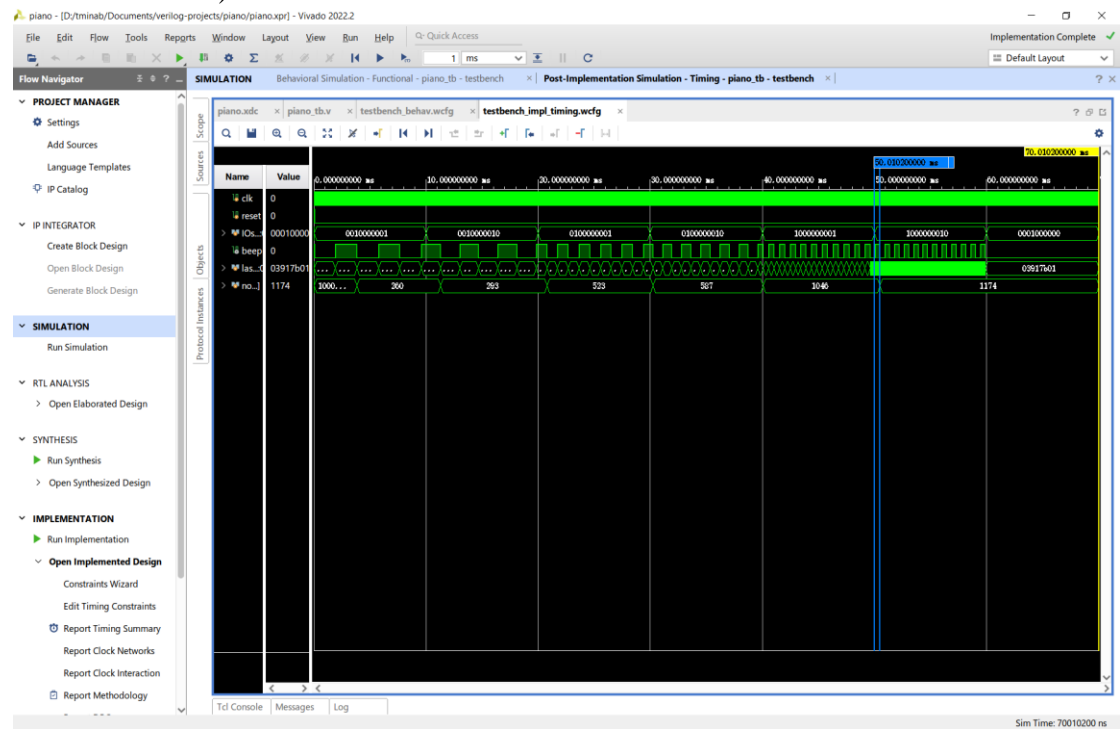
1. Exercise 2A

(without content in this exercise, the points for the other exercise will not be counted.)

A. Screenshot of behavioral simulation (covering entire Vivado window)



B. Screenshot of post-implementation timing simulation (covering entire Vivado window)



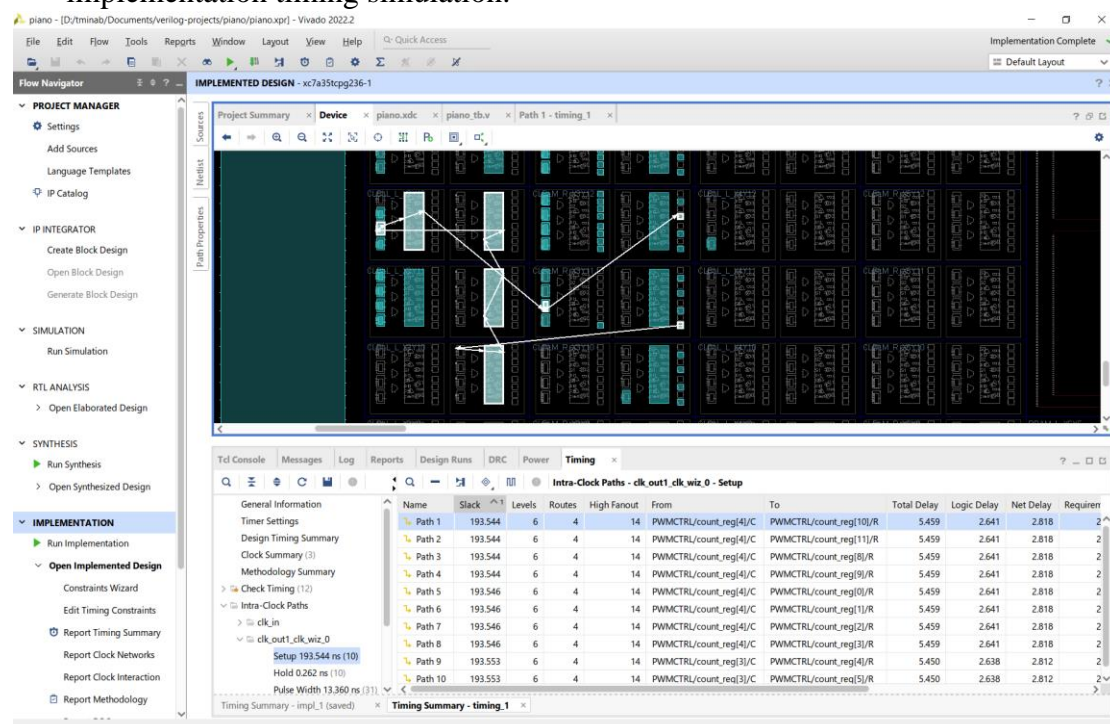
2. Exercise 2B

A. Modify the imported XDC file by changing the line “create_clock -period 10.000 -waveform {0.000 5.000} [get_ports clk_in]” to set a tighter clock period constraint. Change the clock period to 2 ns instead of 10 ns. (2 points)

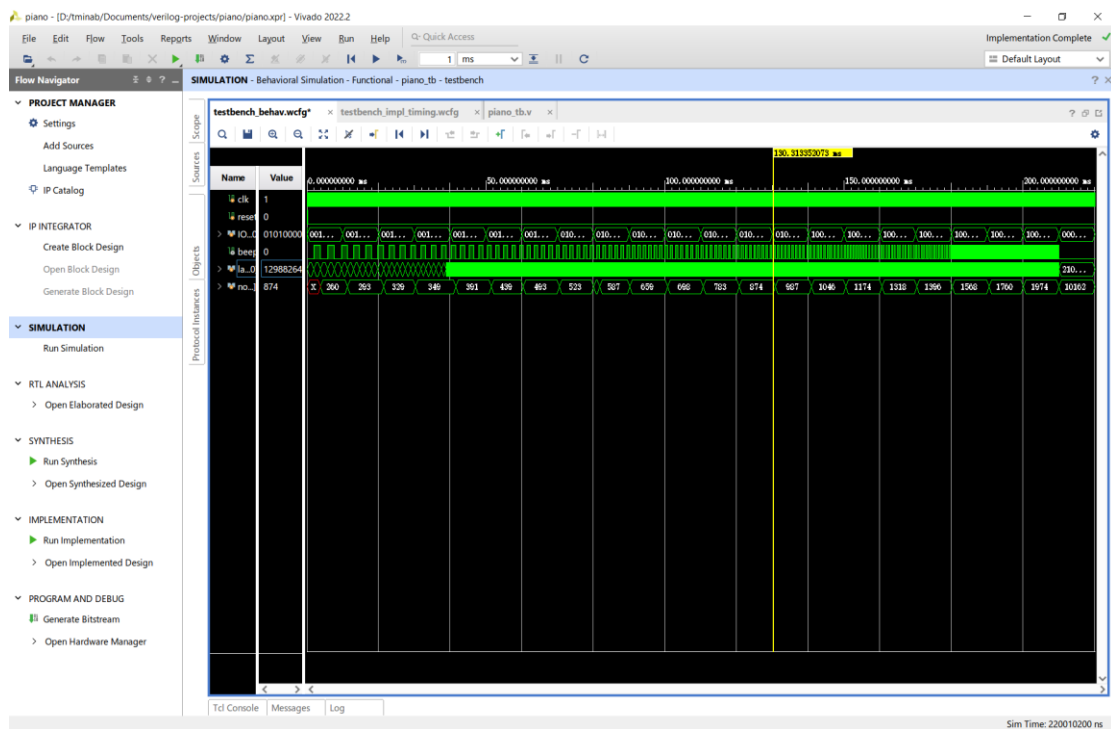
A1) Did your design meet timing?

A: No, the design has a maximum total delay of 5.459 ns, which is larger than the 2 ns clock period.

A2) If your design meets the timing, please provide screenshots of post-implementation timing simulation.



B. Modify the testbench.v file to provide different inputs to test your design. Repeat behavioral simulation and save the new testbench.v and a corresponding simulation screenshot in this report. (1 points)



3. Exercise 2C

Attach your modified *keytofrequency.v* and the behavioral simulation screenshot in this report. (2 points)

1. *keytofrequency.v*:

```
1 `timescale 1ns / 1ps
2
3 module keytofrequency(clk_5MHz, notecode, countStart);
4
5 input  clk_5MHz;
6 input wire[4:0] notecode;
7
8 output wire[13:0] countStart;
9 blk_mem_gen_0 BRAMROM(
10     .clka(clk_5MHz),
11     .addra(notecode),
12     .douta(countStart),
13     .ena(1)
14 );
15
16 endmodule
```

2. screenshot:

