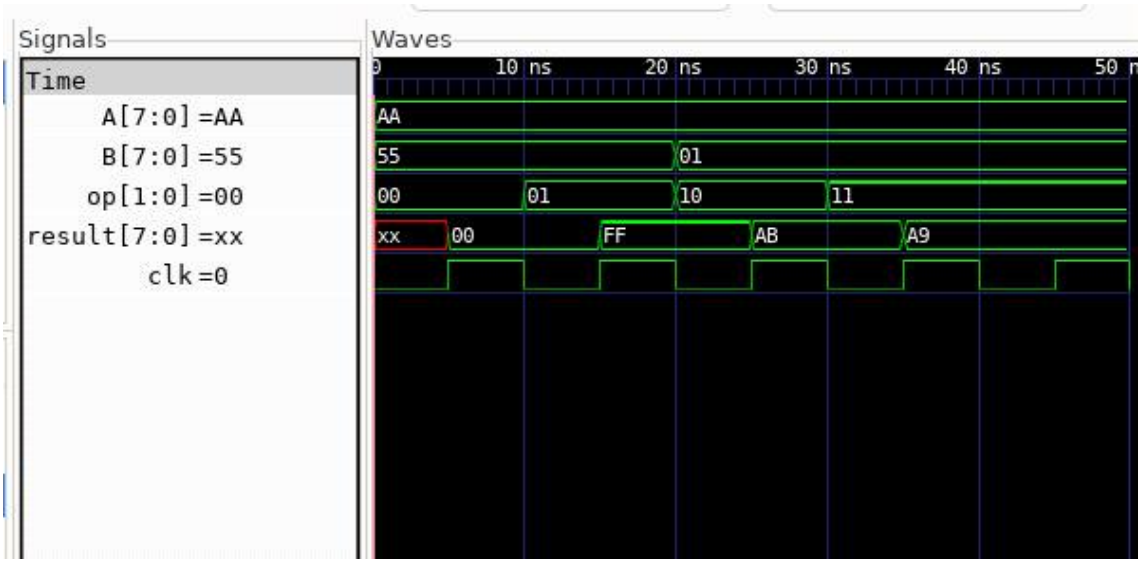
제작 과정

1. Simulation - gtkwave

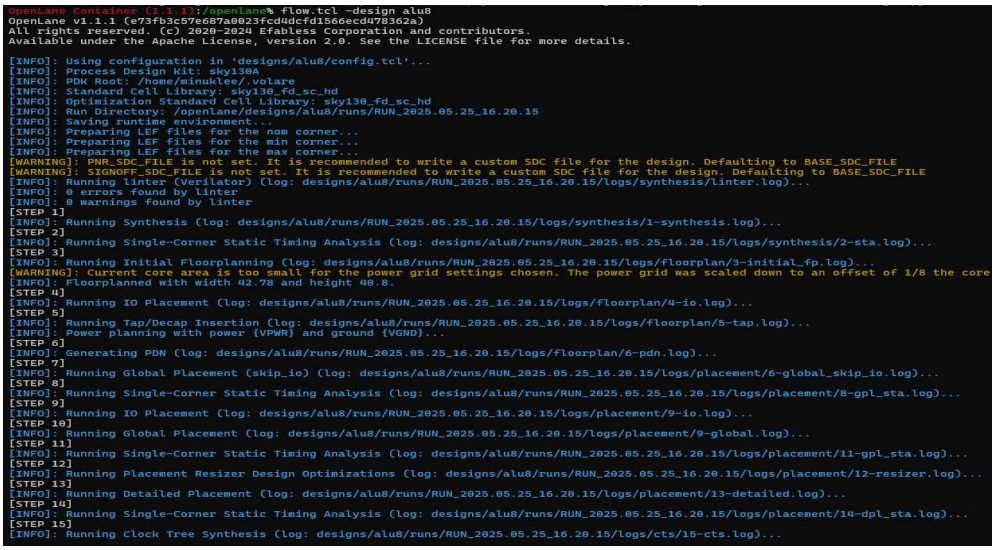


2. Source 파일 & config 파일 준비

```
minuklee@DESKTOP-3HU7P2P:~/OpenLane/designs/alu8/src$ ls
add8.v  alu8bit.v  alu8bit_tb.v  alu8bit_tb.vcd  alu8bit_tb.vvp
and8.v  or8.v  sub8.v
minuklee@DESKTOP-3HU7P2P:~/OpenLane/designs/alu8/src$
```

```
minuklee@DESKTOP-3HU7P2P:~/OpenLane/designs/alu8$ ls
config.tcl  runs  src
minuklee@DESKTOP-3HU7P2P:~/OpenLane/designs/alu8$
```

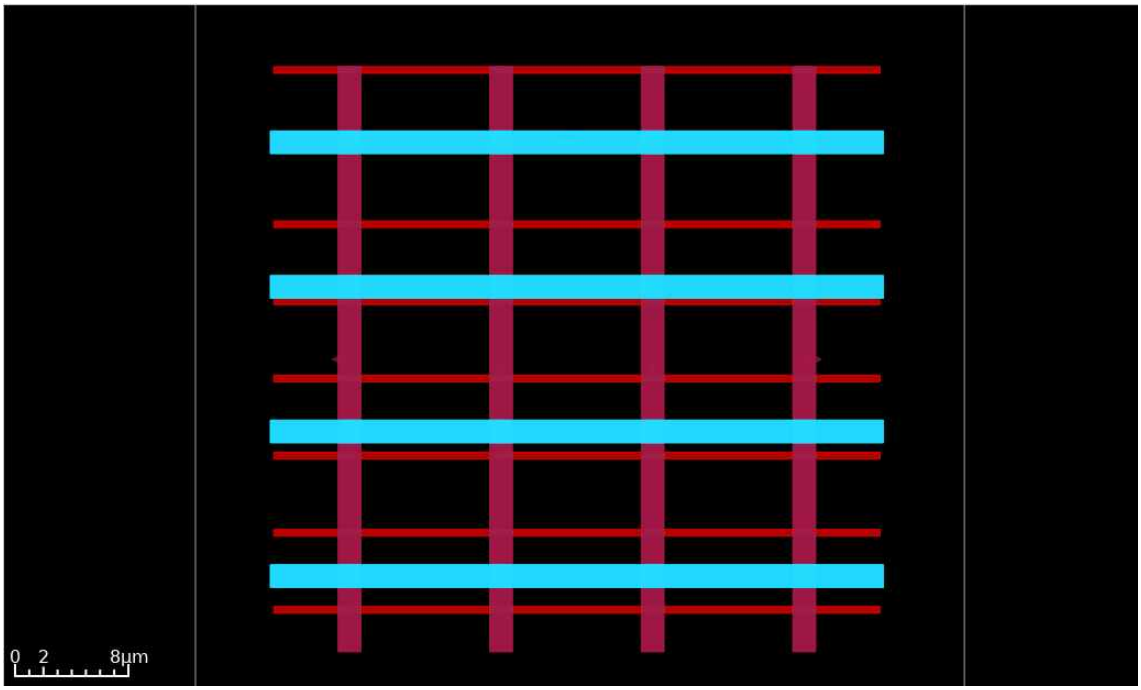
3. OpenLane (EDA TOOL 실행)



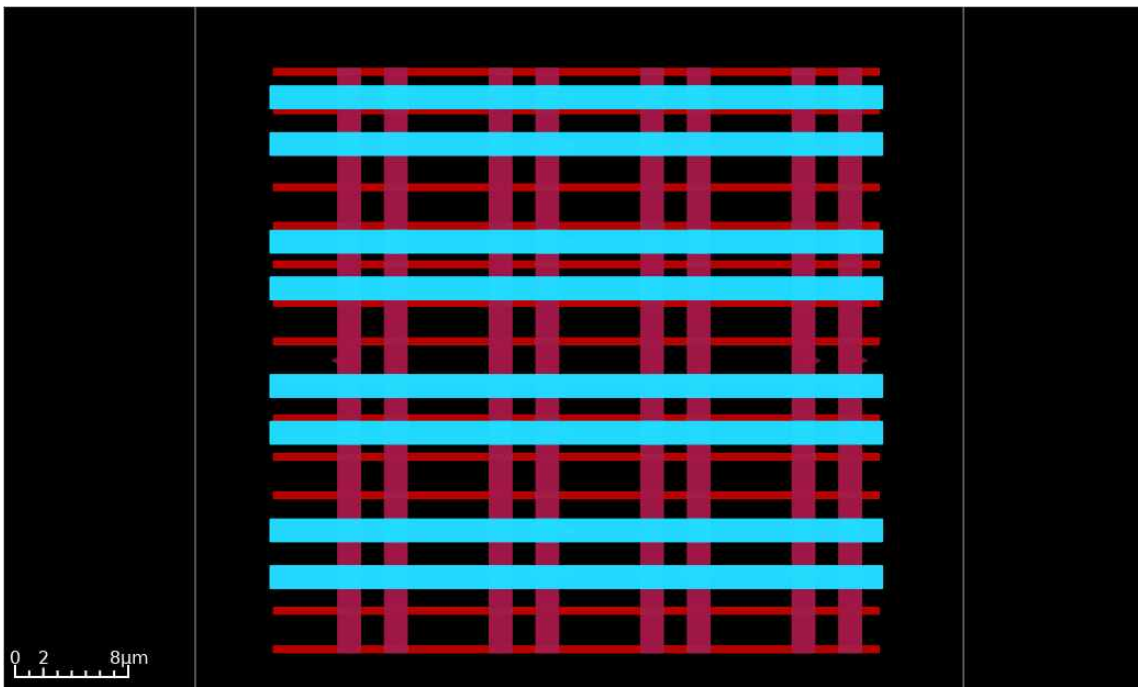
단계	내용
1 설정 및 환경 준비	- PDK: sky130A - 표준 셀 라이브러리: sky130_fd_sc_hd
2 합성 (Synthesis)	- Verilog 합성 및 넷리스트 생성 - Single-Corner STA 수행
3 **Floorplanning**	- 초기 플로어플랜: width=42.78um, height=40.8um - IO 배치, Tap/Decap 삽입 - PDN (Power Delivery Network) 생성
4 **배치 (Placement)**	- 글로벌 배치, 상세 배치 - Resizer Timing 최적화 - Single-Corner STA
5 **CTS (Clock Tree Synthesis)**	- 클럭 트리 생성 및 STA - Timing 최적화
6 **배선 (Routing)**	- 글로벌 및 상세 라우팅 - GDSII, LEF 생성 - Fill 삽입, STA 수행
7 **Signoff**	- Multi-Corner STA 및 SPEF 추출 - IR Drop 분석 - LVS, DRC, Antenna Rule Check - 최종 GDSII 및 보고서 생성

완성된 8bit ALU Layer 구조 해석

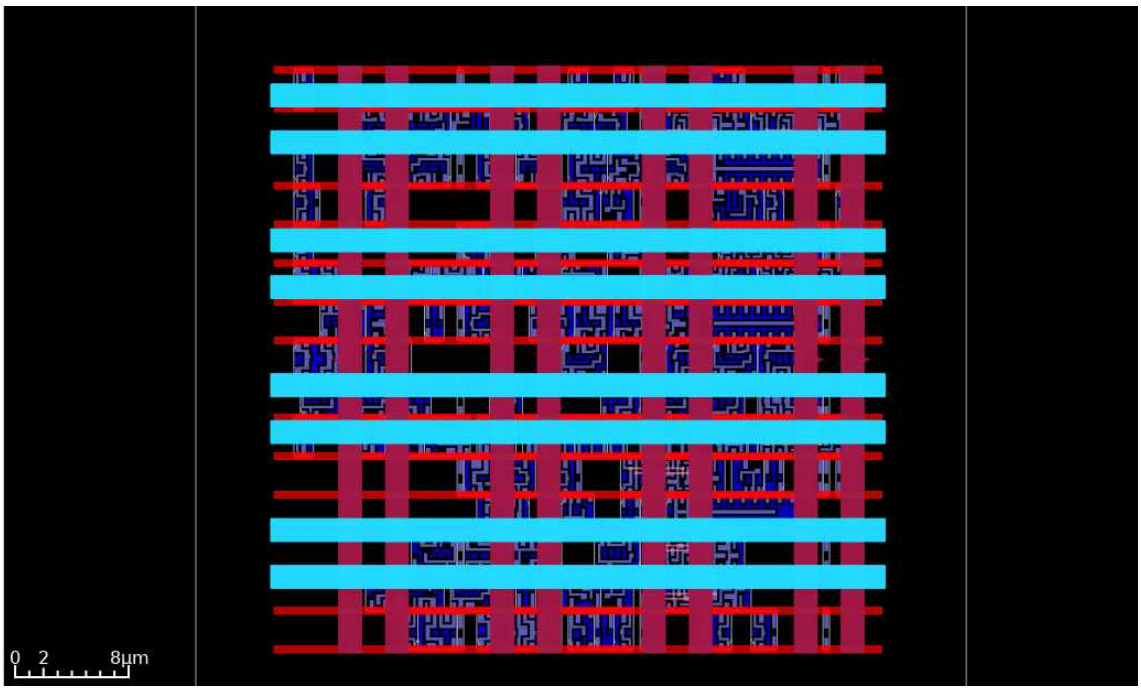
1. Power: 전원 레이어 (VDD/VSS) 배선 구성



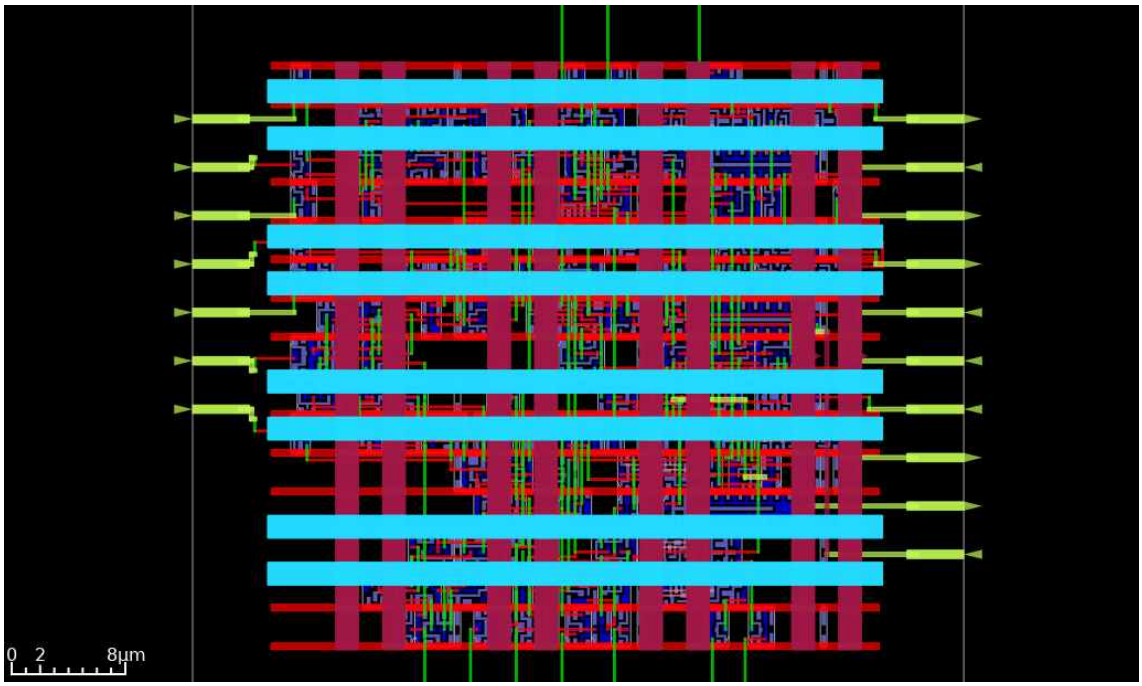
2. Ground: 접지 레이어 배선



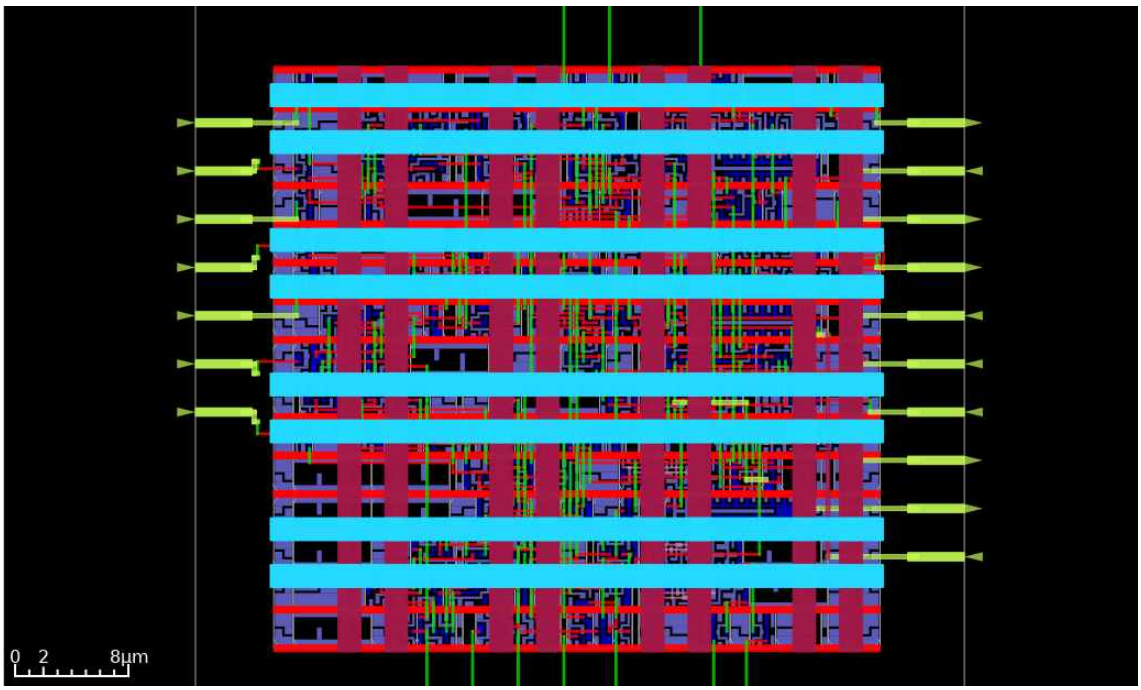
3. Standard cells + Welltap: 표준 셀 및 웰탭 배치



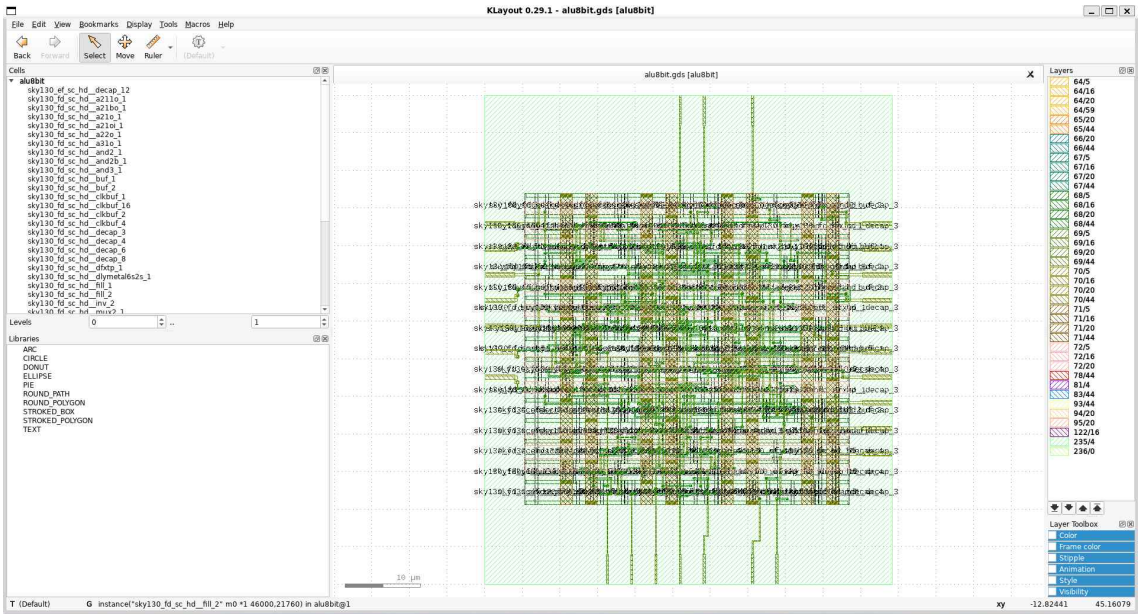
4. Signal + Clock: 신호 배선 및 클럭 트리



5. Fill cell: 더미 셀 삽입 및 밀도 보정



6. klayout (gds 파일) 확인



ALU 제조 및 성능 평가 보고서

1. 제조 적합성 평가 (DRC, LVS, Antenna Summary)

```
Design Name: alu8bit
Run Directory: /openlane/designs/alu8/runs/RUN_2025.05.11_10.03.10
----------------------------------------

Magic DRC Summary:
Source: /openlane/designs/alu8/runs/RUN_2025.05.11_10.03.10/reports/signoff/drc.rpt
Total Magic DRC violations is 0
----------------------------------------

LVS Summary:
Source: /openlane/designs/alu8/runs/RUN_2025.05.11_10.03.10/logs/signoff/41-alu8bit.lef.lvs.log
Number of nets: 136                     |Number of nets: 136
Design is LVS clean.
----------------------------------------

Antenna Summary:
Source: /openlane/designs/alu8/runs/RUN_2025.05.11_10.03.10/logs/signoff/44-arc.log
Pin violations: 0
Net violations: 0
```

DRC 위반 없음 (Magic DRC Clean)
LVS Clean (회로 연결 오류 없음)
Antenna 효과 문제 없음 (Pin/Net 위반 0)

2. synthesis 단계 후 셀 사용량 통계 보고서

```
OpenLane Container (1.1.1):/openlane/designs/alu8/runs/RUN_2025.05.11_10.03.10/reports/synthesis% cat 1-synthesis.AREA_0.stat.rpt

67. Printing statistics.

=== alu8bit ===

   Number of wires:                 83
   Number of wire bits:            105
   Number of public wires:          13
   Number of public wire bits:      35
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 86
     sky130_fd_sc_hd__a211o_2        1
     sky130_fd_sc_hd__a21bo_2        1
     sky130_fd_sc_hd__a21o_2        10
     sky130_fd_sc_hd__a21oi_2        1
     sky130_fd_sc_hd__a22o_2         1
     sky130_fd_sc_hd__a31o_2         6
     sky130_fd_sc_hd__and2_2         3
     sky130_fd_sc_hd__and2b_2        2
     sky130_fd_sc_hd__and3_2         1
     sky130_fd_sc_hd__buf_1          3
     sky130_fd_sc_hd__dfxtp_2        8
     sky130_fd_sc_hd__inv_2          1
     sky130_fd_sc_hd__mux2_2         2
     sky130_fd_sc_hd__nand2_2        5
     sky130_fd_sc_hd__nor2_2         3
     sky130_fd_sc_hd__o211a_2        3
     sky130_fd_sc_hd__o21a_2         7
     sky130_fd_sc_hd__o2bb2a_2       1
     sky130_fd_sc_hd__o311a_2        1
     sky130_fd_sc_hd__o31a_2         1
     sky130_fd_sc_hd__or2_2          4
     sky130_fd_sc_hd__or2b_2         2
     sky130_fd_sc_hd__or3_2          3
     sky130_fd_sc_hd__xnor2_2       11
     sky130_fd_sc_hd__xor2_2         5

   Chip area for module '\alu8bit': 933.395200
```

전체 셀 개수: 86
플립플롭 개수: 8
FF to Standard Cell Ratio(플립플롭 비율): 약 9.3%

3. 성능 (typical corner)

```
========================= Typical Corner ===================================

Startpoint: B[1] (input port clocked by clk)
Endpoint: _155_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Corner: Typical

Fanout     Cap     Slew   Delay    Time   Description
---------------------------------------------------------------------------
                          0.00    0.00   clock clk (rise edge)
                          0.00    0.00   clock network delay (propagated)
                          2.00    2.00 v input external delay
     1    0.00    0.01    0.00    2.00 v B[1] (in)
                                         B[1] (net)
                    0.01    0.00    2.00 v input10/A (sky130_fd_sc_hd__dlymetal6s2s_1)
     5    0.02    0.10    0.18    2.19 v input10/X (sky130_fd_sc_hd__dlymetal6s2s_1)
                                         net10 (net)
                    0.10    0.00    2.19 v _097_/B (sky130_fd_sc_hd__or3_1)
     4    0.01    0.11    0.44    2.63 v _097_/X (sky130_fd_sc_hd__or3_1)
                                         _028_ (net)
                    0.11    0.00    2.63 v _098_/C (sky130_fd_sc_hd__and3_1)
     2    0.01    0.05    0.23    2.86 v _098_/X (sky130_fd_sc_hd__and3_1)
                                         _029_ (net)
                    0.05    0.00    2.86 v _101_/B (sky130_fd_sc_hd__or3_1)
     2    0.01    0.08    0.38    3.23 v _101_/X (sky130_fd_sc_hd__or3_1)
                                         _032_ (net)
                    0.08    0.00    3.23 v _102_/B (sky130_fd_sc_hd__and2b_1)
     2    0.01    0.06    0.20    3.43 v _102_/X (sky130_fd_sc_hd__and2b_1)
                                         _033_ (net)
                    0.06    0.00    3.43 v _109_/A3 (sky130_fd_sc_hd__a31o_1)
     4    0.01    0.09    0.28    3.72 v _109_/X (sky130_fd_sc_hd__a31o_1)
                                         _039_ (net)
                    0.09    0.00    3.72 v _135_/A1 (sky130_fd_sc_hd__a31o_1)
     2    0.01    0.07    0.23    3.95 v _135_/X (sky130_fd_sc_hd__a31o_1)
                                         _063_ (net)
                    0.07    0.00    3.95 v _141_/A2 (sky130_fd_sc_hd__a21o_1)
     1    0.01    0.05    0.21    4.16 v _141_/X (sky130_fd_sc_hd__a21o_1)
                                         _068_ (net)
                    0.05    0.00    4.16 v _145_/A (sky130_fd_sc_hd__xnor2_1)
     1    0.00    0.04    0.12    4.28 v _145_/Y (sky130_fd_sc_hd__xnor2_1)
                                         _002_ (net)
                    0.04    0.00    4.28 v _146_/A1 (sky130_fd_sc_hd__mux2_1)
     1    0.00    0.05    0.29    4.57 v _146_/X (sky130_fd_sc_hd__mux2_1)
                                         _003_ (net)
                    0.05    0.00    4.57 v _147_/A (sky130_fd_sc_hd__clkbuf_1)
     1    0.00    0.03    0.10    4.67 v _147_/X (sky130_fd_sc_hd__clkbuf_1)
                                         mux_out[7] (net)
                    0.03    0.00    4.67 v _155_/D (sky130_fd_sc_hd__dfxtp_1)
                                    4.67   data arrival time

                         10.00   10.00   clock clk (rise edge)
                          0.00   10.00   clock source latency
     1    0.01    0.06    0.04   10.04 ^ clk (in)
                                         clk (net)
                    0.06    0.00   10.04 ^ clkbuf_0_clk/A (sky130_fd_sc_hd__clkbuf_16)
     2    0.02    0.04    0.12   10.16 ^ clkbuf_0_clk/X (sky130_fd_sc_hd__clkbuf_16)
                                         clknet_0_clk (net)
                    0.04    0.00   10.16 ^ clkbuf_1_1__f_clk/A (sky130_fd_sc_hd__clkbuf_16)
     4    0.01    0.03    0.11   10.27 ^ clkbuf_1_1__f_clk/X (sky130_fd_sc_hd__clkbuf_16)
                                         clknet_1_1__leaf_clk (net)
                    0.03    0.00   10.27 ^ _155_/CLK (sky130_fd_sc_hd__dfxtp_1)
                           -0.25   10.02   clock uncertainty
                            0.00   10.02   clock reconvergence pessimism
                           -0.11    9.92   library setup time
                                    9.92   data required time
---------------------------------------------------------------------------
                                    9.92   data required time
                                   -4.67   data arrival time
---------------------------------------------------------------------------
                                    5.25   slack (MET)
```

Performance = (1/(Clock Period - Slack))

Performance of design = 1/(10-5.25) = 2.10526 GHz

4. 소모 전력

```
======================= Typical Corner ===================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------------
Sequential             3.67e-05   8.39e-07   6.73e-11   3.75e-05  24.2%
Combinational          2.33e-05   2.99e-05   3.65e-10   5.32e-05  34.2%
Clock                  5.11e-05   1.35e-05   2.85e-10   6.46e-05  41.6%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------------
Total                  1.11e-04   4.43e-05   7.17e-10   1.55e-04 100.0%
                          71.5%      28.5%       0.0%
```

내부 전력 총합: 111 uW
스위칭 전력 총합: 44.3 uW
누설 전력 총합: 0.717 nW

총 전력 소비량: 155 uW

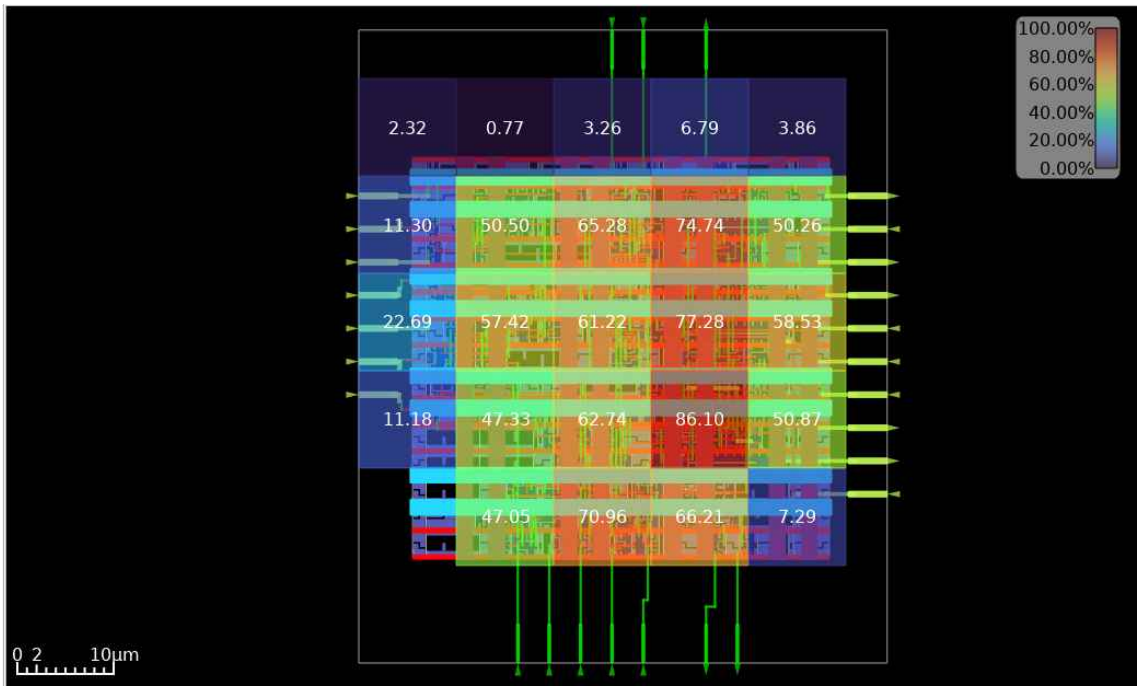
5. 크기

```
OpenLane Container (1.1.1):/openlane/designs/alu8/runs/RUN_2025.05.11_10.03.10/reports/floorplan% cat 3-initial_fp_core_area.rpt
5.52 10.88 48.3 51.68%
OpenLane Container (1.1.1):/openlane/designs/alu8/runs/RUN_2025.05.11_10.03.10/reports/floorplan% cat 3-initial_fp_die_area.rpt
0.0 0.0 54.245 64.965%
OpenLane Container (1.1.1):/openlane/designs/alu8/runs/RUN_2025.05.11_10.03.10/reports/floorplan%
```

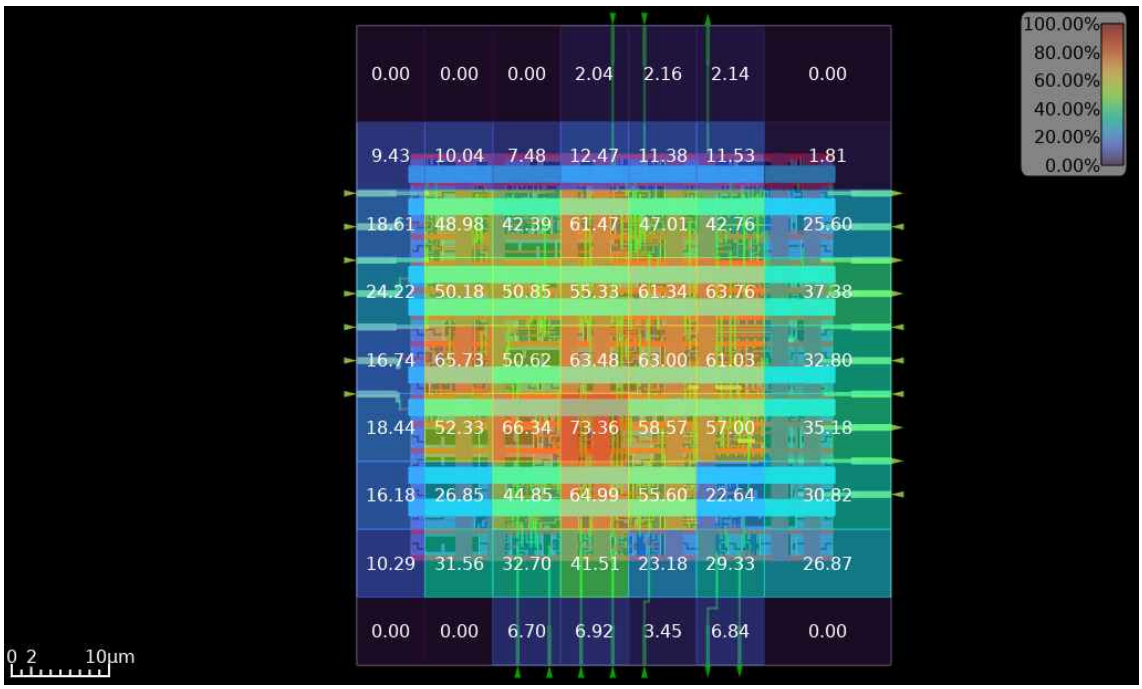
요약

항목	Core Area	Die Area
크기 (Width x Height)	5.52 x 10.88 µm	(좌표 0,0, 크기는 별도)
면적	48.3 µm²	54.245 µm²
배치 밀도	51.68%	64.965%

6. placement density (배치 밀도)



7. estimated congestion (추정 혼잡도)



8. Routing congestion (배치 혼잡도)