Sub-10 nm imprint lithography and applications

Stephen Y. Chou,[a] Peter R. Krauss, Wei Zhang, Lingjie Guo, and Lei Zhuang
NanoStructure Laboratory, Department of Electrical Engineering, University of Minnesota, Minneapolis, Minnesota 55455

New developments, further details, and applications of imprint lithography are presented. Arrays of 10 nm diameter and 40 nm period holes were imprinted not only in polymethylmethacrylate (PMMA) on silicon, but also in PMMA on gold substrates. The smallest hole diameter imprinted in PMMA is 6 nm. All the PMMA patterns were transferred to a metal using a liftoff. In addition, PMMA mesa's of a size from 45 nm to 50 μm were obtained in a single imprint. Moreover, imprint lithography was used to fabricate the silicon quantum dot, wire, and ring transistors, which showed the same behavior as those fabricated using electron (e)-beam lithography. Finally, imprint lithography was used to fabricate nanocompact disks with 10 nm features and 400 Gbits/in.^{2} data density—near three orders of magnitude higher than current critical dimensions (CDs). A silicon scanning probe was used to read back the data successfully. The study of wear indicates that due to the ultrasmall force in tapping mode, both the nano-CD and the scanning probe will not show noticeable wear after a large number of scans. © *1997 American Vacuum Society.* [S0734-211X(97)19706-2]

I. INTRODUCTION

Nanostructure research is a fast growing field. Originated from microelectronics, it has spread into many other disciplines, such as biology, chemistry, medicine, and information storage, to name a few. To accelerate nanostructure research and commercialize its results, we must have a high-throughput and low-cost nanopatterning technology, particularly a nanolithography which allows complete freedom in designing the size, shape, and spacing of a pattern. Currently, a number of nanolithography techniques, such as electron-beam lithography, x-ray lithography, and scanning probe lithography, are under development,[1–6] but they are not yet able to provide the needed high throughput and the low cost.

Nanoimprint lithography (NIL), proposed in 1995, is based on a principle fundamentally different from that for conventional lithographies.[7] Nanoimprint lithography creates a resist relief pattern by deforming the resist physical shape with embossing, rather than by modifying the resist chemical structure with radiation or self-assembly. The difference in principles makes nanoimprint lithography capable of producing sub-10 nm features over a large area with a high throughput and low cost. Previously, we have achieved 25 nm features size and 100 nm pitch and excellent uniformity over an area of 16 mm by 18 mm.[8] In this article, we present new development and further details of nanoimprint lithography which has lead to sub-10 nm features and 40 nm pitch on silicon as well as on gold substrates. We will report applications of NIL in fabricating silicon nanodevices and nano-compact disks with 400 Gbit/in.^{2} density.

II. IMPRINT LITHOGRAPHY PRINCIPLE AND PROCESS

Imprint lithography has two steps: imprint and pattern transfer (Fig. 1). In the imprint, a mold with nanostructures on its surface is pressed into a thin resist cast on a substrate. The resist, a thermal plastic, is deformed readily by the mold when heated above its glass transition temperature (due to a low viscosity). After the resist is cooled below its glass transition temperature, the mold is removed. In the pattern transfer, an anisotropic etching process, such as reactive ion etching (RIE), is used to remove the residual resist in the compressed area, transferring the thickness contrast pattern created in the imprint into the entire resist.

Since imprint lithography is not based on modification of resist chemical structure by radiation, its resolution is immune to many factors that limit the resolution of conventional lithography, such as wave diffraction, scattering and interference in a resist, backscattering from a substrate, and the chemistry of resist and developer.
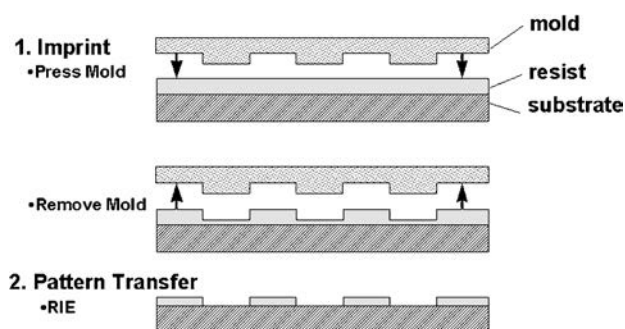

FIG. 1. Schematic of nanoimprint lithography process: (a) imprinting using a mold to create a thickness contrast in a resist, and (b) pattern transfer using anisotropic etching to remove residue resist in the compressed areas.

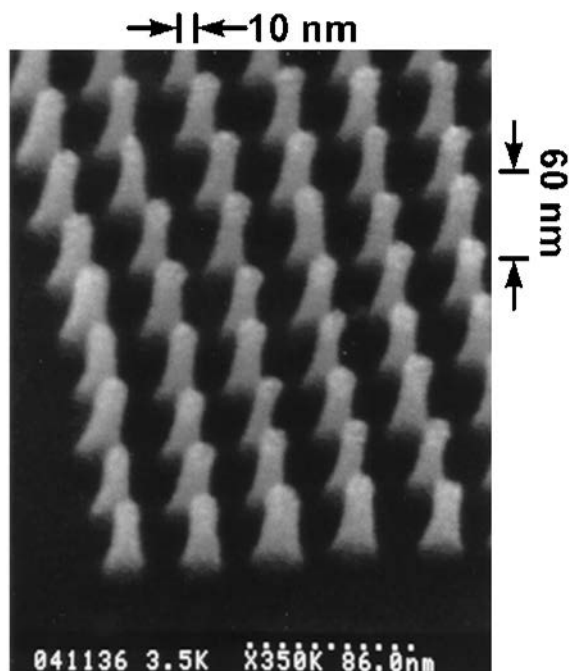[a]Present address: Princeton University, Princeton, New Jersey; Electronic mail: chou@ee.princeton.edu

FIG. 2. SEM micrograph of a SiO$_2$ mold with 10 nm minimum diameter pillars with a 40 nm period which are 60 nm tall, after being used 12 times.

FIG. 4. SEM micrograph of a top view of 10 nm minimum diameter metal dots with a period of 40 nm, formed by imprinting into PMMA and a liftoff process.

III. PMMA HOLES AND METAL DOTS WITH SUB-10 nm DIAMETER AND 40 nm PITCH

To imprint features smaller than the previous work, we fabricated SiO$_2$ molds of pillar arrays with 10 nm minimum diameter, 40 nm pitch, and 60 nm height using high-resolution electron beam lithography, liftoff of chrome, and CHF$_3$ RIE. Figure 2 shows that the pillars have straight side-walls at the upper portion, but become wider in diameter near the base. This profile is a result of the RIE process.

Using this mold, 10 nm diameter and 40 nm pitch holes were imprinted in 78 nm thick 100 K molecular weight polymethylmethacrylate (PMMA) cast on the silicon substrate (Fig. 3). The imprint temperature was 175 °C, which is above the glass-transition temperature of PMMA, 105 °C. The pressure is 4.4 MPa. The holes imprinted in PMMA
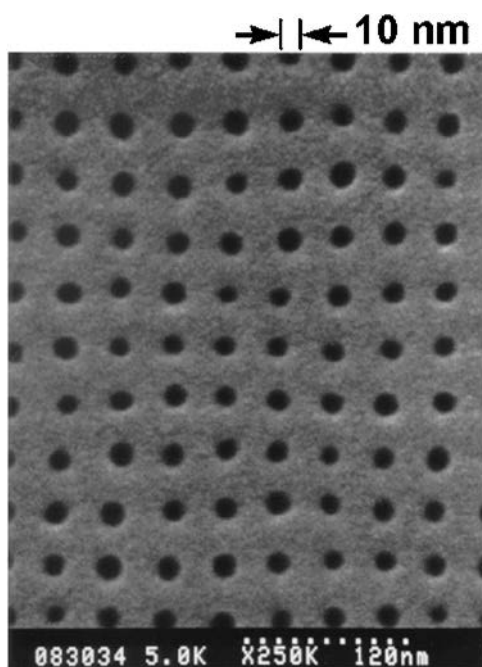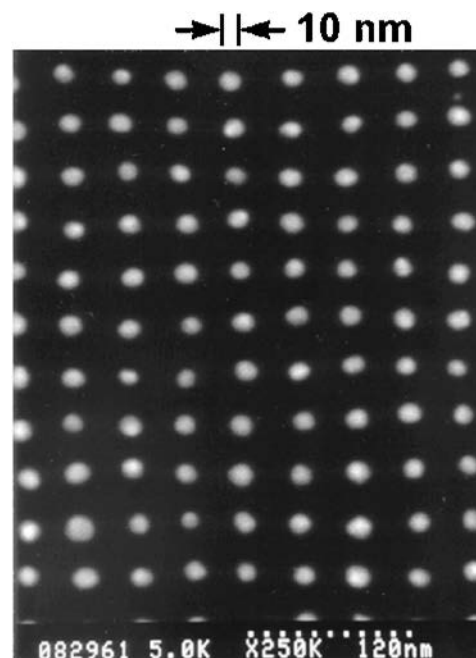

FIG. 3. SEM micrograph of a top view of 60 nm deep holes imprinted into PMMA which have a 10 nm minimum diameter and a period of 40 nm.
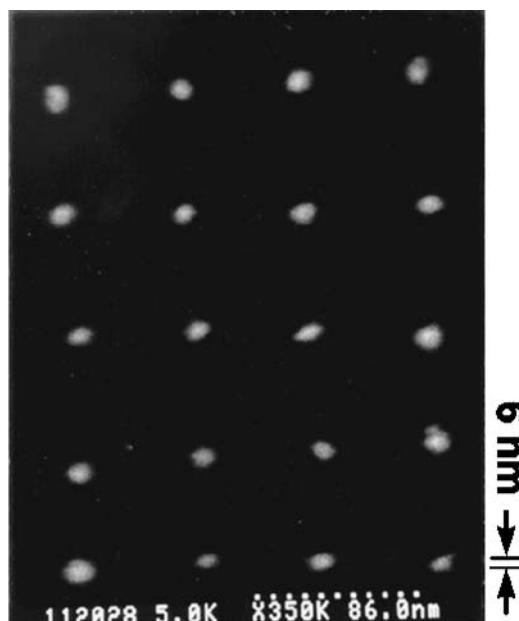

FIG. 5. SEM micrograph of a top view of 6 nm minimum diameter metal dots formed by imprinting into PMMA and a liftoff process.
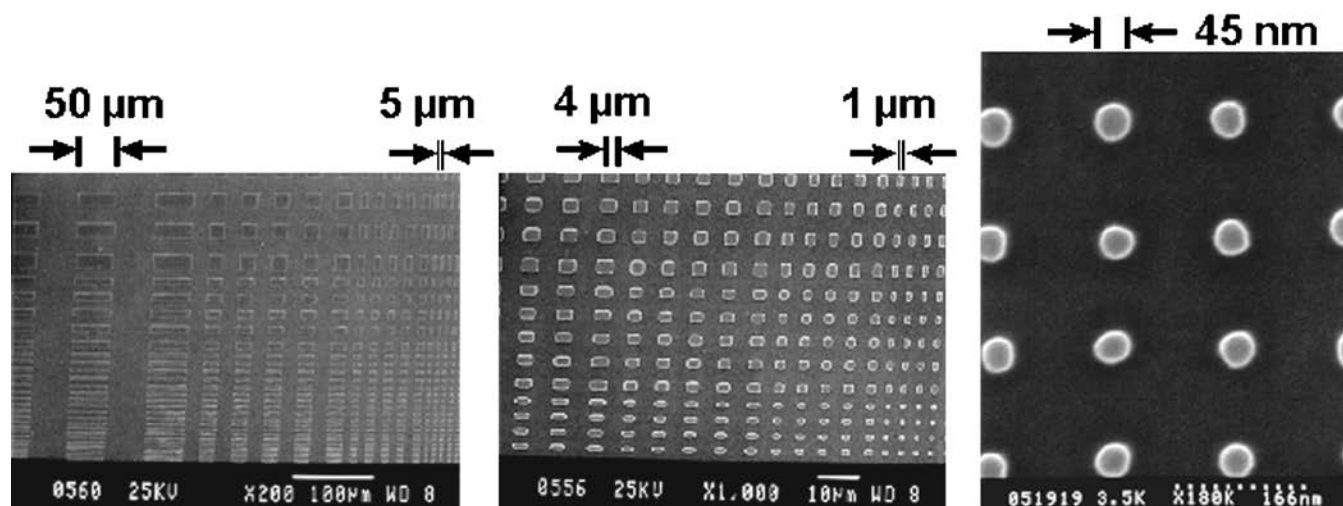
FIG. 6. SEM micrograph of a top view of imprinted PMMA mesas ranging from 45 nm up to 50 μm.

seem to conform with the mold. The dark center of the hole corresponds to the imprint of the narrow shaft of the pillars on the mold, while the few nanometers wide grayscale variation at the perimeter of the holes is due to the imprint of the sloped pillar base. We found that the nanoscale pillars on the SiO$_2$ mold were durable in the imprint and were still intact after imprinting 12 times (Fig. 2).

To check oxygen RIE pattern transfer and the change in lateral pattern dimension during the transfer, the PMMA after the pattern transfer was used as a template for a liftoff of Ti/Au (3 nm/10 nm thick) (Fig. 4). The minimum diameter of dots is 10 nm, consistent with the size of the narrow shaft of the pillars on the mold, indicating that the oxygen RIE

process is highly anisotropic and does not noticeably change the lateral dimension of the imprinted PMMA.

To make the mold with a size smaller than 10 nm, we used HF to reduce the pillar diameter. The metal dots of 6 nm diameter were fabricated using NIL and liftoff (Fig. 5). However, we found that the mold of SiO$_2$ pillars with sub-10 nm feature and aspect ratio greater than 6 is mechanically unstable in the present imprint process. A feature size smaller than 6 nm should be achieved using imprint lithography, but improved mold, resist, and processing conditions are required. Other details of sub-10 nm NIL have been published elsewhere.[9]

FIG. 7. SEM micrograph of perspective view of 45 nm diameter imprinted PMMA pillars.

IV. PMMA MESAS OF 45 nm TO 50 μm IMPRINTED SIMULTANEOUSLY

From the rheology point of view, the resist flow in imprinting resist mesas is different from that in imprinting holes, and the flow should also depend on the feature size. To investigate the resist flow in imprinting the different pattern size in resist, the molds with the square holes of size from 20 nm to 50 μm were fabricated. We found that mesas with a size of 45 nm or larger can be imprinted in PMMA successfully in a single imprint. Figure 6 shows the top view of the PMMA mesas with a size from 45 nm to 5 μm imprinted simultaneously. Figure 7 shows the perspective view of the imprinted 45 nm diameter PMMA mesas. For small PMMA pillars, they melted slightly during SEM inspection.

For the mesas of a size of 30 nm or smaller, some of them were found to tear off from the resist during mold separation, leaving a shallow hole on the substrate at the location of the mesa base. The tearoff problem gets worse as the mesa size becomes smaller. The tearoff can be related to the sidewall shape of a high aspect ratio hole in the mold (e.g., undercut), or the release mechanism in small holes. Further investigations and improvements are in progress.
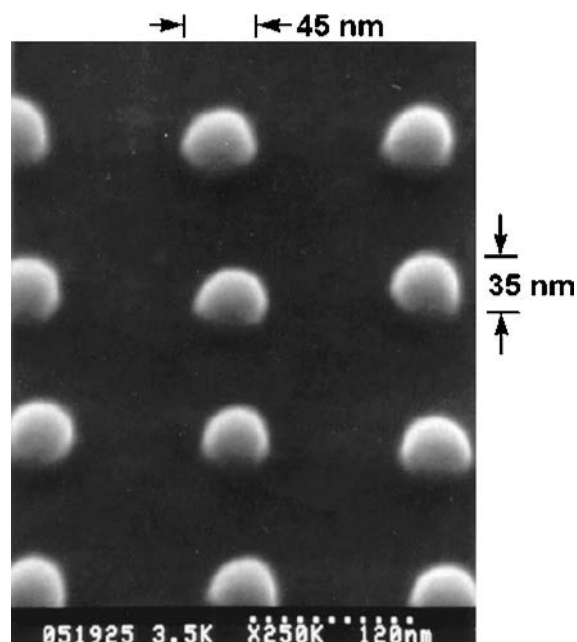
V. 10 nm DIAMETER AND 40 nm PITCH HOLES ON HIGH-ATOMIC NUMBER SUBSTRATES

In many applications, a high-resolution lithography on high atomic number substrates is very desirable. However, for radiation-based lithographies, severe backscattering from a high atomic number substrate makes their resolution orders of magnitude worse than that on a low atomic number substrate. NIL, on the other hand, does not use any radiation, and hence offers a high resolution that is independent of the underlying substrate atomic number. In NIL, high resolution and high pitch density patterns are first fabricated on a mold of a low atomic number material (such as Si and SiO_2) using a conventional high-resolution lithography tool, such as electron-beam lithography. Then the pattern would be duplicated faithfully on a high atomic number substrate.

To test the resolution of NIL on a high atomic number substrate, a substrate with 300 nm thick gold deposited on a silicon wafer was prepared. Then, 78 nm thick 100 K molecular weight PMMA was spun onto the substrate. The PMMA was imprinted with the mold and the conditions discussed in Sec. III. Figure 8(a) shows that an array of 60 nm deep holes with 10 nm minimum diameter and 40 nm period has been imprinted into 100 K PMMA on a gold substrate using the mold shown in Fig. 2. The faint grayscale variations in the background are caused by electron backscattering from different underlying gold grains. An array of uniform 20 nm diameter and 50 nm period holes is shown in Fig. 8(b). The imprinted holes have the same diameter as the mold features. This indicates that the NIL resolution is, as expected, not affected by the underlying high atomic number substrate.

After imprinting and pattern transfer, 13 nm thick nickel was deposited on the entire wafer surface for a liftoff. Nickel was chosen for a better SEM contrast, for its atomic number is significantly different from that of gold. Although 10 nm diameter nickel dots were lifted off, they are extremely hard to photograph in our scanning electron microscope. But the nickel dots with 20 nm diameter and 50 nm period and the nickel gratings with 20 nm linewidth and 80 nm period can be clearly seen with our SEM (Figs. 9 and 10, respectively). The gold grains of different crystalline orientations have a drastically different secondary electron emission rate, making them distinctly visible in SEM. Despite a large variation in the secondary electron emission rate from one gold grain to another, both the dot diameter and the linewidth are uniform over the entire sample. This further demonstrated that the resolution of NIL is independent of the substrate atomic number.

VI. APPLICATIONS OF NANOIMPRINT LITHOGRAPHY

A. Fabrication of Si quantum dot, wire, and ring transistors

To explore the feasibility of nanoimprint lithography in nanodevice fabrication, we have used NIL to fabricate quantum dot, wire, and ring transistors on the silicon-on-insulator
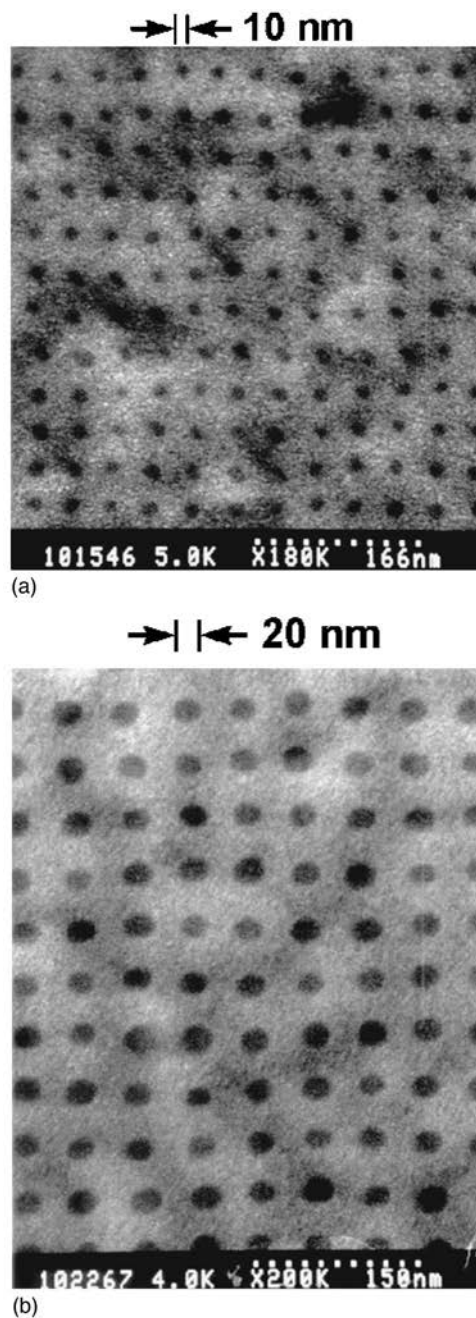

FIG. 8. SEM micrograph of holes imprinted into PMMA on a gold substrate (a) with 10 nm minimum diameter and 40 nm period and (b) with 20 nm minimum diameter and 50 nm period. Grains of the gold substrate are visible beneath the PMMA.

(SOI) substrates and have examined the effects of NIL on the device performance (e.g., the high pressure effects).[10] The transistors were fabricated using a three level lithography process. In the first level, the transistors' active areas that contain nanoscale channel features and the alignment marks for the subsequent photolithography steps were patterned using nanoimprint lithography (see Fig. 11). In the second and the third level, the gates and the final metal contacts were patterned, respectively, using conventional photolithography.

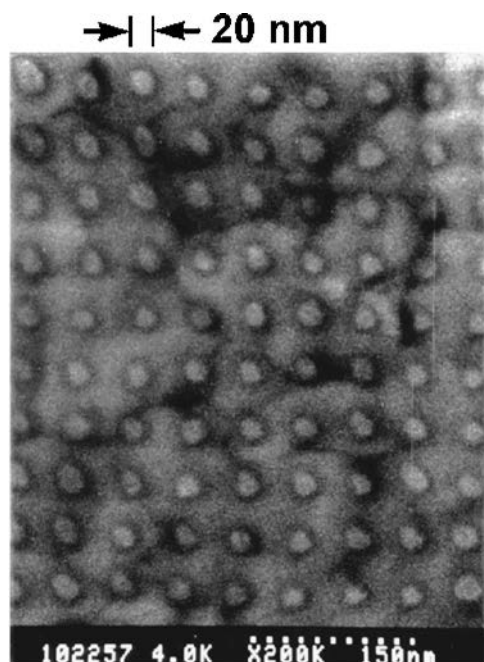In fabricating the mold, the nanoscale channel features in

FIG. 9. SEM micrograph of nickel dots with 20 nm diameter and 50 nm period on a gold substrate fabricated by NIL and liftoff. Grains of the gold substrate are visible beneath the PMMA.

the active area were defined by electron-beam lithography and Cr liftoff; while the large 15 μm×12 μm mesa for the source and drain region of the transistors, and alignment marks were defined by photolithography and Cr liftoff. These patterns were transferred into the mold using CHF$_3$ RIE, and the intrusion of the mold features was 110 nm tall.
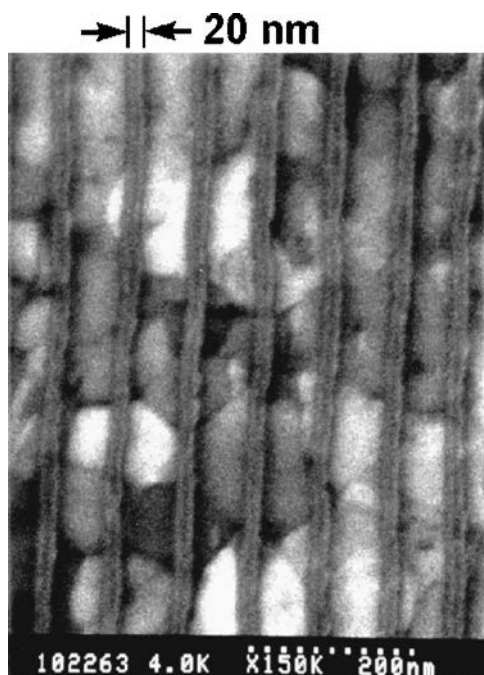

FIG. 10. SEM micrograph of nickel grating with 20 nm linewidth and 80 nm period on a gold substrate fabricated by NIL and liftoff. Grains of the gold substrate are visible beneath the PMMA.
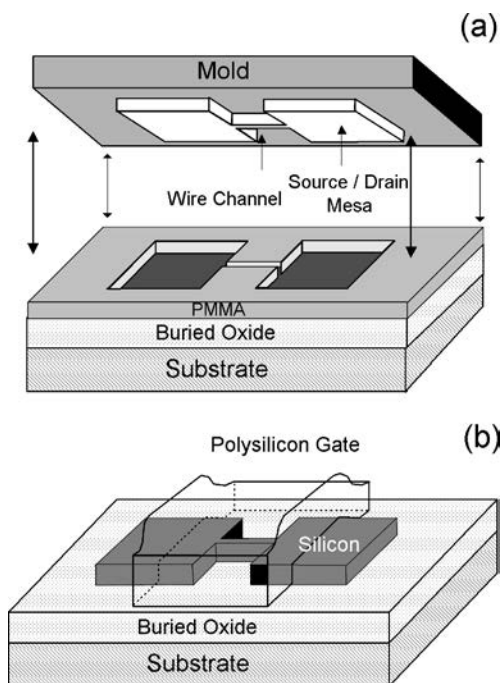
FIG. 11. (a) Imprint lithography based on compression molding to create thickness contrast pattern in PMMA resist carried on the wafer substrate. (For clarity, the feature sizes are not drawn to scale.) (b) Schematic of the wire channel transistor defined by nanoimprint lithography in SOI.

The transistors were fabricated on the top (100) *p*-type silicon layer of a SOI wafer of 3×10^{15} cm^{-3} boron concentration and 70 nm thickness. After growing a 30 nm sacrificial oxide layer to protect the silicon during NIL, a 200 nm thick PMMA layer was spun. In imprinting, a pressure of 4.5 MPa and a temperature of 175 °C were used. The imprint has an excellent uniformity over a 2 cm by 2 cm area. The patterned PMMA was used as a template for a 20 nm Cr liftoff. The Cr pattern was then used as a RIE mask for transferring the pattern into SOI, by first using fluorine-based RIE to etch away the sacrificial oxide and then chlorine-based RIE to etch the pattern into the 70 nm thick silicon layer. Figure 12 shows a 100 nm wire channel MOSFET, a 250 nm quantum dot and a 100 nm wide ring structure in the silicon layer after the Cr mask and the oxide layer were removed. These features have the same shape and size as those in the mold, indicating that the nanoimprint has a high fidelity during pattern transfer. The final device feature sizes were reduced using a subsequent gate oxide growth (a 30 nm gate oxide was grown at 1000 °C, which also annealed the RIE damage). Next, polycrystalline silicon was deposited and photolithography was used to define the polysilicon gate that covers the entire channel region of the transistors. Then an ion implantation was used to form the self-aligned source and drain, and to dope the gate. A second photolithography defined the final metallization contacts, completing the process. The device fabrication is similar to what we have reported previously in the fabrication of the silicon quantum dot transistors using electron-beam lithography.[11]

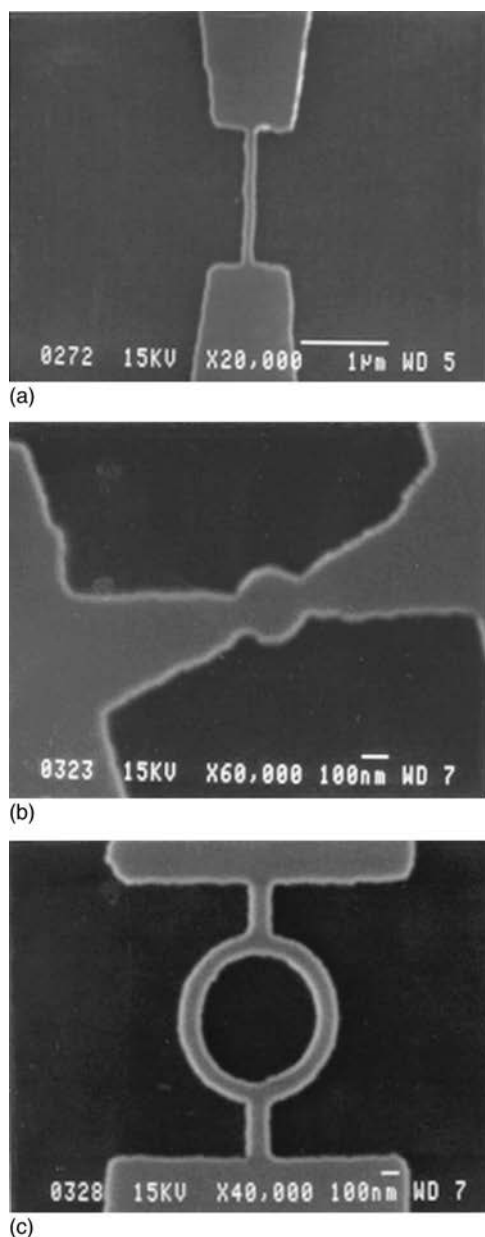The room temperature electric characteristics (i.e., the

(a)

(b)

(c)

FIG. 12. Nanoscale features in top silicon layer of SOI defined by nanoimprint lithography, liftoff and RIE: (a) wire channel, (b) quantum dot channel, and (c) ring channel.

drain current versus the drain bias at different gate voltages) of the 100 nm wire channel MOSFET with 2 μm channel length is shown in Fig. 13. The device is well behaved: a threshold voltage of 0.2 V and a subthreshold slope of 90 mV/dec. The quantum dot devices, measured at 0.5 K, showed strong conductance oscillations as a function of the gate voltage. These oscillations are due to the Coulomb blockade effect of electrons in the confined silicon quantum dot.[12] When compared with the devices fabricated by conventional electron-beam lithography, we did not observe any noticeable difference in the device behavior.
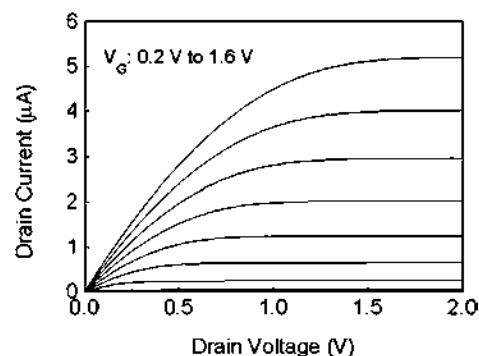
FIG. 13. $I-V$ characteristics of the wire channel MOSFET at room temperature.

B. Nanocompact disks with 400 Gbits/in.^{2} storage density

Read-only memory (ROM) disks, such as compact disks (CDs), are the most popular low-cost information storage media. Currently, they are made by injection molding, have a data storage density of 0.68 Gbits/in.^{2}, and are read by a laser beam. To meet the future demand for ultrahigh density information storage, ROM disks of topographic bits with a 45 Gbit/in.^{2} storage density and 50 minimum feature size have been recently fabricated using photopolymerization (2P) duplication process and read using a scanning proximal probe.[13] To further explore ultrahigh density ROM disk technology, we have fabricated nanocompact disks (nano-CDs) with 400 Gbits/in.^{2} storage density and 10 nm minimum features sizes using nanoimprint lithography, and have studied reading and wearing of nano-CDs using scanning proximal probe techniques.[14] This storage density is nearly three orders of magnitude higher than commercial CDs made by injection molding.

The nanoscale topographic bits on a nano-CD can be made with a variety of materials, such as polymer, amorphous materials, crystalline semiconductors, or metals. Here, we focus our discussion on the nano-CDs consisting of metal bits. The first step in fabricating nano-CDs is to make a SiO$_2$ master mold. The SiO$_2$ is selected because it has a low atomic number for less backscattering and proximity effects during electron-beam lithography. The details of the mold fabrication have been discussed in Sec. III. Once made, the master mold was used to fabricate ''daughter'' molds, that can be the same material as the master or different materials (such as high atomic number materials). Nano-CD daughter molds fabricated using NIL have been found to have the same feature sizes as the master molds.[14]

In nano-CD's fabrication, NIL creates a PMMA pattern on a substrate. One advantage of NIL over the 2P process is that the substrates do not need to be UV transparent. The PMMA pattern, although can be used for readback itself, was transferred to a Ti/Au (5/10 nm thick) pattern using liftoff, since the metal is much more durable in readback. Figure 14 shows a section of a nano-CD with a 40 nm track width and 13 nm minimum feature size. This track width corresponds to a storage density of 400 Gbits/in.^{2}. The nano-CD was fab-
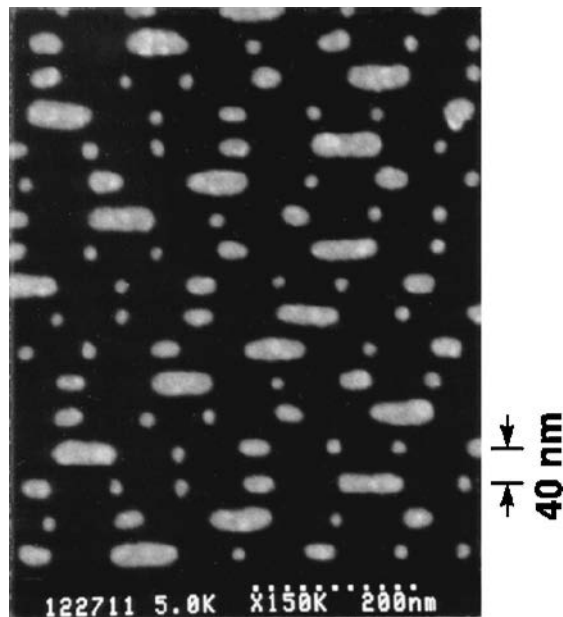
FIG. 14. SEM micrograph of a 40 nm track width nano-CD fabricated by nanoimprint lithography and liftoff.

ricated using a daughter mold. Another example of a nano-CD is shown in Fig. 4 consisting of 10 nm diameter dots with 40 nm pitch and 400 Gbits/in.[2] density. Gold was chosen due to its high contrast on the silicon substrate in the SEM. Other materials may also be used which offer better wear properties than gold, as discussed later.

Since the bits on a nano-CD are too small to be read by a laser beam of visible wavelength, an atomic force microscope (AFM) with commercial silicon scanning probes is used for readback. Both tapping mode and contact mode

Initial TMAFM image of 50 nm period Nano-CD.
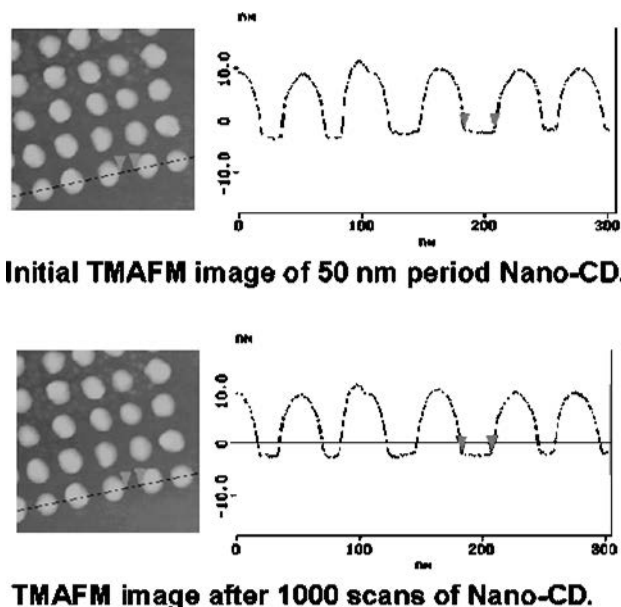

TMAFM image after 1000 scans of Nano-CD.

FIG. 15. Initial tapping mode AFM image (a) and 1000th image (b) of a nano-CD consisting of 50 nm period gold dots fabricated using nanoimprint lithography and liftoff.

were tested. Figure 15(a) shows a tapping mode AFM image and a cross section profile of a nano-CD consisting of a uniform array of gold dots with a 50 nm period. Tapping mode AFM images show that the gold dots are wider than that in the SEM image, which is attributed to the scanning probe's tip size effect. The cross section profile indicates that the probe tip can resolve individual nanoscale dots and the flat silicon substrate between the 50 nm period dots. However, the probe tip does not always reach the substrate between the dots with the same diameter but a 40 nm period, making the height difference measured by AFM smaller than that for 50 nm period dots. This problem can be avoided by using a sharper probe.

The wear of nano-CDs and the scanning probe was investigated. Using tapping mode (a force range of 0.1–1.0 nN) to scan the same location of the nano-CD 1000 times [Fig. 15(b)], we did not observe any discernible change in AFM image. This indicates that neither the silicon proximal probe nor the nano-CD exhibited significant wear during the tapping mode AFM imaging.

However, in a contact mode AFM, which applies a force of tens of nano-Newtons between the tip and the disk wear can be significant. To accelerate the wear test, a larger force was applied in contact mode AFM. The sample was a chrome grating. Chrome has a Mohs hardness of 9 making it more resistant to the wear than gold, which has a hardness of 2.5. We found that the AFM tip force can be increased to 15 μN without creating immediate noticeable change in the AFM image. However, at 19 μN force, the silicon tip will remove the chrome grating line. This test indicates that in the tapping mode where the force is over four orders of magnitude smaller than the damage threshold, both the nano-CDs and the silicon tip have a lifetime at least four orders of magnitude larger than that at the damage threshold. The details of the wear study will be published elsewhere.[14]

VII. CURRENT LIMITATIONS AND FUTURE DEVELOPMENTS

The results achieved by nanoimprint lithography are very promising. Yet, the true potential of nanoimprint lithography has not been fully studied, and substantial further developments are needed to make nanoimprint lithography a manufacturing technology. Here, we will briefly discuss the current limitations and future development.

Presently, 10 nm features and 40 nm periods are achieved in PMMA over an area of about one square inch. But the global fidelity of the patterns, multilevel alignment, nanorheology (effects of pattern shapes and densities), large imprint areas (e.g., 8 in. diameter wafers), and imprint speed have not been tested. Conceivably, some of the issues will be very challenging. We think the future development will be primarily in the development of imprint machines, molds, resists, and nanorheology. Finally, a key application of NIL should be identified to become the driver of NIL development.

VIII. CONCLUSION

We have further developed nanoimprint lithography to achieve 10 nm diameter and 40 period holes in PMMA on either silicon or gold substrates, and 6 nm diameter and 65 nm period holes in PMMA on silicon substrate. PMMA mesas of a size from 45 nm to 50 μm were also achieved in a single imprint. Nanoimprint lithography was used together with optical lithography to fabricate silicon quantum dot, wire, and ring transistors, which showed the same behavior as those fabricated using conventional electron-beam lithography. Finally, nanoimprint lithography was used to fabricate nanocompact disks with 10 nm features and 400 Gbits/in.^{2} data density—near three orders of magnitude higher than current CDs. A silicon scanning probe was used to readback the data successfully. The wear study indicates that due to the ultrasmall force in tapping mode, both the nano-CD and the scanning probe will not show noticeable wear after a large number of scans. We think the future development of NIL will be primarily in the development of imprint machines, molds, resists, and nanorheology. Finally, a key application of NIL should be identified to become the driver of NIL development.

ACKNOWLEDGMENT

[1] A. N. Broers, J. M. Harper, and W. W. Molzen, Appl. Phys. Lett. **33**, 392 (1978).

[2] D. Flanders, Appl. Phys. Lett. **36**, 93 (1980).

[3] K. Early, M. L. Schattenburg, and H. I. Smith, Microelectron. Eng. **11**, 317 (1990).

[4] M. A. McCord and R. F. P. Pease, J. Vac. Sci. Technol. B **4**, 86 (1986).

[5] J. W. Lyding, T. C. Shen, J. S. Hubacek, J. R. Tucker, and G. C. Abelin, Appl. Phys. Lett. **64**, 2010 (1994).

[6] T. R. Albrecht *et al.*, J. Appl. Phys. **64**, 1178 (1988).

[7] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, Appl. Phys. Lett. **67**, 3114 (1995); Science **272**, 85 (1996).

[8] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, J. Vac. Sci. Technol. B **14**, 4129 (1997).

[9] S. Y. Chou and P. R. Krauss, Microelectron. Eng. **35**, 237 (1997).

[10] L. J. Guo, P. R. Krauss, and S. Y. Chou, Appl. Phys. Lett. **71**, 1881 (1997).

[11] E. Leobandung, L. J. Guo, and S. Y. Chou, J. Vac. Sci. Technol. B **13**, 2865 (1995).

[12] See, for example, *Single Charge Tunneling: Coulomb Blockade Phenomena in Nanostructures*, edited by H. Grabet and M. H. Devoret (Plenum, New York, 1992).

[13] B. D. Terris, H. J. Mamin, and D. Rugar, 1996 EIPBN, Atlanta, GA, 1996; B. D. Terris, H. J. Mamin, M. E. Best, J. A. Logan, D. Rugar, and S. A. Rishton, Appl. Phys. Lett. **69**, 4262 (1996).

[14] P. R. Krauss and S. Y. Chou, Appl. Phys. Lett. (in press).