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RESEARCH ARTICLE

Cu(In,Ga)Se_2 superstrate solar cells: prospects and limitations

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ABSTRACT

Superstrate solar cells were prepared by thermal evaporation of Cu(In,Ga)Se2 onto ZnO coated glass substrates. For the first time, photo-conversion efficiencies above 11% were reached without the necessity of additional light soaking or forward biasing of the solar cell. This was achieved by modifying the deposition process as well as the sodium doping. Limitations of the superstrate device configuration and possible ways to overcome these were investigated by analyzing the hetero-interface with electron microscopy and X-ray photoemission spectroscopy measurements, combined with capacitance spectroscopy and device simulations. A device model was derived that explains how on the one hand the GaO_x, which forms at the CIGSe/ZnO interface, reduces the interface recombination. On the other hand how it limits the efficiency by acting as an electron barrier at the hetero-interface presumably because of a high density of negatively charged acceptor states like Cu_{Ga}. The addition of sodium enhances the p-type doping of the absorber but also increases the net doping within the GaO_x. Hence, a trade-off between these two effects is required. The conversion efficiency was found to decrease over time, which can be explained in our model by field-induced diffusion of sodium cations out from the GaO_x layer. The proposed device model is able to explain various effects frequently observed upon light soaking and forward biasing of superstrate devices. Copyright © 2014 John Wiley & Sons, Ltd.

KEYWORDS

CIGSe; superstrate; Ga_2O_3; sodium; tandem; ZnO; capacitance; SCAPS

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1. INTRODUCTION

The semiconductor Cu(In,Ga)Se_2 (CIGSe) is a popular material for thin film solar cells because of its excellent optoelectronic properties. In the last years, CIGSe-based photovoltaic devices with efficiencies above 20% have been successfully fabricated and commercialized. Commonly, CIGSe devices are processed in the so-called substrate configuration, where the p-type absorber layer is deposited onto the hole collecting molybdenum back contact, whereas the emitter materials, CdS and ZnO, are deposited on top of the absorber. This configuration has been shown to lead to highly efficient lab scale devices but also has some drawbacks. The ZnO conductivity tends to degrade in accelerated aging (damp heat) because of the roughness of the absorber and because high deposition temperatures cannot be used for this layer [1]. These limitations are not present in the superstrate configuration, where the absorber layer is deposited on top of the transparent window layer (Figure 1). Also, high-temperature annealing of the ZnO has led to higher electron mobilities, leading to a much better trade-off between sheet resistance and transparency in a solar cell device [2]. If successfully applied, the superstrate configuration is able to offer additional advantages by allowing an easier implementation of light trapping, improved back contact design, or the realization of tandem device structures [3–5]. However, unlike the experience with CdTe solar cells, CIGSe solar superstrate solar cells so far have not reached conversion efficiencies larger than 13%, compared with that of the more than 20% demonstrated for the substrate configuration [6–10]. The main drawback for this alternative approach has been the difficulty to properly design the CIGSe/ZnO hetero-interface, which typically

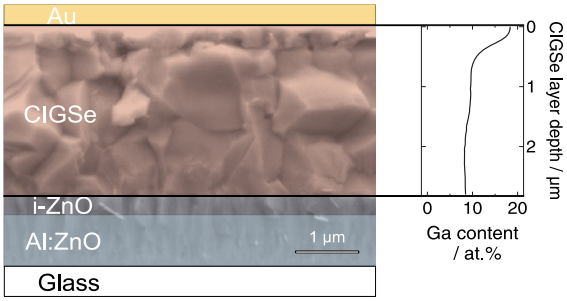

Figure 1. Schematic diagram of a superstrate solar cell overlayed with a typical SEM image of a CIGSe absorber deposited on ZnO at $T_2 = 525\,°C$. On the right side, the Ga concentration profile (measured with GDOES) over the CIGSe layer is shown.

requires the insertion of a buffer layers such as CdS that are, however, not stable at the high temperatures required for absorber preparation [11]. Therefore, the best CIGSe superstrate devices so far [7,12] were obtained using solely undoped ZnO ("i-ZnO") as a "buffer layer." Some additional features are known to improve the efficiency. Nakada *et al*. supplied sodium during the absorber growth in combination with an applied forward bias to the finished device [7]. Instead of adding sodium, Haug *et al*. used long time light soaking to temporarily increase the charge carrier density in their devices [13]. In both of these studies, it was argued that a GaO_x, layer that forms at the interface to the ZnO, somehow limits the efficiency, although the origin of the efficiency limitation was not studied. The aims of this work are to explain the device limitations because of the GaO_x formation and to find ways to overcome these. Also, the influence of sodium on the device characteristics and device degradation, as well as the effect of forward biasing the device will be illuminated.

2. EXPERIMENTAL

The solar cells for the present study consist of a multilayer stack of Al : ZnO (865 nm), i-ZnO (130 nm), CIGSe (3 µm), and Au (200 nm), as shown in Figure 1. The Al : ZnO, used as the window layer, was RF-sputtered onto soda lime glass at 1.5 µbar argon pressure using a substrate temperature of 325 °C. Subsequently, intrinsic ZnO was RF-sputtered at 8 µbar and room temperature. The CIGSe absorber was deposited by thermal evaporation from elemental sources using a processing sequence based on the well-known three-stage process [14]. In this process, an $(In,Ga)_2Se_3$ precursor is deposited at a low substrate temperature T_1 in the first stage followed by the evaporation of Cu and Se at the maximum deposition temperature T_2 in stage 2 until the absorber becomes overall copper rich. The process is completed by the evaporation of In, Ga, and Se in the third stage to make the absorber copper poor again. The deposition process for the superstrate devices was modified to fit the inverted device geometry that requires an inverted Ga gradient within the absorber layer (Figure 1). To achieve this, less Ga was evaporated in the first stage, and Ga was instead co-evaporated with Cu and Se during the second stage. In the third stage, solely Ga and Se were deposited until an overall Cu/(In + Ga) ratio of 0.85 was reached. This leads to a strong increase in Ga concentration close to the back contact and in turn to an efficient electron barrier that eliminates back contact recombination. NaF post-deposition treatments were performed by evaporating several nanometers of NaF on top of the finished CIGSe absorber at a certain temperature T_3. This temperature was held for 10 min before cooling down the substrate. The back contact was realized by electron gun evaporation of 200 nm of gold through a shadow mask. The active area of each solar cell was 25 mm × 25 mm. The current–voltage (*I–V*) characteristics were recorded with a Keithley SMU (Cleveland, Ohio, USA) under 100 mW/cm^2 of AM1.5 light and at 25 °C substrate temperature. The capacitance–voltage (*C–V*) curves were recorded with an HP 4284A LCR meter (Palo Alto, CA, USA) at a low frequency of 1 kHz to ensure that the measured capacitance is not limited by the device's RC time constant. The depth profiles were acquired with a glow discharge optical emission spectrometer (GDOES) GDA 650 from Spectruma (Hof, Germany) with 2.5-mm anode diameter and argon as a discharge gas. Cross sectional specimens for transmission electron microscopy (TEM) were prepared by mechanical grinding and subsequent ion milling up to electron transparency. Scanning electron microscopy was used to study the morphology of the devices using a Zeiss Leo 1530 scanning electron microscope (Zeiss, 73447, Oberkochen, Germany) with a Gemini column and field emission gun as electron source. Investigation of the specimens was carried out in a Zeiss LIBRA 200 FE equipped with a Thermo Noran System 6 for energy dispersive X-ray spectrometry. To investigate the i-ZnO/CIGSe interface, a lift-off procedure was performed in a nitrogen-filled glovebox with direct access to the ultrahigh vacuum chamber of the XPS setup. XPS measurements were carried out with Mg Kα and Al Kα irradiation. For quantitative analysis, the peaks were fitted with Voigt functions and corrected for the ionization cross section and mean free path of the electron lines as well as for the electron analyzer characteristics plus possible surface contamination. The O_{1s} lines typically consist of two lines, and the broad line at higher kinetic energy was discarded as part of the contamination. Device simulation was performed using the program SCAPS [15] with the following standard settings, $N_D(\mathrm{Al:ZnO}) = 10^{21}\,\mathrm{m}^3$, $N_D(\mathrm{iZnO}) = 10^{18}\,\mathrm{cm}^3$, $N_A(\mathrm{CIGSe}) = 10^{15}\,\mathrm{cm}^3$, $\Phi(\mathrm{Au}) = 5.2$ eV, $\chi(\mathrm{CIGSe}) = 4.5$ eV, $\chi(\mathrm{ZnO}) = 4.6$ eV, $\tau_n(\mathrm{CIGSe}) = 10$ ns, and a similar Ga gradient as seen in Figure 1.

3. RESULTS AND DISCUSSION

3.1. Influence of GaO_x formation

Figure 2 shows the influence of the deposition temperature T_2 on the *I–V* characteristics for devices without sodium.

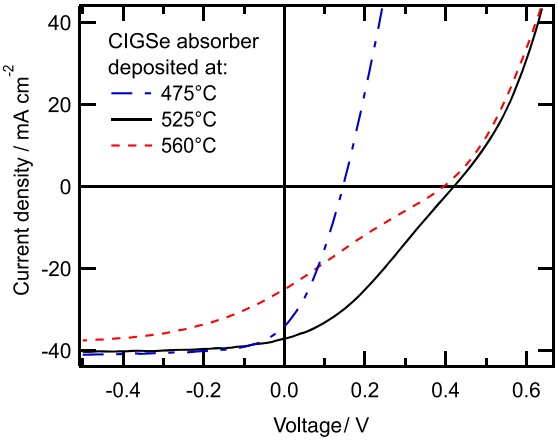

Figure 2. *I–V* curves of Al : ZnO/i-ZnO/CIGSe/Au devices with the CIGSe layer deposited at different temperatures without addition of sodium.

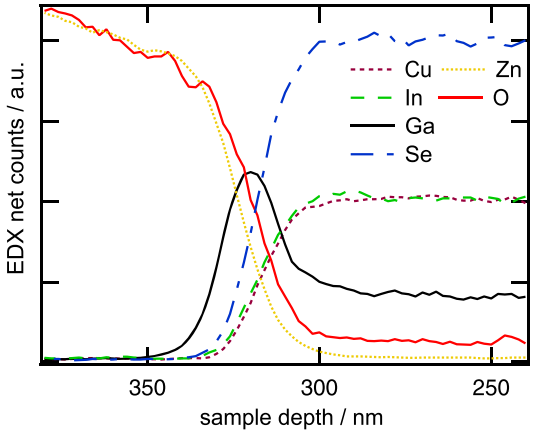

Figure 4. Net counts of an EDX scan over the i-ZnO/CIGSe interface are shown. A maximum of the Ga line counts can be detected at the interface because of the presence of GaO_x. The EDX scan was performed on a different part of the sample; then, the TEM image is shown in Figure 3.

We observe short circuit currents of 37 mA/cm^2, which are higher than typical short circuit currents observed in substrate devices with a similar minimum band gap of 1.18 eV. On the other hand, very low open circuit voltages are found for deposition temperatures T_2 below 500 °C. As T_2 is increased above 500 °C, the open circuit voltage increases, but the fill factor decreases. The best devices with an efficiency of 11.4% were achieved at a deposition temperature $T_2 = 525$ °C.

Figure 3 shows a TEM image of the hetero-junction region of a sample made at $T_2 = 525$ °C. In the region between the CIGSe (left) and the ZnO (right), an approximately 6-nm thick amorphous layer can be observed. An energy dispersive X-ray spectrometry profile of the same sample (Figure 4) shows that this amorphous layer consists of GaO_x. This is consistent with thermodynamic simulations made with the program ChemSage [16], which indicate that the surface of the i-ZnO layer is prone to be

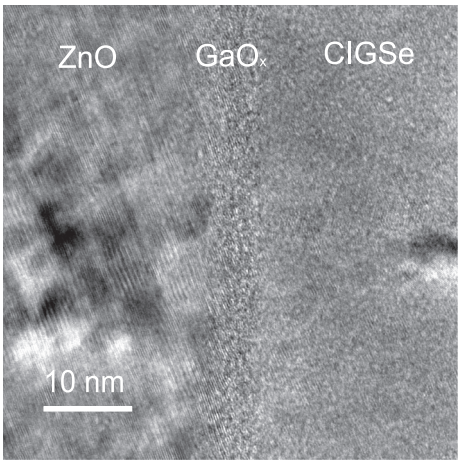

Figure 3. TEM image of the i-ZnO/CIGSe interface. A 6-nm thick amorphous GaO_x layer at the interface can be seen.

transformed into ZnSe by the formation of interfacial GaO_x during absorber deposition. This is due to the very high formation enthalpy of Ga_2O_3 (−1100 kJ/mol) compared with ZnO (−348 kJ/mol) as well as In_2O_3 (−926 kJ/mol) and Cu_2O (−157 kJ/mol) at 298 K [17]. From a purely thermodynamic point of view, the formation of GaO_x should consume all of the oxygen from the ZnO. The experimental findings of a limited thickness of this layer may be explained with a slow diffusion of Ga and O through the dense GaO_x layer. Higher deposition temperatures T_2 enhance this diffusion as well as the diffusion of sodium from the glass substrate to the interface. Sodium has a catalytic effect on the GaO_x formation, which is further discussed in Section 3.2. Thus, the GaO_x thickness is expected to increase with deposition temperature, which indeed was observed in a previous study [18]. The thickness was found to be also dependent on the process conditions of the ZnO. Higher substrate temperatures during the ZnO deposition lead to a less pronounced formation of GaO_x at the hetero-interface.

For the sample deposited at $T_2 = 525$ °C, the GaO_x thickness is around 6 nm (as measured by TEM). Assuming the previously described chemical reaction, 9 nm of ZnO react with the supplied Ga_2Se_3 into 6 nm Ga_2O_3 and 9 nm ZnSe. This leads to a Zn concentration of around 0.3 at.%. The influence of these Zn impurities in chalcopyrite crystals is not finally clarified [19]. On the one hand, a preferred occupation of In sites by Zn has been reported [20,21]. On the other hand, an increase of donor states because of Zn on Cu sites for Cu-poor samples has been suggested [22]. From *C–V* measurements on Zn-doped substrate devices (not shown), we found that the effective p-type doping density and with it the open circuit voltage increase until a Zn concentration of 0.1 at.% is reached and then fall again for higher Zn concentrations. At Zn concentrations above 0.4 at.%, the charge carrier density was measured to be smaller than samples without any Zn

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content. It can be assumed that the Zn atoms at the concentration of 0.3 at.%, as found in the superstrate devices fabricated at $T_2 = 525\,°C$, are more likely to be found on In/Ga sites than on Cu sites and increase the effective p-type doping. The lower fill factor of the sample fabricated at $T_2 = 560\,°C$ could be explained by an increase in Zn concentration and with it a decrease in the effective p-type doping. The optimum temperature of 525 °C may partly originate from this effect. The low open circuit voltage for lower deposition temperatures can not originate from the doping effect of Zn, because we would assume smaller Zn concentration and thus higher absorber p-type doping and higher open circuit voltages.

Despite the Zn impurities, the diffusion length for samples made at the optimum T_2 temperature was determined to be close to 1800 nm by fitting an electron collection function to an electron beam induced current cross sectional profile, as done in [23]. Nevertheless, the corresponding *I–V* curve shown in Figure 2 shows a very poor fill factor. This indicates an electron barrier at the interface to the ZnO that limits the charge carrier extraction. In order to better understand the interface properties, the sample was cleaved at the CIGSe/ZnO interface and analyzed with XPS. Measurements on both resulting surfaces were performed, and the quantitative results are shown in Table I. It is seen that the "ZnO surface" mainly consists of GaO_x. For T_2 lower than 500 °C, it is not possible to cleave the sample, and we conclude from this that insufficient GaO_x is formed at these temperatures. This GaO_x layer could be responsible for the observed low fill factor, which would be related to a barrier in the conduction band at the CIGSe/GaO_x interface. The electron affinity χ of GaO_x is not known precisely; in [24], it was estimated from GaO_x/Au Schottky barrier measurements to be 4 eV. Such a low electron affinity should lead to a large conduction band spike of 500 meV at the CIGSe/GaO_x interface, essentially inhibiting current flow. However, this may not be the case here because the XPS results show large quantities of Cu, In, Zn, and Se impurities on the order of several atomic percentages within the GaO_x. This may have a strong influence on the electron affinity, that is, in [25], an electron affinity of 5.1 eV was reported for $GaInO_3$. The current flow through the GaO_x could also be assisted by tunneling through defect states. A better explanation for the observed low fill factor may be band bending at the hetero-interface because of a high negative charge density within the GaO_x layer caused by acceptor states.

To test this hypothesis and to get insight into the defect distribution within the device, *C–V* measurements were performed. The inset of Figure 5 shows the measured capacitance over the applied voltage of one of the samples fabricated at $T_2 = 525\,°C$. From this, the corresponding depth profile of the charge carrier density N_A was calculated, assuming that the space charge region within the ZnO is negligible and that no deep defects within the absorber bulk contribute to the capacitance, with the following equation [26]:

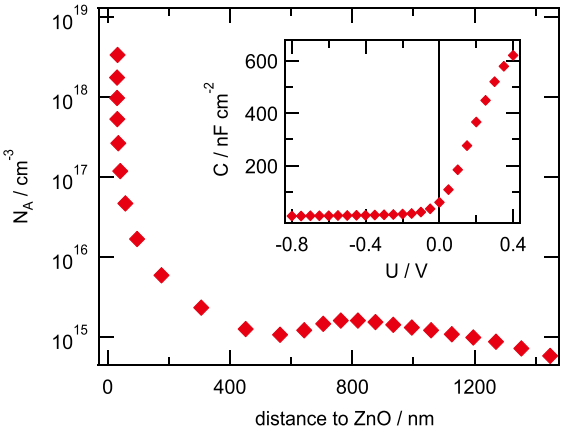

Figure 5. Charge carrier density N_A plotted versus the space charge width of a device with an absorber deposited at 525 °C without NaF. The charge carrier density is calculated with Eq. 1 from the *C–V* curve that is shown in the inset. Note that DLCP measurements resulted in similar curves. The strong increase close to the interface does not originate from diffusion capacitance or bulk defects but from acceptor states within the GaO_x.

Table I. Quantitative results from XPS measurements shown in atomic per cent of all elements within a sample without sodium, a sample with sodium, and a degraded sample with sodium.

Unit	ZnO fresh (at.%)	ZnO with Na fresh (at.%)	ZnO with Na old (at.%)	CIGSe fresh (at.%)	CIGSe with Na fresh (at.%)	CIGSe with Na old (at.%)
Cu	3	1	1	13	13	11
In	5	2	2	25	24	26
Ga	44	27	30	6	12	10
Se	17	8	7	54	42	36
Zn	1	1	1	1	0	0
Na	0	6	5	0	4	11
O	32	56	53	1	4	6

All samples were cleaved at the CIGSe/ZnO interface. Care is to be taken because the relative error of the atomic concentrations is between 50% and 60%. Because we only compare similar samples and because the error is systematic (mainly originating from uncertainties of the mean free path of the X-rays, the ionization cross section, and the transmission function), it is still possible to analyze and interpret trends between these samples.

$$N_A(\mathrm{d}) = -\frac{C^3}{\mathrm{q}\varepsilon A^2(dC/dV)} \quad (1)$$

where A is the device area, q the elemental charge, ε the dielectric constant of CIGSe, and d the width of the depletion region, which was calculated with

$$d = \varepsilon A/C \quad (2)$$

Within the bulk of the absorber, a low charge carrier density around $10^{15}\,\mathrm{cm}^{-3}$ was calculated that rises to $10^{19}\,\mathrm{cm}^{-3}$ at the ZnO interface vicinity (values of up to 600 nF/cm^2 at forward bias). From admittance measurements at forward bias (not shown), an activation energy of 300 meV was determined for these charge carriers. This rise might originate from the zinc impurities. However, device simulation with the program SCAPS could not produce any qualitatively similar curves assuming any kind of defect, which is homogeneously distributed or located close to the interface within the absorber bulk. By assuming that the charge carrier concentration of around $10^{19}\,\mathrm{cm}^{-3}$ originates from deep acceptor states within the GaO_x and setting the shallow donor state concentration to a similar value within the i-ZnO, it is possible to simulate the *C–V* curve perfectly (simulation results shown in Figure 8 and Table II).

When assuming such a high density of acceptor states at the interface between ZnO and CIGSe, the width of the space charge region (as defined in Eq. 2) becomes limited to the width of the GaO_x layer already at short circuit condition (which was confirmed via electron beam induced current profiles, not shown). As shown in Figure 6, the high acceptor density at the interface leads at positive bias voltages to an upward bending of the absorber conduction band and thus forms a voltage dependent photoelectron barrier. This effect could explain the observed low fill factor and low power conversion efficiency of the superstrate CIGSe solar cells. The low open circuit voltage of typically 200 mV for T_2 values below 500 °C can be explained by the small recombination activation energy at the ZnO interface between the ZnO conduction band and the CIGSe valence band. For low T_2 temperatures, the GaO_x thickness becomes smaller and tunneling processes although the GaO_x layer becomes a possible limitation for the open circuit voltage. This could explain why Nakada *et al.* were only able to achieve efficient devices for Cu/III ratios of 0.4, because the CIGSe valence band is lowered for this ratio [27]. For temperatures above 500 °C, the GaO_x is thick enough to block the interface recombination current between CIGSe and ZnO.

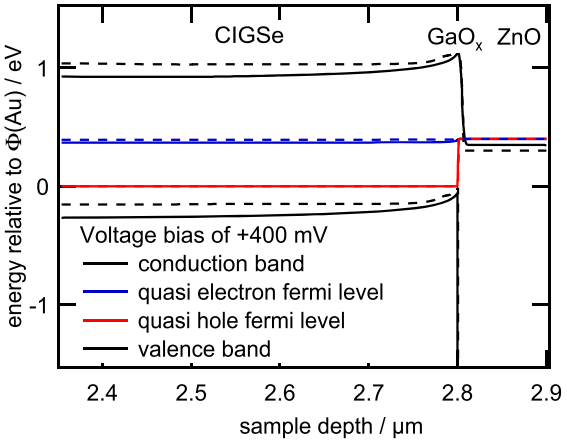

Figure 6. Calculated energy band diagram of the CIGSe/GaO_x/ZnO interface without sodium (solid lines) and with sodium (dashed lines) under 400-mV forward bias. Because of the high acceptor density within the GaO_x, the conduction band on the absorber side bends upward and causes an electron barrier. The values used for the simulations are shown in Table I. In this model, the electron affinity of CIGSe and GaO_x was set to the same value of 4.5 eV.

The origin of the assumed high acceptor density within the amorphous GaO_x layer may be inferred from the results of the XPS measurements shown in Table I. The surface of the ZnO consists of GaO_x with large amounts of impurities of all other elements, whereas In and Se are supposed to induce no acceptor states, both states Cu_{Ga} and Zn_{Ga} do [27,28]. This could explain the origin of a high density of acceptor states within the GaO_x. It has to be kept in mind though that the GaO_x layers appear to be oxygen poor that could induce cation interstitials like Ga_i or anion vacancies like V_O, both leading to donor states [29]. The maximum charge carrier concentration reported previously for oxygen-poor Ga_2O_3 is $10^{18}\,\mathrm{cm}^{-3}$ [24], which is below the acceptor state density of around $10^{19}\,\mathrm{cm}^{-3}$ measured in this study. Nevertheless, the acceptor-type states Cu_{Ga} and Zn_{Ga} may be partly compensated by anion vacancies like V_O. This also gives a hint on how to overcome the device performance limitation. By purposely adding donors into

Table II. Overview of the *I–V* characteristics in Figures 9 and 10 as well as the acceptor state densities of the GaO_x, the CIGSe close to the interface, and the CIGSe bulk derived from *C–V* curve simulations from Figures 8 and 11.

Unit	η(%)	FF(%)	V_{oc}(mV)	N_A GaO_x(cm^{-3})	N_A CIGSe interface(cm^{-3})	N_A CIGSe bulk(cm^{-3})
Without Na	5.6	29	610	1.6×10^{19}	5.0×10^{14}	5×10^{14}
With Na at 400 °C	3.3	20	670	3.7×10^{19}	1.1×10^{18}	5×10^{16}
With Na at 300 °C	11.4	51	675	2.3×10^{19}	1.0×10^{18}	5×10^{16}
Stored at 0 V	5.2	32	672	2.8×10^{19}	2.0×10^{18}	5×10^{16}
Stored at 1 V	9.9	48	659	2.3×10^{19}	2.0×10^{18}	5×10^{16}

the GaO_x, it would be possible to fully compensate the existing acceptor states and thus allow efficient current transport over the interface. From literature, the elements Si, Ge, and Sn are known to be n-type dopants [29].

3.2. Influence of sodium

The addition of sodium is essential for high efficiency CIGSe solar cells because of the permanent increase of the positive charge carrier density induced by it [30–33]. The origin of the doping effect is still under debate, but the disappearance of low energetic peaks in photoluminescence spectra, after introducing sodium to the absorber, leads to the assumption that sodium passivates the donor states V_{Se} or In_{Cu} [33,34]. In superstrate devices, it was so far not possible to achieve functional devices after the addition of sodium without special treatments such as voltage biasing the device. Thus, different ways to increase the majority charge carrier density have been used such as light soaking [13].

A possible reason for the difficulties of sodium incorporation can be observed in GDOES elemental depth profiles (not shown), which show that the addition of a NaF precursor deposited on the ZnO prior to the absorber deposition leads to a strongly enhanced formation of GaO_x at the interface, which prohibits any current flow through the interface. Also, the addition of sodium during or after the CIGSe deposition at the temperature T_2 leads to a similar current blocking effect. The increased oxidation of gallium at the interface can be explained by the catalytic effect of sodium on the oxidation process [34]. To overcome this problem, we varied the temperature during the NaF post-deposition to prevent strong oxidation of the interface. The change in deposition temperatures leads to a change in the sodium diffusion profile measured by GDOES depth profiling as shown in Figure 7. The elemental depth profiles indicate that at post-deposition temperatures T_3 of around 100 °C, all the sodium remains at the top surface. Indeed, no increase in bulk charge carrier density could be observed in *C–V* measurements for these samples. However, this leads to a highly p-type doped top surface and improves the back contact quality, which otherwise tends to have a Schottky character in superstrate cells because of the copper-poor composition at the top surface. The low temperature NaF treatment solely results in a reduction of the series resistance (*I–V* curve not shown here). For higher T_3, sodium starts to diffuse into the bulk of the absorber that leads to the desired increase in the absorber charge carrier density of values above $10^{16}\,cm^{-3}$. Figure 7 shows that for T_3 temperatures higher than 200 °C, the NaF also starts to accumulate at the CIGSe/ZnO interface. And simulation results of *C–V* measurements (Figure 8 and Table II), which were performed on these devices, indicate that the acceptor density increases significantly not only in the absorber bulk but also at the hetero-interface and in the absorber close to the hetero-interface.

The corresponding *I–V* curves and parameters are shown in Figure 9 and Table II. The values for J_{sc}, V_{oc}, and FF increase until a post-deposition temperature of 300 °C because the bulk absorber doping increases, but it drops again for higher temperatures because the acceptor density within the GaO_x increases strongly (Table II). The energy band alignment shown in Figure 6 can explain the origin of this effect. The dashed line shows the simulated energy bands of a NaF-treated device at 300 °C with the parameters determined from the simulation of the *C–V* curves. The upward bending of the conduction band is reduced compared with the case without the addition of NaF that is drawn as a solid line. The lower band bending improves the charge carrier collection and with it the fill factor. Thus, it is important to find an optimum between doping the absorber as high as possible without introducing too many new acceptor states within the GaO_x layer.

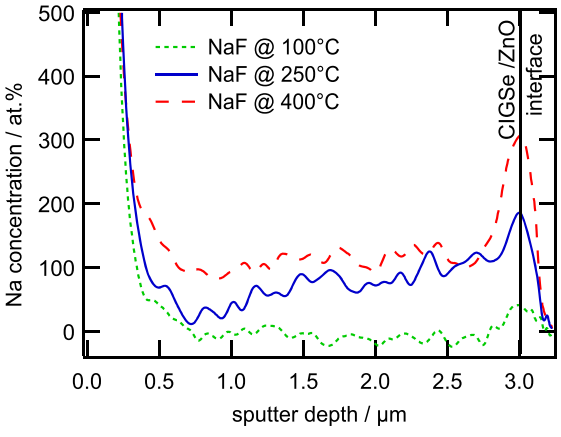

Figure 7. GDOES depth profiles of samples with different NaF post-deposition treatments. The amount of sodium at the interface depends critically on the T_3 temperature.

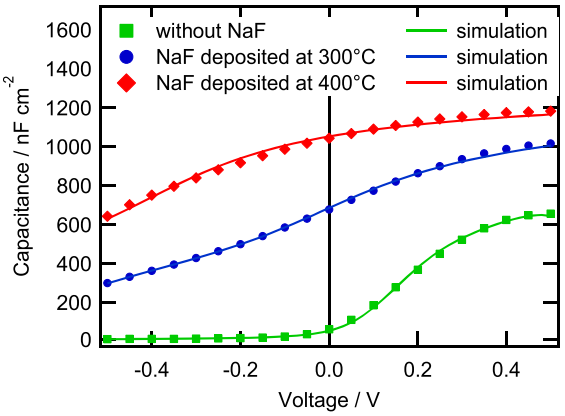

Figure 8. *C–V* curves of devices made at $T_2 = 525$ °C with different NaF post-deposition treatments together with the corresponding simulated curves. Within the simulations, the acceptor density N_A in the GaO_x layer is the dominant factor influencing the shape of the *C–V* curves; for each simulation, the value used for N_A is given in Table II.

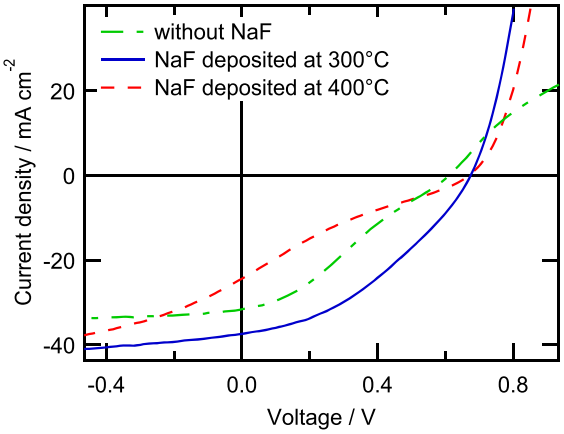

Figure 9. *I–V* curve of devices made at $T_2 = 525$ °C but different NaF post-deposition treatments.

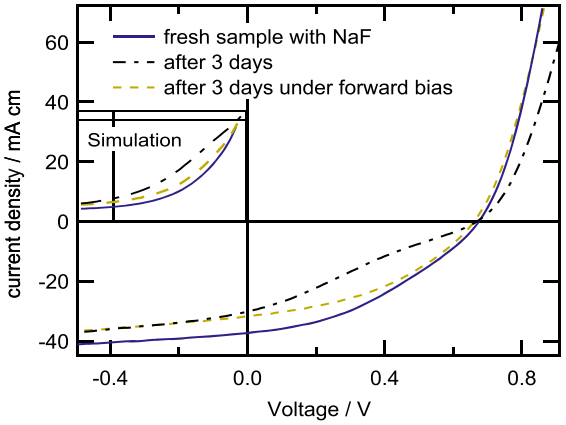

Figure 10. Effect of degradation and forward bias on the *I–V* curves of a sample with a NaF post-deposition treatment at 300 °C. The photocurrent decreases over time independent of the storage condition, whereas the kink does not show up if the sample is stored under a forward bias voltage of +1 V. The simulated *I–V* curves use the same parameters as the simulated *C–V* curves shown in Figure 9.

This can be achieved by using temperatures below 300 °C during the NaF treatment.

The reason for the assumed increase of the acceptor state density within the GaO_x because of the presence of sodium may be again inferred from the results of the XPS measurements shown in Table I. The GaO_x layer of the sample without sodium shows an overall oxygen-poor composition, even including the contribution of selenium, whereas the sample including sodium shows an oxygen-rich composition. This proves the catalytic effect of sodium on the oxidation process of gallium at the interface to ZnO even at low temperatures. Because oxygen vacancies are known to act as donor states in Ga_2O_3, they partly compensate the acceptor states like Zn_{Ga} and Cu_{Ga} within the GaO_x, as discussed in Section 3.1. Thus, the presence of sodium at an elevated temperature seems to eliminate the compensating donor states V_O and increase the overall p-type character compared with the sample without sodium present at the interface. The doping effect of sodium within GaO_x hence appears to be similar as in the case of the absorber bulk; instead of acting directly as an acceptor, it decreases the amount of donor states by catalyzing the oxidation of the gallium atoms.

3.3. Stability

Although the degradation for samples without sodium is almost negligible, it becomes strongly accelerated by the presence of sodium at the ZnO/CIGSe interface, indicating that sodium is triggering the degradation or may even be the origin of it. The samples containing sodium degrade initially because of losses of the fill factor and finally also of the short circuit current. An example is given in Figure 10 that shows the *I–V* curve of a device with sodium after 3 days of storage under open circuit condition in the dark.

I–V analysis shows that in our case, the series resistance did not increase that rules out the degradation of the back contact as has been reported by other authors. However, the onset of the diode current is pushed to slightly higher voltages, and a kink develops in the fourth quadrant of the *I–V* curve. This can be explained by an increased electron barrier at the hetero-interface caused by the GaO_x layer, which reduces the photoelectron collection across the GaO_x layer as well as the diode current. *C–V* measurements on degraded samples show an increase in capacitance with advanced degradation over the full range of applied voltages (Figure 11). This can be reproduced by device simulations with SCAPS by increasing the acceptor-type defects within the GaO_x in combination

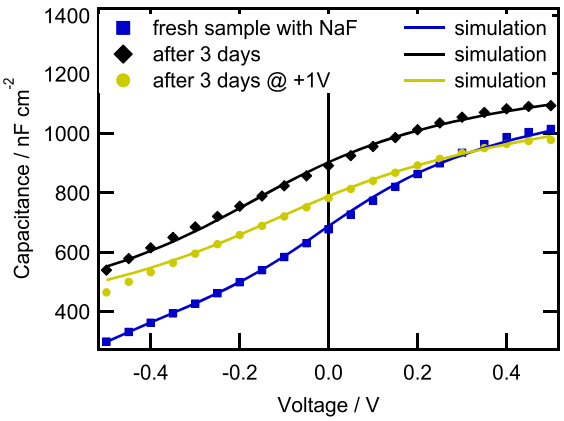

Figure 11. Effect of degradation and forward bias on the *C–V* curves of a sample with a NaF post-deposition treatment at 300 °C. The capacitance increase at negative bias over time is simulated by an increase of the acceptor state density within the CIGSe in the vicinity of the interface to GaO_x. The capacitance increase at positive bias is simulated by an increase of acceptor states within the GaO_x. The values used for the simulation are given in Table II.

with increasing the absorber doping in the vicinity of the GaO_x/CIGSe interface (Table II). The assumed increase of the acceptor state density in the GaO_x further lifts the conduction band within the GaO_x, which could be the reason for the observed kink in the *I–V* curve. Simulation of the *I–V* curves with the parameters obtained from the *C–V* simulations showed the same trend as the measured *I–V* curves (Figure 10).

A possible explanation for the assumed increase in acceptor states is yet again obtained from the XPS measurements performed on the surfaces of a fresh and a degraded sample both cleaved at the interface. The results show an increase in Na concentration within the absorber surface and a decrease in Na concentration within the GaO_x. This indicates a possible migration of the mobile sodium ions from the GaO_x into the absorber by field-induced migration of the positive Na ions within the large potential drop inside the GaO_x layer. No literature value for the mobility of Na ions in GaO_x exists, but the Na_2O–$6Ga_2O_3$ system shows very high mobilities of Na, comparable with those of liquids [35]. At storage condition in the dark without any voltage bias, the electric field within the sodium doped GaO_x is about 6 MV/cm in our model, which is close to the estimated breakdown field of 8 MV/cm [36], and strong enough to cause electromigration of sodium or copper ions. Because the GaO_x has an oxygen-rich composition after the Na treatment, the out diffusion will lead to a reduction of Na_{Ga} states and in turn lead to the formation of V_{Ga} acceptor states. This means that sodium not only eliminates donor states within the GaO_x layer during the high-temperature NaF post-deposition but it can also increase the acceptor state density when it drifts out of the GaO_x during room temperature storage.

3.4. Effect of forward biasing

By applying a forward bias of +1 V to the sodium-containing devices, it is possible to increase the fill factor of degraded devices and also prevent the degradation of the fill factor from the beginning. This can be seen in the *I–V* curves shown in Figure 10. Another effect of forward biasing is that the capacitance measured at forward biases is decreased down to the value of a fresh device (Figure 11). Simulations of the *C–V* curves show (Table II) that this implies a reduction of acceptor states only inside the GaO_x and with it a reduction of the conduction band barrier. If the solar cell is kept at open circuit condition in the dark for several hours, the fill factor slowly starts to decrease again, which shows that this effect is reversible. As discussed in Section 3.3, the degradation seems to be induced by electromigration of Na and possibly Cu ions out of the GaO_x layer, which changes the density of V_{Ga} defect states within the GaO_x in our model. Thus, this effect should be controllable and reversible by changing the electric field inside the GaO_x, just as it is observed. At zero-applied voltage, the electric field of the junction region is limited to the GaO_x layer (compared with Figure 6) that causes the out diffusion of positively charged cations like Cu^+ or Na^+. By applying +1 V to the device, the electric field is strongly reduced, which lowers or even reverts the driving force for the ion movement and thus the degradation.

The short circuit current does not recover despite the applied voltage, which may originate from sodium also diffusing from the bulk absorber material into the hetero-interface region over time.

3.5. Prospects

Using our model, one possible way to further increase the device efficiency is to enhance the charge carrier lifetime. At higher lifetimes, charge carriers are able to overcome the energetic barrier at the hetero-interface before recombining. Simulations with SCAPS resulted in an efficiency of 16% for an assumed lifetime of 100 ns, compared with that of 11% with 10 ns. In order to reach efficiencies of 20% or higher, our model requires the presence of donor states within the GaO_x layer, for example, by doping it with elements like Si, Ge, or Sn [37]. Alternatively, new buffer layers have to be found, with formation energies higher then Ga_2O_3, tolerant to sodium doping, and most importantly with electron affinities lower than that of ZnO. In addition, this requires a low Transparent Conductive Oxide series resistance while keeping the light transmission high. For this purpose, high-temperature-annealed ZnO or TCOs with similar high electron mobilities would be necessary [2]. Furthermore, a highly reflective back contact, that is MoO_x/Ag, should allow the use of ultrathin absorbers without losses in the short circuit current.

4. SUMMARY AND CONCLUSIONS

A model based on the results of *C–V* and XPS measurements is presented to explain the typically observed low fill factor and the effects upon light soaking and forward biasing of superstrate CIGSe solar cells. For the first time, superstrate CIGSe devices with conversion efficiencies above 11% were measured without prior light soaking or forward biasing. This was achieved by adapting the sodium doping procedure and the absorber deposition from the substrate configuration to the superstrate configuration.

It is found that the main device limitation is a photocurrent barrier at the hetero-interface, which we assume in our model to originate from a high density of deep acceptor states within the interfacial GaO_x. Presumably, the high density of negatively charged acceptor states are induced by Zn and Cu dopants within the GaO_x layer, whose presence was confirmed by XPS measurements. The negative charge within the GaO_x acts similar to a p^+ layer [23] and causes an upward bending of the conduction band thus inducing a voltage dependent electron collection barrier. The thickness of the GaO_x can be controlled by the deposition temperature, and best results were obtained for thicknesses around 6 nm. Lower thicknesses lead to a V_{oc} limitation, presumably because of interface recombination, and thicker layers increasingly reduce the fill factor. Even

for the best cells, the main limiting factor of the superstrate devices is the low fill factor.

It was possible to increase the efficiency further by increasing the p-type doping of the absorber with a sodium post-deposition treatment. The higher charge carrier density lowers the upward conduction band bending relative to the GaO_x layer. Based on the *C–V* and GDOES measurement results, we assume that the presence of sodium at the hetero-interface also increases the acceptor state density within the GaO_x. Therefore, a trade-off is required, which leads to an optimum post-deposition temperature of 300 °C.

The presence of sodium at the interface also induces degradation of the device, but it is possible to prevent the degradation and even increase the fill factor compared with the initial state by applying a positive voltage bias to the device. Both effects were explained in our model by the drift of the highly mobile sodium ions in the strong electric field of the space charge region inside the GaO_x. The out diffusion of the sodium ions under open circuit conditions increases the amount of the acceptor states V_{Ga}. By applying a permanent forward bias to the device, the electric field within the GaO_x can be reduced, which stops or even reverts the drift of the sodium ions and thus the degradation.

In conclusion, despite the possible advantages of being able to optimize the TCO and the back contact in superstrate devices, the inherent interface formation of GaO_x at the surface of ZnO, or any TCO with lower formation enthalpy than GaO_x, will not allow conversion efficiencies as high as for devices in substrate configuration. Thus, to successfully enable superstrate or tandem structures for CIGSe solar cells, new thermally stable n-type buffer layers have to be found, with an electron affinity lower than 4.5 eV and tolerant to the presence of sodium. A possible candidate would be Ga_2O_3 itself, n-type doped with Si, Ge, or Sn.

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