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Capacitance-voltage investigation of high-purity InAs/GaSb superlattice photodiodes

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The residual carrier backgrounds of binary type-II InAs/GaSb superlattice photodiodes with cutoff wavelengths around 5 μm have been studied in the temperature range between 20 and 200 K. By applying a capacitance-voltage measurement technique, a residual background concentration below 10^{15} cm^{-3} has been found. At temperatures below 100 K carrier freeze-out is observed with a thermal activation energy of 4.5 meV, leading to net carrier concentrations at 77 K in the mid 10^{14} cm^{-3}. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2172399]

Diodes based on InAs/GaSb short-period superlattices (SLs) form material systems that can be considered as III-V-based alternatives to the established mercury cadmium telluride (MCT) systems. InAs and GaSb constitute nearly lattice matched material systems offering great flexibility in the design of optoelectronic devices. InAs/GaSb superlattices were considered by Sakaki and Esaki[1] in the late 1970s. About 10 years later the material system was proposed for infrared (IR) detection devices by Smith and Mailhiot.[2] First reports on detection devices with promising electro-optical properties[3,4] followed in the late 1990s. Progress in band-structure modeling,[5] processing, and material quality enabled the first infrared images[6] in this material system, showing promise as an alternative to the established MCT material system. Most recently, promising detection performance at room temperature[7] as well as observation of negative luminescence[8,9] was reported.

The performance of minority carrier devices, such as infrared detectors strongly depends on the residual carrier background concentration. The carrier background in the nonintentionally doped (nid) region of a p^+-nid-n^+ diode defines the extension of the depletion width and the minority carrier lifetime. For example, n-type carrier backgrounds in long wavelength SLs have been demonstrated to give rise to efficient Auger recombination channels.[10] Therefore, a major task in the optimization of growth conditions is the reduction of the carrier background. Measurement of the transport properties in InAs/GaSb SLs applying Hall measurement techniques have been performed successfully on SL layers grown on semi-insulating GaAs substrates.[11] However, Hall measurements of high-quality layers grown on GaSb require electrical isolation of the SL layer from the highly conductive GaSb substrate by growing an isolating lattice matched AlGaAsSb buffer,[12,13] raising questions about the influence of such a buffer on the residual carrier concentration in the SL layer. For further optimization of the growth technique and device performance, the direct measurement of the carrier background in the very same device structure that is used for the application is highly desirable.

In this paper we report on measurements of the residual carrier background of midwavelength infrared (MWIR) InAs/GaSb photodiodes applying capacitance-voltage (CV) analysis in the temperature range between 20 and 200 K. By optimizing the processing of the samples and the electrical contacting scheme in the cryogenic environment, the residual stray capacitances of the system could be reduced to a level below 1 pF, necessary to assess carrier concentrations below 10^{15} cm^{-3}.

Type-II InAs/GaSb superlattice diodes were grown on GaSb (001) undoped wafers using an Intevac Modular Gen II molecular beam epitaxy system equipped with valved As/Sb cracker cells and Ga/In SUMO® cells. The material growth details have been published previously.[14] The binary-binary InAs/GaSb superlattice device structure consisted of a 500-nm Be-doped contact, 2-μm unintentionally doped region, and a 500-nm n-doped contact. The superlattice was designed to have a cutoff wavelength of 4.8 μm at 80 K. The mesa devices were processed using standard UV photolithography and citric acid-based wet etching. Large area diodes ($A=400\times400$ μm^2) were patterned so that the capacitance, upon full depletion of the 2-μm-thick nid region, could be maximized. Essential for successful measurements was the removal of undesired capacitance contributions from the charging effects caused by the hetero interface between the MWIR SL and the GaSb buffer layer. In order to avoid voltage and capacity offsets caused by this interface the etching needed to be stopped in the Be-doped superlattice bottom p^+contact of the diode. With this type of processing the measurement current passes through the InAs/GaSb SL only. Ti/Pt/Au metal contacts were evaporated on the top InAs cap and the p^+ superlattice contact layer. The diodes were not passivated, but care was taken to ensure minimal exposure to ambient atmospheric conditions.

In order to further reduce the influence of residual stray capacitances, the electrical setup was designed to provide a four-point contacting scheme using a 50-Ω technique. For the short circuit and the open loop calibration of the impedance measurement, this four-point contacting scheme was fed through the two chamber cryosystem to contacts on the diode chip, with the diodes immersed in the He or N_2 exchange gas. The calibration and the measurements were performed by using a high-performance switching matrix (Keithley 7174A) between the diode chip and the low-frequency impedance analyzer HP 4192A. In this way, the residual stray capacitance could be reduced to values below 1 pF. Five different diodes were measured with frequencies in the

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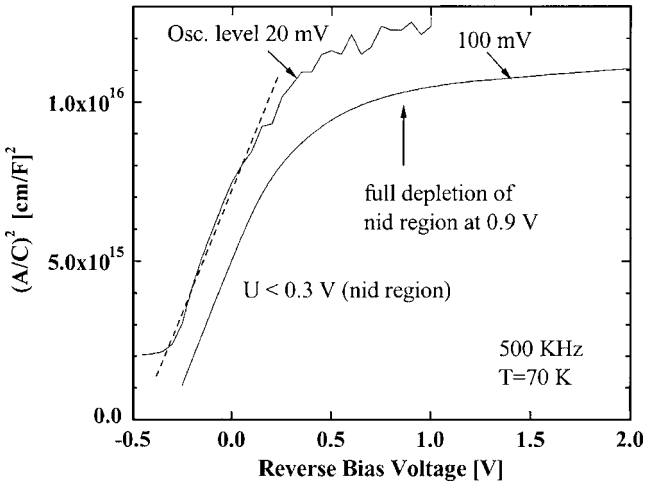

FIG. 1. Plot of the square of A/C vs the reverse bias voltage measured at 70 K. For the slope close to 0 V, an oscillation level of 20 mV was chosen. The large voltage sweep has been performed with a 100-mV oscillation level. The slope close to 0 V results in a carrier concentration of 5×10^{14} cm^{-3}. Consistent with this value is the observation of saturation at 0.9 V because of full depletion of the 2-μm nid layer. The 20-mV data have been vertically offset for clarity.

range between 50 and 900 kHz. The applied bias voltage ranged between a small forward bias of 0.3 V and reverse bias of up to 2 V.

Prior to the impedance analysis, current-voltage analysis on a set of diodes on the same chip with different sizes had been performed. With this procedure, (i) diodes could be selected, free from defect related leakage, and (ii) it was ensured that no surface leakage contributions affect the capacitance measurements.[15] The 77-K zero-bias resistance-area product (R_0A) values of these diodes were found to be above $10^5\ \Omega\,\mathrm{cm}^2$ decreasing to approximately $1\ \Omega\,\mathrm{cm}^2$ at 200 K. The reduced carrier concentration was extracted by fitting a linear curve to the data using the relationship between reverse bias voltage, V, and the squared ratio of $A/C(V)$.[16]

$$\left(\frac{A}{C(V)}\right)^2=\frac{2V_D}{q\epsilon\epsilon_0N_{\mathrm{red}}}-\frac{2}{q\epsilon\epsilon_0N_{\mathrm{red}}}V, \tag{1}$$

where V_D is the built-in potential of the diode, q is the electron charge, and ϵ_0 is the dielectric constant. For the relative dielectric constant, ϵ_r, a value between InAs and GaSb of 15.4 was chosen. This value has been found to be consistent with the optical analysis of InAs/GaSb multilayer structures.[13] In general, Eq. (1) provides the reduced carrier concentration $1/N_{\mathrm{red}}=1/N_A+1/N_D$. In the case of depletion at an n^+p or p^+n junction, N_{red} represents the lower carrier concentration. From the CV analysis no information about the polarity of the carrier background in the low-doped nid region is provided without further input.

Figure 1 shows a plot of the square of A/C versus the reverse bias voltage measured at 70 K. Measurements with two oscillation levels are shown. Close to 0 V, an oscillation level of 20 mV was chosen, while the larger voltage sweep has been performed with an oscillation level of 100 mV, providing better noise performance in the range of small capacitance. The 20 mV data have been vertically offset for clarity. Around 0 V a linear slope is observed resulting in a carrier concentration of 5×10^{14} cm^{-3}. Consistent with this value is the observation of saturation at 0.9 V. At that bias voltage, full depletion of the 2-μm nid layer is expected, leading to a weaker dependence of the capacitance on voltage. Exceeding a reverse bias voltage of 0.9 V, the doped contact regions of the SL start to be depleted.

In Fig. 2 the carrier concentration for the temperature range between 20 and 200 K is shown. In the left panel between 100 and 180 K the saturation regime, offering a concentration of 6×10^{14} cm^{-3}, is found. The increase in carrier concentration due to the generation of intrinsic carriers starts at 180 K. At temperatures below 100 K, carrier freeze-out with a single thermal activation energy of 4.5 meV is observed down to 20 K (Fig. 2, right panel). The full lines show the calculated carrier concentration assuming an impurity background of 6.5×10^{14} cm^{-3}. The dashed line corresponds to the intrinsic concentration, taking into account the decrease of the band gap with increasing temperature.

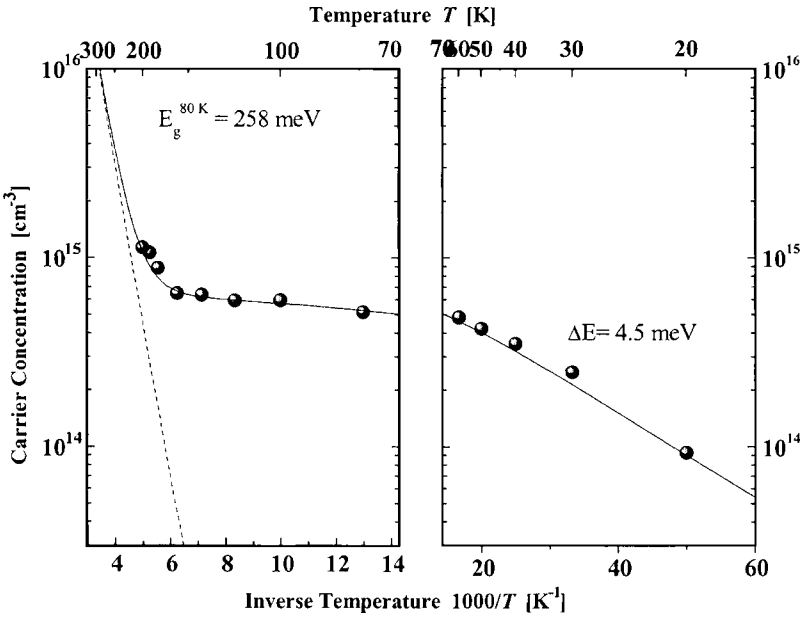

FIG. 2. The temperature dependence of the carrier concentration. The left panel shows the intrinsic and the saturation regimes above 100 K. At lower temperatures, carrier freeze-out with a thermal activation energy of 4.5 meV is observed. The full line shows the expected carrier concentration assuming an impurity background of 6.5×10^{14} cm^{-3}. The dashed line shows the intrinsic concentration taking into account the decrease of the band gap with increasing temperature.

The observed thermal activation energy of 4.5 meV in the freeze-out regime is not necessarily identical to the ionization energy of the electrical active defect.[16] At low temperatures, in the case of compensating acceptors and donors, the thermal activation energy is expected to be about half the ionization energy of the dominating impurity. If compensation can be ruled out, the observed thermal activation energy is close to the ionization energy. The acceptor binding energy of carbon in GaSb (Ref. 17) has been determined to be 12.9 ± 1 meV. For doping with Si and Ge, values of 9.4 and 9.5 meV, respectively, are reported.[18] Thus, assuming the nid region of the present SL to be compensated, our value of 4.5 meV may correspond to an acceptor with about 9 meV ionization energy, close to these values reported from GaSb. However, within a hydrogen model assuming a shallow effective mass-type impurity we have to expect a significant enhancement of the excitonic binding energy due to the strong two-dimensional (2D) confinement of heavy holes in the present SL leading to values between 20 and 30 meV.[19] In the present material system with the effective mass value of $0.025m_0$, the ionization energy of a shallow donor neglecting additional confinement effects is expected at 1.4 meV. Again, increasing 2D confinement will enhance this value up to a factor of 4.[19] We get an excellent fit to the data by assuming an *n*-type impurity with a concentration of 6.5×10^{14} cm^{-3} and a binding energy of 7 meV (Fig. 2, full line). Assuming a *p*-type background, additional assumptions on the degree of compensation have to be made to obtain a comparable quality of theoretical description, which is beyond the scope of this paper.

In summary, capacitance-voltage analysis has been demonstrated to provide a powerful tool to directly assess the residual carrier background concentration in type-II InAs/GaSb SL diodes in the saturation and freeze-out temperature range. Excellent material quality, competitive to the established MCT system, could be demonstrated. At 77 K, carrier concentrations in the mid 10^{14} cm^{-3} are found confirming the potential for high-performance infrared optical devices based on InAs/GaSb superlattices.

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