Renewable Energy 74 (2015) 247–254

Contents lists available at ScienceDirect

Renewable Energy

journal homepage: www.elsevier.com/locate/renene

New multi-stage DC–DC converters for grid-connected photovoltaic systems

Yihua Hu [a], Wenping Cao [b, *], Bing Ji [c], Jikai Si [d], Xiangping Chen [e]

[a] Department of Electronic & Electrical Engineering, Strathclyde University, G1 1XQ, UK
[b] School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast, Belfast BT9 5AH, UK
[c] School of Electrical and Electronic Engineering, Newcastle University, NE1 7RU, UK
[d] School of Electrical Engineering and Automation, Henan Polytechnic University, Henan, China
[e] College of Electrical Engineering, Guizhou University, Guiyang, China

ARTICLE INFO

Article history:
Received 2 January 2014
Accepted 4 August 2014
Available online 24 August 2014

Keywords:
DC–DC power conversion
Harmonic distortion
Hysteresis
Converters
Multilevel systems
Photovoltaic power systems

ABSTRACT

Renewable energy is high on international and national agendas. Currently, grid-connected photovoltaic (PV) systems are a popular technology to convert solar energy into electricity. Existing PV panels have a relatively low and varying output voltage so that the converter installed between the PVs and the grid should be equipped with high step-up and versatile control capabilities. In addition, the output current of PV systems is rich in harmonics which affect the power quality of the grid. In this paper, a new multi-stage hysteresis control of a step-up DC–DC converter is proposed for integrating PVs into a single-phase power grid. The proposed circuitry and control method is experimentally validated by testing on a 600 W prototype converter. The developed technology has significant economic implications and could be applied to many distributed generation (DG) systems, especially for the developing countries which have a large number of small PVs connected to their single-phase distribution network.

1. Introduction

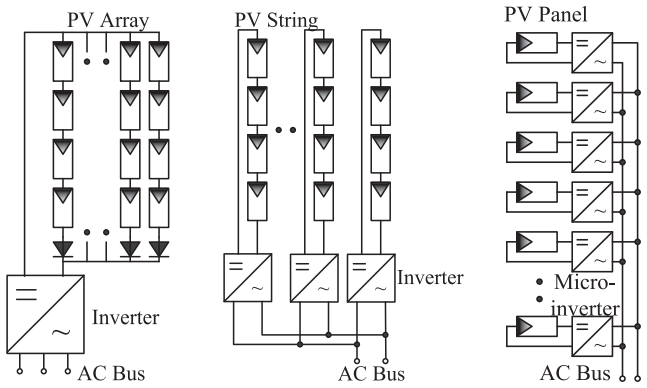
With increasing concerns over global warming and the depletion of fossil fuels, substantial investment and effort has been directed towards developing renewable energy technologies. The clean electricity generation based on photovoltaic (PV) technologies is one of the prevalent solutions. In the literature, there are three reported types of grid-connected PV system configurations reported: the central type, string type and modularized type [1–3], as depicted in Fig. 1. The first systems connect PV modules in series and then in parallel so as to increase their direct current (DC) bus voltage and power. They generally have high-voltage high-current output and are suited for large-scale (>5 kW) three-phase systems. But they suffer from high power losses and high current harmonics, PV module mismatch and shade effects [4]. The second require an individual maximum power point tracking (MPPT) for each string [5,6]. They have high-voltage low-current output, and they are efficient and suitable for medium-scale (2–5 kW) single-phase systems. In contrast, the third type of systems requires an individual power converter and MPPT for each PV module. As a result, these systems typically have low-voltage low-current output and require high capital investment. They are limited to small-scale (<2 kW) single-phase systems. In practice, the second configuration is the dominant type in PV applications and is therefore the focus of this paper.

In theory, the output voltage of one PV string is very low and varies over a wide range despite the use of MPPT. This requires the front-end DC–DC converter to be equipped with a step-up capability for grid connection [7–12] at the expense of power quality. In this case, the multilevel converter technology is advantageous to incorporate PVs into the power grid while achieving good output waveforms, reduced filter sizes and reduced electromagnetic interference (EMI) [13–15]. However, these converters are complex, costly, and low in voltage amplification. Therefore, it is desired to develop an advanced converter combining features of high step-up and multilevel so as to reduce the number of active switching devices in the converter.

When connected to a power network, the PV systems must meet stringent power quality requirements set by the utility including low total harmonic distortion (THD) and fast dynamic response. In this regard, hysteresis current control is often chosen owing to its simplicity, robustness and good large-signal response. Nevertheless, the switching frequency of the converter varies with the bus

* Corresponding author. Tel.: +44 (0)28 90974058.
E-mail address: w.cao@qub.ac.uk (W. Cao).

http://dx.doi.org/10.1016/j.renene.2014.08.009
0960-1481/



(a) The central type. (b) The string type. (c) The modularized type.

Fig. 1. Three types of PV system configurations.

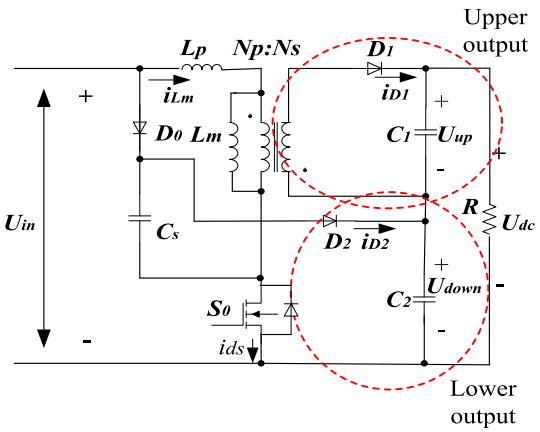


Fig. 3. Equivalent circuit of the high step-up DC–DC converter.

voltage, filter inductance and bandwidth [16–18]. In the literature, the variable-hysteresis-band current control technique [16,19] and digital hysteresis modulation technique [20] are reported in use. They require multiple samples within a switching period and are thus complicated and computationally costly. Moreover, these hysteresis control methods are hardly used for asymmetric multilevel converters [21] which are the case for this study.

To tackle the problem, this paper proposes a new asymmetry multilevel DC–DC converter with improved hysteresis control. Section 2 introduces the proposed converter topology. Section 3 discusses an improved hysteresis control scheme. Section 4 presents and analyzes the simulation and experimental results for validation purposes, followed by a brief conclusion in Section 5.

2. Proposed multilevel converter

The proposed topology consists of a high step-up DC–DC converter, a three-level DC–DC converter and a line frequency commutated bridge. See Fig. 2 for details.

2.1. High step-up DC–DC converter

The equivalent circuit of the proposed converter is shown in Fig. 3. In the figure, S_0 is the main switch, D_0 and D_2 are the regenerative diodes, D_1 is the rectifier diode, C_1 and C_2 are the output filter capacitors, C_s is the bootstrap capacitor, R is the load, U_{in} and U_{dc} are the input and output voltages, respectively. A coupled inductor L_C with primary and secondary turns of N_p and N_s is also used to increase voltage gain. It is equivalent to an ideal transformer whose primary winding connected in parallel with a magnetizing inductor L_m and then in series with a leakage inductance L_p.

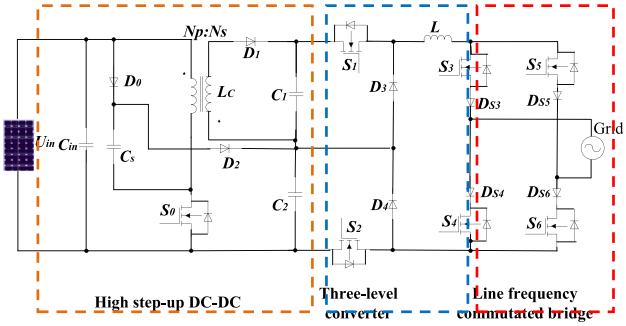
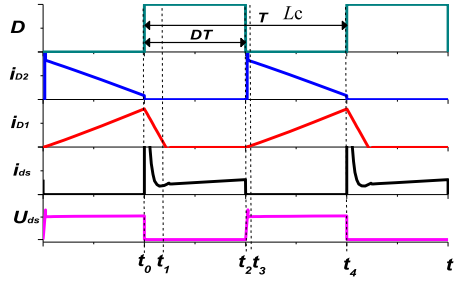


Fig. 2. The proposed high step-up multilevel converter.

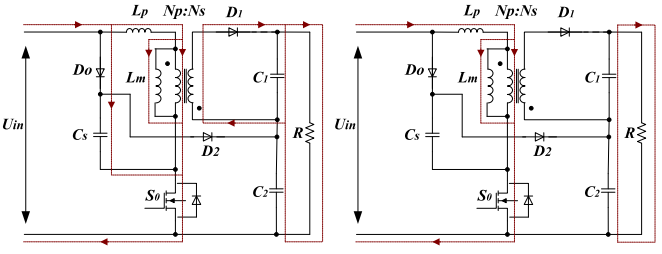
The converter operates on two modes: continuous and discontinuous conduction, depending on the load.

2.1.1. Continuous conduction mode

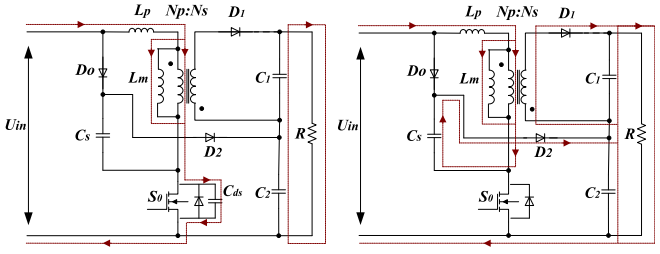
Voltage and current waveforms of the high step-up DC–DC converter in the continuous conduction mode (CCM) are presented in Fig. 4(a) and four stages and current flow paths are shown in Fig. 4(b)–(e) for one full period and explained in detail as follows.



(a) Waveforms of the main devices



(b) Stage 1 (c) Stage 2



(d) Stage 3 (e) Stage 4

Fig. 4. Operation of the CCM during a period (T is the period and D is the duty ratio).

- *Stage 1* ($t_0 - t_1$): S_0 is turned on and D_0 becomes forward biased. The current i_{L_m} increases and i_{D_1} decays quickly since the magnetizing inductance is energized from the input voltage source. Similarly, C_s is charged by the source through D_0.
- *Stage 2* ($t_1 - t_2$): S_0 stays on. D_1 is reverse biased. The energy from the source is stored in L_m, L_p and C_s. C_1 and C_2 are discharged through the load.
- *Stage 3* ($t_2 - t_3$): at the time t_2, S_0 is turned off. The stored energy starts to charge the parasitic capacitor C_{ds} of S_0.
- *Stage 4* ($t_3 - t_4$): S_0 stays off. D_1 and D_2 conduct and D_0 is reverse biased. C_1 is charged through the secondary-side winding of L_C while C_2 is charged through C_s and L_C.

When S_0 conducts, the input voltage imposes across C_s and the magnetizing current increases by:

$$\Delta i_{L_m(0\sim DT)} = \frac{U_{in}}{L_m + L_p} DT \tag{1}$$

When S_0 is turned off, C_2 is charged by the input source via C_s and L_C. The loop voltage equation is given by,

$$U_{in} + U_{L_m} + U_{C_s(DT\sim T)} = U_{down} \tag{2}$$

where U_{L_m} is the primary side voltage of L_C, $U_{C_s(DT\sim T)}$ is the voltage across C_s, and U_{down} is the voltage across C_2.

The voltage ripple can be calculated by:

$$\Delta U_{C_s(DT\sim T)} = \frac{1}{C_s} \int_{DT}^{T} i_{D_2}\, \mathrm{d}t \approx \frac{(1-D)}{C_s f} I_{D_2} \tag{3}$$

where I_{D_2} is the average current flowing through D_2, and f is the switching frequency of S_0.

The ripple in the primary-side current of L_C is

$$\Delta i_{L_m(DT\sim T)} = \frac{U_{down} - U_{C_s(DT\sim T)} - U_{in}}{L_m + L_p}(1-D)T \tag{4}$$

Over one switching cycle, the net current change is zero in the inductor. Therefore,

$$\frac{U_{in}}{L_m + L_p} DT = \frac{U_{down} - U_{C_s(DT\sim T)} - U_{in}}{L_m + L_p}(1-D)T \tag{5}$$

The step-up ratio can be computed from the sum of upper- and lower-output voltages divided by the input voltage:

$$G = \frac{U_{dc}}{U_{in}} = \frac{U_{up} + U_{down}}{U_{in}} \approx \frac{2 - D + \frac{N_s}{N_p} D}{1 - D} \tag{6}$$

$$\frac{U_{down}}{U_{up}} = \frac{2 - D}{\frac{N_s}{N_p} D} \tag{7}$$

The voltage stress of S_0 can be expressed as:

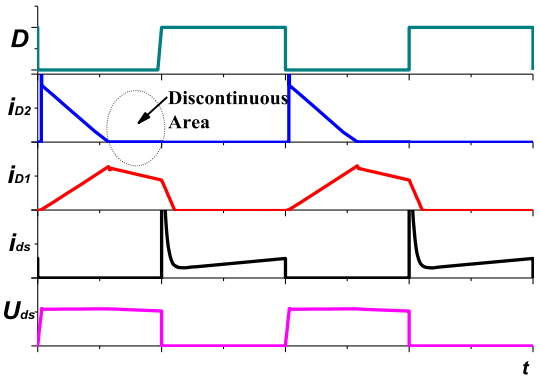
$$U_{ds} = U_{down} - U_{in} + U_{leak} \tag{8}$$

where U_{leak} is the leakage voltage.

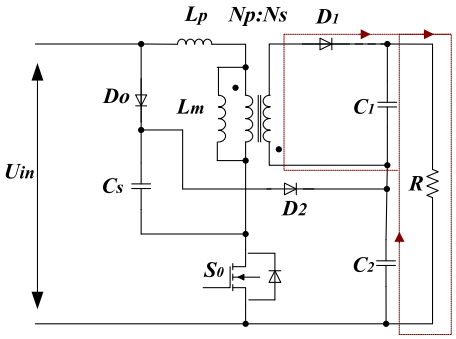
2.1.2. Discontinuous conduction mode

When S_0 is turned off, the upper output is in the CCM whilst the lower output is in the discontinuous conduction mode (DCM). Fig. 5(a) and (b) shows the voltage and current waveforms, and the current flow paths in the converter, respectively.

The DCM coefficient ζ can be found by,



(a) Waveforms of the main devices



(b) Current flow paths

Fig. 5. Operation of the DCM during a period.

$$\zeta = \frac{D_{iD_2} T}{(1-D)T} \tag{9}$$

where $D_{iD_2}T$ represents the conduction time for D_2.

In order to establish the relationship between the lower-output voltage and input voltage in the DCM, Eq. (10) can be derived from the volt-second balance.

$$\int_0^{DT} U_{in}\, \mathrm{d}t = \int_{DT}^{(D+D_{iD_2})T} \left(U_{down} - U_{C_s(DT\sim D_{iD_2}T)} - U_{in}\right) \mathrm{d}t \tag{10}$$

where $U_{C_s(DT\sim D_{iD_2}T)}$ is the bootstrap capacitor voltage.

The lower-output voltage gain for steady-state operation under the DCM can be derived from Eqs. (1), (9) and (10),

$$\frac{U_{down}}{U_{in}} = 2 - \frac{D}{\zeta(1-D)} \tag{11}$$

Similarly, the output voltage gain under the DCM is given by,

$$G = \frac{U_{dc}}{U_{in}} = 2 + \frac{\left(\frac{N_s}{N_p} - \frac{1}{\zeta}\right) D}{1 - D} \tag{12}$$

Because the off-state voltage of S_0 is clamped to $U_{down} - U_{C_s(DT-T)}$, the proposed DC–DC converter has a low voltage stress, low rated voltage and low conduction losses. More importantly, it can also generate double asymmetric output voltages (U_{up}, U_{down}). The ratio U_{down}/U_{up} is determined by the turn's ratio of L_C (as in Fig. 6) and the related control strategy. The turns ratio of the

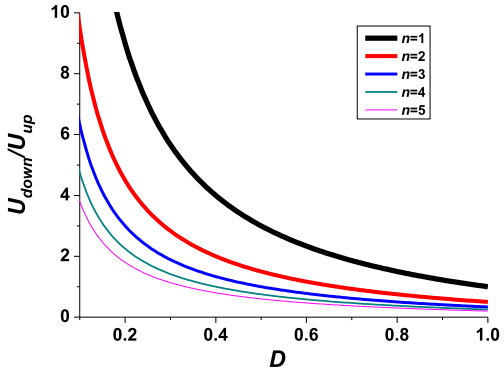


Fig. 6. U_{down}/U_{up} varied with turns ratio.

coupled inductor can be designed to manipulate the ratio U_{up}/U_{down}, which is the key to forming asymmetric multilevel voltages in the converter. For instance, if a low turns ratio is chosen, the duty ratio changing rate is low and so is the voltage gain suggested by Eqs. (7) and (12). In this paper, the turns ratio of the coupled inductor is chosen to be 3 to strike a balance between the voltage gain and the U_{up}/U_{down} ratio.

In effect, the PV module has both current-source and voltage-source characteristics [22]. Therefore, an input voltage control loop is employed to improve the system stability by controlling S_0 directly [22]. The input energy can be isolated from the grid-connected energy by the bus capacitor. In the proposed DC–DC converter, the dual asymmetrical output voltage is formed to generate multilevel outputs.

2.2. Three-level converter and line commutated bridge

With double asymmetric output voltages, a three-level converter can be realized by controlling S_1 and S_2 in a manner presented in Fig. 7. The bus voltage of 0, U_{up}, U_{down}, and $U_{up}+U_{down}$ can be obtained from the three-level converter and used as the input to the line frequency commutated bridge.

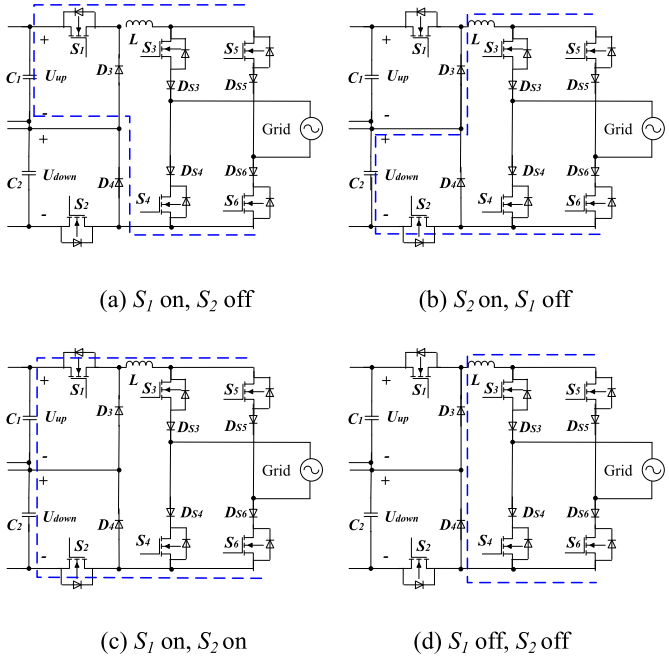


Fig. 7. Switching operation of the three-level DC–DC converter.

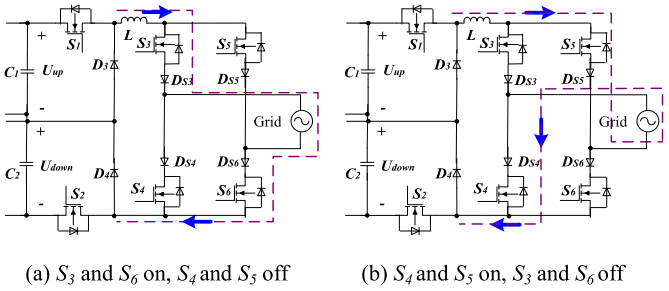


Fig. 8. Switching operation of the line frequency commutated bridge.

As for the bridge operation, S_3 and S_6 are turned on and S_4 and S_5 are off when the instantaneous grid voltage is greater than zero, as presented in Fig. 8(a). When the grid voltage is below zero, S_4 and S_5 are on and S_3 and S_6 are off, as in Fig. 8(b). Obviously, this topology removes the dead time as appeared in conventional voltage-source converters [23]. Because of the switch capacitor structure of the three-level converter, the voltage stress of S_1 is clamped to U_{up} and that of S_2 to U_{down}.

3. Grid-connected current control

Traditionally, the synchronized pulse-width modulation(SPWM) is widely used for cascade multilevel converters but it is not readily suited for asymmetric voltage inputs. The proposed converter has the same transfer function with the traditional Buck converter that has not right-half-plane zero [24]. In this work, hysteresis control is considered and modified since it has excellent closed-loop performance, system stability [25] and small phase lags.

The switching frequency for the hysteresis control is,

$$f_h = \frac{U_{dc}^2 - u_{grid}^2}{4HLU_{dc}} \tag{13}$$

where u_{grid} is the instantaneous line voltage, H is the hysteresis bandwidth. However, neither the hysteresis band nor the filter inductance can be largely altered to allow a low switching frequency. Thus, the bus voltage is controlled according to the instantaneous grid voltage, which provides a fast dynamic response and simple current regulation for grid connection.

The block diagram and the switching schemes of the hysteresis control are depicted in detail in Figs. 9 and 10, respectively. In Fig. 9, constant voltage control of the front-end DC–DC converter is

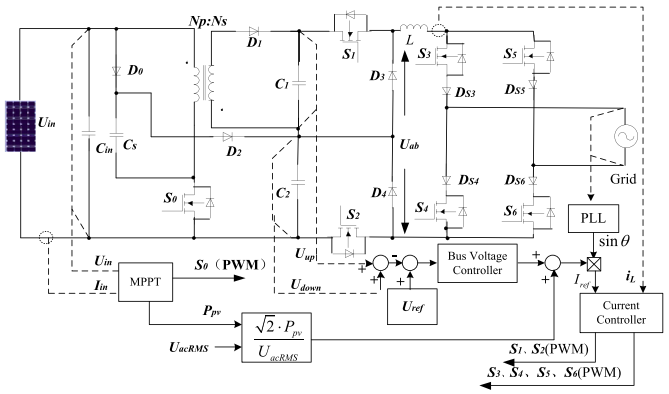


Fig. 9. Block diagram of the hysteresis control scheme.

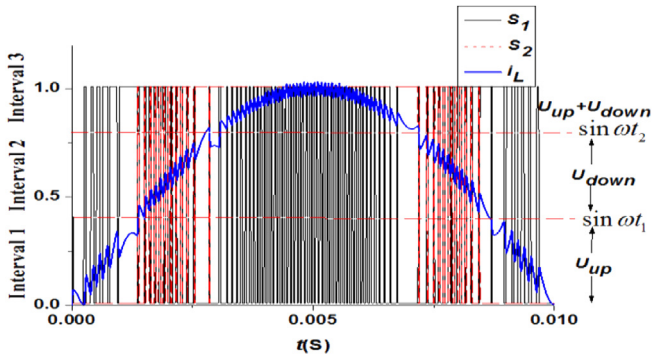


Fig. 10. S_1 and S_2 switching schemes and the voltage waveforms.

implemented to achieve the maximum power point tracking [26]; the input PV array energy is isolated from the grid-connected energy by the bus capacitors C_1 and C_2. The grid current reference I_{ref} is calculated from outputs of the PV power and the bus voltage controller. The DC-link capacitor voltage is fed back and compared with the reference voltage U_{ref}. The bus voltage controller provides proportional control to compensate the grid-connected current amplitude. By adjusting the grid current, the bus voltage can be controlled indirectly. The required current is calculated and updated in every line cycle for fast response.

In Fig. 10, it can be seen that the bus voltage is divided into three stages: 0 ~ U_{up}, U_{up} ~ U_{down}, U_{down} ~ (U_{up} + U_{down}). The edge of each stage is determined by t_1 and t_2. During the interval 0 ~ sin ωt_1 (ω is the line angular frequency), S_1 is chopping and S_2 is turned off. The bus voltage changes between 0 and U_{up}.

The maximum switching frequency of S_1 can be computed by:

$$f_{1\max} = \frac{U_{up}}{2HL} \tag{14}$$

When the grid voltage increases to U_{grid} sin ωt_1 (where U_{grid} is the amplitude of grid voltage), the switching event changes to the interval sin ωt_1 ~ sin ωt_2. That is, S_2 is chopping and S_1 is turned off. The bus voltage varies between U_{up} and U_{down}. The maximum switching frequency of S_2 is given by:

$$f_{2\max} = \frac{U_{down}^2 - \left(U_{grid} \sin \omega t_1\right)^2}{2HLU_{down}} \tag{15}$$

When the grid voltage reaches U_{grid} sin ωt_2, S_1 is chopping and S_2 stays on for the interval sin wt_2 ~ 1. The bus voltage changes between U_{down} and U_{dc}. The switching cycle of S_1 can be calculated by:

$$T_3 = \frac{2HL(U_{dc} - U_{down})}{\left(U_{dc} - U_{grid}\right)\left(U_{grid} - U_{down}\right)} \tag{16}$$

The switching frequency as a function of the graded voltage levels for the three-stage hysteresis control scheme is summarized in Table 1. It can been observed that the voltage difference at each stage in the three-stage hysteresis control is still high, making it difficult to further decrease the switching frequency variations. Thereby, a five-stage hysteresis control is proposed with a detailed switching scheme also given in Table 1. For this five-stage hysteresis control, the output voltages can be obtained between 0 ~ U_{up}, 0 ~ U_{down}, U_{up} ~ U_{down}, U_{up} ~ (U_{up} + U_{down}) and U_{down} ~ (U_{up} + U_{down}). For the three stage hysteresis control, 0 ~ U_{up}, U_{up} ~ U_{down}, and U_{down} ~ (U_{up} + U_{down}) can be attained.

Fig. 11(a) presents a comparison of the switching frequency between the traditional hysteresis control with full bridge topology and the five-stage hysteresis control scheme [27], under the same condition over one quarter of the cycle. Clearly, the five-stage control scheme has lower switching frequencies (5–35 kHz) than the traditional hysteresis control (30–80 kHz). This implies a relaxed switching requirement, less EMI and THD, and lower switching losses. Fig. 11(b) and (c) presents the switching devices junction temperatures in a half line-frequency cycle between the traditional hysteresis control and the proposed multi-stage hysteresis control. As can be seen that the switching frequency and the junction temperature by the proposed multi-stage hysteresis control are reduced which eases the heat sink design.

Table 1
Comparison of the 3- and 5-stage hysteresis control.

Control	Stage	S_1	S_2	Switching frequency
3-Stage	1	PWM	Off	$\frac{U_{up}^2 - U_{grid}^2}{4HLU_{up}}$
	2	Off	PWM	$\frac{U_{down}^2 - U_{grid}^2}{4HLU_{down}}$
	3	PWM	On	$\frac{(U_{dc} - U_{grid})(U_{grid} - U_{down})}{2HLU_{up}}$
5-Stage	1	PWM	Off	$\frac{U_{up}^2 - U_{grid}^2}{4HLU_{up}}$
	2	Off	PWM	$\frac{U_{down}^2 - U_{grid}^2}{4HLU_{down}}$
	3	PWM	PWM	$\frac{(U_{down} - U_{grid})(U_{grid} - U_{up})}{2HL(U_{down} - U_{up})}$
	4	On	PWM	$\frac{(U_{dc} - U_{grid})(U_{grid} - U_{up})}{2HLU_{down}}$
	5	PWM	On	$\frac{(U_{dc} - U_{grid})(U_{grid} - U_{down})}{2HLU_{up}}$

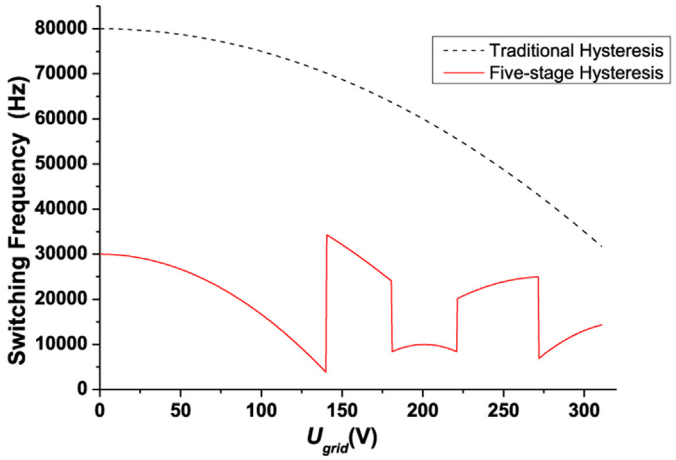
4. Simulation and experimental results

The proposed converter topology and control scheme are simulated in Matlab/Simulink environment and implemented in a 600 W prototype (see Fig. 12(a)). The PV array (Fig. 12(b)) includes six panels of the polycrystalline PV module controlled with a Texas Instruments TMS320F2812 controller. The specifications of the PV module and the converter are tabulated in Table 2. The coupled inductor is constructed from the Ferrites EE 40 magnetic material.

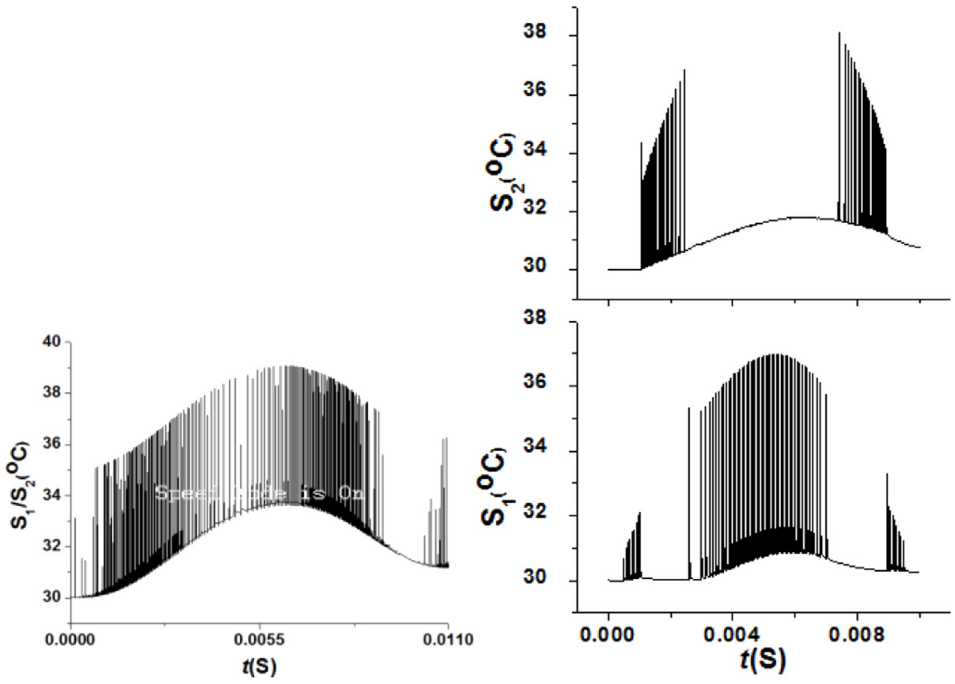
Matlab simulation results for the three-stage and five-stage hysteresis control schemes are demonstrated in Fig. 13 for comparison. Clearly, the five-stage hysteresis control scheme produces a much more balanced switching frequency distribution and output current distribution, and two more voltage stages than the three-stage control scheme, leading to improved thermal and EMI performance of the converter.

Fig. 14 shows the experimental results from the DC–DC converter with 49.3 V input, 220 V output and 0.4 duty ratio. The measured and calculated voltage gains are 4.46 and 4.66, respectively, which agree well with one another. Compared to the topologies presented in Refs. [7,10], the proposed topology can achieve a 38% and 23% higher voltage gain, respectively.

Fig. 15 presents the experiment results of multi-stage hysteresis control for comparison. Fig. 15(a) and (b) is for the traditional hysteresis and three-stage hysteresis control schemes, and Fig. 15(c)–(e) is for the five-stage control scheme. It is observed that the output current is approximately sinusoidal for five-stage hysteresis control with a lower current ripple (0.15 A) and an improved switching frequency distribution.

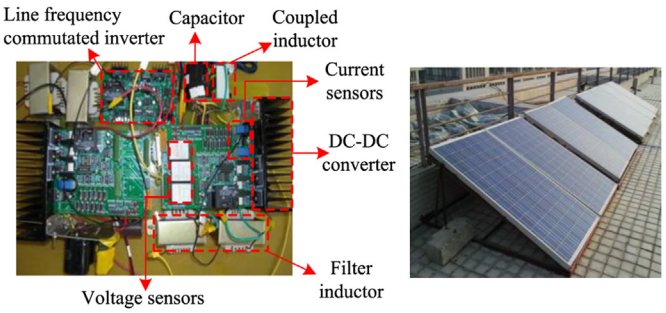


(a) Switching frequency



(b) Traditional hysteresis (c) Proposed hysteresis

Fig. 11. The switching frequency and junction temperature for the traditional and the proposed hysteresis control.



(a) The prototype converter. (b) The PV array

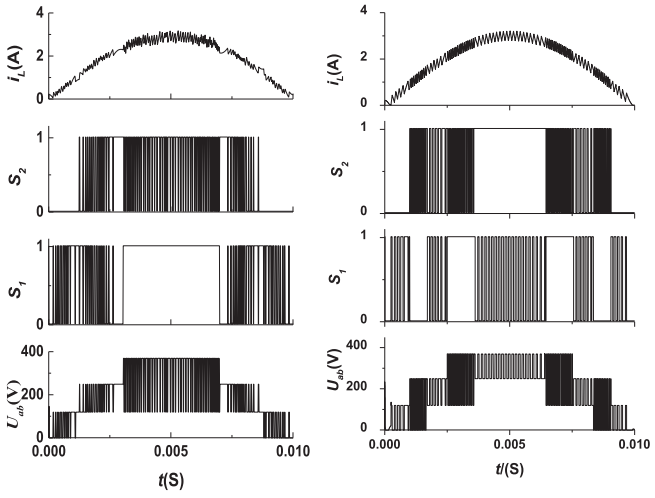
Fig. 12. Experimental setup.

The voltage U_{ab} in Fig. 15(d) presents four distinct voltage levels and thus the current is highly sinusoidal and synchronized well with U_{grid}. Fig. 15(e) shows the waveforms of the bus voltage, line current and lower-output voltage with 75 V input voltage. In this case, the voltage gain is 5.13, which proves the step-up capability of the proposed converter. The efficiency of the proposed converter at rated conditions is 94.4% which is higher than that for a similar five-level converter reported in Ref. [14].

Furthermore, a spectrum analysis using the fast Fourier transform (FFT) is carried out whose results are presented in Fig. 16 for comparison. The THD for the first 50 harmonic components in the output current is 6.8% under the traditional hysteresis control and 3.6% under the five-stage hysteresis control schemes. Again, this confirms that the improved scheme helps reduce the THD and improves the switching frequency distribution of the converter.

Table 2
Specifications OF PV module and converter.

Item	Parameter	Value
PV	Open voltage (V)	44.8
	Short current (A)	5.29
	MPP current (A)	5
	MPP voltage (V)	36
	Current temperature coefficient (%/°C)	0.037
	Voltage temperature coefficient (%/°C)	−0.34
	Power temperature coefficient (%/°C)	−0.48
Converter	Output power (W)	600
	Input voltage (V)	50–80
	Bus voltage (V)	380
	Sampling frequency (kHz)	20
	C_s (μF)	100
	C_1 and C_2 (μF)	450
	L (mH)	2.5
	Turns ratio of L_C	20:60
	Grid voltage/frequency	220 V/50 Hz
	D_0, D_1, D_2, D_3, D_4	600 V/30 A
	S_1, S_2, S_3, S_4, S_5, S_6	500 V/20 A
	D_{S_3}, D_{S_4}, D_{S_5}, D_{S_6}	600 V/25 A



(a) Three-stage hysteresis control. (b) Five-stage hysteresis control

Fig. 13. Simulation results for the two hysteresis control schemes.

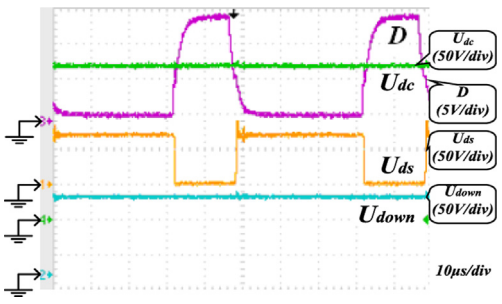
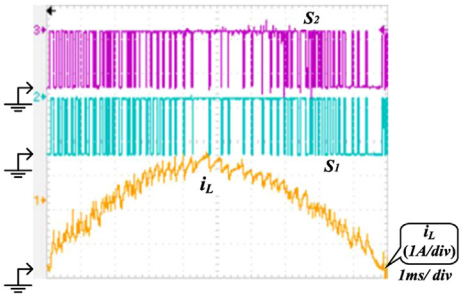
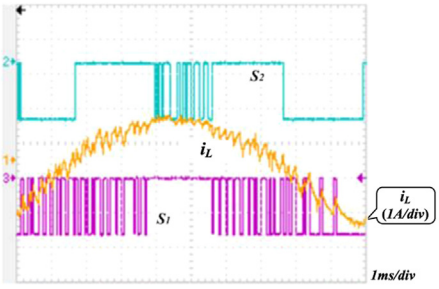


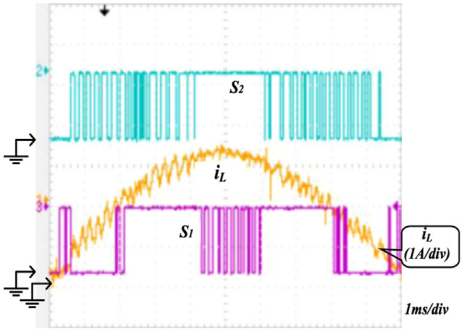
Fig. 14. Measured waveforms from the DC–DC converter.



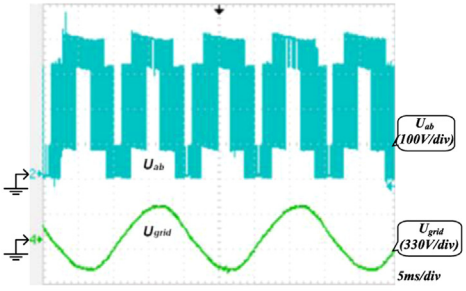
(a) Experimental results of traditional hysteresis control



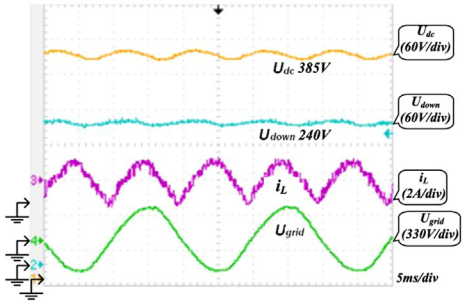
(b) Experimental results of the three-stage hysteresis control



(c) Experimental results of the five-stage hysteresis control

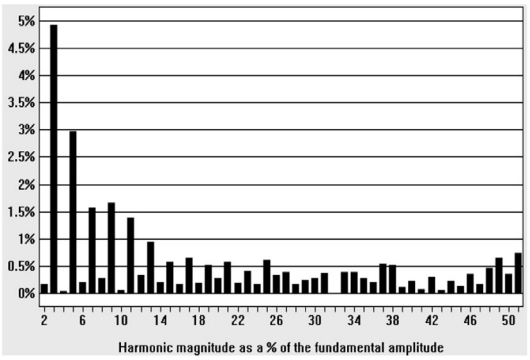


(d) Experimental results for the five-stage control

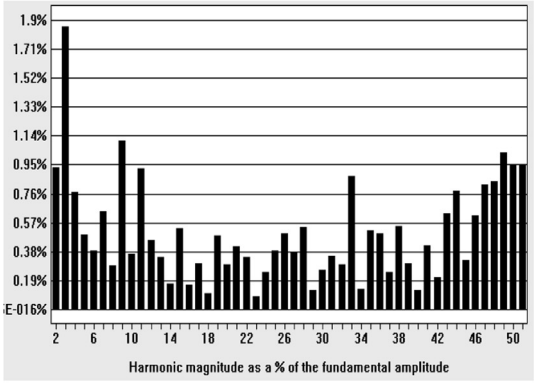


(e) Experimental results of the bus voltage, line current and voltage

Fig. 15. Measured waveforms from the hysteresis control schemes.



(a) Traditional hysteresis control



(b) Five-stage hysteresis control

Fig. 16. Harmonic analysis of the output current.

5. Conclusions

This paper has presented a new converter topology with an improved control scheme for grid-connected PV systems. The high step-up DC–DC converter is employed to provide a high voltage gain. A range of voltage levels can be attained from the converter with the proposed hysteresis control scheme. The effectiveness of the converter is validated by experiential tests on a 600 W prototype converter. The proposed converter topology with multi-stage hysteresis control has following features: (1) The asymmetrical high voltage output is realized by using one switch in the high step-up DC–DC converter; (2) The multilevel output is achieved by controlling two active switches; (3) Because of the multi-stage hysteresis control, the required switching frequency is significantly decreased and the output current quality is thus improved. (4) The developed photovoltaic systems are flexible, scalable and cost-effective, suited particularly for developing countries with low-voltage distributed-generation power networks.

References

[1] Yi H, Peng FZ, Jin W, Yoo DW. Survey of the power conditioning system for PV power generation. In: The 37th IEEE power electronics specialists conference; 2006. p. 1–6.
[2] Li Q, Wolfs P. A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations. IEEE Trans Power Electron May 2008;23(3):1320–33.
[3] Alam MK, Khan F, Imtiaz AM. Optimization of subcell interconnection for multijunction solar cells using switching power converters. IEEE Trans Sustain Energy April 2013;4(2):340–9.
[4] Alajmi BN, Ahmed KH, Finney SJ, Williams BW. A maximum power point tracking technique for partially shaded photovoltaic systems in microgrids. IEEE Trans Ind Electron April 2013;60(4):1596–606.
[5] Subudhi B, Pradhan R. A comparative study on maximum power point tracking techniques for photovoltaic power systems. IEEE Trans Sustain Energy Jan. 2013;4(1):89–98.
[6] Barrade P, Delalay S, Rufer A. Direct connection of supercapacitors to photovoltaic panels with on–off maximum power point tracking. IEEE Trans Sustain Energy April 2012;3(2):283–94.
[7] Zhao Q, Lee FC. High-efficiency, high step-up DC–DC converters. IEEE Trans Power Electron Jan. 2003;18(1):65–73.
[8] Kjaer SB, Pedersen JK, Duan RY. A review of single-phase grid connected inverters for photovoltaic modules. IEEE Trans Ind Appl Sep/Oct. 2005;41(5):1292–369.
[9] Wai RJ, Lin CY, Duan RY, Chang YR. High-efficiency DC–DC converter with high voltage gain and reduced switch stress. IEEE Trans Ind Electron Feb. 2007;54(1):354–64.
[10] Ismail EH, Al-Saffar MA, Sabzali AJ, Fardoun AA. A family of single-switch PWM converters with high step-up conversion ratio. IEEE Trans Circuits Syst May 2008;55(4):1159–71.
[11] Zhao Z, Xu M, Chen Q, Lai JS, Cho Y. Derivation, analysis, and implementation of a boost-buck converter-based high-efficiency PV inverter. IEEE Trans Power Electron Mar. 2012;27(3):1304–13.
[12] Chen SM, Liang TJ, Yang LS, Chen JF. A safety enhanced, high step-up DC–DC converter for ac photovoltaic module application. IEEE Trans Power Electron Apr. 2012;27(4):1809–17.
[13] Monge SB, Rocabert J, Rodríguez P, Alepuz S, Bordonau J. Multilevel diode-clamped converter for photovoltaic generators with independent voltage control of each solar array. IEEE Trans Power Electron July 2008;55(7):2713–23.
[14] Rahim NA, Selvaraj J. Multistring five-level inverter with novel PWM control scheme for PV application. IEEE Trans Ind Electron June 2010;57(6):2111–23.
[15] Chavarria J, Biel D, Guinjoan F, Meza C, Negroni JJ. Energy-balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs. IEEE Trans Ind Electron Jan. 2013;60(1):98–111.
[16] Buso S, Fasolo S, Malesani L, Mattavelli P. A dead-beat adaptive hysteresis current control. IEEE Trans Ind Appl July/Aug. 2000;36(4):1174–80.
[17] Mao X, Ayyanar R, Krishnamurthy HK. Optimal variable switching frequency scheme for reducing switching loss in single-phase inverters based on time-domain ripple analysis. IEEE Trans Power Electron Apr. 2009;24(4):991–1001.
[18] Lopez-Lapena O, Penella MT, Gasulla M. A closed-loop maximum power point tracker for subwatt photovoltaic panels. IEEE Trans Ind Electron March 2012;59(3):1588–96.
[19] Ho CN, Cheung VSP, Chung HS. Constant-frequency hysteresis current control of grid-connected VSI without bandwidth control. IEEE Trans Power Electron Nov. 2009;24(11):2484–95.
[20] Stefanutti W, Mattavelli P. Fully digital hysteresis modulation with switching-time prediction. IEEE Trans Ind Appl May/June 2006;42(3):763–9.
[21] Corzine KA. A hysteresis current-regulated control for multi-level drives. IEEE Trans Energy Convers Jun. 2000;15(2):169–75.
[22] Nousiainen L, Puukko J, Mäki A, Messo T, Huusari J, Jokipii J, et al. Photovoltaic generator as an input source for power electronic converters. IEEE Trans Power Electron Jun. 2013;28(6):3028–38.
[23] Liu Y, Ge B, Abu-Rub H, Peng FZ. Control system design of battery-assisted quasi-Z-source inverter for grid-tie photovoltaic power generation. IEEE Trans Sustain Energy Oct 2013;4(4):994–1001.
[24] Erickson RW, Maksimovic D. Fundamentals of power electronics. Springer; 2001.
[25] Park JH, Cho BH. Small signal modeling of hysteretic current mode control using the PWM switch model. IEEE COMPEL Workshop, New York, USA; 2006. p. 225–30.
[26] Mutoh N, Ohno M, Inoue T. A method for MPPT control while searching for parameters corresponding to weather conditions for PV generation systems. IEEE Trans Ind Electron Nov. 2006;53(4):1055–65.
[27] Hu Y, Deng Y, Liu Q, He X. Asymmetry three-level grid-connected current hysteresis control with varying bus voltage and virtual over-sample method. IEEE Trans Power Electron Jun. 2014;29(6):3214–22.