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BROADER PERSPECTIVE

Techno-economic analysis of three different substrate removal and reuse strategies for III-V solar cells

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ABSTRACT

The high cost of wafers suitable for epitaxial deposition of III-V solar cells has been a primary barrier to widespread use of these cells in low-concentration and one-sun terrestrial solar applications. A possible solution is to reuse the substrate many times, thus spreading its cost across many cells. We performed a bottom-up techno-economic analysis of three different strategies for substrate reuse in high-volume manufacturing: epitaxial lift-off, spalling, and the use of a porous germanium release layer. The analysis shows that the potential cost reduction resulting from substrate reuse is limited in all three strategies—not by the number of reuse cycles achievable, but by the costs that are incurred in each cycle to prepare the substrate for another epitaxial deposition. The dominant substrate-preparation cost component is different for each of the three strategies, and the cost-ranking of these strategies is subject to change if future developments substantially reduce the cost of epitaxial deposition. Copyright © 2016 John Wiley & Sons, Ltd.

KEYWORDS

photovoltaics; III-V; substrate; reuse

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1. INTRODUCTION

Solar cells based on III-V compound semiconductors have attained the highest reported efficiency of any photovoltaic devices to date. A number of different approaches for designing and fabricating these devices have yielded efficiencies in excess of 45% under concentrated sunlight [1–3]. However, high cell cost has limited their use to high concentration, space power systems, or other specialized applications [4].

The market demand for III-V solar cells could be substantially increased if the cost of these cells was reduced to a level suitable for low-concentration or one-sun applications. Figure 1 illustrates the breakdown of the cost elements that would compose a simple GaAs solar cell if today's state-of-the-art techniques were scaled up to high-volume manufacturing [5]. As shown, the cost of the substrate dominates over the metal-organic chemical vapor phase epitaxy and device processing. Significant cost reduction requires that the expensive substrate—either GaAs or Ge—not be incorporated into the finished device. Therefore, we examine the costs associated with three different substrate removal and reuse strategies that are currently being explored for high-quality III-V epitaxial crystal growth. These strategies are epitaxial lift-off (ELO), spalling, and the use of a porous-Ge release layer.

This analysis will focus solely on the costs directly associated with the steps necessary to remove the device epi-layers from the parent substrate and return that substrate to a condition suitable for regrowth of additional device structures. Costs associated with the deposition of the device layers, processing these device layers into practical working solar cells, and attachment of the thin layer to a mechanical handle are not considered here.

Costs are computed using National Renewable Energy Laboratory's bottom-up methodology, discussed in detail in [5,6]. This approach involves first mapping out a representative manufacturing process flow that would be suitable for high-volume manufacturing and then computing the materials, labor, utilities, equipment, facilities costs, and yield loss associated with each step. Input data are gathered from equipment vendors, material suppliers, and

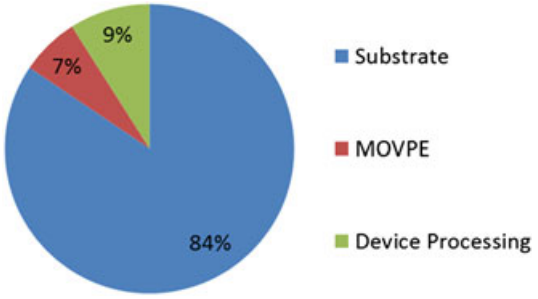

Figure 1. Cost breakdown for a simple GaAs solar cell without substrate reuse. The total cost per 150-cm^2 cell is \$200 if the yield is 90% [5]. MOVPE, metal-organic chemical vapor phase epitaxy.

photovoltaics industry members. This entails gathering enough information to complete a cost of ownership calculation for each step in the process flow. In addition to these individual step costs, we include costs associated with labor and equipment required between steps (i.e., for transferring material between machines) based on industry feedback on total labor rates and total capital equipment expense. In the event that a process has not yet been implemented in the industry (as is the case for some of the reuse methods discussed here), such that there is little information on tool costs or industry cycle times, we use a combination of literature and data for analogous tools or processes to construct the model. All costs are adjusted as necessary to correspond to 2015 US dollars.

In the following sections, we present specific assumptions regarding the constraints for each reuse technique, manufacturing process flows for each case, and the associated costs. All costs are per cell. Each cell is assumed to be a 125-mm pseudo-square fabricated from a 150-mm-diameter crystalline substrate wafer, as would be appropriate for low-concentration or one-sun applications. Such substrates (whether GaAs or Ge) are projected to cost \$150 per wafer in high volume [5].

2. EPITAXIAL LIFT-OFF

Epitaxial lift-off refers to a technique that exploits the selective wet etching chemistry of III-V compounds to remove a thin release-layer that is deposited on the substrate prior to epitaxial growth of the device structure. As early as 1978, the extreme etch selectivity of AlGaAs relative to GaAs in hydrofluoric acid was used in this manner to remove GaAs films from their parent substrates [7]. The primary challenge to making ELO a viable commercial technology centers around the etching properties of the release layer and the condition of the substrate after the etch process is complete.

Etching of the thin release layer tends to be mass-transport limited. The reaction can be slow and sometimes stops prematurely, making lift-off from full wafers difficult. An early solution to this problem involved covering the surface of the epitaxial film with black wax, creating stress that curls or peels the film, opening up the etch front and allowing the etch to continue [8]. This method is best suited to lab-scale processes. In recent years, process tapes and flexible, temporary handles have been employed that lend themselves to scale up and automation [9]. Tooling has been created that can apply these materials and perform the lift-off in batch processes. Future improvements in transporting the reactants to and from the etch site could potentially eliminate the need for a peeling apparatus, allowing wafers to be stacked in cassettes while the etch proceeds [10]. However, the ELO of films from full GaAs wafers is a process that is measured in hours [11] and would likely remain so.

Epitaxial films grown on recycled substrates (after the epi-layers are removed) suffer from high dislocation density because of surface roughness unless protective layers are deposited as part of the structure [12]. Even with these layers, chemo-mechanical polishing (CMP) may be required to prepare the surface for high-quality epitaxy. We consider two scenarios: one with CMP after every reuse cycle and one with CMP after every 10 reuse cycles. Even less frequent use of CMP may be considered, but this does not substantially reduce cost.

Epitaxial lift-off techniques have been implemented in industry at small scale, for example by MicroLink Devices and Alta Devices. Because these companies use proprietary processes for the lift-off, publicly available information on these systems and their capabilities is lacking. Therefore, we constructed a process flow based on available literature [9–15]. The process flow associated with removing the epitaxially grown device layers from the parent substrate and returning that substrate to a condition suitable for subsequent growth is illustrated in Figure 2.

We model the ELO station after a patent application filed by Alta Devices [15]. It is a one-step, integrated, mechanized process tool whereby a temporary handle or tape is applied to the substrate as it is moved on a conveyor into the chemical etching bath. This system is configured in such a way as to provide the upward force on the tape or handle necessary to facilitate the peeling function during lift-off. The etch rate for this process depends greatly on how much stress is applied to the substrate. Reported etch rates range from 0.3 to 30 mm/h, though a high risk of breakage was noted at the high end of this range [11]. We use 7.5 mm/h in our model, this being the median of the four etch rates mentioned in the Alta Devices patent application. This gives an etch time of 10 h for 150-mm-diameter wafers, which means that a large area of the production facility must be dedicated to the etch baths. We estimate that the ELO station would have a capital cost per square meter of footprint that is similar to high-throughput wet-etch tools currently used in silicon solar cell production. Maintenance cost for this tool is assumed to scale with the capital cost. However, the cost of operator labor and consumables is assumed to be no greater than for the smaller etch tools used in silicon solar cell production.

The key cost inputs for this process flow are listed in Table I. The resultant cost per cell is illustrated in

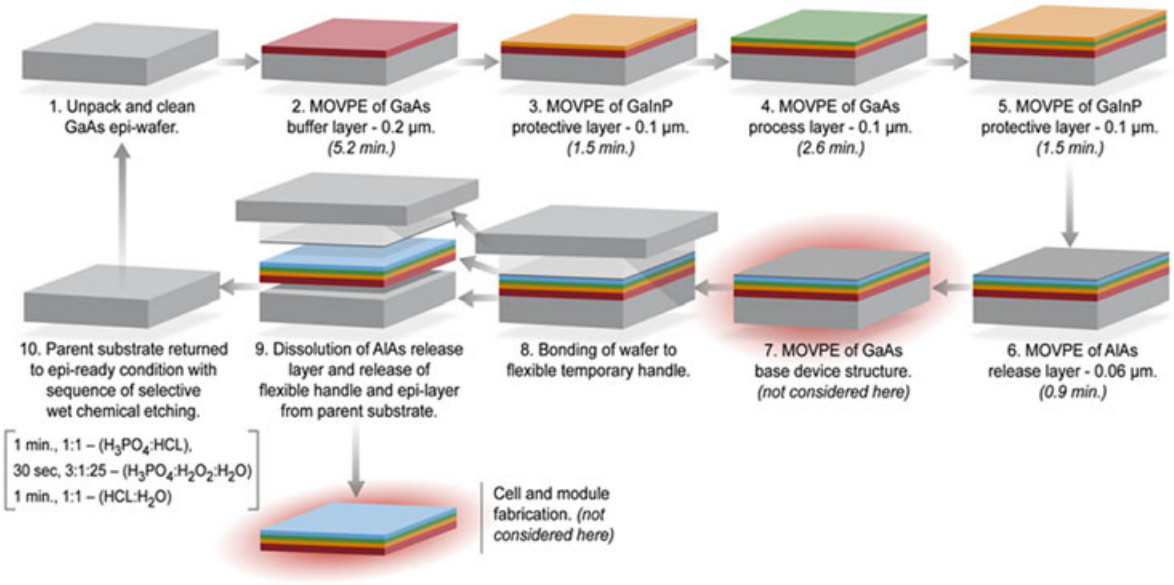

Figure 2. Process flow for substrate reuse using epitaxial lift-off. Chemo-mechanical polishing (not shown) is inserted after the last step when it is included in the cycle. MOVPE, metal-organic chemical vapor phase epitaxy.

Table I. Key cost inputs for ELO.

Cost element	Cost basis
ELO station capital cost	\$50 k per m^2 of tool
ELO etch time	10 h
Chemo-mechanical polish (one sided)	\$11 per wafer
Cladding layers (0.2 µm GaInP, 0.3 µm GaAs, and 60 nm AlAs)	\$2 per wafer

ELO, epitaxial lift-off.

Figure 3 for the two options regarding the use of CMP. The cost per cell is a strong function of the number of times the substrate can be reused—up to about 30 reuses. Beyond that, the costs associated with the substrate are dominated by the residual costs incurred in preparing the substrate for reuse after each cycle. In the case where CMP is used in every reuse cycle, the cost of CMP dominates the residual cost of the process. In the case where the frequency of CMP is reduced to every 10 cycles, the CMP cost is reduced substantially, to well below the cost of depositing the cladding layers (steps 2–6 in Figure 2).

In a future where the cost of CMP and the cost of depositing the protective layers are both substantially lower, the substrate-related cost per cell would be dominated by the cost of the substrate itself up to a much larger number of reuse cycles. Factors that will ultimately limit the number of times a substrate can be reused are presented in the Section 5.

3. SPALLING

To spall is to chip, fragment or flake. Spalling has been studied for many years as a failure mechanism in civil and structural engineering. However, it was not until the 1980s that an analytical framework for understanding the mechanics of substrate spalling was clarified [16]. This work opened up the possibility of controlled spalling for use in manufacturing. The physical mechanism exploited is one in which a stressor layer that is deposited on a brittle substrate can generate two stress modes. One is a tensile stress perpendicular to the surface and the other is a shear stress parallel to the surface. The perpendicular mode is relaxed with the initiation of a crack extending to the depth below the film/substrate interface where the shear field is zero. At this point, the crack propagates approximately parallel to the surface because the stress increases if the crack deviates from this depth, either up or down. There is thus a direct relationship between the thickness of the layer that is spalled off of a substrate and the stress in the deposited stressor layer [17].

Controlled spalling from a semiconductor substrate is a recent innovation in comparison with the ELO technique previously described. One of the first successful attempts to spall a thin layer from a Si substrate was reported in 2007 [18]. More recently, others have advanced the state of the art by developing techniques applicable for Ge and III-V substrates [19]. In the research environment, III-V devices have been fabricated on spalled epi-layers. These devices demonstrated nearly identical performance characteristics when compared with control devices that remained on the parent substrate after growth [20].

Spalling is attractive for manufacturing because it is a relatively fast process. However, spalling for substrate reuse has several issues that need further investigation. The application of the stressor layer requires an additional manufacturing step, such as electrodeposition of a nickel film, which must be very uniform over the full wafer.

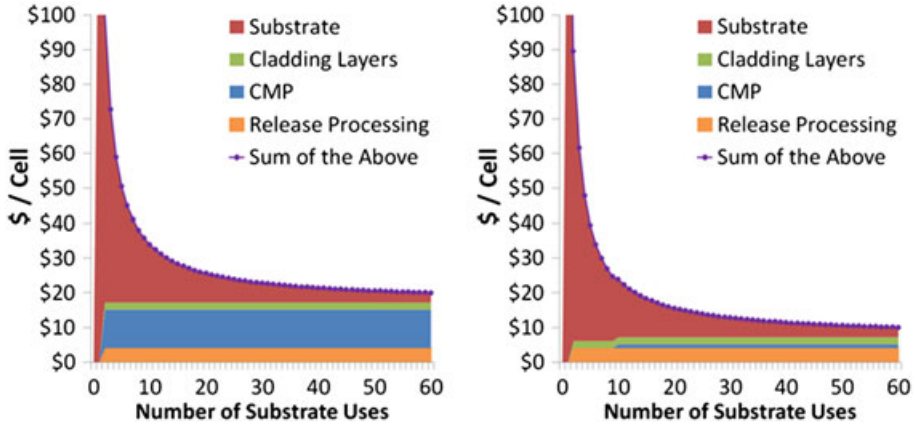

Figure 3. Cost of substrate reuse per cell using epitaxial lift-off with (a) chemo-mechanical polishing (CMP) after each cycle or (b) CMP after every 10 cycles.

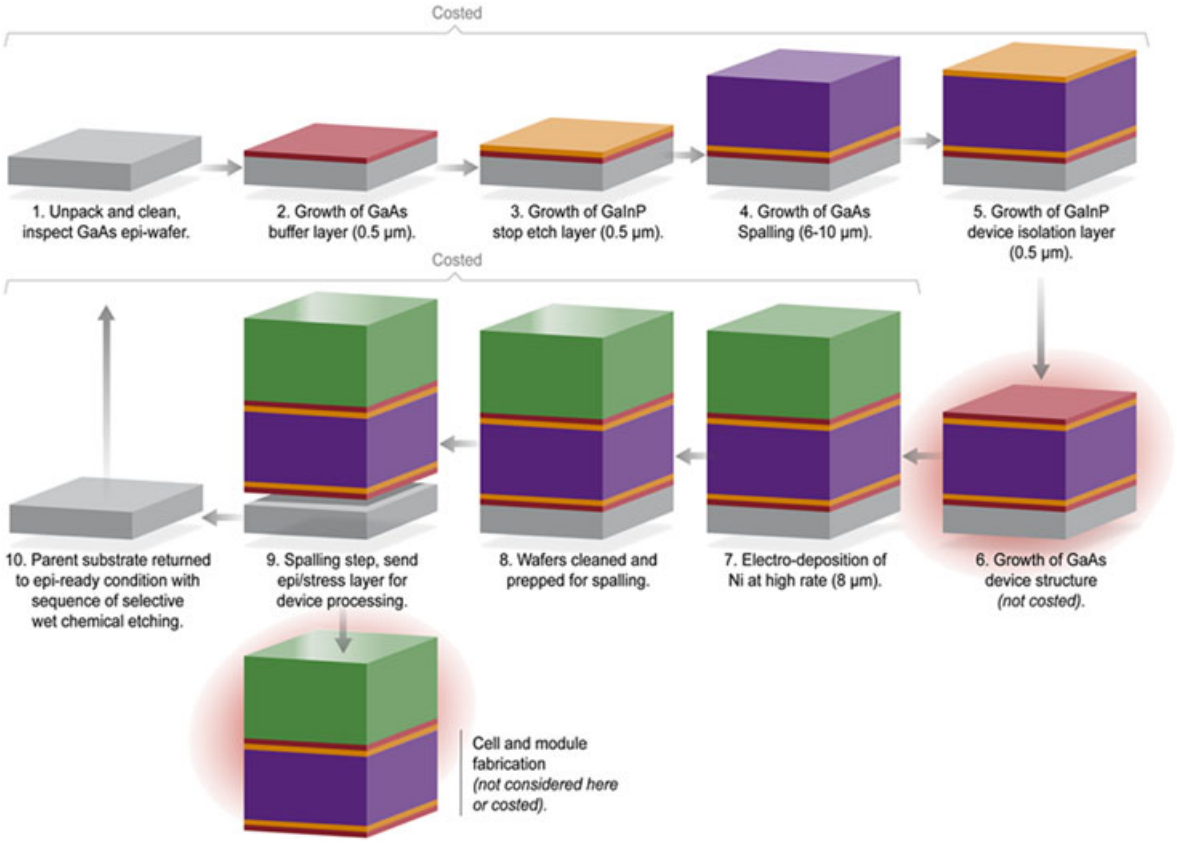

Figure 4. Process flow for substrate reuse using spalling. The protective layers shown in steps 2 and 3 can be omitted if chemo-mechanical polishing is used after every reuse cycle.

Additionally, the lateral crack formed by the act of spalling is problematic for the <100> crystallographic orientation of GaAs normally used for device deposition, because the natural cleavage planes in GaAs are <110>. The unstable nature of the fracture along this plane requires the growth of a "spalling buffer layer," typically 6–10 µm thick, to encompass the roughness of the spall and thus avoid excessively reducing the wafer thickness in each reuse cycle [21]. CMP could be used after every reuse cycle to return the substrate to epi-ready condition. Alternatively, protective layers may be deposited prior to the spalling buffer layer to reduce the frequency of CMP to only every 5 or 10 reuse cycles. Using protective layers to avoid CMP is expected to be more challenging with spalling than with

ELO, because of the irregular roughness that occurs near the wafer edges where the spalling crack is initiated.

In our model process flow, shown in Figure 4, we assume the stressor layer consists of nickel that is electrodeposited at a high rate using an inexpensive electrolyte. The spalling station is a mechanical roller-type apparatus. A handle tape is fed onto the roller with a sleeve, and the substrate, epi-side up, comes through on a conveyor and slides under the roller. The stressor layer and film are then spalled off of the substrate onto the handle tape. The sleeve, tape, and film are ejected from the roller, and the bare substrate is transferred to the steps required to prepare it for regrowth.

The key cost inputs for this process flow are listed in Table II. The resultant cost per cell is illustrated in Figure 5. Because of the high cost of depositing the thick spalling layer, the cost per cell approaches its lower bound after only about 20 reuse cycles.

Spalling is a comparatively new approach, so there are many potential opportunities for savings as the technique matures. For example, we assume GaAs substrates with <100> surface orientation because the highest efficiency III-V cells are grown on such wafers. This has typically necessitated the inclusion of the expensive GaAs spalling buffer layer, but the spalling layer could possibly be Ge, which might give a smoother spall. Alternatively, Ge substrates could possibly be used to avoid the need for a spalling buffer layer altogether.

Table II. Key cost inputs for spalling.

Cost element	Cost basis
Spalling station (1 wafer per second)	\$2m per tool
Chemo-mechanical polish (one-sided)	\$11 per wafer
Protective layers (0.5 µm GaInP and 0.5 µm GaAs)	\$4 per wafer
Spalling buffer layer (8 µm GaAs)	\$12 per wafer
Device isolation layer (0.5 µm GaInP)	\$3 per wafer

4. POROUS GE RELEASE LAYER

Porous Ge as a release layer is the least mature of the three technologies under consideration in this analysis; it has never been successfully used to produce an efficient III-V solar cell. This process was originally proposed as a way to reduce the weight of high efficiency multijunction GaInP/GaAs/Ge cells used in space applications, where watts per gram is a key specification [22]. The basic concept is to use electrochemical etching to create a mesoporous layer of Ge that is mechanically weak enough to act as a release layer. The surface of this mesoporous layer can be reconstructed with a thermal annealing step, resulting in a single-crystal surface potentially suitable for III-V epitaxy. This approach was first demonstrated with Si by Canon in 1994 [23], and a few years later, it was applied to Si photovoltaics at Institute for Solar Energy Research Hamelin in Germany [24].

The group at Institute for Solar Energy Research Hamelin subsequently applied their porous-etching process to Ge wafers. It was possible to reconstruct a continuous monocrystalline Ge surface after a heat treatment in a hydrogen atmosphere [25]. However, attempts to epitaxially grow GaAs on this surface resulted in a microcrystalline structure, and no functional solar cells were produced [26]. The interpretation given was that the reconstructed surface was too rough for device-quality III-V growth. We therefore conclude that it is necessary to polish the Ge surface after reconstruction, prior to epitaxial III-V deposition.

We have combined an understanding of the well-developed porous-Si process with what is known from laboratory work on porous-Ge release layers to construct our model process flow shown in Figure 6.

The process begins with a <100> Ge wafer. It is subject to an electrochemical porous etching process like that described in [26,27]. The first 2 µm of the wafer surface is reduced to a mesoporous condition. An annealing step at 600°°C in H_2 reconstructs the surface, upon which 5 µm of epitaxial Ge can be grown by chemical vapor

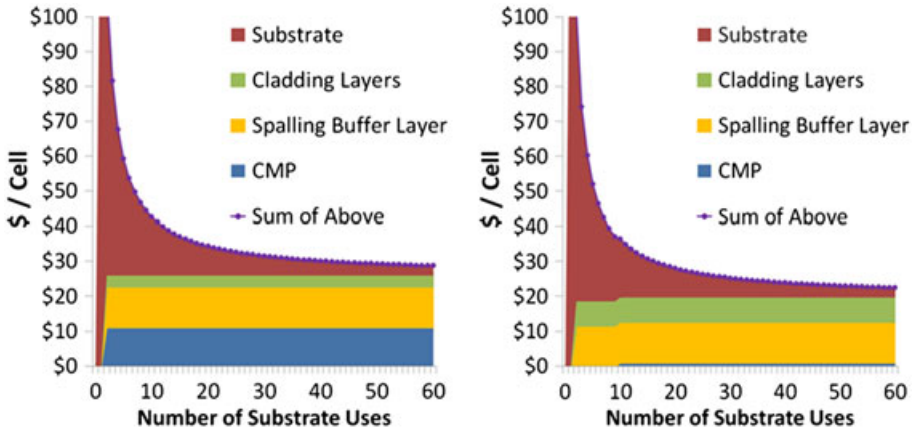

Figure 5. Cost of substrate reuse per cell using spalling with (a) chemo-mechanical polishing (CMP) after each cycle or (b) CMP after every 10 cycles.

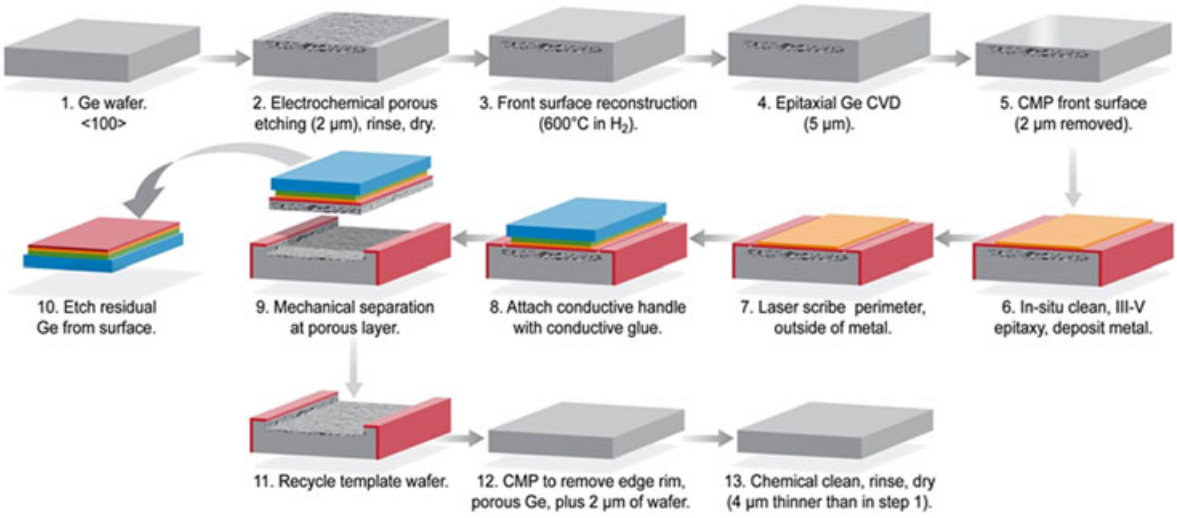

Figure 6. Process flow for substrate reuse using porous Ge as a release layer. CMP, chemo-mechanical polishing; CVD, chemical vapor deposition

deposition, enough to accommodate the subsequent CMP step that is needed to make the surface smooth enough for high-quality III-V epitaxy.

The standard approach for the porous etching is using an O-ring arrangement that electrically isolates one surface of the wafer from the other, forcing current in the electrolyte to pass directly through the wafer. This means that the perimeter of the wafer protected by the O-ring will not be etched, leading to an unavoidable thickness variation. Even so, this edge rim is probably necessary to stabilize the edges of the epitaxial Ge layer so that it does not release prematurely during the CMP step that occurs prior to III-V deposition.

Laser scribing around the perimeter is necessary to separate the epi-layer from the unetched perimeter rim. The layer release itself is assumed to be a simple mechanical separation using vacuum suction. The rim created by the O-ring, along with the damage inflicted by the laser scribing, requires that the wafer be planarized using CMP prior to reuse. The model process flow for porous Ge thus includes two CMP steps per reuse cycle.

The key cost inputs for this process flow are listed in Table III. The resultant cost per cell is illustrated in Figure 7. Because of the inclusion of two CMP steps-per-reuse cycle, the cost per cell approaches its lower bound after only about 20 reuse cycles.

The two CMP steps alone contribute $22 to the cell cost (including yield loss). Avoiding CMP should be a high priority for any effort to reduce the cost of this approach.

Table III. Key cost inputs for porous Ge.

Cost element	Cost basis
Chemo-mechanical polish (one-sided)	$11 per wafer per step
Chemical vapor deposition of epitaxial Ge (5 μm)	$1 per wafer

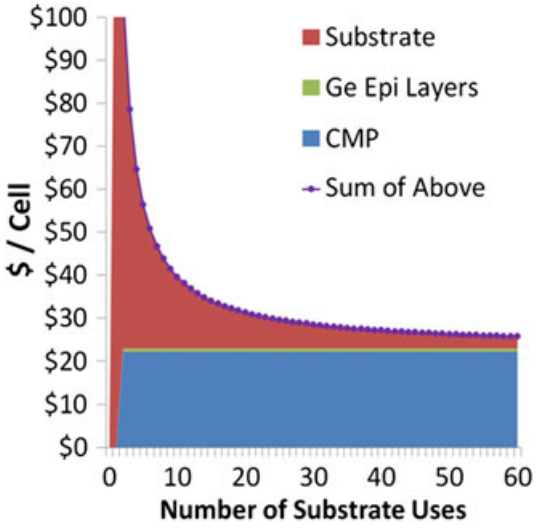

Figure 7. Cost of substrate reuse per cell using porous Ge. CMP, chemo-mechanical polishing.

Additionally, because about 4 μm of the substrate material is consumed during each cycle, the number of potential substrate reuses is more limited than with the other two approaches, as discussed further in the following section.

5. DISCUSSION

All of the cost parameters used in this study are uncertain, so each parameter in the model was varied to see how it would affect the substrate cost. By far, the greatest effects were the number of reuse cycles and the frequency of CMP. Table IV shows the cost associated with the substrate for 10, 20, 50, and 100 reuse cycles when applying each of the substrate reuse methods discussed here. These

Table IV. Cost per cell for each reuse strategy as a function of substrate reuse cycles (values in parentheses assume negligible cost for epitaxial deposition).

Reuse strategy	10 times	20 times	50 times	100 times
ELO with CMP every cycle	$34 ($32)	$26 ($24)	$21 ($18)	$19 ($17)
ELO with CMP every 10 cycles	$24 ($22)	$16 ($13)	$11 ($8)	$9 ($7)
Spalling with CMP every cycle	$43 ($28)	$35 ($20)	$30 ($15)	$28 ($13)
Spalling with CMP every 10 cycles	$37 ($18)	$28 ($10)	$23 ($5)	$22 ($3)
Porous Ge with two CMP per cycle	$40 ($39)	$32 ($31)	$27 ($26)	$25 ($24)

CMP, chemo-mechanical polishing; ELO, epitaxial lift-off.

Table V. Factors limiting the number of substrate reuse cycles (most restrictive limitation for each method is shown in bold).

Cycle limitation	GaAs/ELO	GaAs/spalling	Porous-Ge
Accumulation of dislocations	Not expected to be a limitation. Undoped substrate is recommended to minimize formation of dislocation loops.		This has not been a significant limitation in Si epitaxy on porous surfaces, so not expected for Ge.
Wafer gets too thin to reuse	Assume 400 μm starting thickness, can thin to 300 μm. With 2 μm removed per CMP. Reuse limited to 50 times cycles-per-CMP.	Like ELO, because spalling buffer layer avoids excessive thinning. Reuse limited to 50 times cycles-per-CMP.	Assume a starting thickness of 500 μm, remove 4 μm per cycle, thin to 300 μm. Reuse limited to 50 times.
Wafer is broken or chipped in handling and/or thermal cycling.	Expect only 1% mechanical yield loss per full process cycle because of gentle chemical processing. Average reuse cycles limited to ~100.	Compared with ELO, spalling is mechanically stressful. Assume yield loss double that of ELO. Average reuse cycles limited to ~50.	Ge is not as fragile as GaAs, but the layer release is a mechanically harsh process. Average reuse cycles limited to ~50–100.
Excessive bowing of wafer	Expected to be acceptable if CMP is used after every 10 or fewer cycles.		Bowing is not observed in Si, thus not expected for Ge.
Accumulation of wafer contamination	Not expected to be a limitation because GaAs is relatively tolerant of chemical impurities.		Expected to be acceptable because the substrate is cleaned in every cycle.
Excessive spatial thickness variability	Expected to be acceptable if CMP is used after every 10 or fewer cycles.		

CMP, chemo-mechanical polishing; ELO, epitaxial lift-off.

figures compare with a cost of $165 per wafer ($150 direct wafer cost plus $15 for yield loss) in the absence of substrate reuse. In this table, the values shown in parentheses apply if, in the future, the cost of epitaxial deposition is substantially reduced, as would be necessary for III-V cells to be cost competitive for low-concentration or one-sun applications. This reduced deposition cost especially reduces the cost for spalling, because that approach includes a thick epitaxial deposition.

The cost benefit of multiple reuses raises the important question of how many reuses are ultimately feasible in a manufacturing environment. Table V lists several factors that can limit the number of reuse cycles for each of the three approaches. Substrate thinning appears to be the dominant limitation for porous Ge, while wafer breakage appears to be the limiting factor for ELO and spalling. It seems unlikely that more than 50 reuse cycles can be consistently obtained using spalling or porous Ge, while ELO has the potential for up to 100 reuse cycles.

Even in a future where the cost of epitaxial deposition is substantially reduced (values shown in parentheses in Table IV), none of these substrate reuse methods approach the low cost of silicon wafers (about $1 per wafer). The other residual cost elements identified in this study will also need to be substantially reduced or avoided altogether if III-V cells are to be cost-competitive with silicon for low-concentration or one-sun applications.

In the meantime, substrate reuse might be a viable way in the relatively near term to reduce the cost of III-V solar cells for use in high-concentration systems. In such systems, high cell cost is accommodated by increasing the concentration ratio, but this incurs an additional cost to maintain high-tracking accuracy. Lower-cost cells would reduce the optical concentration ratio required and thereby reduce total system cost. Note that efficiency is a key parameter for such systems, so it is essential that substrate reuse not reduce the cell efficiency.

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6. CONCLUSIONS

We began our investigation of this topic with a consideration of the primary cost elements that compose a III-V solar cell. In that analysis, it was noted that the major cost is associated with the substrate, which was then the focus of this paper.

We performed a bottom-up techno-economic analysis of three different strategies for substrate reuse as a way of reducing the substrate cost per cell. We considered an ELO approach, spalling, and the use of a porous Ge release layer. The key results are summarized in Table IV. The analysis shows that extensive reuse of the substrate does not eliminate the cost associated with the substrate, because there are substantial costs incurred in preparing the substrate for each reuse cycle.

Of the three approaches, ELO is the most mature, with small-scale manufacturing operations already underway. It appears to have the lowest cost of the three approaches if scaled up for high-volume manufacturing. Spalling is much less mature and has only been used to demonstrate good III-V devices in the laboratory. Its projected cost in high volume is higher than that for ELO. The use of a porous Ge release layer is still in a primitive state of development; no good III-V devices have been demonstrated using this approach, even at laboratory scale. If technically successful, its cost in high volume would be similar to spalling.

If the cost of epitaxial deposition is substantially reduced in the future (as would be necessary for III-V solar cells to be cost-competitive for low-concentration and one-sun terrestrial applications), then the cost associated with the substrate will also be reduced because deposition of cladding layers is a significant cost in the reuse cycle. A reduction in deposition cost would particularly benefit the spalling approach, potentially making it the least expensive of the options considered. For spalling and porous Ge, the primary residual cost in this low-deposition-cost scenario would be CMP. For ELO (using CMP every 10 reuse cycles), the primary residual cost would be the etch-release step.

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