Задание 1

```
module top_5 (
    input wire clk,
    input wire rst_n,
    input wire j,
    input wire k,
    input wire shift_in,
    input wire sel,
    input wire [3:0] data,
    input wire [1:0] sell,
    output wire q,
    output wire [7:0] shift_reg,
    output wire shift_y,
    output wire encoder_y,
    output wire [1:0] enc_out
);

shift_reg_jk_ff_mux shift_reg_jk_ff_mux_inst (
    .clk(clk),
    .rst_n(rst_n),
    .j(j),
    .k(k),
    .shift_in(shift_in),
    .sel(sel),
    .q(q),
    .shift_reg(shift_reg),
    .y(shift_y)
);

encoder_mux encoder_mux_inst (
    .data(data),
    .sel(sell),
    .enc_out(enc_out),
    .y(encoder_y)
);

endmodule
```

Top_5

```
module encoder_mux (
    input wire [3:0] data,
    input wire [1:0] sel,
    output wire [1:0] enc_out,
    output wire y
);
    reg [1:0] encoded_data;


    always @(*) begin
        case (data)
            4'b1000: encoded_data = 2'b11;
            4'b0100: encoded_data = 2'b10;
            4'b0010: encoded_data = 2'b01;
            4'b0001: encoded_data = 2'b00;
            default: encoded_data = 2'b00;
        endcase
    end
    assign enc_out = encoded_data;


    assign y = (sel == 2'b00) ? enc_out[0] :
               (sel == 2'b01) ? enc_out[1] :
               (sel == 2'b10) ? data[0] :
               data[1];
endmodule
```

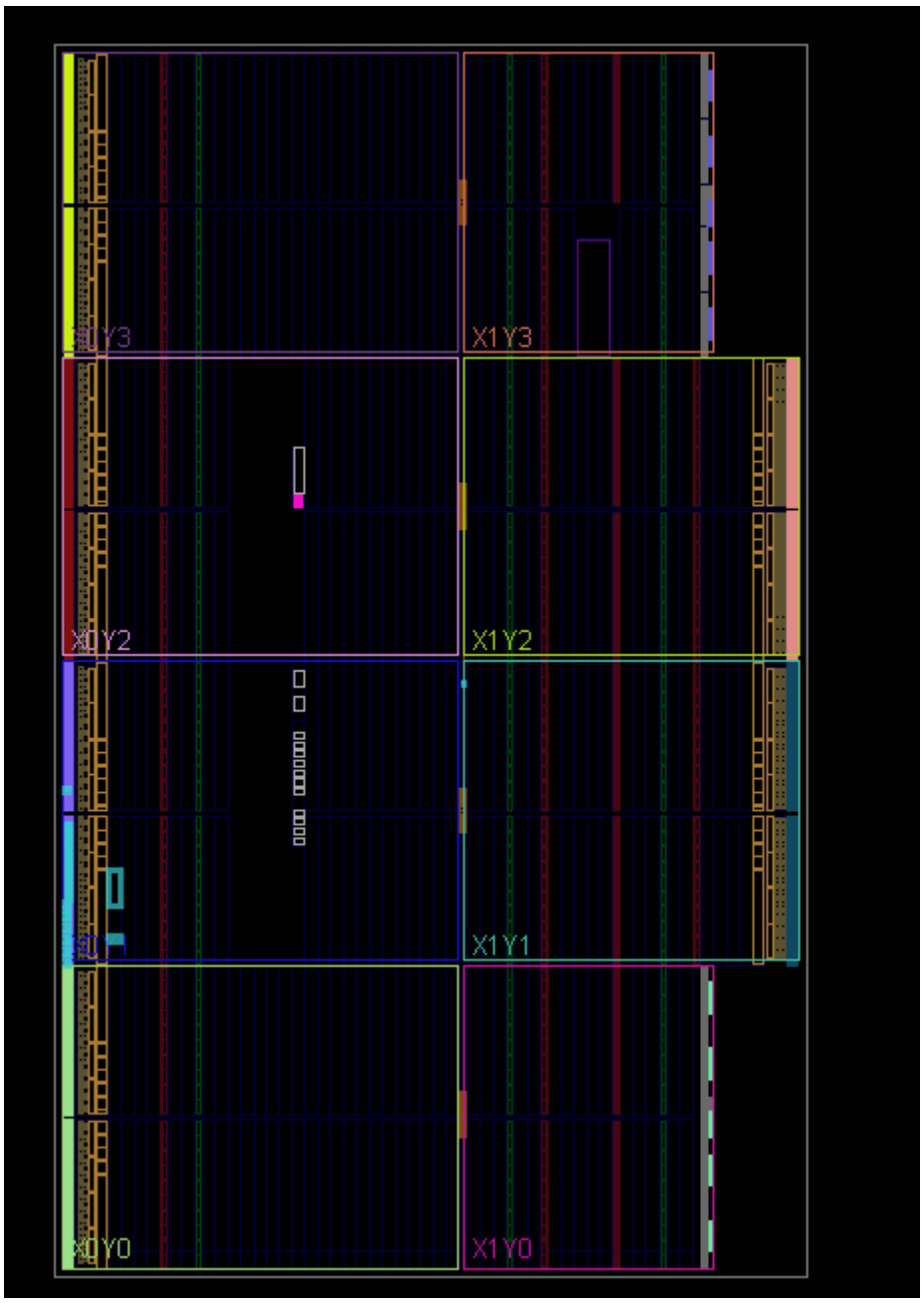
Encoder_mux

```
module shift_reg_jk_ff_mux (
    input wire clk,
    input wire rst_n,
    input wire j,
    input wire k,
    input wire shift_in,
    input wire sel,
    output reg q,
    output reg [7:0] shift_reg,
    output wire y
);

    always @(posedge clk) begin
        if (!rst_n)
            shift_reg <= 8'b0;
        else
            shift_reg <= {shift_reg[6:0], shift_in};
    end


    always @(posedge clk) begin
        if (!rst_n)
            q <= 1'b0;
        else if (j && !k)
            q <= 1'b1;
        else if (!j && k)
            q <= 1'b0;
        else if (j && k)
            q <= ~q;
    end


    assign y = sel ? q : shift_reg[0];
endmodule
```

Shift_reg_jk_ff_mux

```
set_property CLOCK_REGION_X1Y3 [get_cells {shift_reg_jk_ff_mux_inst}]
set_property CLOCK_REGION_X1Y1 [get_cells {encoder_mux_inst}]
```

Файл проектных ограничений



Размещение