The SDHCAL technological prototype Construction, first results and ongoing R&D

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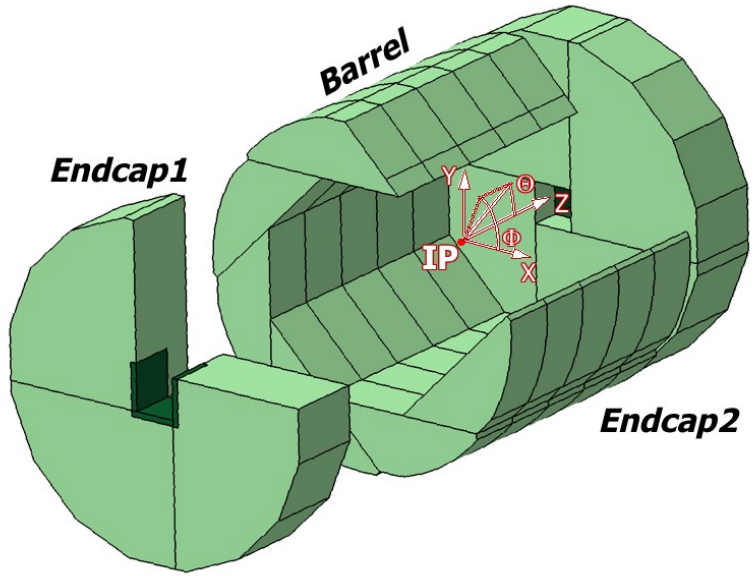
Introduction

Context

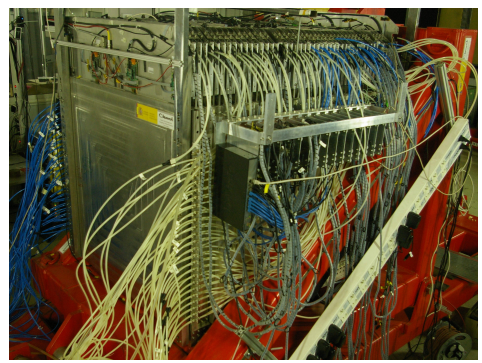
The SDHCAL-GRPC is one of the two HCAL options proposed in the ILD Letter Of Intent (LOI). Modules are made of 48 RPC chambers ($6\lambda_I$) equipped with power-pulsed electronics readout.



SDHCAL-ILD

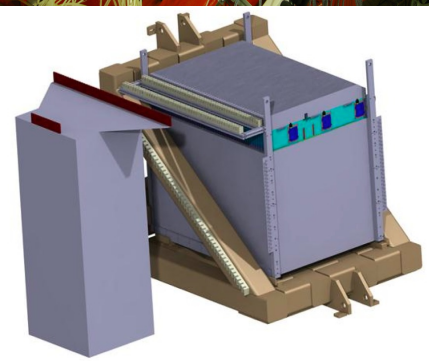
The structure proposed for the SDHCAL-ILD :

→ Is self-supporting
→ Has negligible dead zones
→ Eliminates projective cracks
→ Minimizes barrel / endcap separation



Chamber challenges

→ Thickness of only few mms
→ Homogeneity for large surfaces
→ Services from one side
→ Embedded power-pulsed electronics
→ Self-supporting mechanical structure

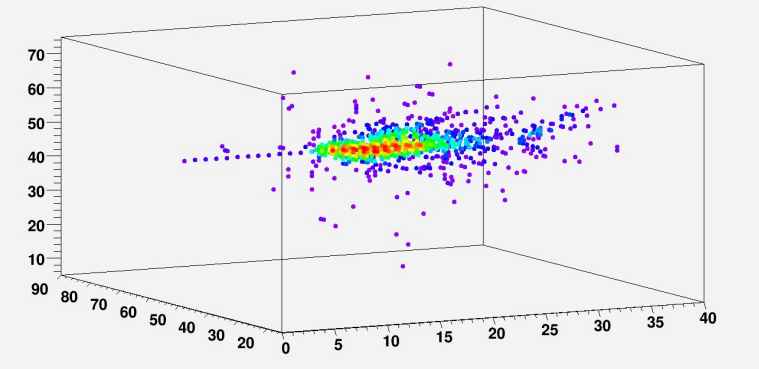


Detector Choice

Glass Resistive Plate Chamber

$\rightarrow$ Thin, homogeneous, cost-effective

$\rightarrow$ Avalanche $\simeq 1mm$ radius: High granularity achievable



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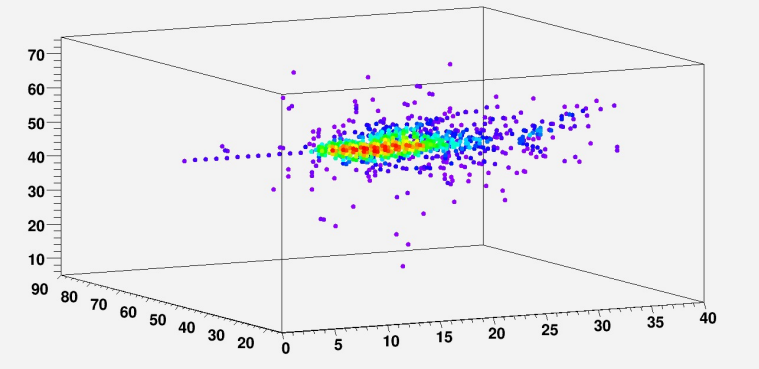
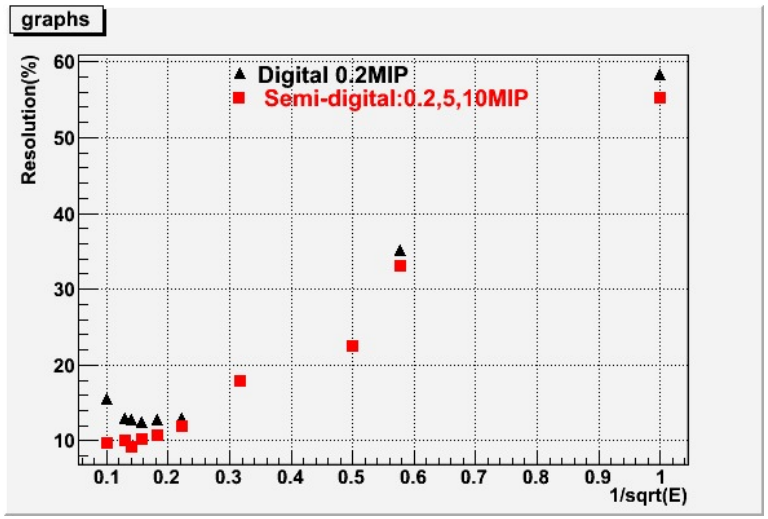


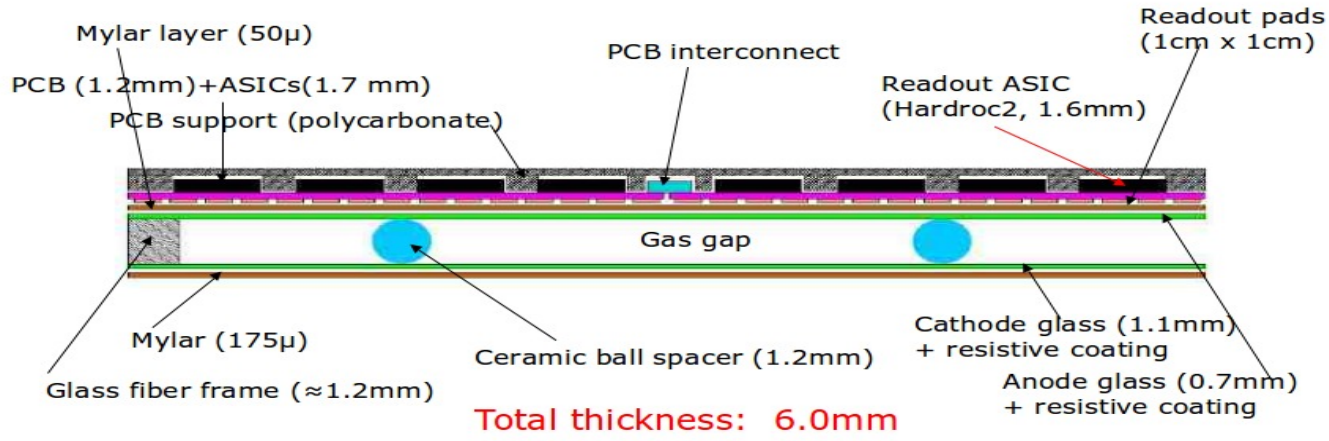
Semi Digital

$\rightarrow$ Saturation on 1 cm^2 pad in the core of hadronic showers

$\rightarrow$ 2-bits semi-digital readout improves resolution



GRPC design


Mylar layer (50µ)
PCB (1.2mm)+ASICs(1.7 mm)
PCB support (polycarbonate)
PCB interconnect
Readout pads
(1cm x 1cm)
Readout ASIC
(Hardroc2, 1.6mm)
Gas gap
Mylar (175µ)
Glass fiber frame (≈1.2mm)
Ceramic ball spacer (1.2mm)
Cathode glass (1.1mm)
+ resistive coating
Anode glass (0.7mm)
+ resistive coating
Total thickness: 6.0mm

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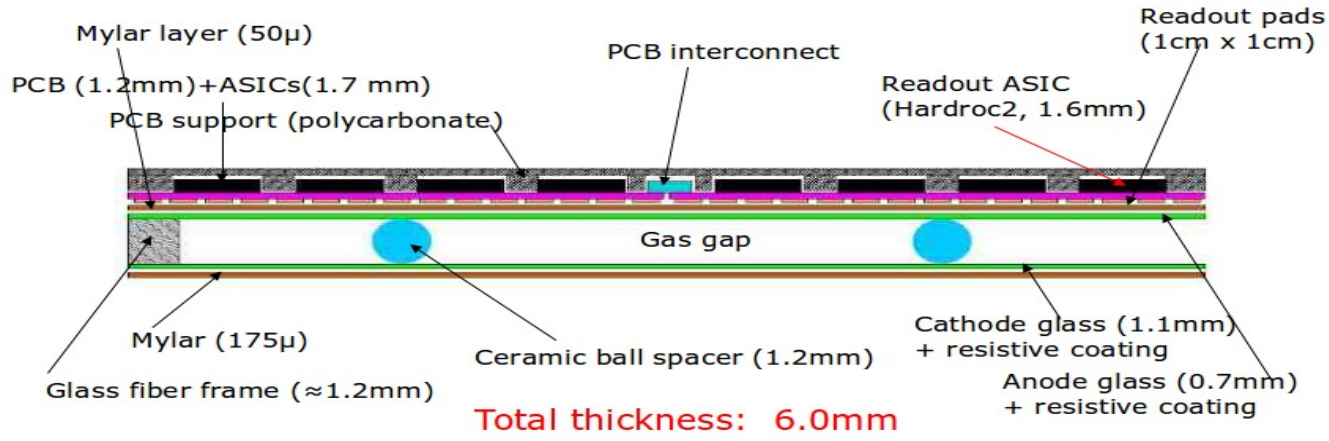
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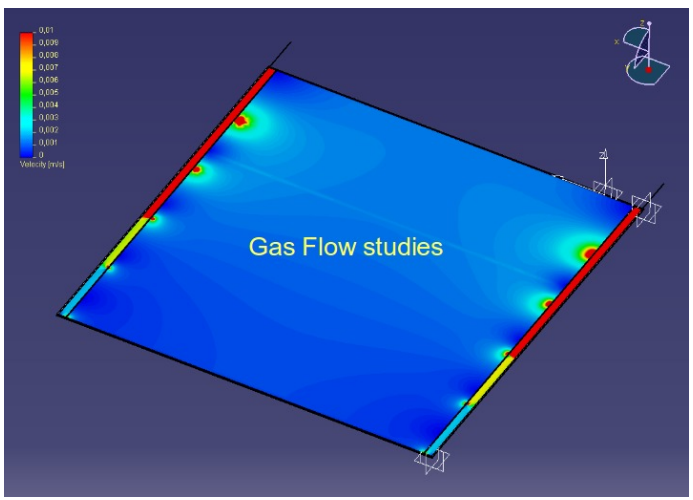
Gas Flow studies

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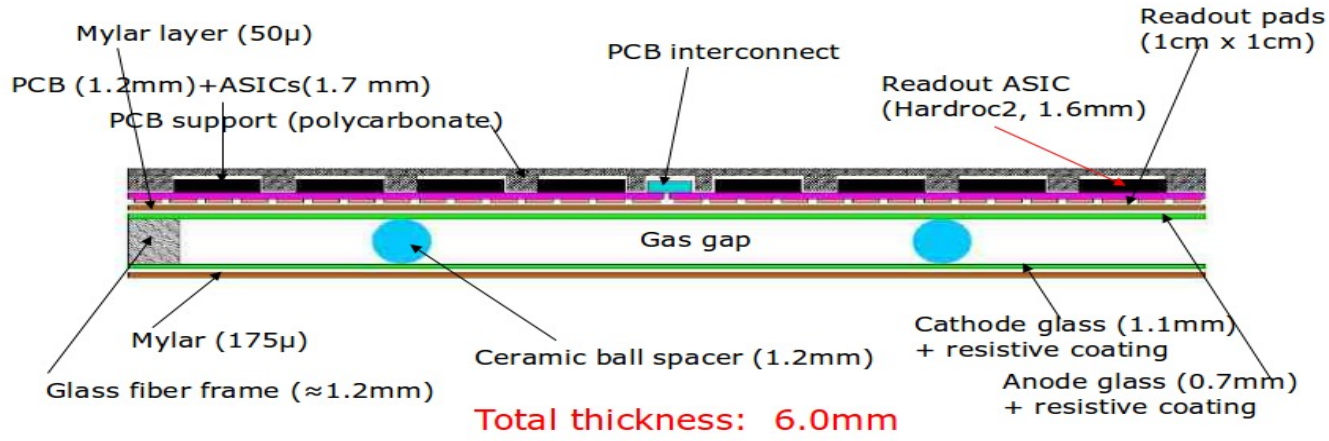
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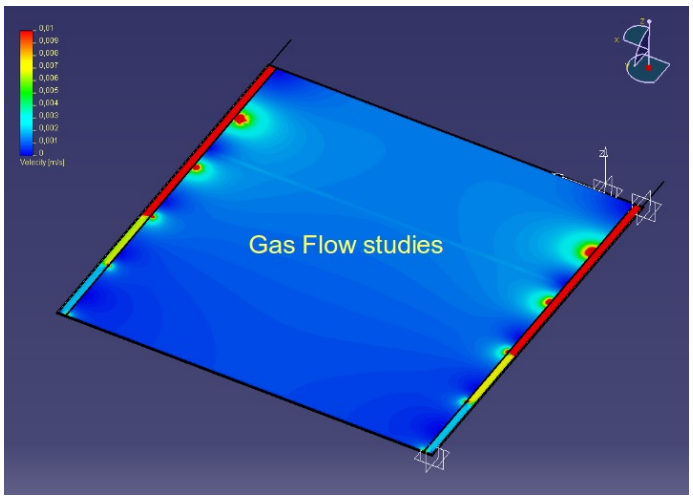
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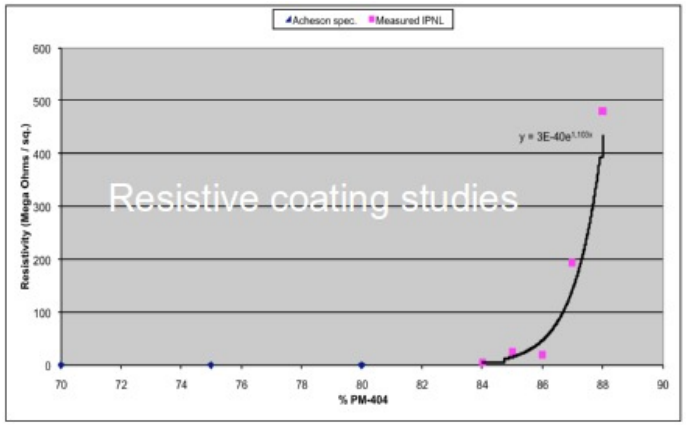
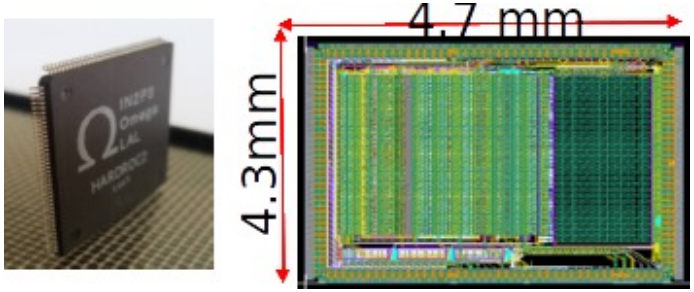
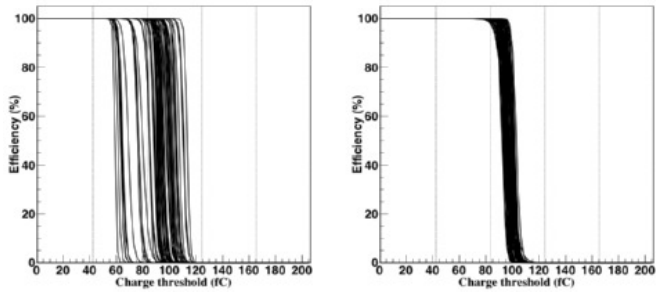

Acheson spec.
Measured IPNL
Resistivity (Mega Ohms / sq.)
% PM-404
Resistive coating studies

Readout Electronic

HardRoc ASIC

developped by Omega
→ 64 channels, triggerless mode, 127 memory slots
→ 3 thresholds , range [10 fC, 15 pC]
→ Channel gain : Uniformity correction
→ Analog power switch: Power-pulsed capability, low consumption





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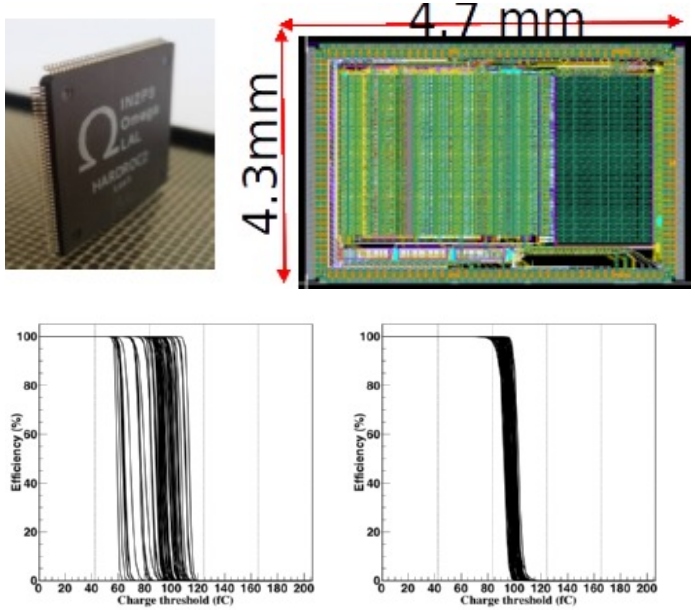
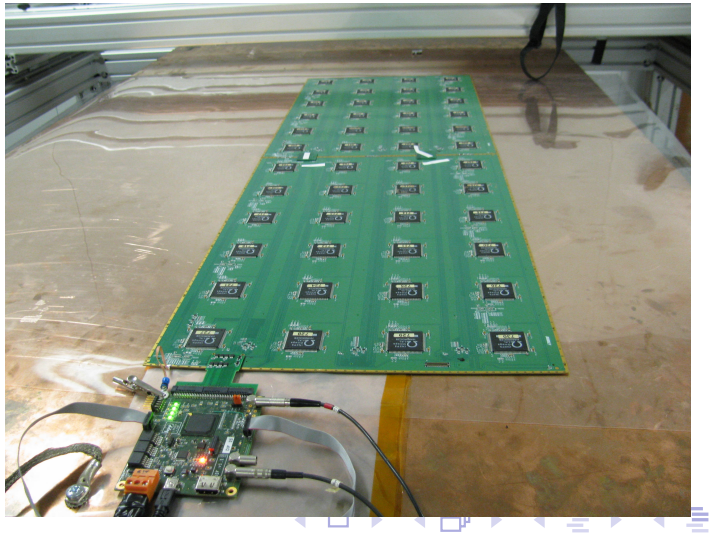
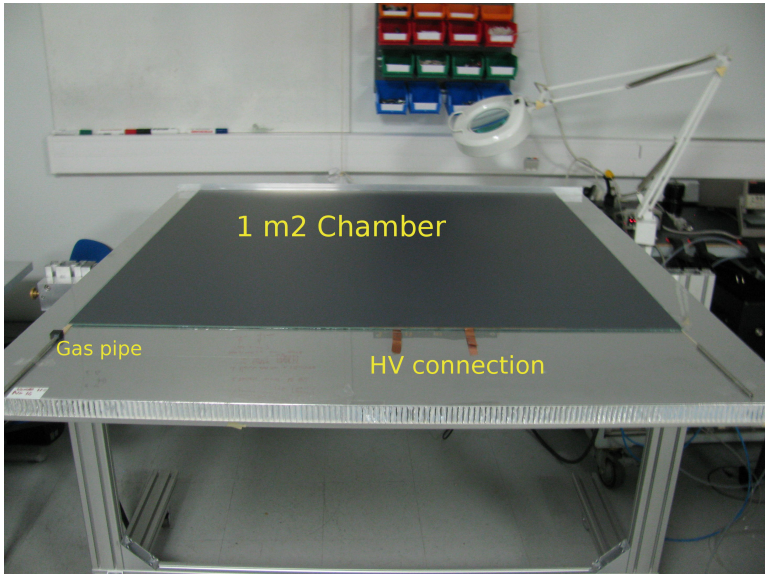


ASU PCB development

→ 8-Layers, buried vias, 50 x 33 cms
→ Two 24 asics PCB connected with flat connectors
→ DAQ board (DIF) controls and read the 48 daisy chained chips (developped by LAPP)



Cassette assembly



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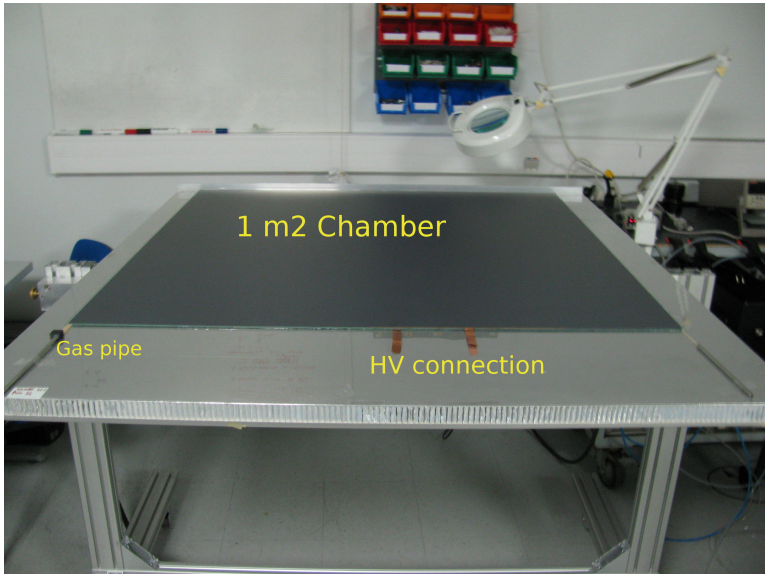

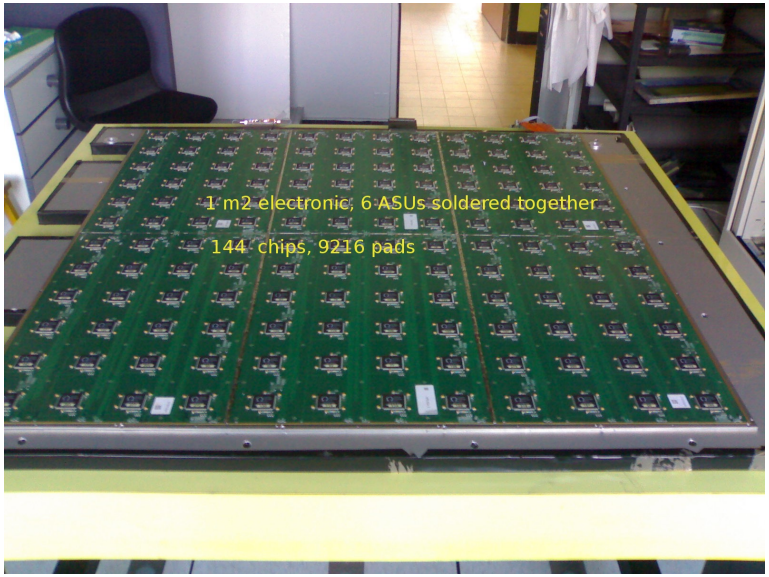

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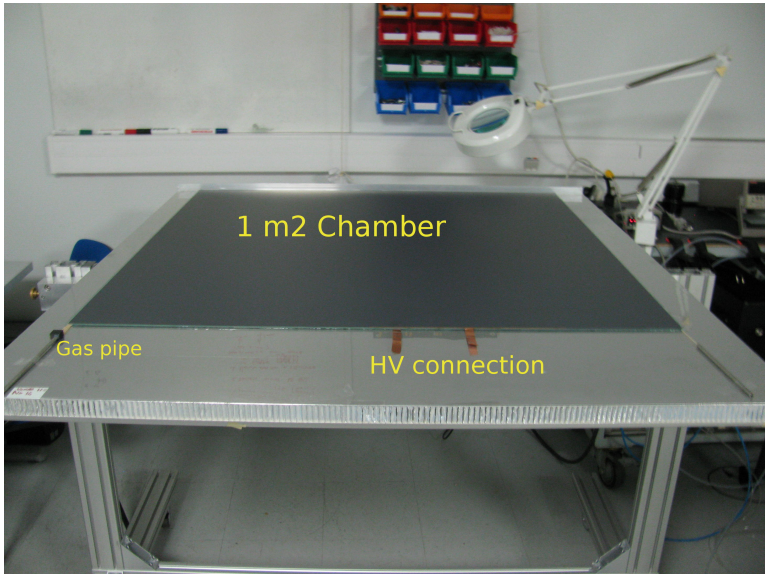

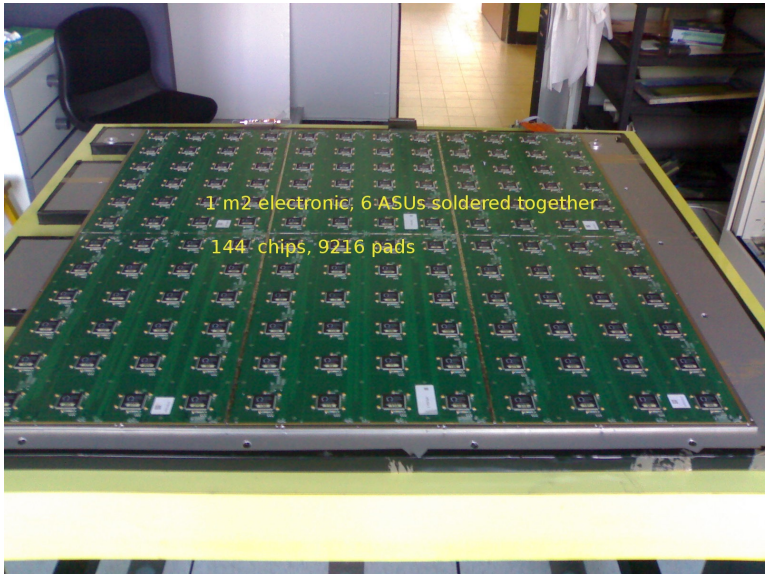

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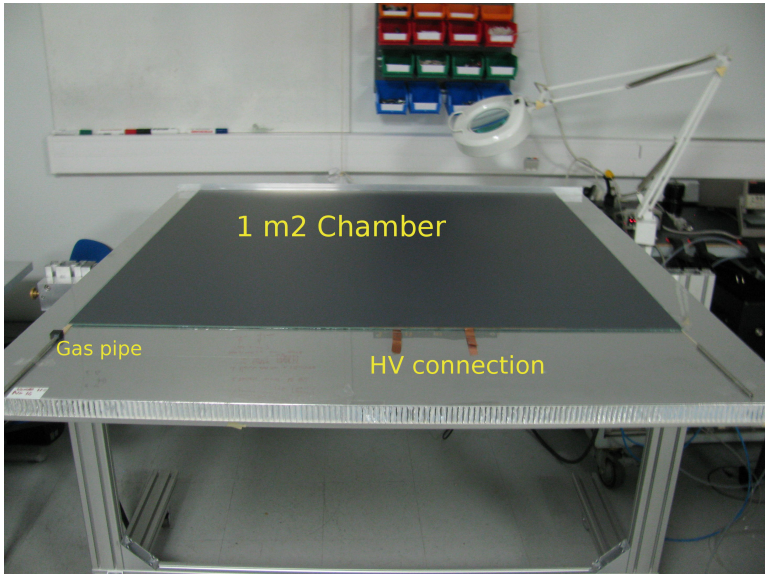
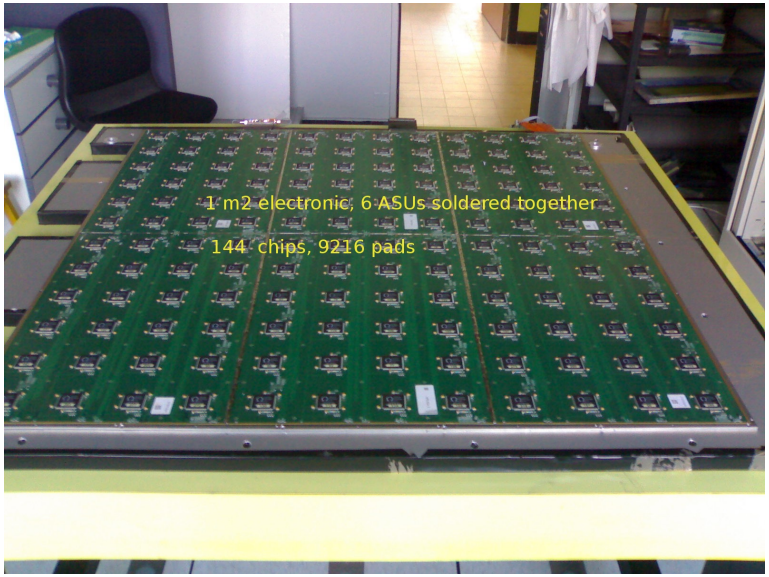
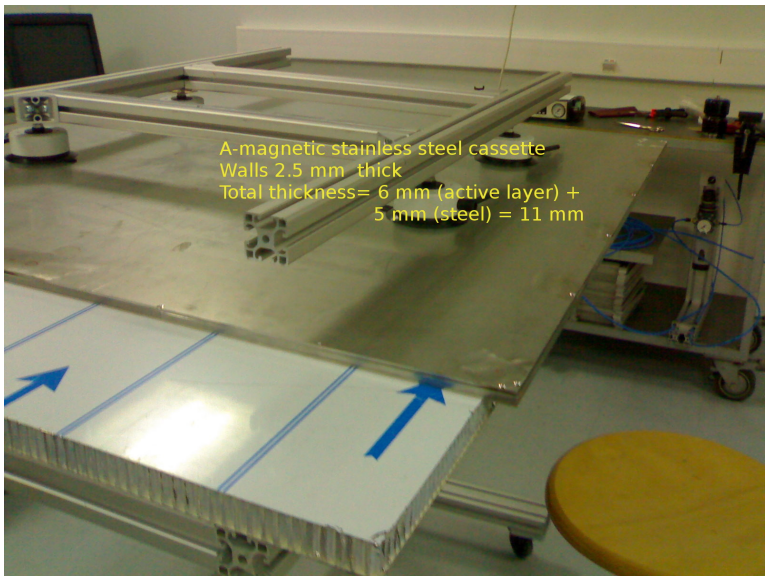
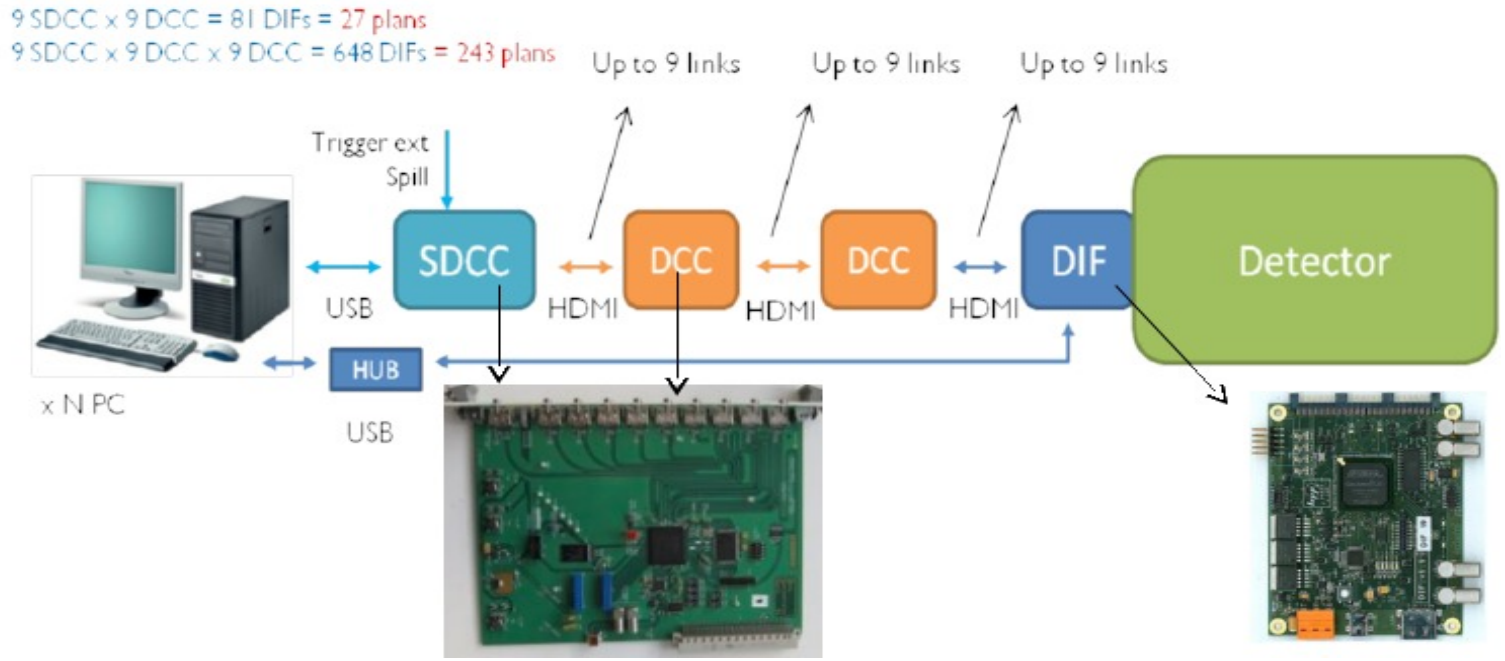






Acquisition system



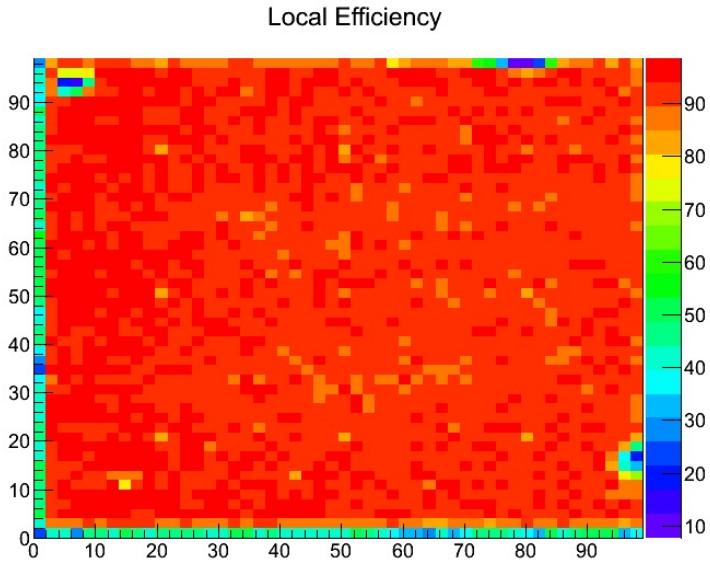
- Oracle configuration data base
- Event building with CMS Event Event builder (XDAQ)
- Up to 150 USB links on 4 PCs
- Rate limited by USB1 links and 5 MHz readout of ASIC daisy chained

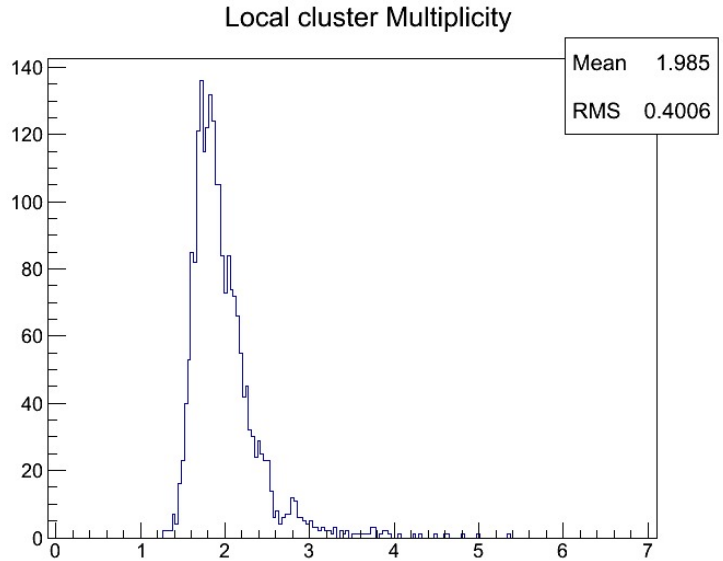
Chamber performances

Working point

- Gas: TFE(92 %), CO2 (5 %), SF6 (2 %)
- HV : -7.0 kV (20° C, 1020 mbar)
- Efficiency $\simeq$ 95 %
- Pad Multiplicity $\simeq$ 1.7

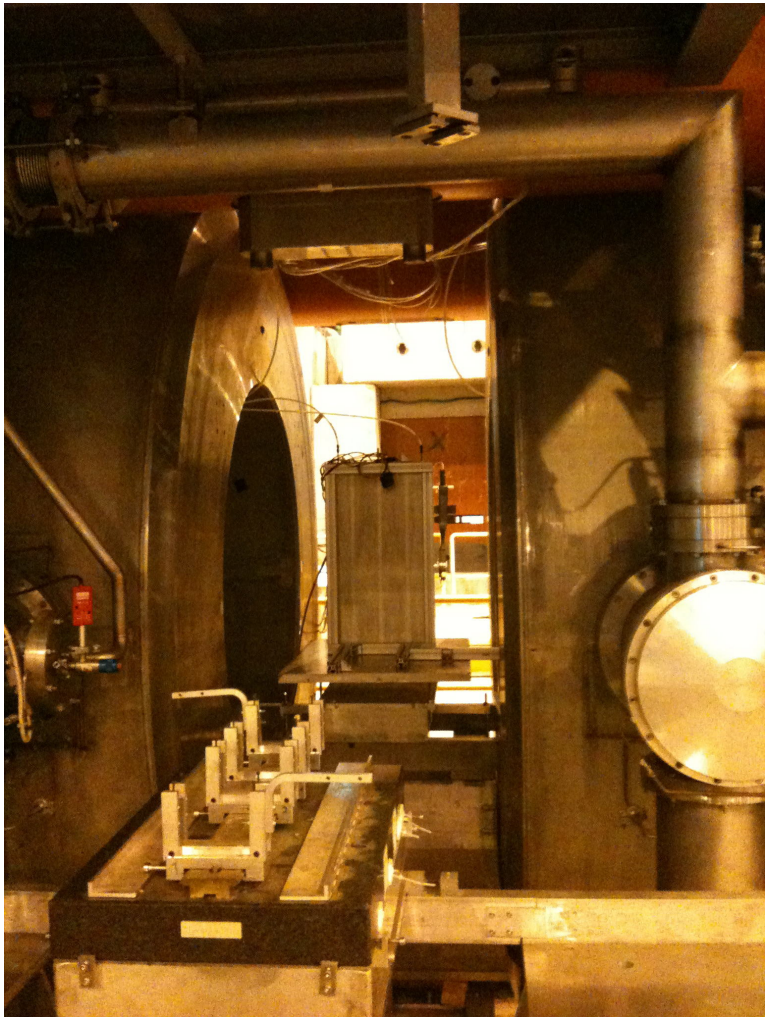
Cosmic muons studies

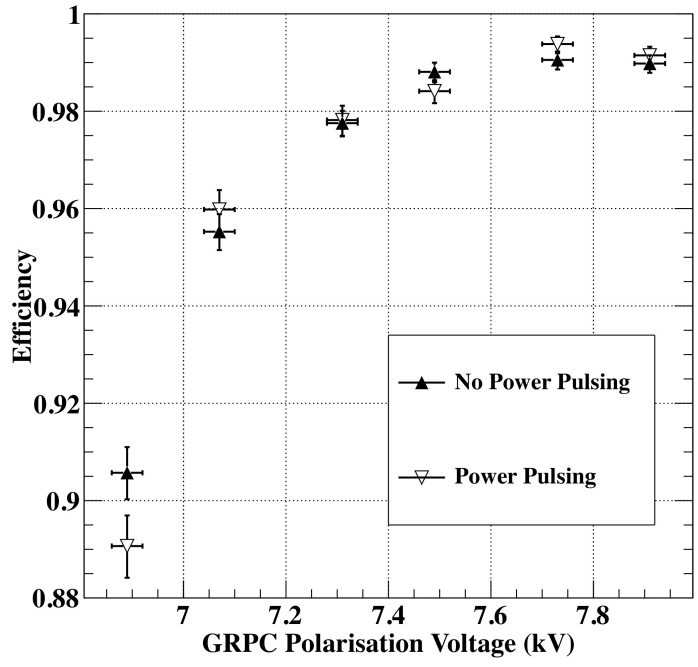




Chamber performances

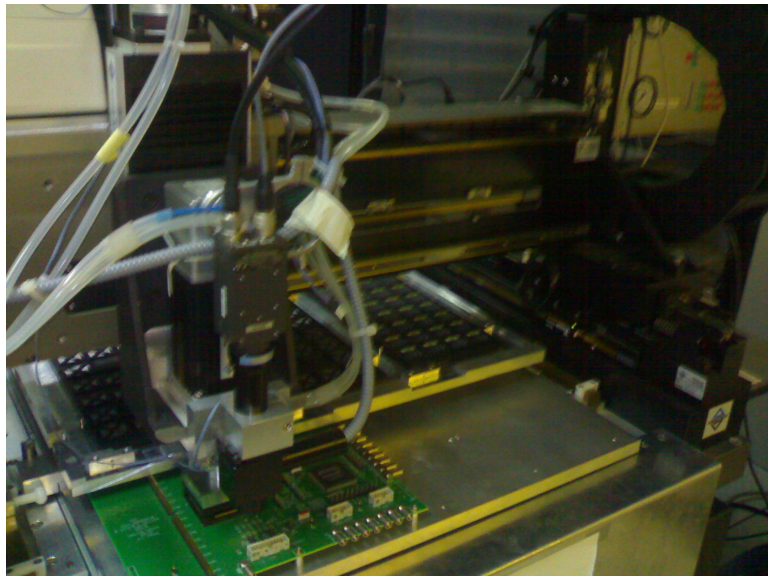
Power-pulsed performances in 3T B field (H2-CERN)





Prototype construction

Production and test of
 → 10500 HR2 chips (LAL Omega)
 → 150 ASU + 300 interconnection PCBs
 → 170 DIF (LAPP) and 20 DCC (LLR)



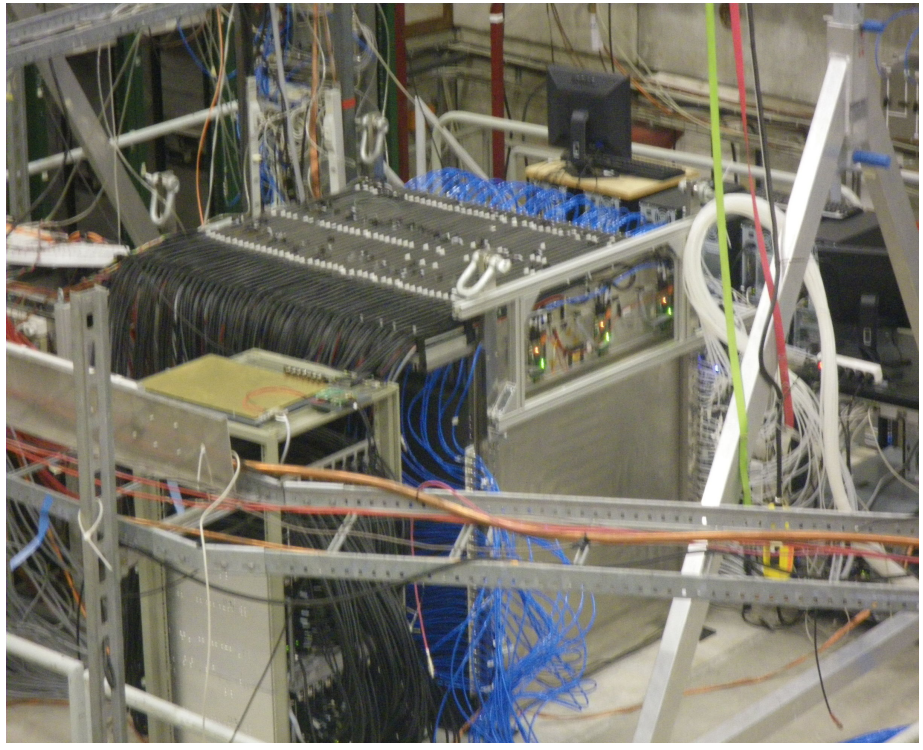
Production and test of
 → 50 chambers and cassettes
 → 8 storage racks used as cosmic muon stand

Final integration at CERN

- Mechanical structure developped by CIEMAT
- HV and cooling services developped by Gent and Louvain
- Full assembly made at CERN before the beam tests

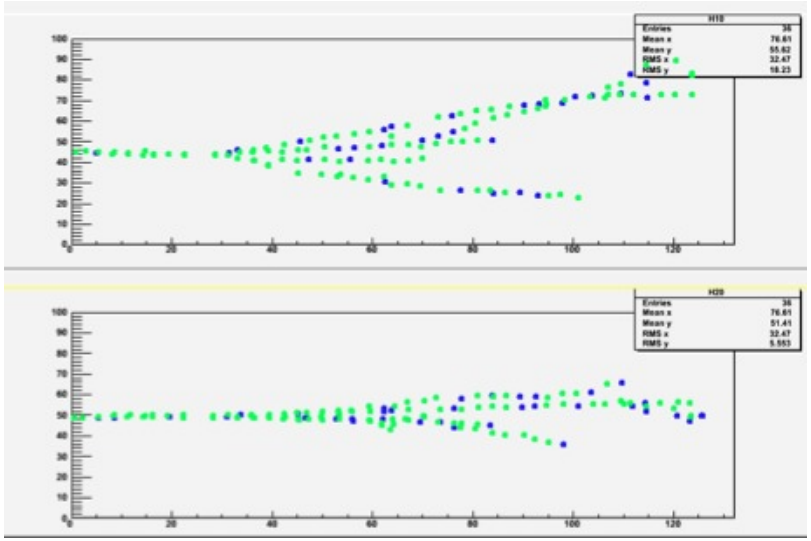
Beam tests in 2012

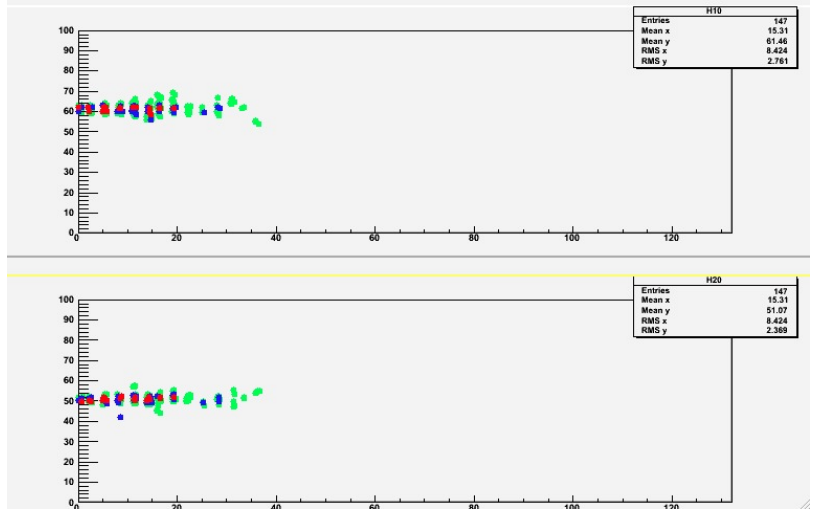
- 5 weeks of data taking on PS and SPS lines at CERN
- π and e beams from 3 to 100 GeV allowing to study both hadronic and electromagnetic showers in a large energy range
- power pulsing mode (Analog on during spill) minimized the required cooling
- Trigger less mode $\rightarrow$ better daq efficiency, beam muons to monitor the rate and the chambers efficiency



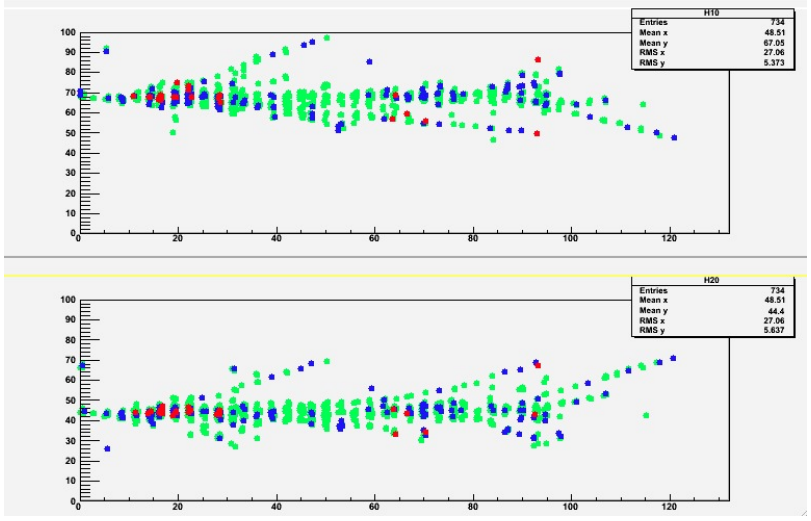
Showers

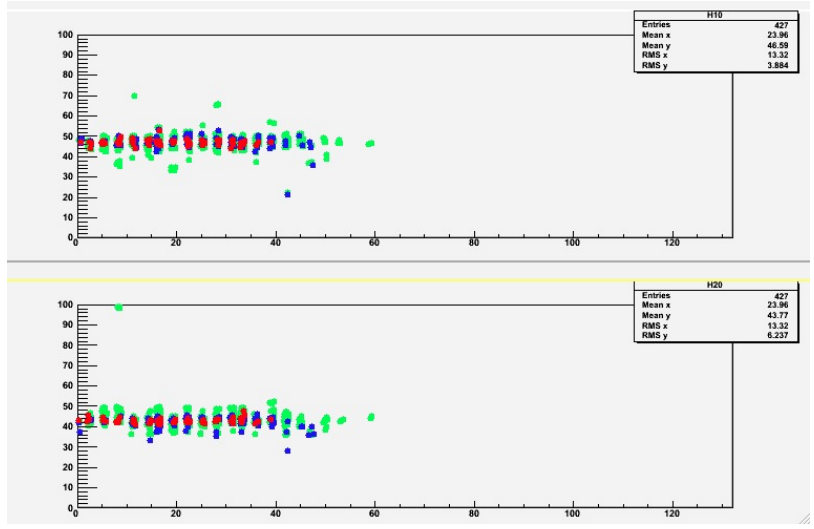
10 Gev π and e





50 Gev π and e

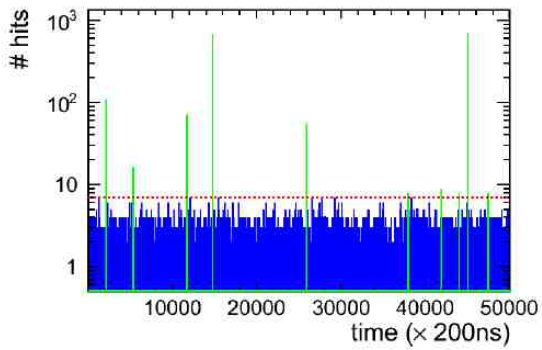


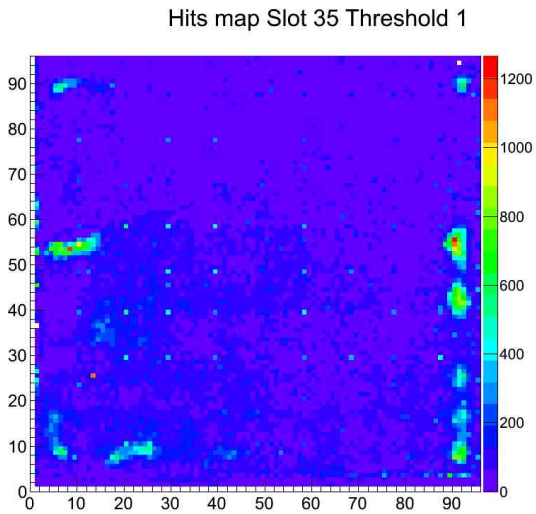


Commissioning

Noise Studies

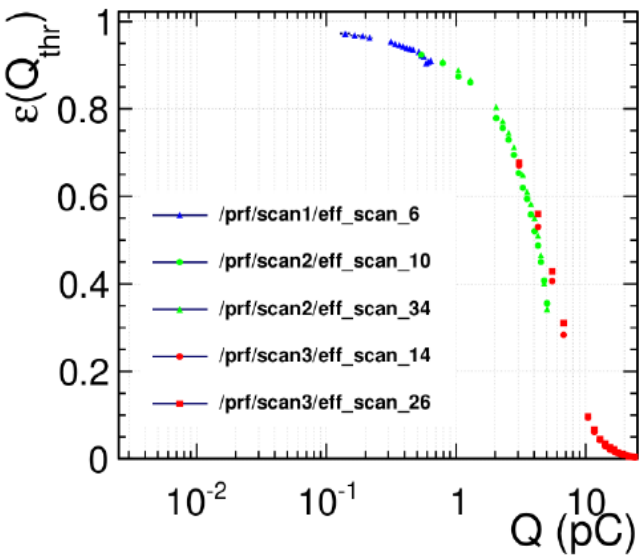
$\rightarrow < 1$ Hz/pad,
$\simeq 0.35$ Hit/ Bx (200 ns)
$\rightarrow$ Locally high noise (mask or gain adjust)





Threshold study

$\rightarrow$ Dedicated μ runs
$\rightarrow$ Scan efficiency for the 3 thresholds
$\rightarrow$ MC Polya response adjust from it



Analysis path

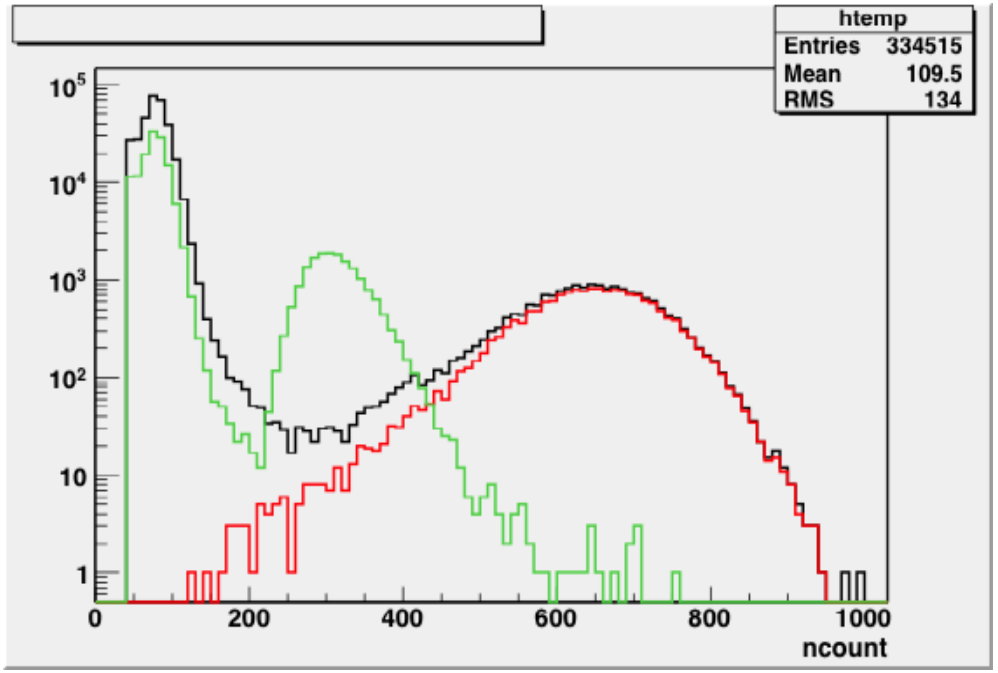
μ and e rejection

$\rightarrow$ Shower starts after 5th layer or more than 30 layers have at least 4 hits. (electron rejection)

$\rightarrow$ Mean number of hits in fired layers above 2.2. (μ rejection)

$\rightarrow$ At least 20 % of the fired layers should have a spatial hit distribution with RMS $>$ 5cm (radiative μ rejection)

$\rightarrow$ At least 4 hits in the first 5 layers (neutral rejection)



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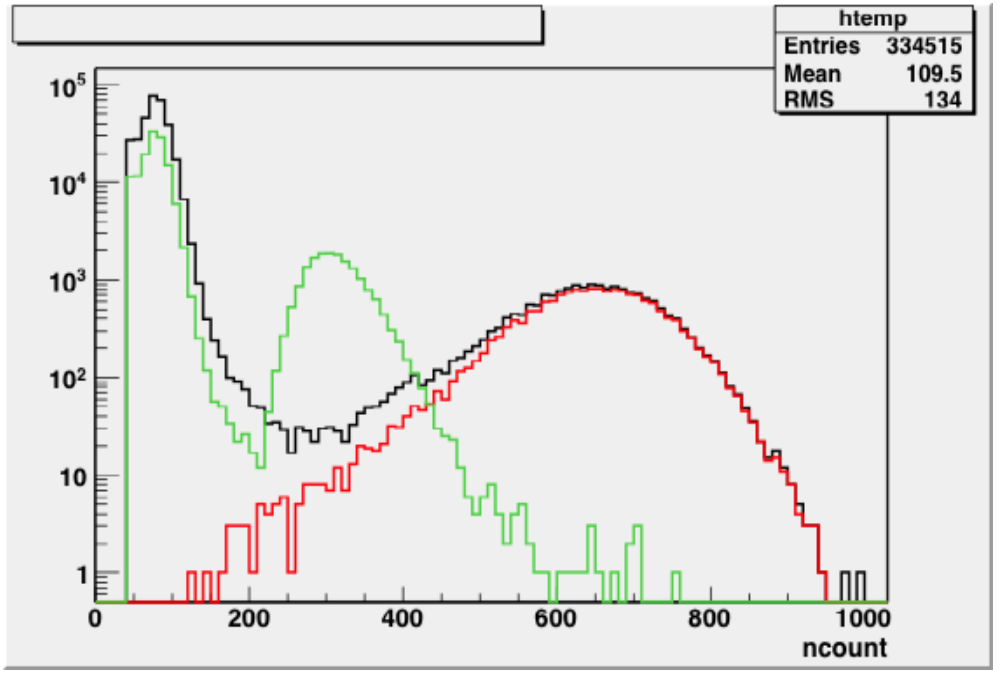
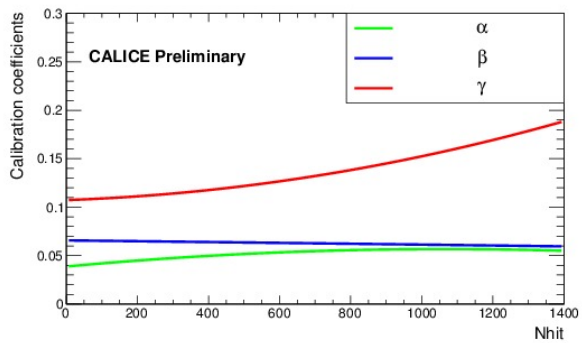


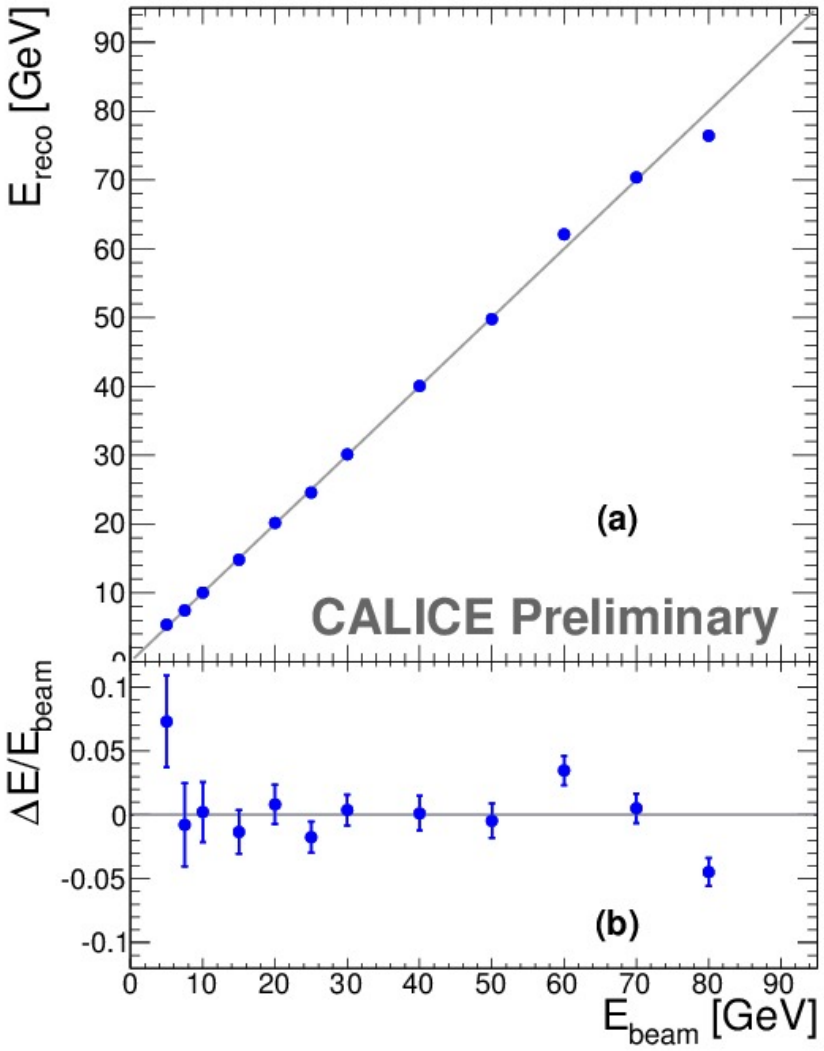
Energy calibration

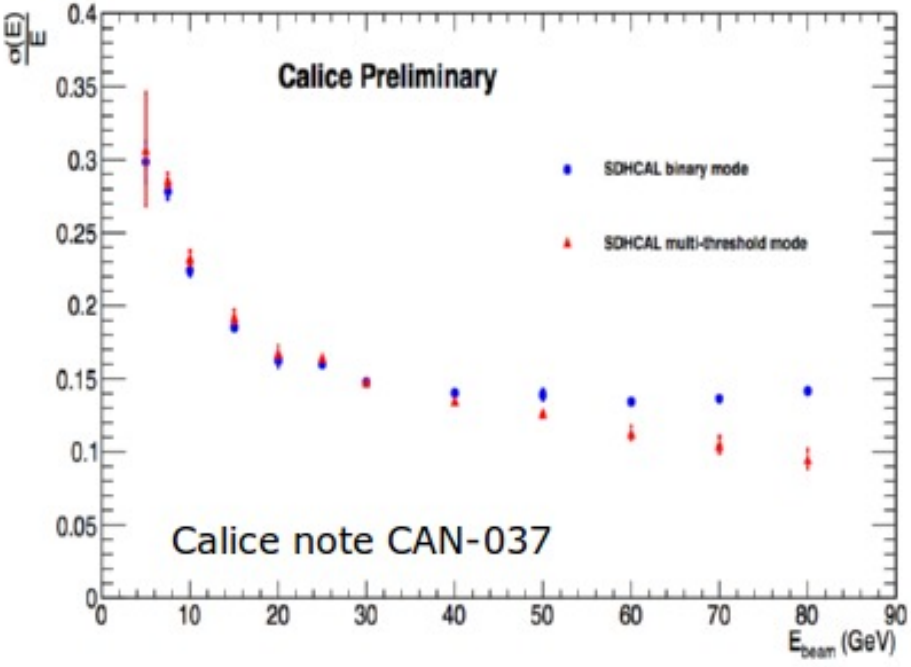
$E_R = \alpha N_1 + \beta N_2 + \gamma N_3$

where α, β, γ are quadratic functions in $N_{tot} = N_1 + N_2 + N_3$ and fitted from data



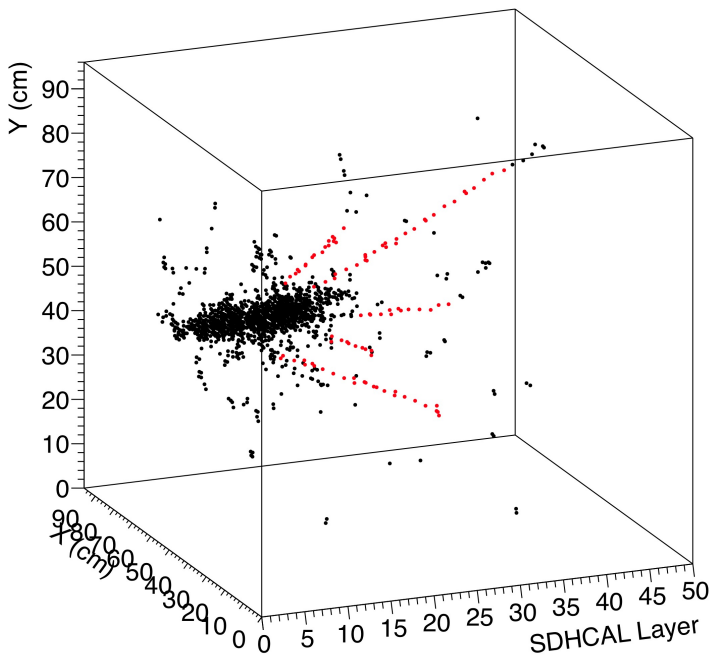
Results


E_{reco} [GeV]
(a)
CALICE Preliminary
$\Delta E/E_{beam}$
(b)
E_{beam} [GeV]

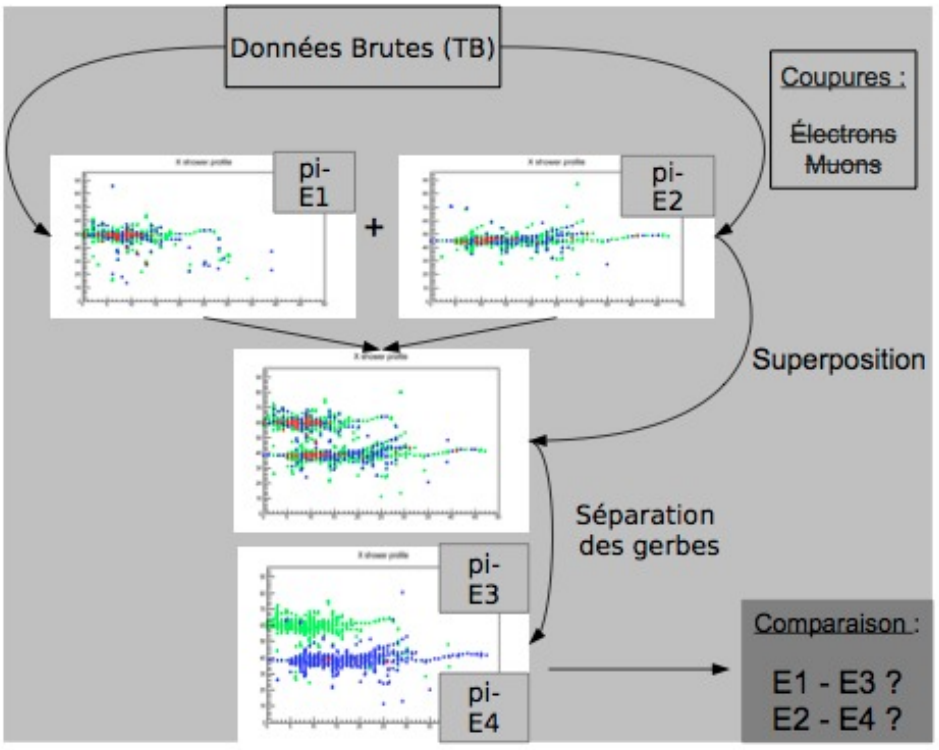

$\frac{\sigma(E)}{E}$
Calice Preliminary
SDHCAL binary mode
SDHCAL multi-threshold mode
Calice note CAN-037
E_{beam} (GeV)

Current software improvements

Tagging MIPs hits (Hough transform,combinatorial) separatly in E_R fit, improves resolution from 7%-15 %



New Shower reconstruction algorithm Arbor (MST based) improves shower separation



Next data taking

Improve statistic

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- Some 2012 runs were taken with > 100 Hz/pad, efficiency is currently corrected. Long low intensity runs needed
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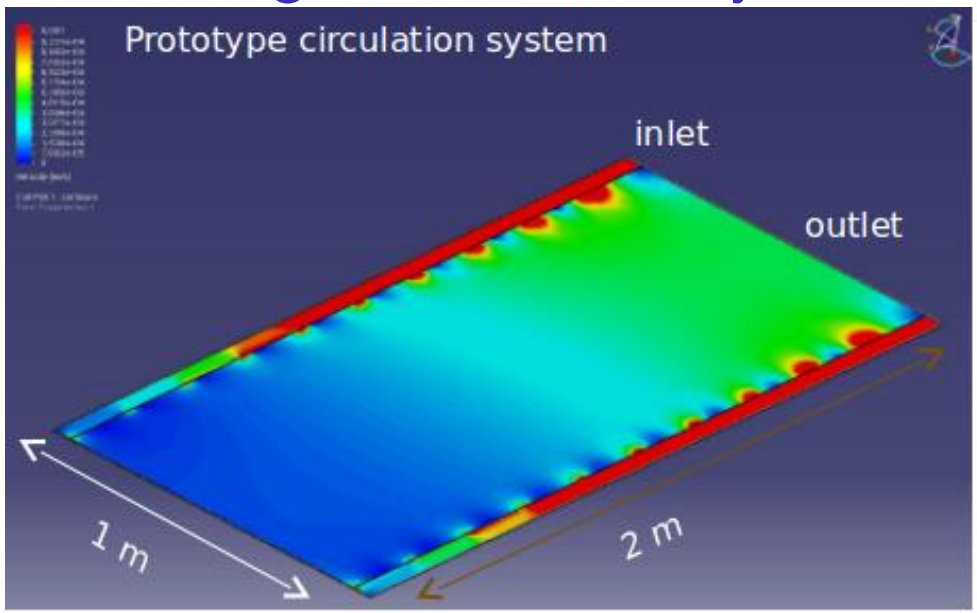
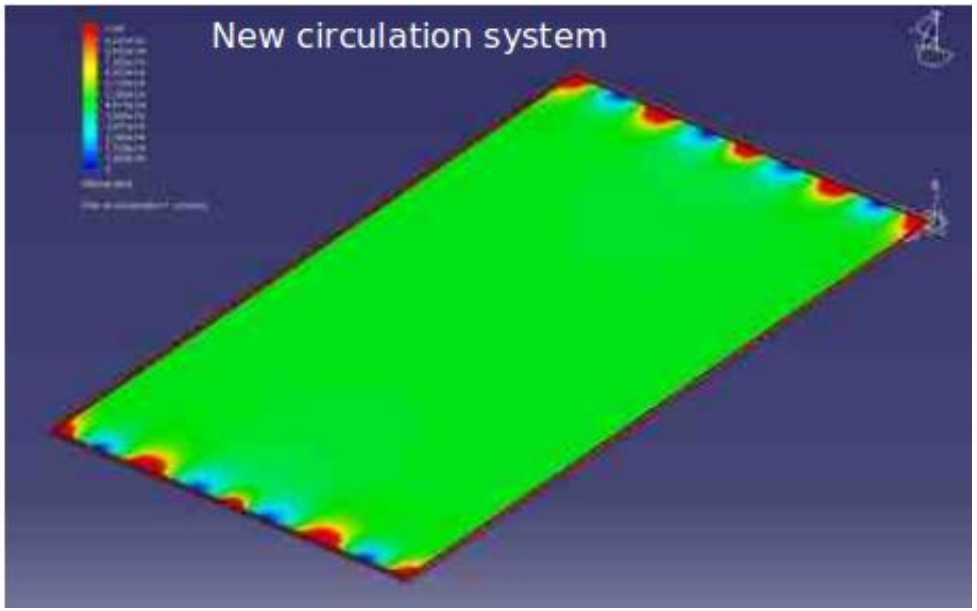
New DAQ

- Low consumption, integrated PC (raspberry pi), one for 4 chambers
- Lighter DAQ framework (DIM)

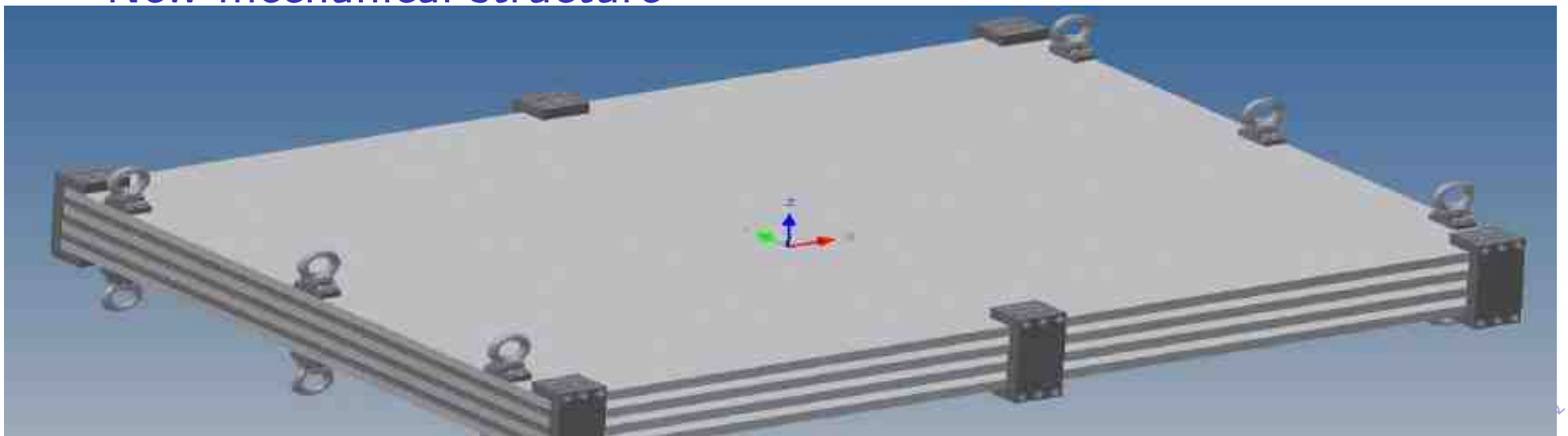
2 m long chambers

New gas distribution system





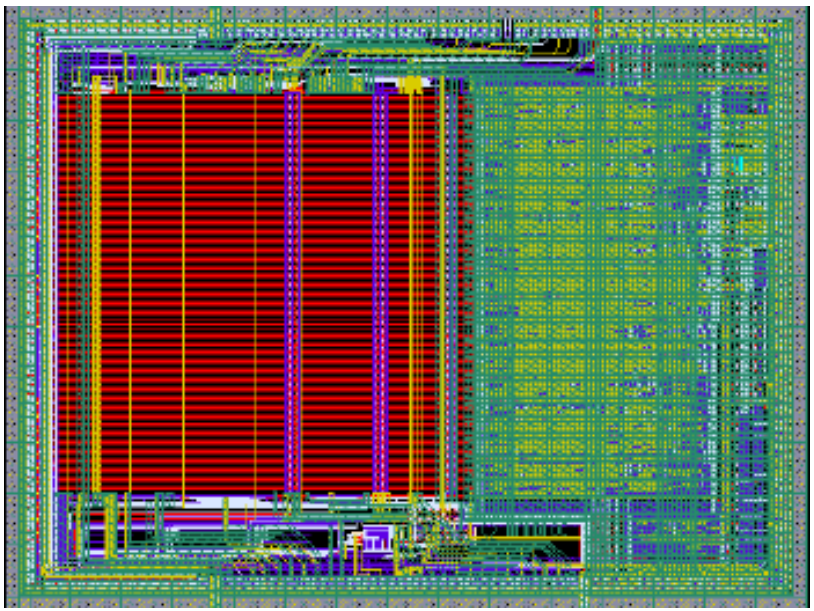
New mechanical structure



New electronic

HardROC3 (Omega)

- Independant 8-slots buffer per channel
- I2C configuration
- Better dynmamic range



DIF3 (CIEMAT)

- One DIF per plane (432 chips in 12 paralell lines)
- Ethernet (commercial chip) readout, TTC clock & commands
- Spare SFP cage for bi-directionnal serial link implemnentation (GBT)