Vcc

ISO+

G1
4.7u

ISO−

Vee

R3 1k
R2 1k
R4 1k

CTRL

R5 10k

Trig

Q1
BC547

GND

OPT1
VOW3120

1 N/C
2 LED+
3 LED−
4 N/C

Vcc 8
Vo   7
N/C 6
Vee 5

Vcc

Vee

sHV

sTrig

sGND

sHV

s*

sw+

s*

Vee

sw−

sGND

Inverting buffer ensures LED remains
off, despite stray capacitive coupling.

Coincidentally, this creates a sort of
logical High/Low compatibility with
low side N−Channel devices.

Pins sHV and sGND are optional.
Used with high−voltage cascodes.