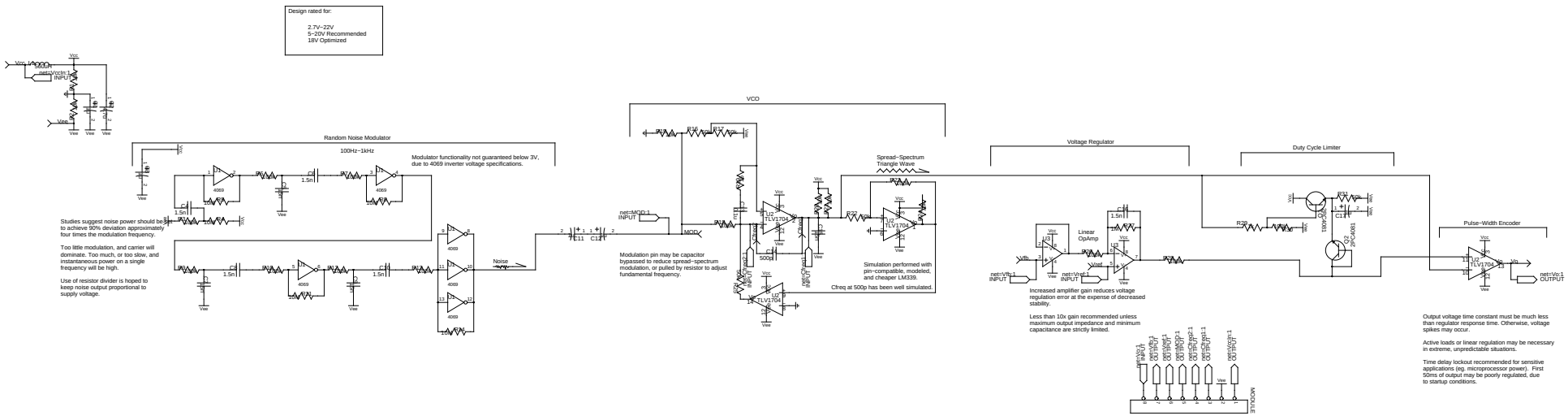
Design rated for:
2.7V~22V
5~20V Recommended
18V Optimized
Vcc
net=Vccin:1
INPUT
500R
Vset
Random Noise Modulator
100Hz~1kHz
Modulator functionality not guaranteed below 3V, due to 4069 inverter voltage specifications.
Studies suggest noise power should be 5% to achieve 90% deviation approximately four times the modulation frequency.
Too little modulation, and carrier will dominate. Too much, or too slow, and instantaneous power on a single frequency will be high.
Use of resistor divider is hoped to keep noise output proportional to supply voltage.
4069
Noise
net=MOD:1
INPUT
MOD
VCO
Modulation pin may be capacitor bypassed to reduce spread−spectrum modulation, or pulled by resistor to adjust fundamental frequency.
TLV1704
Spread−Spectrum Triangle Wave
Simulation performed with pin−compatible, modeled, and cheaper LM339.
Chreq at 500p has been well simulated.
Voltage Regulator
Linear OpAmp
net=Vfb:1
net=Vout:1
Increased amplifier gain reduces voltage regulation error at the expense of decreased stability.
Less than 10x gain recommended unless maximum output impedance and minimum capacitance are strictly limited.
Duty Cycle Limiter
2PCA081
Pulse−Width Encoder
net=Vo:1
OUTPUT
Output voltage time constant must be much less than regulator response time. Otherwise, voltage spikes may occur.
Active loads or linear regulation may be necessary in extreme, unpredictable situations.
Time delay lockout recommended for sensitive applications (eg. microprocessor power). First 50ms of output may be poorly regulated, due to startup conditions.
MODULE