Course: CS-223 Digital Design
Section 01
Final Project

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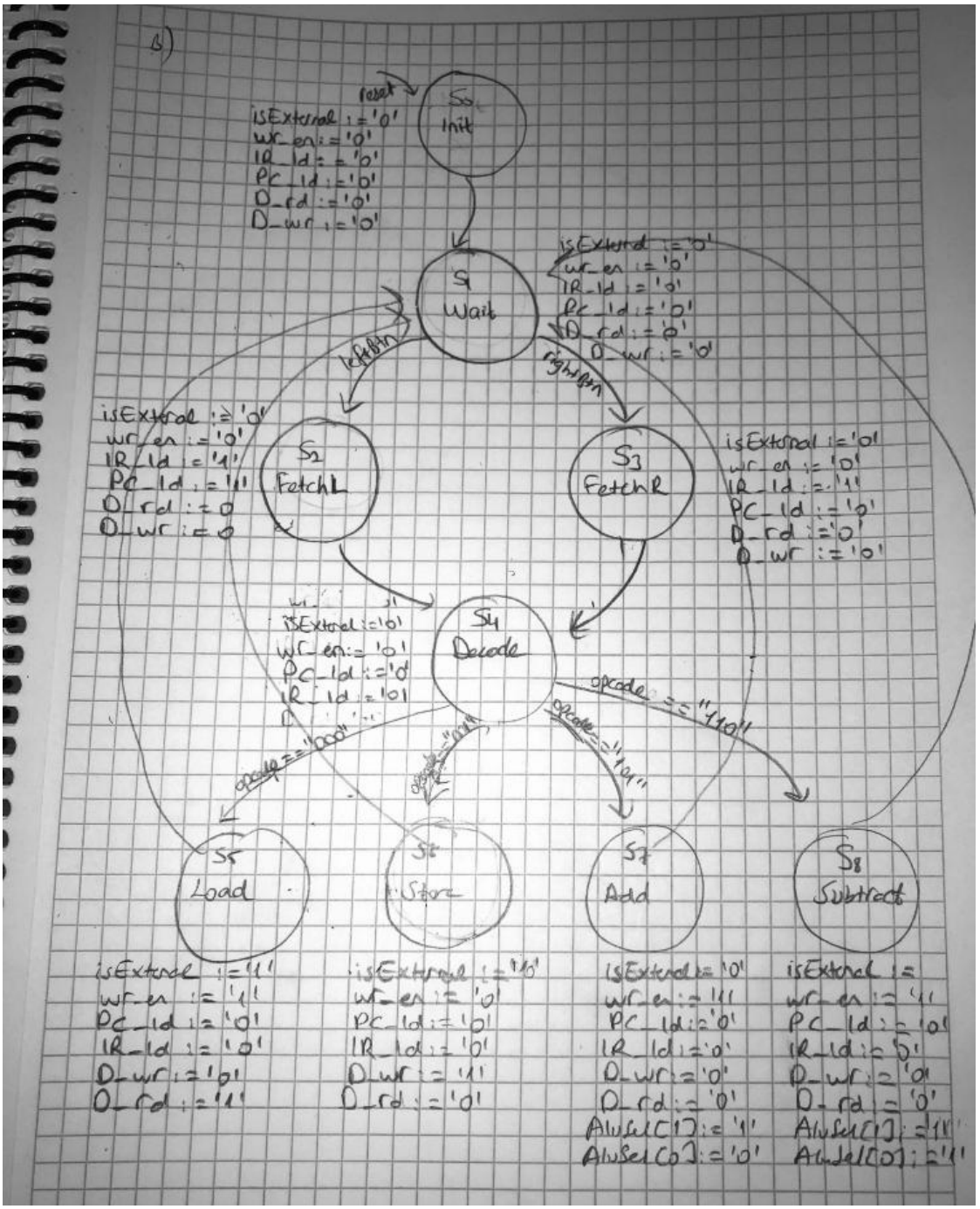
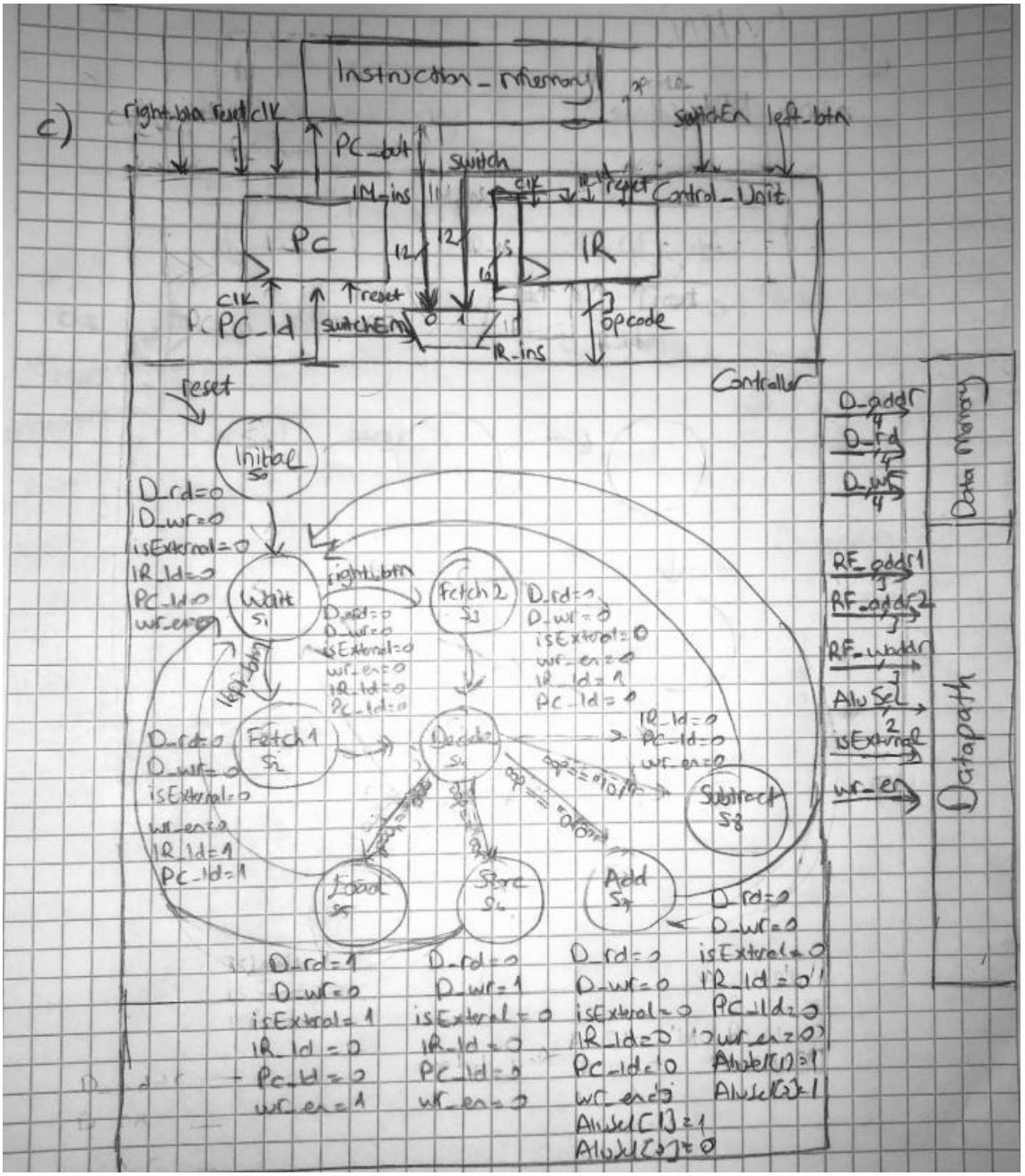
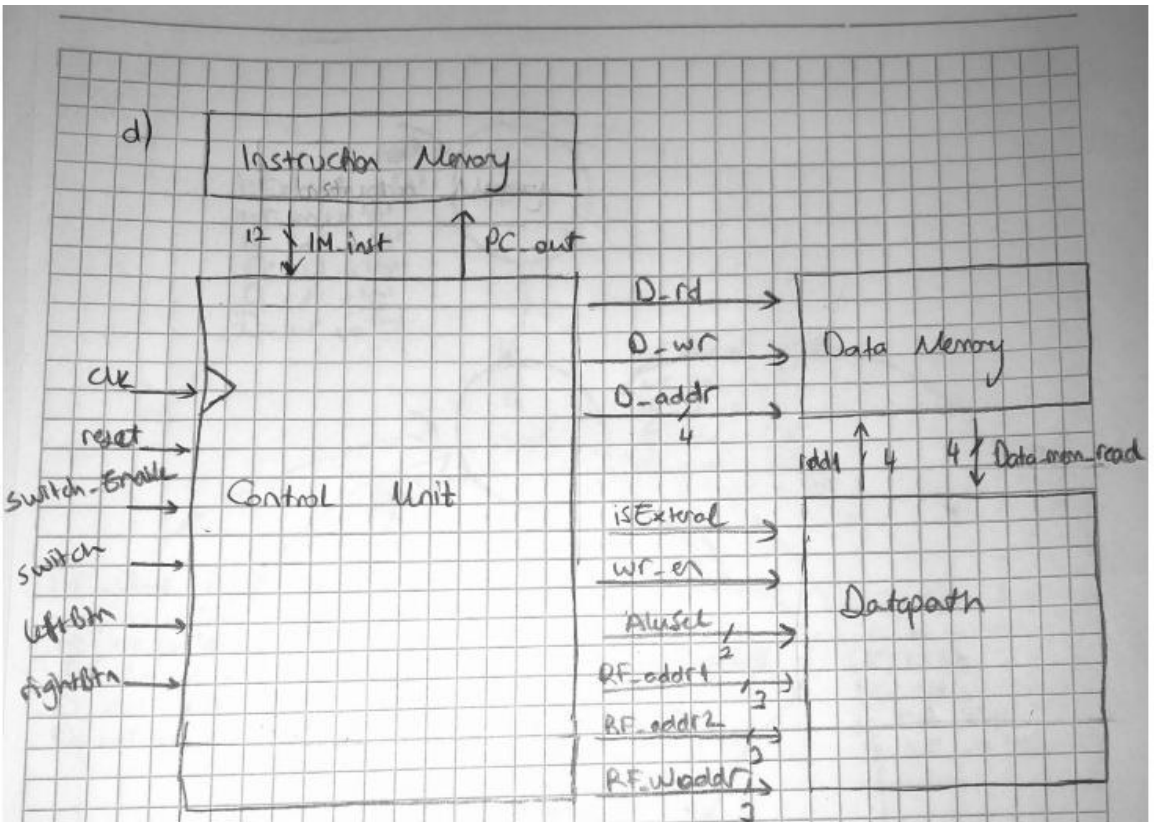
PART B) Controller High-Level State Machine Diagram



PART C) Controller Block Diagram



PART D) Controller/Datapath Top Module Block Diagram



PART E) TESTBENCH

```
module tb_control_unit(    );
logic clk, reset, leftBt, rightBt, switchEn;
logic [11:0] switch;
logic  [3:0] D_addr;
logic D_rd, D_wr;
logic [2:0] RF_addr1;
logic  [2:0] RF_addr2;
logic  [2:0] RF_waddr;
logic  [1:0] ALUSel;
logic  isExternal, wr_en;
logic[11:0]  IM_ins ;

Control_Unit dut(clk, reset, leftBtn, rightBtn, switchEn, switch, D_addr,
D_rd, D_wr, RF_addr1, RF_addr2, RF_waddr,  ALUSel, isExternal, wr_en, IM_ins);

initial
       clk = 1;
   always
```

```
        begin
        #15;
        clk = ~clk;
        end

    initial begin
    #10; reset = 1;
    #10; reset = 0;
    #20; leftBtn = 1;
    #30; leftBtn = 0;
    #20; leftBtn = 1;
    #50; leftBtn = 0;
    #20; leftBtn = 1;
    #30; leftBtn= 0;
    #20; leftBtn = 1;
    end


endmodule

module testbench_sp();

    logic clk, rightBtn, switchEn, leftBtn, reset;
    logic [11:0] switch;
     logic [11:0]IM;
    logic [6:0] seg;
    logic [3:0] an;
     logic [3:0] Rel;
    logic dp;

    Simple_Processor dut_sp ( clk, reset, leftBtn, rightBtn, switchEn, switch,seg,  dp, an, Rel,
IM );

    initial
        clk = 1;
    always
        begin
        #1;
        clk = ~clk;
        end

    initial begin
    #10; reset = 1;
    #15; reset = 0;
    #20; leftBtn = 1;
    #25; leftBtn = 0;
    #20; leftBtn = 1;
    #30; leftBtn = 0;
```

```
    #30; leftBtn = 1;
    #40; leftBtn = 0;
    #35; leftBtn = 1;
    end

endmodule
```