CSE 3203 CT 4 Assignment
Roll No: 1903179

Assignment : *Built a CPU based on following requirements:*

1. **Word Size of CPU = 3**
2. **ALU Operations = ADD, ROL, OR**
3. **Register Number = 5**
4. **Size of RAM = 7**
5. **Word size of ISA and RAM = 16**
6. **CPU Instructions = Branching(JC, JMP), Reg, Imm**

Solution:

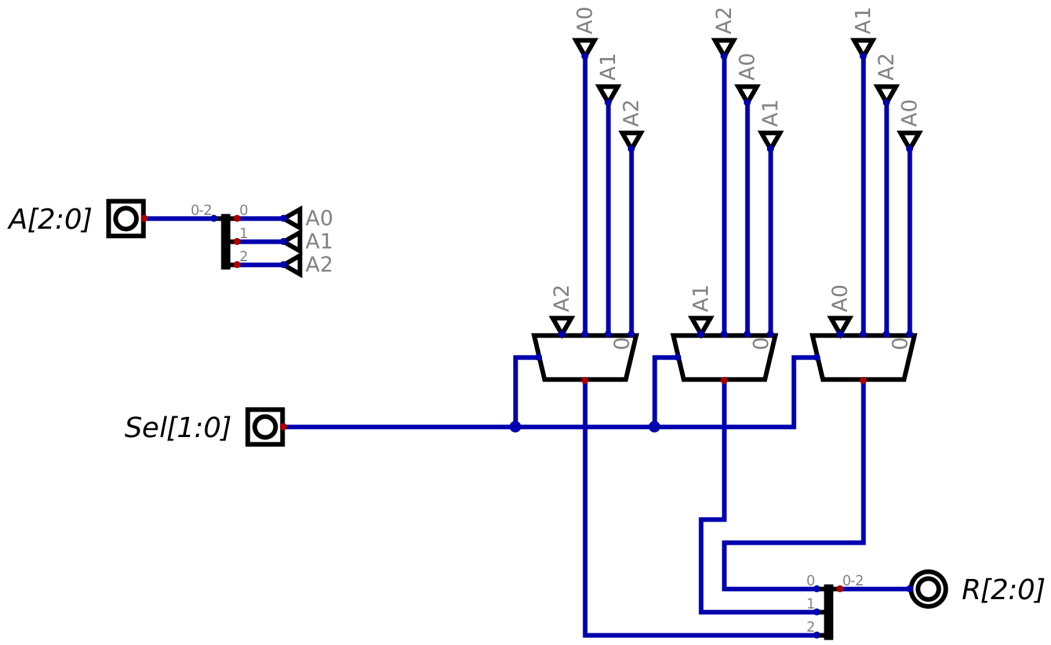
Video Link (Youtube Video Link): https://youtu.be/Rh-h33NvQTE

In the first 7 clock cycle, instructions from ROM were copied to RAM. Then the PCenable pin was turned to 1 and ROM was practically disabled. Instructions from RAM began executing in every clock cycle.

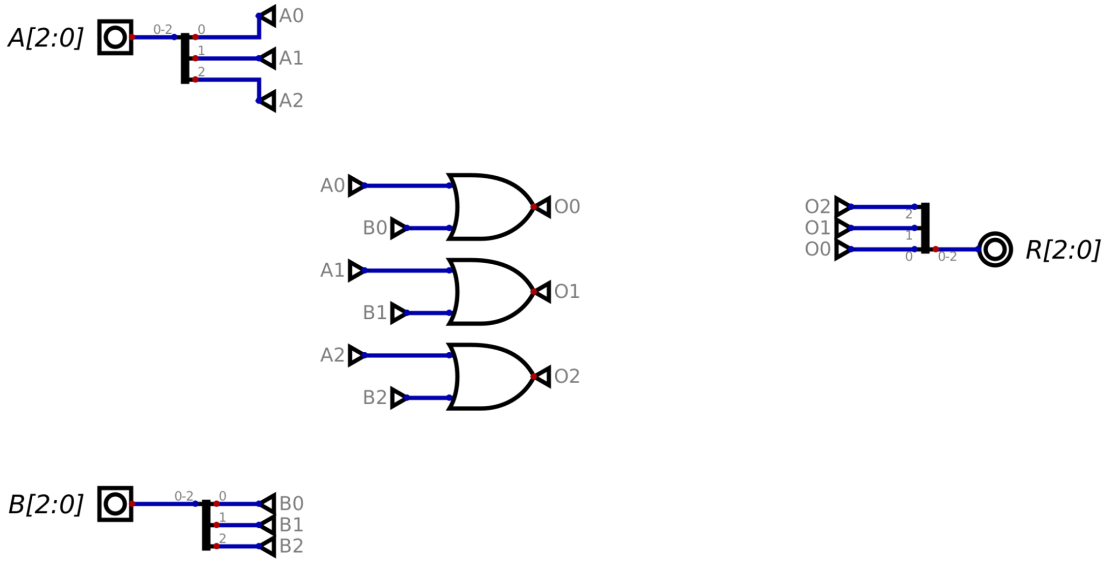
Simulator Design:

1. **ALU Circuit (Show all circuits except FA circuit)(Marks 5):**
   Check List:

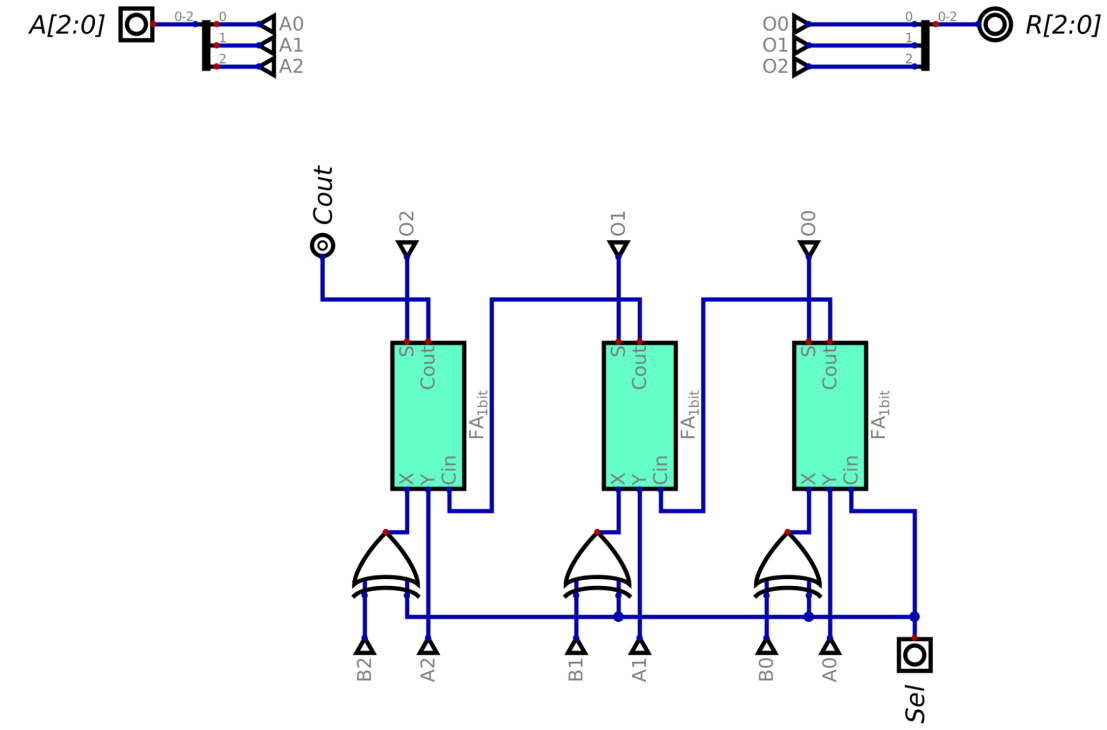
Have you added all circuits of ALU from FA to ALU Operations Circuits (ADD, XOR, SHL etc.) to Top Level ALU Circuit?	YES



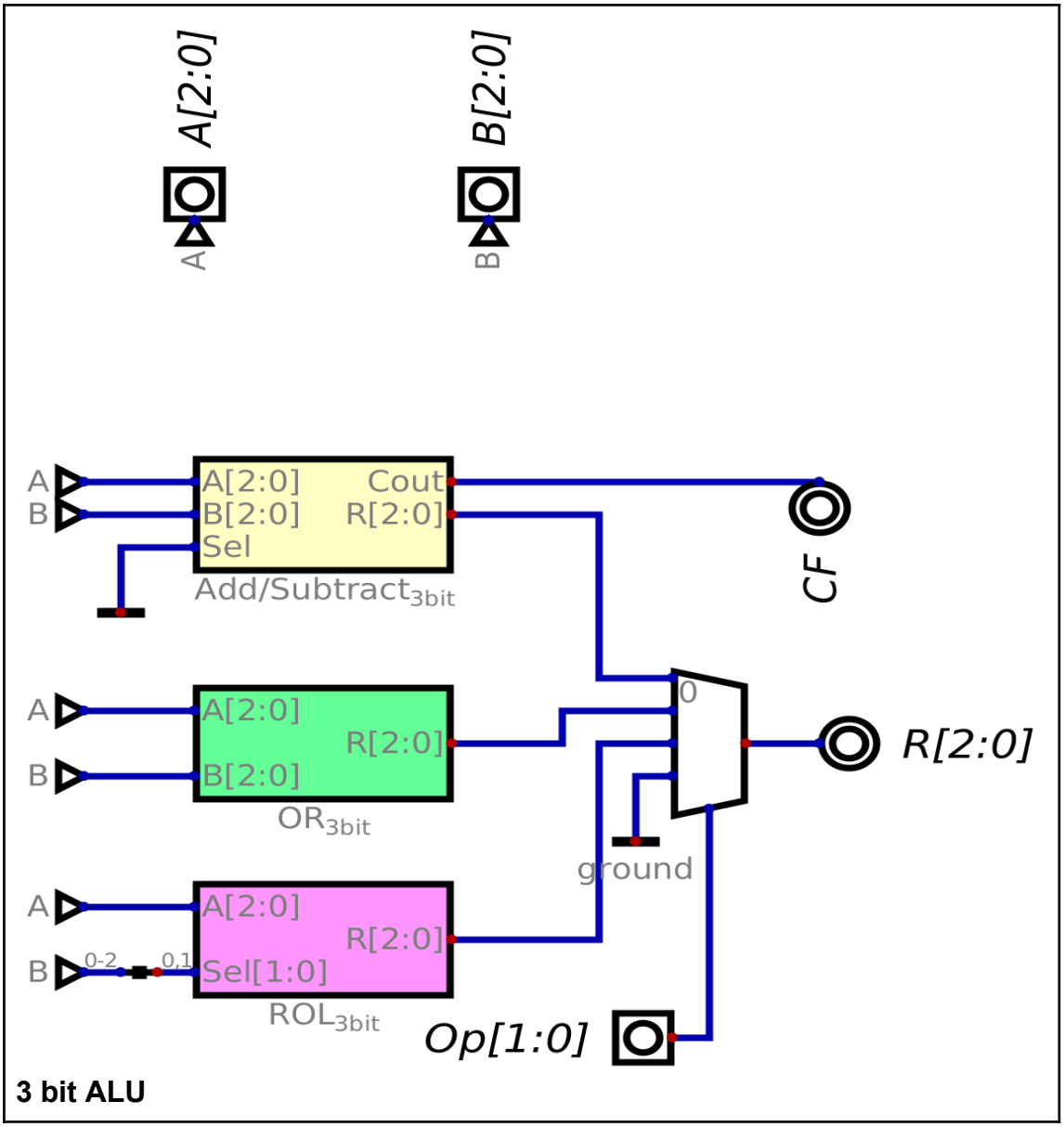
3 bit ROL



3 bit OR



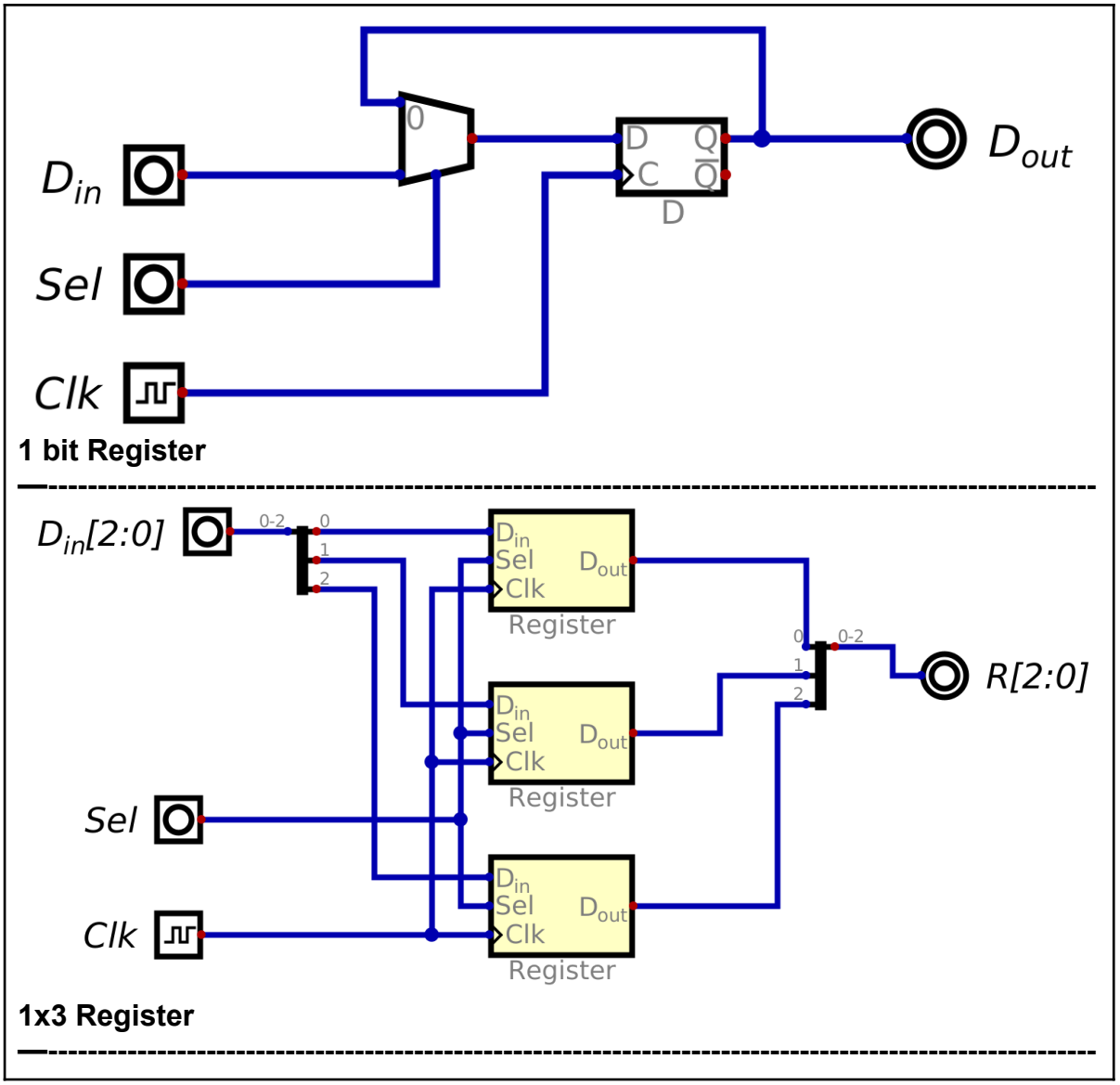
3 bit Adder

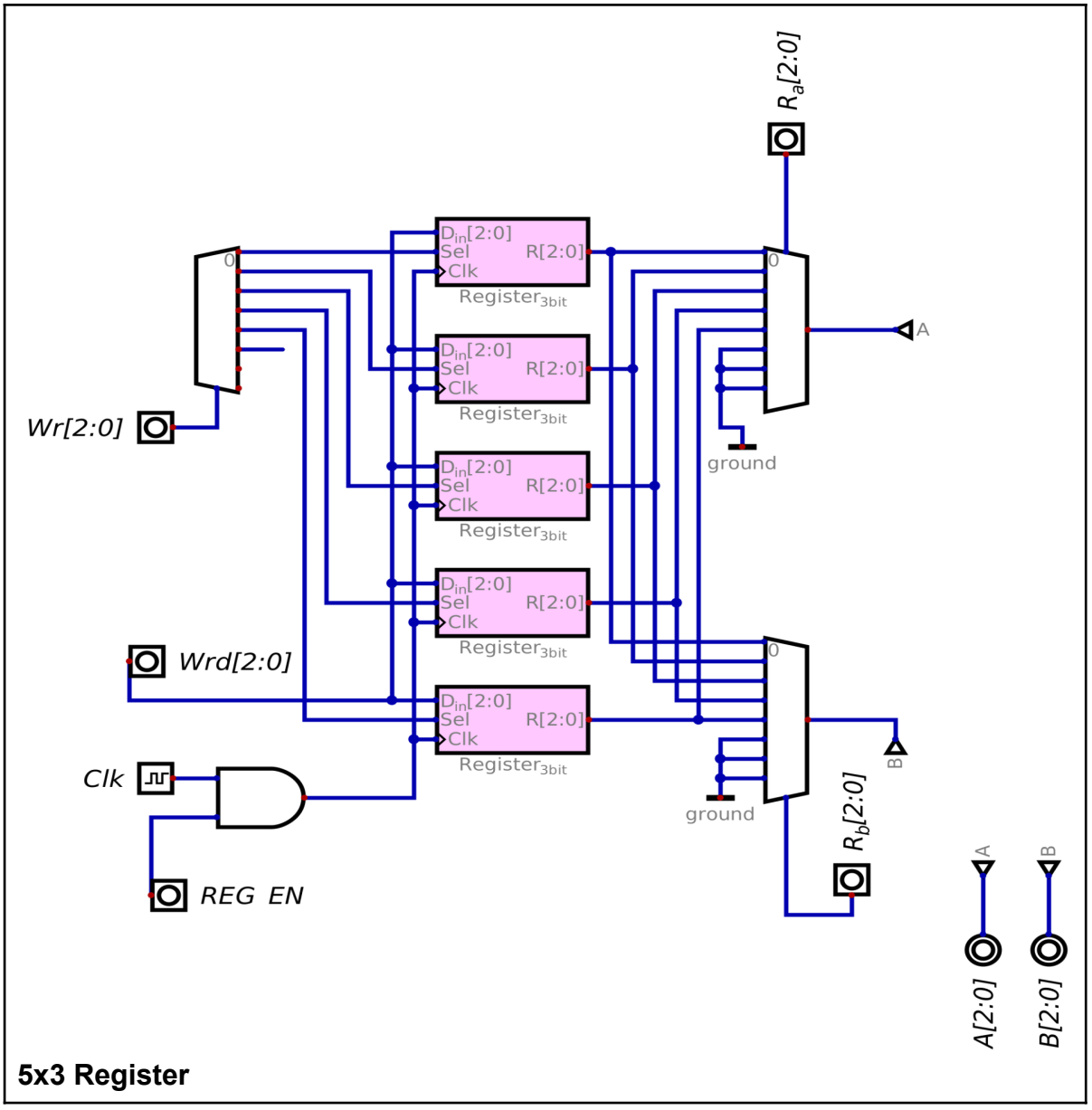


3 bit ALU

2. **Register Set Circuit (Top to Bottom all circuits)(5 Marks):**
   Check List:

Have you added all circuits of Register Set from 1 bit Register to n bit Register to Top Level Register Set Circuit.?	YES

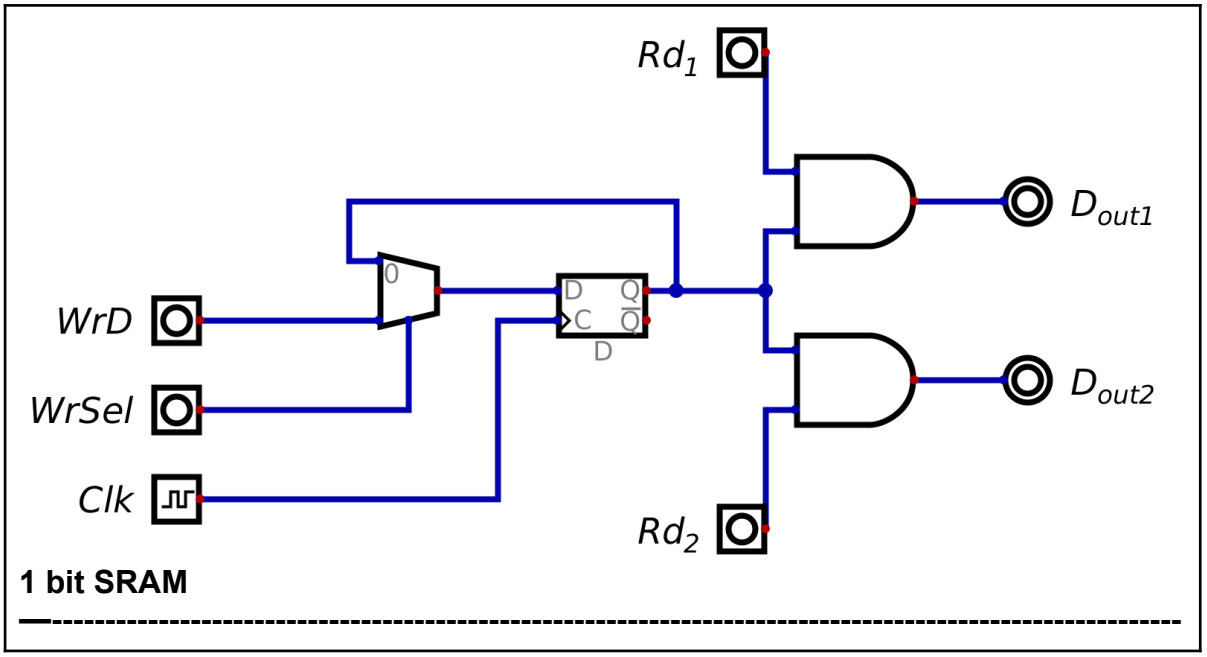

D_{in}
Sel
Clk
0
D
Q
C
$\overline{Q}$
D
D_{out}
1 bit Register
$D_{in}[2:0]$
0-2
0
1
2
D_{in}
Sel
Clk
D_{out}
Register
Sel
Clk
0-2
$R[2:0]$
1x3 Register



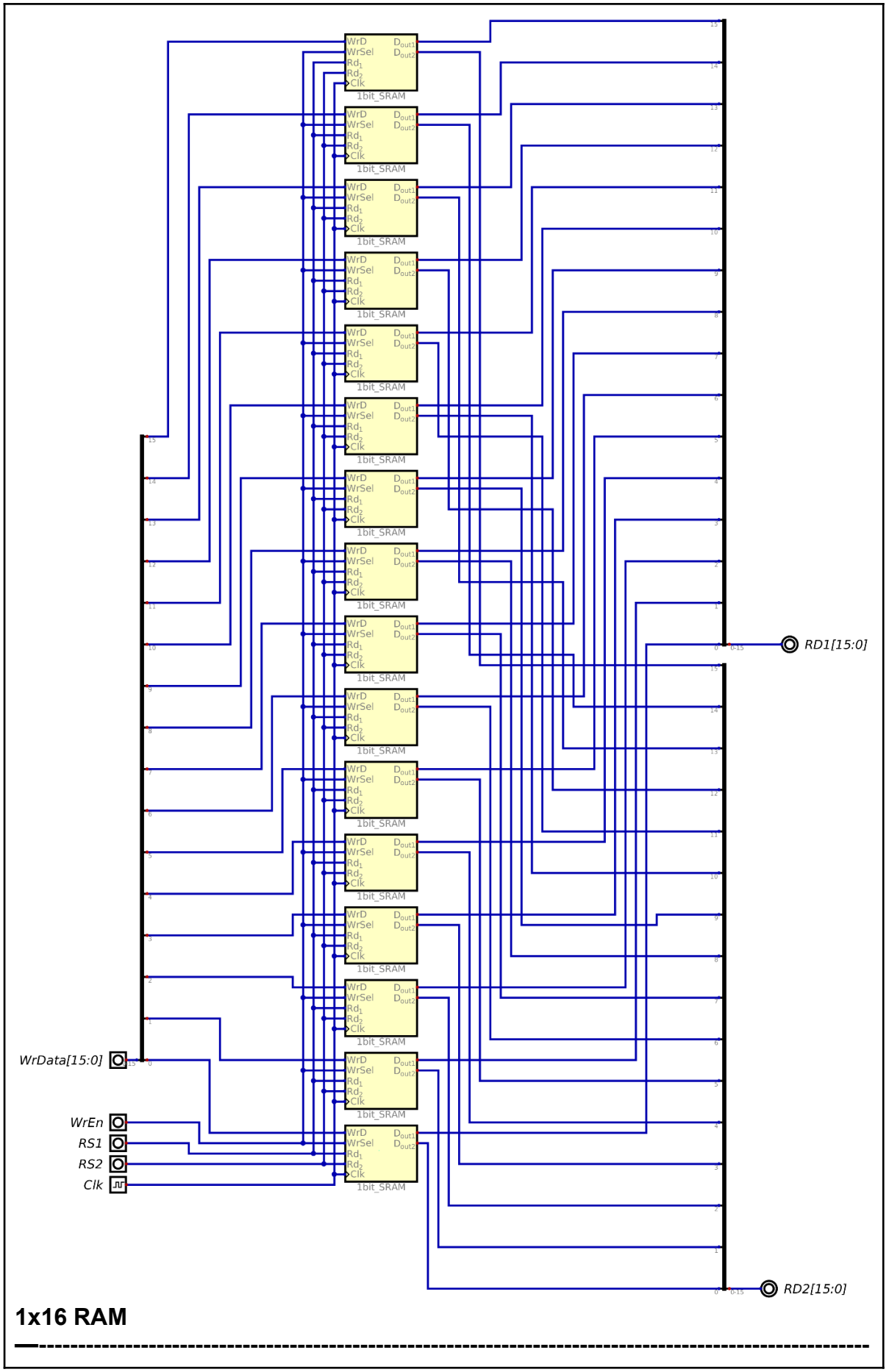
5x3 Register

3. **RAM Circuit (Top to Bottom all circuits)(5 Marks):**
   Check List:

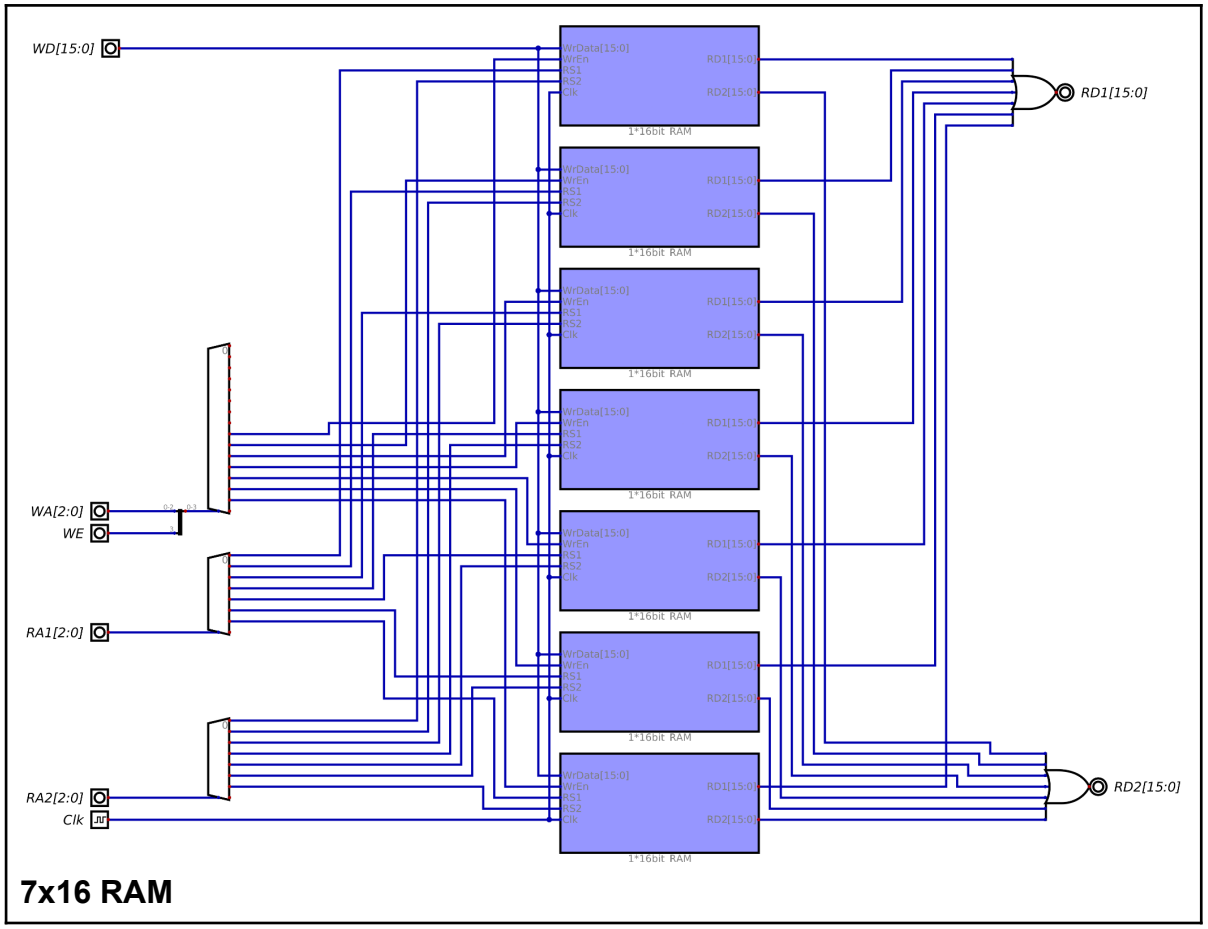
Have you added all circuits of RAM from 1x1 RAM to 1xN RAM to MxN RAM?	YES



1 bit SRAM


WrD
WrSel
Rd1
Rd2
Clk
Dout1
Dout2
1bit_SRAM
WrData[15:0]
WrEn
RS1
RS2
Clk
RD1[15:0]
RD2[15:0]

1x16 RAM



4. **a) ISA (2 Marks)**

Check List:

Have you added all ISA of CPU along with its sample machine code to be run on CPU?	YES
16 bit ISA with 7 addressable RAM and 5 addressable Register slots. CPU has 3 bit word size.	

ISA (Register Mode):

Opcode (4 bit)		Register 1	Register 2	Unused
2 bits	**2 bits**	**3 bits**	**3 bits**	**6 bit**
00	**00 -ADD 01 - OR 10 -ROL**	**Ra (000-100)**	**Rb (000-100)**	**XXXXXX**

ISA (Immediate Mode):

Opcode (4 bit)		Register 1	Constant	Unused

2 bits	2 bits	3 bits	3 bits	6 bit
01	00 -ADD 01 - OR 10 -ROL	Ra (000-100)	000-111	XXXXXX

ISA (Branching Mode):

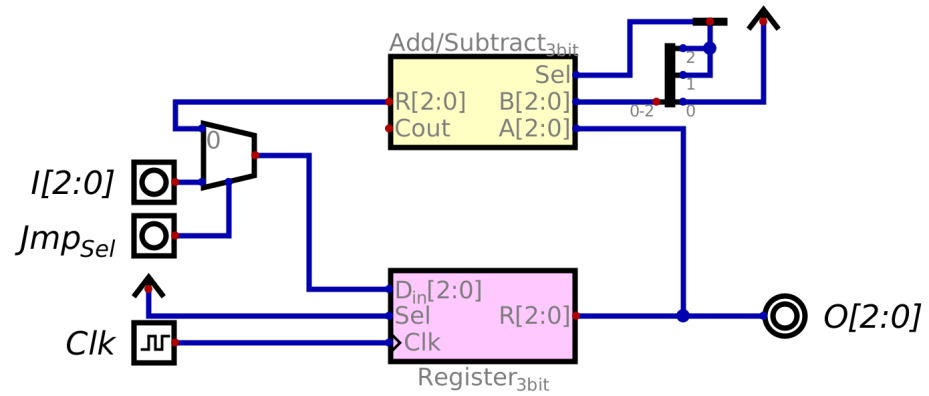
Opcode (4 bit)		Address	Unused
2 bits	2 bits	3 bits	9 bit
10	00 -JMP 01 - JC	000-110	XXXXXXXXX

Sample Machine Code with assembly code in comments to be run on CPU (You will make a video running this machine code on CPU in order to prove that your CPU is working perfectly)

Machine Code	Assembly Code
0100001101xxxxxx	ADD A1, 5
0110001001xxxxxx	ROL A1, 1
0001011001xxxxxx	OR A3, A1
0100001101xxxxxx	ADD A1, 5
1001001xxxxxxxxx	JC 1
0000011001xxxxxx	ADD A3, A1
0001011000xxxxxx	OR A3, A0
1000100xxxxxxxxx	JMP 4

b) CPU (Top to Bottom all circuits)(3 Marks):
Check List:

Have you added all circuits of CPU from Program Counter to Control Unit to Top Level CPU Circuit with **Output Pins showing contents of ALU, Register Set, RAM etc. (Important for CPU Verification, Check Tutorial Videos for Details)**?	YES

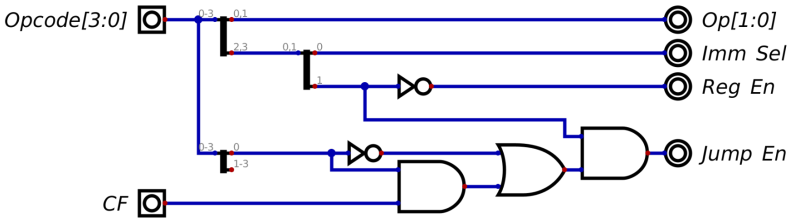


3 bit Program Counter

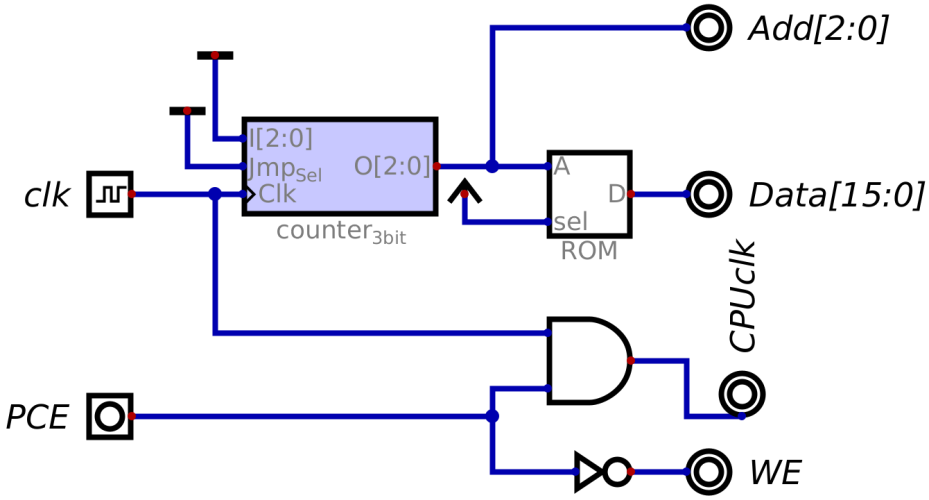
Reg
00 00 add
00 01 or
00 10 rol

Imm
01 00 add
01 01 or
01 10 rol

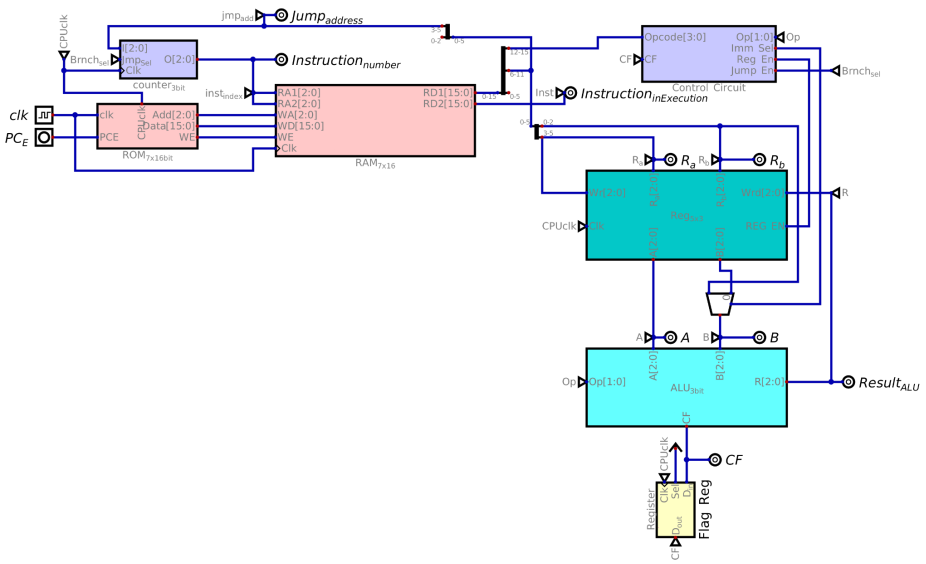
Brn
10 00 jmp
10 01 jc
10 10 xx



Control Logic



8x16 ROM

 3 bit CPU	
Have you made a video running this sample machine code on the CPU (1 instruction at a time in a similar way shown in video) in order to prove that your CPU is working perfectly. **CPU Simulation Video**	YES