PCIe enumeration in-stability issue in IDCEvo:-

Contents

1. Block Diagram showing Power-On-GPIO and Reset signals :-

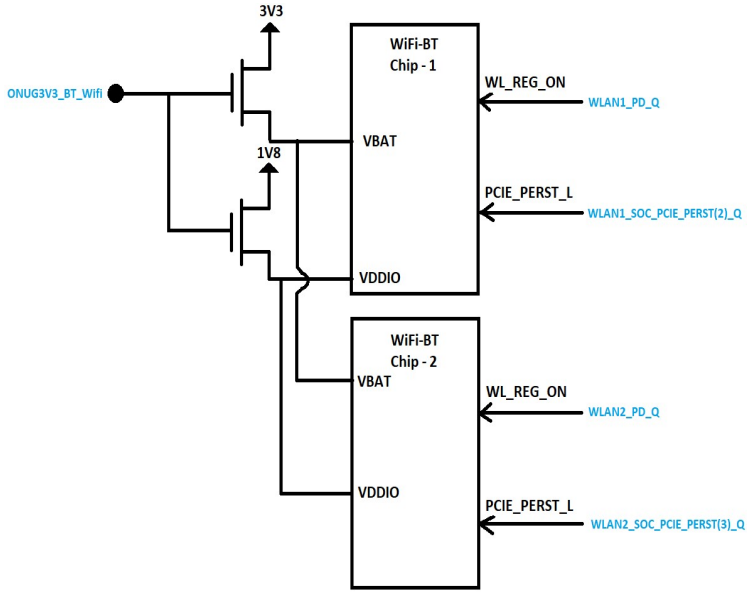

Figure – 1

2. Power-On-GPIO becoming high after PERST# is releasing, which is not correct:-

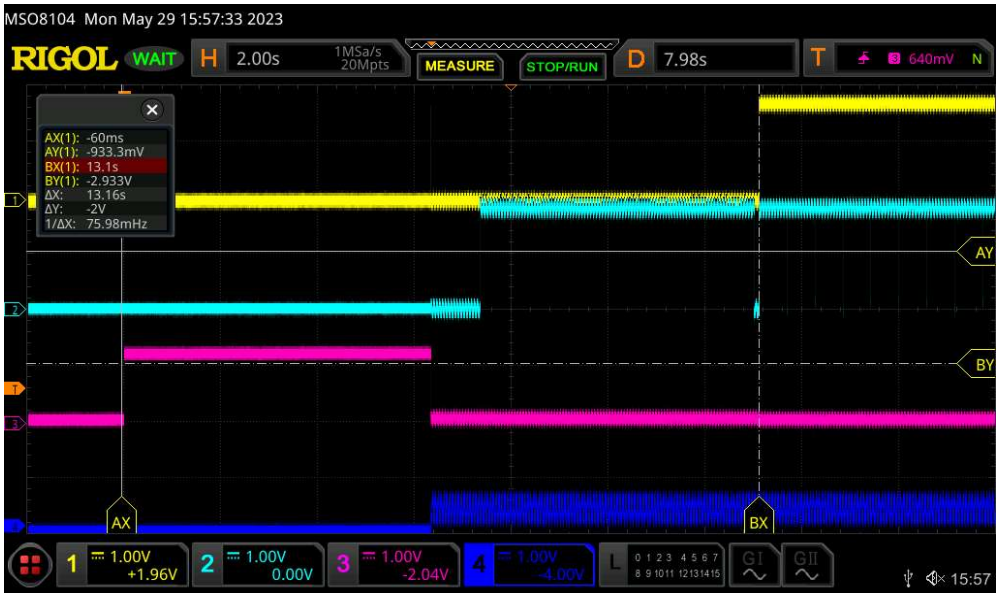

Figure – 2

Legend:

Yellow: ONUG3V3_BT_Wifi
Cyan: WLAN1_SOC_PCIE_PERST(2)_Q
Violet: WLAN1_SOC_PCIE_CLKREQ(2)_Q
Blue: WLAN1_SOC_PCIE2L_REFCLK0_P

The above waveform is not following PCIe compliance. Power to PCIe-Endpoint should become stable before release of PERST# signal.

Fix: - This we are correcting with a patch to Android-kernel repo, by asserting “ONUG3V3_BT_Wifi” signal in probe function of Exynos PCIe controller driver using “Pinctrl” select state.

3. Power sequence time diagram as per PCIe specification:-

As per PCIe specification “PCI Express® Card Electromechanical Specification Revision 3.0 July 21, 2013”, page No – 30, the initial power up sequence should be as below.

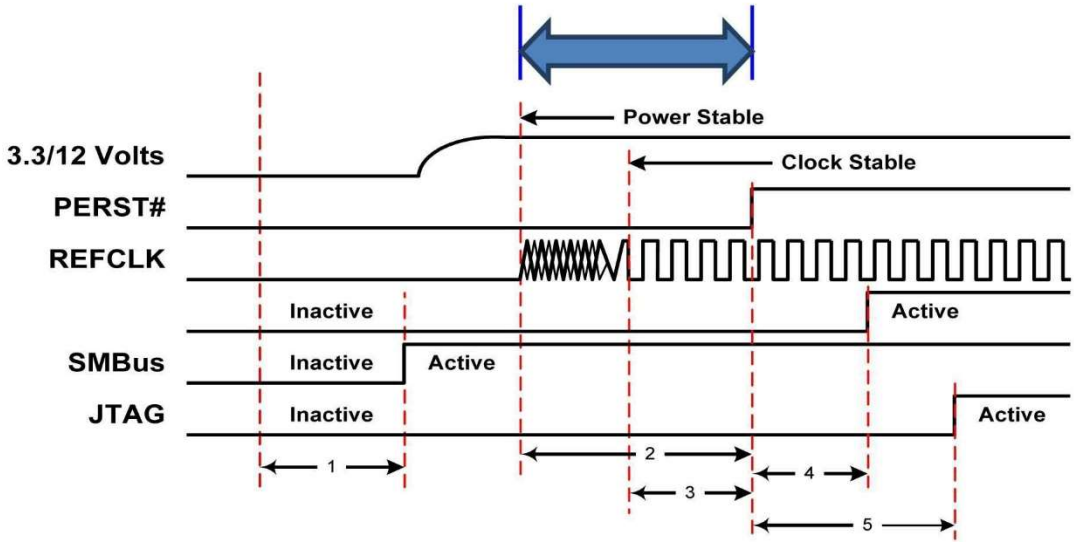

Figure - 3

Same we can see in WiFi chip (Cypress: CYW8x570) data sheet, page no - 86, Power to the chip should be stable before release of PERST# signal. It is shown below.

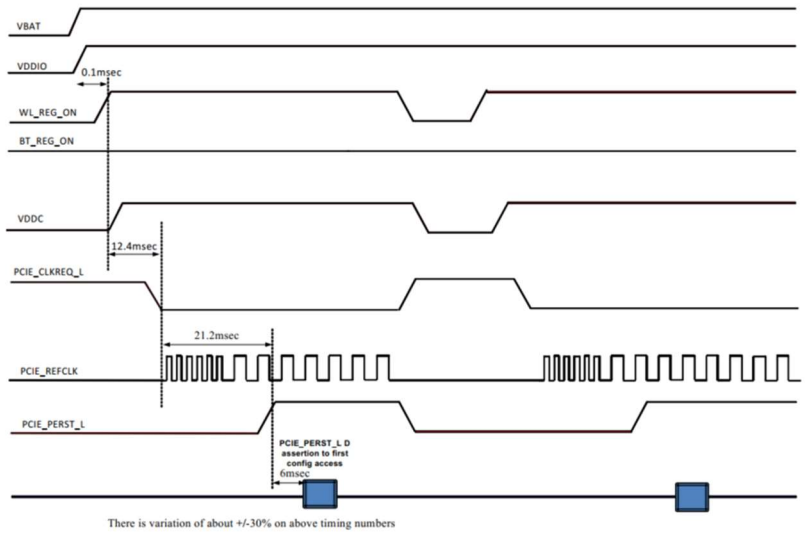

Figure – 4

4. Correction in power-up sequence with our patch:-

Figure – 5

Legend:

Yellow: ONUG3V3_BT_Wifi
Green: WLAN1_SOC_PCIE_PERST(2)_Q
Blue: WLAN1_SOC_PCIE_CLKREQ(2)_Q
Violet: WLAN1_SOC_PCIE2L_REFCLK0_P

5. Result:-

1. Power to Wifi chip is enabled about 11.54 seconds before release of PERST# signal.
2. PCIE_CLKREQ signal goes to LOW about 6.26s after Power to WiFi chip is stable.

It follows PCIe Electromechanical specification and WiFi chip data sheet.