ExynosAutoV9

ITMON

Revision 1.10
May 2021

Application Note

Important Notice

Samsung Electronics Co. Ltd. (“Samsung”) reserves the right to make changes to the information in this publication at any time without prior notice. All information provided is for reference purpose only. Samsung assumes no responsibility for possible errors or omissions, or for any consequences resulting from the use of the information contained herein.

This publication on its own does not convey any license, either express or implied, relating to any Samsung and/or third-party products, under the intellectual property rights of Samsung and/or any third parties.

Samsung makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Samsung assume any liability arising out of the application or use of any product or circuit and specifically disclaims any and all liability, including without limitation any consequential or incidental damages.

Customers are responsible for their own products and applications. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by the customer's technical experts.

Samsung products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Samsung product could reasonably be expected to create a situation where personal injury or death may occur. Customers acknowledge and agree that they are solely responsible to meet all other legal and regulatory requirements regarding their applications using Samsung products notwithstanding any information provided in this publication. Customer shall indemnify and hold Samsung and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim (including but not limited to personal injury or death) that may be associated with such unintended, unauthorized and/or illegal use.

Samsung Electronics Co., Ltd.
1-1,Samsungjeonja-ro,Hwaseong-si,
Gyeonggi-do Korea 18448

Contact Us: *myunggeun.ji@samsung.com*

Home Page: *http://www.samsungsemi.com*

Trademarks

All brand names, trademarks and registered trademarks belong to their respective owners.

- Exynos, FlexOneNAND, and OneNAND are trademarks of Samsung Electronics.
- ARM, Jazelle, TrustZone, and Thumb are registered trademarks of ARM Limited.
- Cortex, ETM, ETB, Coresight, ISA, and Neon are trademarks of ARM Limited.
- Java is a trademark of Sun Microsystems, Inc.
- SD is a registered trademark of Toshiba Corporation.
- MMC and eMMC are trademarks of MultiMediaCard Association.
- JTAG is a registered trademark of JTAG Technologies, Inc.
- Synopsys is a registered trademark of Synopsys, Inc.
- I2S is a trademark of Phillips Electronics.
- I2C is a trademark of Phillips Semiconductor Corp.
- MIPI and Slimbus are registered trademarks of the Mobile Industry Processor Interface (MIPI) Alliance.

All other trademarks used in this publication are the property of their respective owners.

Chip Handling Guide

Precaution against Electrostatic Discharge

When using semiconductor devices, ensure that the environment is protected against static electricity:

1. Wear antistatic clothes and use earth band.
2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

Contamination

Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

Revision History

Revision No.	Date	Description	Author(s)
1.00	April, 2021	• Initial version of the document	S.LSI
1.10	May, 2021	• Applied reviewed comment	S.LSI

TABLE OF CONTENTS1 ITMON (IPS TRAFFIC MONITOR) 12

List of Figures

Figure Number	Title	Page Number

목차 항목을 찾을 수 없습니다.

List of Tables

Table Number	Title	Page Number

목차 항목을 찾을 수 없습니다.

List of Examples

List of Conventions

Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
W	Write Only	The application has permission to write in the Register field.
RW	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1'b1 and clears it by writing 1'b0.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

List of Terms

Terms	Descriptions

List of Acronyms

Acronyms	Descriptions

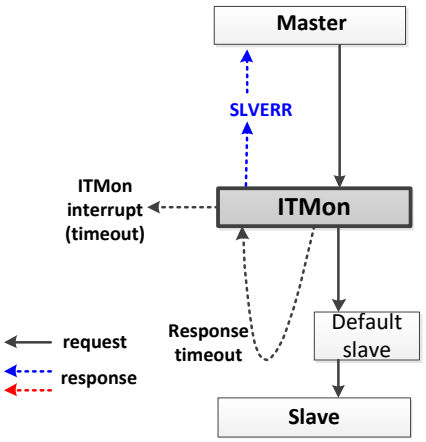
1 ITMon (IPs Traffic Monitor)

1.1 Background

IPs Traffic Monitor (ITMon) is a H/W debugging unit which helps to identify slaves that generate bus error responses and deadlocks. Whenever a master requests a transaction from a slave, the transaction is logged with ITMon and responded from a slave through the bus. ITMon supports triggering a bus timeout and propagating bus errors.

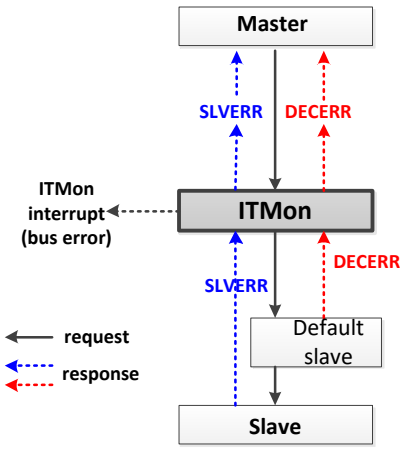
1.1.1 Bus Timeout Triggering

A bus timeout function was developed to avoid situations where ARM cores gets locked up in terms of hardware. Once a master requests data from a slave, it would waits for a response to its request from the slave. If the slave is powered off, the master would wait infinitely. On this condition, if the other master such as an ARM core issues another requests to a slave using the same bus path, the ARM cores also waits infinitely until the bus is free from the occupation of the previous master. This kind of deadlock situations would leads to an ARM core lock-up



A master on the bus interfaces with multiple slaves by requesting data transactions. If there is no response from a slave after some requests are issued by way of the bus, this monitor unit creates an error response on the bus after waiting for specified cycles and also generates an ITMon interrupt pointing out the bus timeout. Also, ITMon returns SLVERR on the bus instead of the slave which cannot return the request.

1.1.2 Bus Error Propagation



The ITMon has a capability to propagate bus errors (SLVERR and DECERR) to the master which issues the data transaction request. The originator of these bus errors can be either slaves or ITMon itself. When the bus error arrives at the master, reactions to the bus error response varies by bus master. A DMAable IP would generate an interrupt, whereas other DMAable IPs does nothing on the same condition. In case of ARM cores, when the bus error comes back, a dedicated abort (SError) would be triggered to the cores. (Please refer to https://developer.arm.com/documentation/102412/0100/Exception-types)

1.2 How to understand ITMon log in a guest OS kernel log

```
ITMON Detected: 27 irq, PERIO_CORE group, 0x28 vec, err_cnt:0 err_cnt_by_cpu:0
-------------------------------------------------------------------------
     ITMON Report (READ)
-------------------------------------------------------------------------
     PATH Information
Internal error: Oops - bad mode: 0 [#1] PREEMPT SMP
     >       SCI_IRPM,   M_NODE(0x1BA43040)
     >  PDCORE_PBUSMC, T_S_NODE(0x1BA13040)
     >  PDCORE_PBUSMC, T_M_NODE(0x1CA63040)
     >          SIREX,   S_NODE(0x1CA13040)
-------------------------------------------------------------------------
     Transaction Information

     > Master         : CPU0 Cluster1
     > Target         : SIREX
     > Target Address : 0xED60000
     > Type           : READ
     > Error code     : Error Detect by the Slave(SLVERR)
     > Size           : 4 bytes x 1 burst => 4 bytes
     > Burst Type     : 1 (0:FIXED, 1:INCR, 2:WRAP)
     > Level          : Privileged access
     > Protection     : Non-secure access
     > Path Type      : PERI(SFR) Path transaction (0x0 ~ 0x1fff_ffff)
-------------------------------------------------------------------------
```

Master : Which master initiates this data transaction ?

Target : Which slave's resource does the master try to access ?

Target Address : At which address does the master access the resource of the slave ?

Type : Is the master trying to do Read access or Write access ?

Error code : Which error does ITMon relay or generates ?

SLVERR : A real slave, a protection unit(SFMPU), or ITMon replies to the master's access request with this AXI bus error response.

DECERR : A protection unit(TZPC or SFASC) or a default slave returns the masters' access request with this AXI bus error response.

Timeout : When there is no reply with a certain period of time from a slave to an access request of a master , ITMon generates a bus timeout interrupt to GIC (and replies with SLVERR to the masters' request).

Protection : Which world does the master belongs to (secure world or normal(non-secure) world) ?

Path Type : Which physical memory does the target address falls under (PERI(SFR) or DRAM memory) ?

1.2.1 Blocks

Master and Target will be one of the following HW blocks. Other useful information is also available at the ExynosAuto user manual Chapter 1.5 Bus Interconnects

- ACC : Part of ISP (Camera)
- ALIVE : Alive power block
- AUD : Audio block including HiFi4 DSP
- BUSC : Bus block including Security IPs (SSS, SIREX, RTIC)
- BUSMC : Bus block including PDMA
- CMU : Clock management unit
- CORE : Bus block located in the center of the chip
- CPUL0 : Enyo CPU Cluster 0
- CPUL1 : Enyo CPU Cluster 1
- DPTX : Display
- DPUM : Display
- DPUS : Display
- FSYS0 : PCIe & relative HW IPs(SYSMMU, Interrupt and so on),
- FSYS1 : USB
- FSYS2 : Ethernet & relative HW IPs, UFS
- G2D : G2D & relative HW IPs, JPEG, M2M Scaler
- G3D0 : MP3 GPU
- G3D1 : MP12 GPU
- ISPB : ISP block
- MFC : Video codec HW
- MIF : Memory controller

- NPU0 : NPU block
- NPU1 : NPU block
- PERIC0 : USI0 ~ USI5
- PERIC1 : USI6 ~ USI11
- PERIS : Interrupt controller, OTP, TMU, Watchdog
- RTC : Real Time Clock
- SFI : Safety Island
- TAA : 3AA camera IP (auto focusing, auto white balancing, auto exposure)
- TAA2 : 3AA camera IP 2nd instance

1.2.2 Target address

If operation is related with specific purpose to the internal HW blocks, please refer to the Exynos Auto V9 user manual Chapter 3 Memory Map

1.3 3 Types of ITMon Logs

1.3.1 Timeout error

```
--------------------------------------------------------------------------
      ITMON Report (READ)
--------------------------------------------------------------------------
      PATH Information
 >       SCI_IRPM,   M_NODE(0x1AA43040)
 >      CORE_BUSC, T_S_NODE(0x1AA13040)
 >      CORE_BUSC, T_M_NODE(0x1B5C3040)
 >         PERIC1,   S_NODE(0x1B4A3040)
--------------------------------------------------------------------------
      Transaction Information

      > Master         : CPU0 Cluster1
      > Target         : PERIC1
      > Target Address : 0x10870048
      > Type           : READ
      > Error code     : Timeout error - response timeout in timeout value
      > Size           : 4 bytes x 1 burst => 4 bytes
      > Burst Type     : 1 (0:FIXED, 1:INCR, 2:WRAP)
      > Level          : Privileged access
      > Protection     : Non-secure access
      > Path Type      : PERI(SFR) Path transaction (0x0 ~ 0x1fff_ffff)
--------------------------------------------------------------------------
```

1.3.2 SLVERR

Slave error is used when the access has reached the slave successfully, but the slave wishes to return an error condition to the originating master.

```
-------------------------------------------------------------------------------
      ITMON Report (READ)
-------------------------------------------------------------------------------
      PATH Information
      >       SCI_IRPM,   M_NODE(0x1AA43040)
      >      CORE_POP1, T_S_NODE(0x1AA03040)
      >      CORE_POP1, T_M_NODE(0x1AC03040)
      >         CPUCL1,   S_NODE(0x1AC53040)
-------------------------------------------------------------------------------
      Transaction Information

      > Master         : CPU0 Cluster1
      > Target         : CPUCL1
      > Target Address : 0x1D120120
      > Type           : READ
      > Error code     : Error Detect by the Slave(SLVERR)
      > Size           : 4 bytes x 1 burst => 4 bytes
      > Burst Type     : 1 (0:FIXED, 1:INCR, 2:WRAP)
      > Level          : Privileged access
      > Protection     : Non-secure access
      > Path Type      : PERI(SFR) Path transaction (0x0 ~ 0x1fff_ffff)
-------------------------------------------------------------------------------
```

1.3.3 DECERR

Decode error is generated typically by an interconnect component, to indicate that there is no slave at the transaction address.

```
-------------------------------------------------------------------------------
      ITMON Report (READ)
-------------------------------------------------------------------------------
      PATH Information
      >        BUSC_DP,   M_NODE(0x1B9B3040)
      >          FSYS0,   M_NODE(0x1B113040)
      >      BUSC_CORE, T_S_NODE(0x1B833040)
      >      BUSC_CORE, T_M_NODE(0x1AC13040)
      >          ALIVE,   S_NODE(0x1AC83040)
-------------------------------------------------------------------------------
      Transaction Information

      > Master         : BUSC_DP
      > Target         : ALIVE
      > Target Address : 0x0
      > Type           : READ
      > Error code     : Decode error(DECERR)
      > Size           : 4 bytes x 2 burst => 8 bytes
      > Burst Type     : 1 (0:FIXED, 1:INCR, 2:WRAP)
      > Level          : Unprivileged access
      > Protection     : Non-secure access
      > Path Type      : PERI(SFR) Path transaction (0x0 ~ 0x1fff_ffff)
-------------------------------------------------------------------------------
      >        BUSC_DP,   S_NODE(0x1B1E3040)
-------------------------------------------------------------------------------
```

<End Of Document>