ES_SAF400x

Errata sheet SAF400x

Rev. 0.6 — 10 October 2017 Errata sheet

Document information

Info	Content
Keywords	Mercury, SAF400x, Errata
Abstract	This document describes deviations of the SAF400x release

Revision history

Rev	Date	Description
0.1	20160308	First version; MRA1 gate
0.2	20160914	A1 gate
0.3	20170607	V1 gate
0.4	20171005	A2 gate
0.5	20171114	Updated with MS3174
0.6	20171116	Update of MS3174 after review

Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

This document describes the functional or performance deviations of the SAF400x (nickname: Mercury) from the datasheet.

2. Product identification

Table 1. Revision overview table

Revision identifier	Revision description
SAF400x ES2	Silicon (ES2.0) provided to Customers
Reference Board: n.a.	Board release
Software: n.a.	Functionality according to the software release notes.

3. Errata overview

Table 2. Errata summary table

Erratum ID	Short description	Detailed description
MS1528	JTAG password change	Section 4.1
MS1599	Triple DAB ensemble reception	Section 4.2
MS1697	Audio ADC performance	Section 4.3
MS1805	Power-On-Reset for 1V2	Section 4.4
MS1825	DAB sensitivity	Section 4.5
MS1952	AM sensitivity	Section 4.6
MS2232	FM AGC	Section 4.7
MS2321	AM Power supply rejection	Section 4.8
MS2316	WBT0 performance at high voltage	Section 4.8
MS2366	Pin changes between ES1 and ES2 (removed power pair)	Section 4.10
MS2428	Phase diversity Mercury/Titan and Merlin	Section 4.11
MS2544	AM AGC	Section 4.12
MS1444	Additional functionality: AM Wideband Noise Cancellation	Section 4.13
MS3174	IIS3_SD0 to be configured as input	Section 4.14

4. Errata details

4.1 MS1528: JTAG password change

Description:

For debugging and developing software on HiFi3, JTAG debugging is supported. In the JTAG initialization sequence, a password needs to be provided to open the JTAG port. The password for ES2 will be different compared to ES1.

Status:

Consequences for user of ES1:

- Besides access to the HiFi3 processor, also the HiFi2 and BBE16 processors are visible for the JTAG debugger.

Solution for Mercury ES2:

A new JTAG password is provided for ES2 for the new software releases, requiring an update of the JTAG initialization sequence. The BBE16 and HiFi2 processors are not visible for the JTAG debugger.

4.2 MS1599: Triple DAB ensemble reception

Description:

The baseband receiver of Mercury should be able to decode three full-DAB ensembles concurrently. The baseband receiver consists of combination of hardware processing blocks and software processing blocks. For ES1, one of the hardware processing blocks (de-interleaver) is not capable of decoding three full-ensembles.

Status:

Consequences for user of ES1:

- Mercury ES1 can support decoding of 2 full-ensembles concurrently.

Solution for Mercury ES2:

A hardware update in ES2 will enable the hardware processing block to decode three full-ensembles concurrently.

4.3 MS1697: Audio ADC performance

Description:

In order to optimize audio ADC performance, a process calibration loop is performed at system boot. This calibration loop is not operating properly in ES1.

Status:

Consequences for user of ES1:

- A few Mercury samples (worst-case process corner) might have a degraded performance in the audio ADC.

- The THD of the audio ADC of these samples will be increased by 10-20 dB compared to other samples.
- Updated calibration values can be provided to improve the THD again. These values can be downloaded by the host.

Solution for Mercury ES2:

The process calibration loop works as expected in ES2. The THD of the audio ADC will be similar for all process corners. Corner silicon for ES2 is being validated.

4.4 MS1805: Power-On-Reset for 1V2

Description:

The Power-On-Reset (POR) is not triggered when the 1V2 supply has a slow ramp. A ramp is slow if the time is 2.5ms/V or longer.

Status:

Consequences for user of ES1:

- In case of a slow voltage ramp, the POR is not triggered and the device is not starting properly.
- The following solutions are possible on ES1:
    1. Use a supply with a fast ramp time for the 1V2 supply OR
    2. Keep the pin RESET_N low until the 1V2 supply is above 1V0

Solution for Mercury ES2:

A hardware update is implemented in Mercury ES2 such that a slower ramp is supported. Corner silicon for ES2 is being validated.

The solutions for ES1 remain working for ES2.

4.5 MS1825: DAB sensitivity

Description:

DAB sensitivity is lower compared to the target specification of -102 dBm (typical).

Status:

Consequences for user of ES1:

- For DAB channels 6B and 11C, the sensitivity will be around -100 dBm.
- The sensitivity for the other channels will be around -101 dBm.

Figure 1 shows the measured sensitivity for Mercury ES1. The green line represents the measured values.

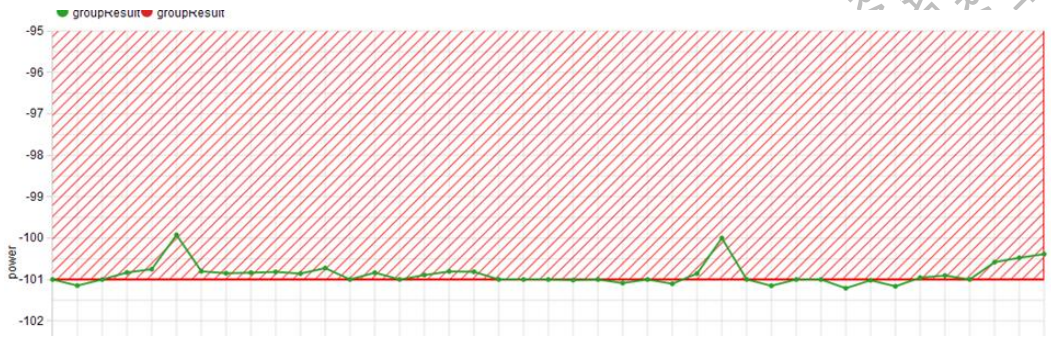

Figure 1 DAB sensitivity

Solution for Mercury ES2:

A hardware update is implemented in Mercury ES2 such that:

- the noise figure for DAB is improved,
- the gain of the signal is increased.

Corner silicon for ES2 is being validated.

4.6 MS1925: AM sensitivity

Description:

AM sensitivity is lower compared to the target specification.

Status:

Consequences for user of ES1:

- AM sensitivity for ES1 depends on the AM band (AM-LW, AM-MW and AM-SW)
- Sensitivity is approximately 0.5dB lower for AM-SW and up to 2dB for AM-LW and AM-MW.
- Therefore, DRM30 and HD-AM will have lower sensitivity. It will be 0.5 dB (AM-SW band) to 2 dB (AM-LW and AM-MW) lower.

Solution for Mercury ES2:

A hardware update is implemented in Mercury ES2 such that the noise figure for AM is improved.
Corner silicon for ES2 is being validated.

4.7 MS2232: FM AGC

Description:

Automatic Gain Control (AGC) for FM has the following limitations on ES1:

- AGC hysteresis can vary over threshold settings,

- The starting point of the RF-AGC can be too low,
- The overall FM AGC range is too low.

Status:

The AGC behavior of ES1 will be different compared to ES2 under varying signal conditions.

Solution for Mercury ES2:

A hardware and software update is implemented in Mercury ES2 such that AGC starting-point and range is as specified.

4.8 MS2321: AM Power supply rejection

Description:

AM PSRR is insufficient when applying at 1V8 supply a 100Hz or 1kHz 100mVpp ripple. Such ripple on the supply will leads to audio output ripples beyond -60 dB in AM with respect to the nominal audio level.

Status:

Ripples on audio can be expected using ES1 under these conditions.

Solution for Mercury ES2:

A hardware update is implemented in Mercury ES2 such that the PSRR for AM is according to specification.

4.9 MS2316: WBT0 performance at high voltage

Description:

For voltages above 1V25, the output of Wideband Tuner 0 (WBT0) can have bit errors. The bit errors occur in the IQ-signal before decimation. This is related to a timing issue in the digital part of ES1.

The bit errors affect tuner performance for AM, FM and DAB.

Status:

For ES1, the digital voltage should remain below 1V25 to prevent bit errors in the IF path. WBT1 is not affected by this timing issue.

Solution for Mercury ES2:

A hardware update is implemented in Mercury ES2 such that the timing issue is corrected. Corner silicon for ES2 is being validated.

4.10 MS2366: Pin changes between ES1 and ES2 (removed power pair)

Description:

A power pair for VDDM (memory supply pins) will not be connected in ES2. Affected pins are R2 and R4. The figure below shows the different pinning between ES1 and ES2.

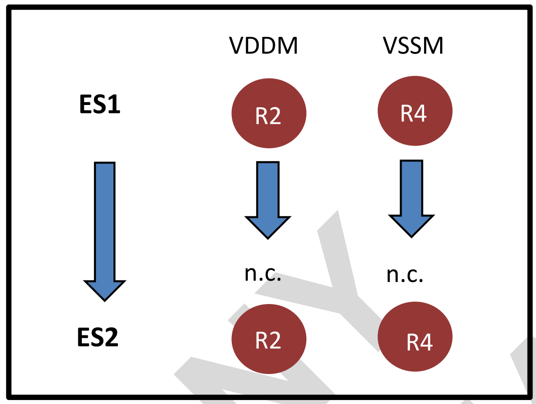

Figure 2 Pin change ES1 and ES2

Status:

The memory power supply pair can result in interferences in AM, FM and DAB. These interferences can degrade the tuner performance.

Solution for Mercury ES2:

Pins R2 and R4 are not connected in ES2. Board design for ES1 is compatible to ES2. Corner silicon for ES2 is being validated.

4.11 MS2428: Phase diversity Mercury/Titan and Merlin

Description:

Mercury/Titan and Merlin can be connected for FM phase diversity using a I2PD connection.

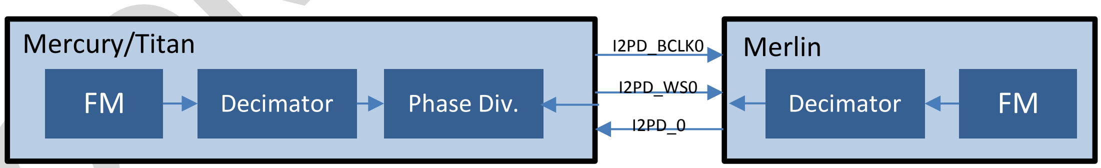

Figure 3 Mercury/Titan and Merlin connections

Mercury/Titan receives FM data from Merlin and synchronizes the data between the internal FM tuner and the FM data received from Merlin. Due to a limitation in Mercury ES1 hardware, the performance of phase diversity is limited for multi-path conditions.

Status:

The mentioned performance degradation is not applicable for:

- Phase diversity with the internal tuners of Mercury / Titan
- Phase diversity between Mercury and Titan

Solution for Mercury ES2:

Hardware in Mercury ES2 is updated such that phase diversity with Mercury/Titan and Merlin has the expected performance. Software developed for ES1 can also be used for ES2.

4.12 MS2345: AM AGC

Description:

For frequencies above 10 MHz, hysteresis for some AM AGC steps is limited. This also applies for DRM30

Status:

For strong signals, the performance of Mercury ES1 will be reduced due to this issue.

Solution for Mercury ES2:

A hardware update is implemented in Mercury ES2 such that the hysteresis for AM steps is according to specification.

4.13 MS1444: Additional functionality: AM Wideband Noise Cancellation

Description:

AM cancellation requires a noise probe (DiRaNA5 in diagram). In order to reduce the noise from an AM broadcast, Mercury subtracts the probe signal from the received AM signal.

The figure below shows a set-up with Mercury and DiRaNA5:

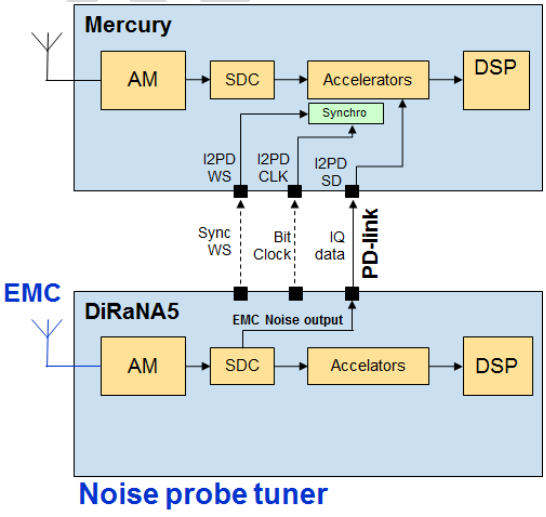

Figure 4 AM Wideband Noise Cancellation

Mercury ES2:

The added hardware is available in Mercury ES2 to perform noise cancellation. Signal decimation is done in HW (using accelerators) as this is MIPS intensive. Cancellation is done in software on a DSP for flexibility and algorithm refinements. The I2PD interface is used for IQ data and control bits and synchronization is done in Mercury (in the set-up of Figure 4). The software is under development.

Note that Merlin is not compatible with this set-up.

4.14 MS3174: IIS3_SD0 to be configured as input

Description:

IIS3 synchronous output and IIS3 asynchronous output is not implemented in ROM.

Status:

IIS3 can be configured as synchronous input and asynchronous input. IIS3_SD0 can be configured as input only.

Mercury ES2:

A software update in ROM will enable output functionality on IIS3_SD0.

5. Solved Errata Items

This section lists the items that have been solved.

Table 3. Solved Errata items table

Erratum ID	Short description	Detailed description
MS1484	SPI read	Section 5.1
MS1500	Power-up sequencing	Section 5.2
MS1514	Pin changes between ES1 and ES2 (additional power pair)	Section 5.3
MS1373	Memory access	Section 5.4
MS1217	Primary boot loader system hang-up	Section 5.5
MS1516	Primary boot loader	Section 5.6
MS2345	Spurious response	Section 0
MS1915	Additional functionality: BiQuad accelerator for HiFi3	Section 5.8

5.1 SOLVED MS1484: SPI read

Description:

During a read on the SPI MISO line of Mercury, the data can be shifted by 1 bit.

Status:

The following requirements apply for host software in combination with Mercury ES1:

- Mercury host protocol can detect this bit shift using CRC
- Host software to execute CRC check for a fixed-size frame
- In case of a bit shift, host has to perform frame correction.

NXP Radio driver for host incorporates this workaround. Host software can use this radio driver as reference.

Solution for Mercury ES2:

The hardware in Mercury ES2 will be updated such that the bit shift will not occur.

Host software for ES2 is backwards compatible to ES1. No change in software on host is required. Optionally the CRC and correction software can be removed from the host

5.2 SOLVED MS1500: Power-up sequencing

Description:

When 1V8 and 1V2 start-up at the same time, Mercury occasionally does not start-up properly. SPI communication to Mercury is not possible in those cases.

Status:

The following requirements are applicable for board design and board application using Mercury ES1:

- Mercury will start properly when the 1V8 supply is started first and the 1V2 supply is started after that. The delay needs to be 20 ms or more
- Two solutions are identified for ES1:

  1) Updated 1V2 voltage regulator circuitry (as described in the application note).

  2) Host software to control the 1V2 supply line.

Solution for Mercury ES2:

A hardware update in ES2 will be made such that power sequencing is not required any more.

Board designs or host software that includes the power sequencing of ES1 can remain the same for ES2. Optionally this power sequencing can be removed for ES1

5.3 SOLVED MS1514: Pin changes between ES1 and ES2 (added power pair)

Description:

Mercury ES2 will have an additional power pair for VDDC_1V2. The affected pins: H19, H21 and H22.

Status:

The following requirements apply for an application using Mercury ES1:

- 1V2 supply needs to be between 1.19V – 1.25V (voltage on pin).
- Pin GPIO_10 cannot be used in ES1.
- VSSC/VDDC can be connected to H19/H21, but no current will flow over VDDC power lines in ES1

The application for the1V2 regulator is adapted to incorporate higher voltage.

Solution for Mercury ES2:

Board design for ES1 is compatible to ES2. The figure below shows the different pinning between ES1 and ES2.

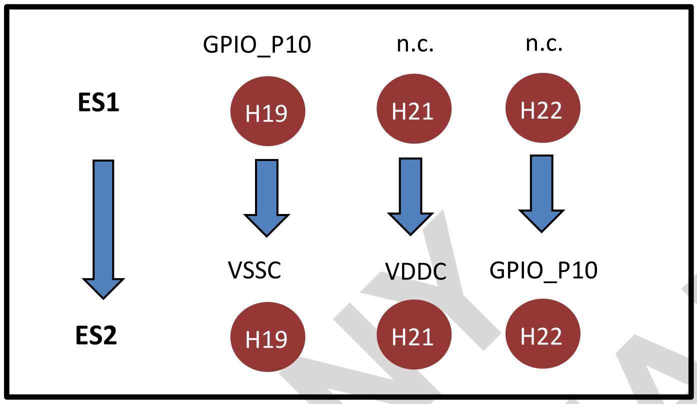

Figure 5 Pin change ES1 and ES2

The restriction on the supply voltage is relaxed (1.14V – 1.3V).

Pin GPIO_10 can be used in ES2.

5.4 SOLVED MS1373: Memory access

Description:

Uncached byte or half-word write to shared RAM is not possible. Cached writes to shared RAM are possible. Memories that are tightly-coupled to the processors can be accessed using uncached byte and half-word writes.

Status:

Consequences for users of ES1:

- Writing to shared memory should always be done via cache on HiFi3.
- Certain ES2 software will not run on Mercury ES1 due to increased need of MIPS.

Solution for Mercury ES2:

Uncached byte or half-word write to shared RAM will be enabled. Software developed for ES1 on HiFi3 using the cache access can also be used for ES2.

5.5 SOLVED MS1217: Primary boot loader system hang-up

Description:

Mercury ES1 is not robust against receiving multiple wrong flash commands during primary boot loader execution.

The primary boot loader of Mercury accepts flash commands 0xA32 (boot from flash) or 0xA31 <address> (boot from specific address in flash). In case there is no flash connected or a wrong address in flash is provided, the system can hang when the flash commands are send multiple times.

Status:

Requirements for host software in combination with Mercury ES1:

- During primary boot, a flash command should only be sent once. If this command fails, the device should be reset and the boot sequence can start again.

Solution for Mercury ES2:

Robustness for wrong commands in the primary boot loader will be improved in ES2. ES1 host software is compatible to ES2 software with respect to these changes.

5.6 SOLVED MS1516: Primary boot loader

Description:

The Mercury type number cannot be read-out in primary boot loader. As the secondary boot loader for SAF400e and SAF4000 is different, the host cannot read from the primary boot loader which secondary boot loader to load.

Status:

Requirements for host software in combination with Mercury ES1:

- In order to check which secondary boot loader to load, the different secondary boot loader images can be downloaded sequentially. A wrong boot loader image will result in an error. Then the next image can be loaded.

Solution for Mercury ES2:

Variant can be read-out in ES2 via a boot ROM update. ES1 software is compatible to ES2 software with respect to these changes. Optionally, the boot procedure can be changed by reading the variant number in the primary boot loader.

5.7 SOLVED MS2345: Spurious response

Description:

When tuned to e.g. 65 MHz, spurious responses are visible with a blocker signal at 106.6 MHz and 23.4 MHz. The difference to the tuner frequency is 41.6MHz. The amplitude of the spurious response can vary after re-tuning.

The issue is related to a state machine in the digital part of ES1.

Status:

Spurious mixing with 41.6 MHz can occur in ES1.

Solution for Mercury ES2:

A hardware update is implemented in Mercury ES2.

5.8 SOLVED MS1915: Additional functionality: BiQuad accelerator for HiFi3

Description:

The following biquad implementation is available as special instructions on HiFi3 for ES2:

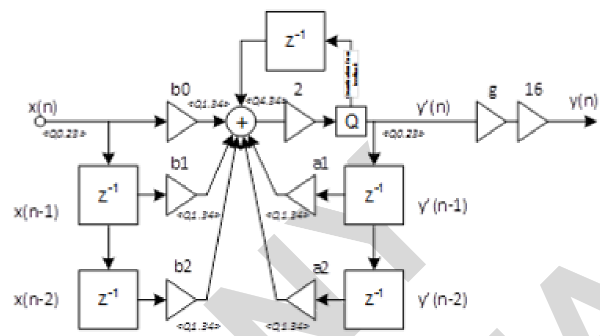

Figure 6 BiQuad accelerator

Mercury ES2:

The added hardware is available in Mercury ES2. HiFi3 software for ES1 is compatible to ES2.

HiFi3 cycle estimations:

- without TIE instruction (C-library): 19 cycles
- with TIE instruction: 1 cycle (parallel operation)

6. Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

7. List of tables

8. Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in the section 'Legal information'.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 10 October 2017
Document identifier: ES_SAF400x