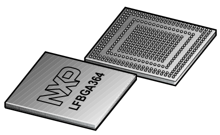


SAF400X_101_SAF777X_201

One-chip multi-tuner car radio and audio system

Rev. 1.0 — 30 October 2017 **Objective data sheet**

1. General description

The SAF400x family of multi standard multi tuner Car DSPs offers software defined radio capabilities through monolithic integration of up to four tuners including the analog and digital radio processing and a multichannel audio processing. The innovative wideband tuner-concept allows for exceptional performance compared to conventional narrowband tuners. Very fast and flexible Turbo Tuners operating in the digital domain ensure high speed band scans for analog and digital radio in AM/FM and DAB 3 bands.

The integrated high-performance DSP cores in combination with NXPs unique radio software algorithms deliver optimal reception, demodulation, decoding and audio processing for various analog and digital radio standards (AM/FM/weatherband/HD Radio/DAB/DAB+/T-DMB/DRM) using the integrated memory.

The 46 MHz wideband-ADC converters digitize the full AM or FM band or half DAB band for use with the four software definable turbo tuners enabling new use cases like dual phase diversity with a single chip.

High performance audio processing up to 1000 MIPS is performed by the integrated set of specialized audio DSPs with a powerful set of full parameterized audio functions and filters including a customer programmable 32-bit Cadence/Tensilica Hifi3 core.

Full cost scalability is ensured via software definable feature and function sets and a scalable product family from pure analog radio variants to full blown analog and digital radio + audio processing.

2. Features and benefits

2.1 AM/FM features

The list describes the maximum hardware configuration

- High dynamic range Sigma-Delta (SD) IF Analog-to-Digital Converter (ADC) with an absolute bandwidth of 46 MHz, covering full FM band, full AM band and half DAB3 band.
- Digital IF signal processing including decimation, shift to baseband, AGC control, I/Q
- Alignment free digital receiver including tuner and software-defined radio processing
- FM receiver with a tuning range from 65 MHz to 108 MHz covering Eastern European (OIRT), Japan, Europe and US bands
- AM receiver covering Long Wave (LW), Medium Wave (MW) and full Short Wave (SW) bands
- WX receiver with a tuning range from 162.4 MHz to 162.55 MHz

- Fully integrated tuning system with digital tuning using up to four turbo tuners
- Hybrid DAB / FM Low-Noise Amplifier (LNA) with Automatic Gain Control (AGC)
- FM Stereo Improvement algorithm (FMSI)
- FM iPD - innovative higher performance phase diversity algorithm
- FM improved multipath suppression
- FM channel equalization
- Soft mute on modulation
- Stereo high blend
- AM LNA with AGC, matching active and passive antenna applications
- AM and FM noise blanking, Signal quality detection and weak signal processing correction, variable IF bandwidth filtering (PACS) and demodulation
- Advanced RDS and RBDS demodulation and decoding
- MPX output supporting DARC demodulator
- Signal reconstruction after impulsive noise with INCA

2.2 HD radio features

- HD Radio signal decoding for AM and FM digital audio
- Supports HD Radio single, dual and triple tuner use cases
- HD all-digital mode support
- Meta data support for HD Radio reception
- Data services support for HD Radio reception
- Advanced HD Radio feature support for Apple ID3 tag and multicasting
- Electronic Program Guide (EPG)
- Off-chip LOT processing
- Reception improvement (Maximum Ratio Combining (MRC))

2.3 DRM

- DRM signal decoding for AM and FM digital audio
- Support of second station for background scanning and data services
- Channel decoder reception improvements
- Supports xHE-AAC codec
- Prepared for DRM+

2.4 DAB, DAB+, and T-DMB radio technology

- Data service reception and filtering
- Dual reception processing with on-chip dual DAB front-end, ADC, memory and source decoding
- DAB3 receiver with a tuning range from 167 MHz to 240 MHz
- Full dual ensemble processing (2 × 1.8 Mbit/s)
- Integrated DAB-FM/DAB-DAB time alignment and seamless blending Integrated support for all actual audio codecs (AAC, HE-AAC, MP2, and BSAC)
- Reception improvement algorithms for single antenna systems delivering additionally improved BER

- Diversity reception improvement through advanced Maximum Ratio Combining (MRC) algorithms
- External tuner interface to enable background service scan or data services
- Third tuner support using wideband ADC or via serial I²S-bus type interface
- Integrated antenna splitter enabling antenna diversity

2.5 Audio features

The list describes the maximum hardware configuration

- Four mono Analog-to-Digital Converters (ADC) multiplexed on seven analog input pins
- Audio Inter-IC Sound bus (I²S-bus) input/output (I/O) port with 14 inputs or outputs with an option to use an external audio master sample rate
- Sony/Philips Digital Interface (S/PDIF): one input or one output
- Time Division Multiplex (TDM) with optional two separate clock domains: eight inputs or eight outputs
- Pulse Code Modulation (PCM) interface
- 32-bit fixed point Cadence/Tensilica HiFi3 DSP for advanced audio or radio processing
- Blending function for HD Radio reception
- NXP advanced seamless blending system for FM/DAB

2.6 System control

- Software defined radio capability with free definable feature sets
- API for radio and audio control, combining flexibility with ease of programming
- Two fast mode Inter-IC buses (I2C)
- Two SPI buses
- Quad-SPI bus for fast boot
- Up to 16 general-purpose I/O for applications and diagnostics
- JTAG interface for diagnostics
- Secure booting
- Stand-alone booting from external flash device within 250 ms.
- Alternatively booting supported by host controller
- Hardware Advanced Encryption Standard (AES) accelerator
- Qualified in accordance with AEC-Q100
- In field software upgrade
- Single system XTAL with optional clock reference output capabilities
- Small PCB footprint using state-of-the-art BGA package

3. Applications

- Global car radio and audio Original Equipment Manufacturer (OEM) platforms
- High-end aftermarket car radios

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SAF4000EL/101	LFBGA364	plastic low profile fine-pitch ball grid array package; 364 balls	SOT1457-1
SAF4001EL/101			
SAF7770EL/201			
SAF7771EL/201			

4.1 Ordering options

Table 2. Ordering options

Type	HD	DAB	DRM	Audio	AM/FM
SAF4000EL/101	X	X	X	X	X
SAF4001EL/101	-	X	-	X	-
SAF7770EL/201	tuning only	tuning only	tuning only	X	X
SAF7771EL/201	tuning only	tuning only	tuning only	X	X

5. Block diagram

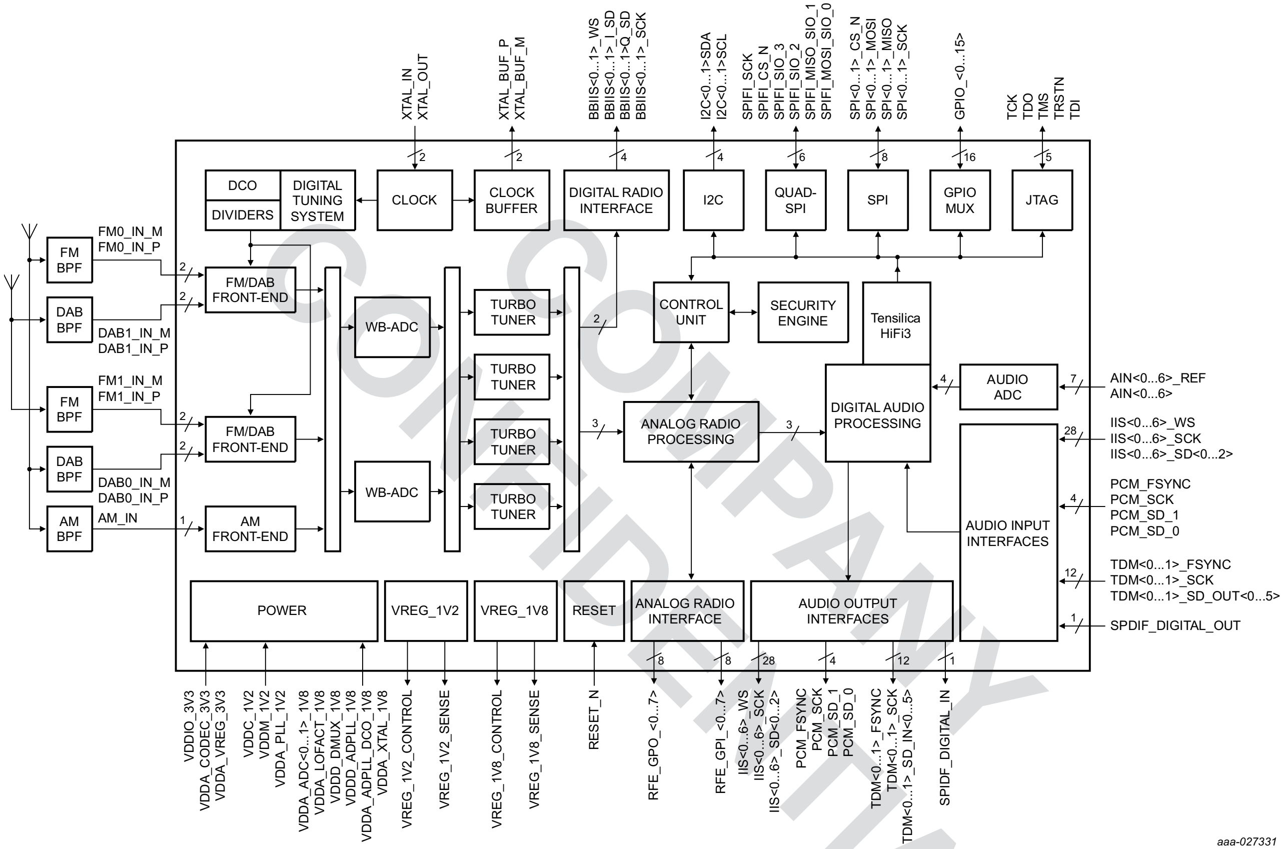


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

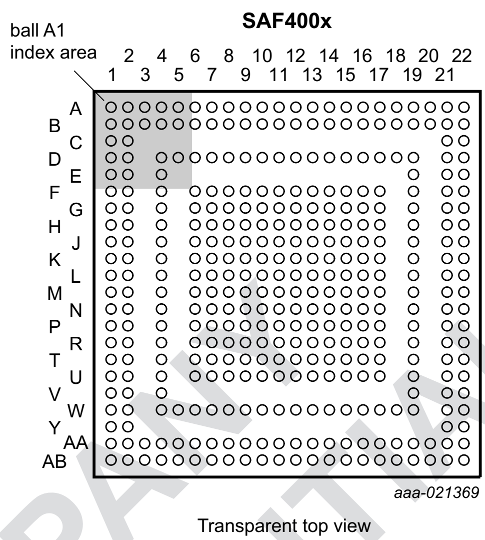


Fig 2. Pin configuration SAF400x (LFBGA364)

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
A1	VSSA_VREG	A2	VDDA_VREG_3V3	A3	VREG_1V8_CTRL	A4	VSSA_LOFACT
A5	VDDA_ADC1_1V8	A6	VDDA_ADC0_1V8	A7	XTAL_OUT	A8	XTAL_IN
A9	VDDA_ADPLL_1V8	A10	VDDD_ADPLL_1V8	A11	VDDD_DMUX_1V8	A13	VDDA_PLL_1V2
A14	SPI0_SCK	A15	SPI0_MOSI	A16	TRSTN	A17	TCK
A18	AIN0	A19	AIN1	A20	CODEC_VREFNEG	A21	CODEC_VREF
Row B							
B1	VDDA_AM	B2	VSSA_AM	B3	VREG_1V8_SENSE	B4	VDDA_LOFACT_1V8
B5	VSSA_ADC1	B6	VSSA_ADC0	B7	VSSA_XTAL_PLL	B8	VDDA_XTAL_1V8
B9	VDDA_ADPLL_DCO_1V8	B10	VSSA_ADPLL	B11	VSSD_DMUX	B13	VSSA_PLL
B14	SPI0_MISO	B15	VSSIO	B16	TDI	B17	TDO
B18	AIN0_REF	B19	AIN1_REF	B20	CODEC_VREFNEG_AD	B22	VDDA_CODEC_3 V3
Row C							
C1	AM_IN	C2	AM_CM	C21	AIN2_REF	C22	AIN2
Row D							
D1	VSSA_AM	D2	VSSA_AM	D4	VDDA_AM	D5	VSSA_VREG
D6	VSSA_VREG	D7	XTAL_BUF_M	D8	XTAL_BUF_P	D9	VSSA_VREG
D10	VSSD_ADPLL	D11	VSSA_SEALRING	D13	VDDD_QPS_2V5	D14	VDDIO_3V3

Table 3. Pin allocation table *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
D15	SPI0_CS_N	D16	TMS	D17	IC	D18	VSSA_SUBA_CODEC
D21	AIN3_REF	D22	AIN3				
Row E							
E1	FM0_IN_P	E2	FM0_IN_M	E4	VREF_AM	E19	VSSA_CODEC
E21	AIN4_REF	E22	AIN4				
Row F							
F1	DAB1_IN_M	F2	FM0_DAB1_CM	F4	VSSA_FMDAB	F21	AIN5_REF
F22	AIN5						
Row G							
G1	DAB1_IN_P	G2	VSSA_FMDAB	G4	VSSA_FMDAB	G21	AIN6_REF
G22	AIN6						
Row H							
H1	VDDA_FMDAB	H2	VDDA_MIX0	H4	VSSA_FMDAB	H19	VSSC
H21	VDDC_1V2	H22	GPIO_10				
Row J							
J1	VDDA_MIX1	J2	FM1_IN_P	J4	VSSA_MIX0	J19	VSSC
J21	IIS5_SD0	J22	IIS5_SD1				
Row K							
K1	FM1_IN_M	K2	FM1_DAB0_CM	K4	VSSA_MIX1	K19	VSSM
K21	VDDC_1V2	K22	IIS5_SCK				
Row L							
L1	DAB0_IN_M	L2	IC	L4	IC	L19	VSSC
L21	VDDM_1V2	L22	IIS5_WS				
Row M							
M1	DAB0_IN_P	M2	VSSA_FMDAB	M4	VSSA_SEALRING	M19	VSSCWT
M21	IIS4_SD2	M22	IIS4_SD0				
Row N							
N19	VDDIO_3V3	N21	VDDC_1V2	N22	IIS4_SCK		
Row P							
P1	RESET_N	P2	GPIO_15	P4	GPIO_0	P19	VSS_VREG
P21	VDDCWT_1V2	P22	IIS4_SD1				
Row R							
R1	GPIO_1	R2	NC	R4	NC	R19	IIS2_SCK
R21	VSSIO	R22	I2C0_SCL				
Row T							
T1	BBIIS0_WS	T2	BBIIS0_I_SD	T4	BBIIS0_Q_SD	T19	VSSC
T21	VREG_1V2_SENSE	T22	I2C0_SDA				
Row U							
U1	RFE_GPI_6	U2	BBIIS0_SCK	U4	VDDIO_3V3	U19	IIS2_SD1

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
U21	IIS4_SD3	U22	VREG_1V2_CONTROL				
Row V							
V1	RFE_GPO_7	V2	VSSIO	V4	RFE_GPI_3	V19	IIS0_SD0
V21	VDDC_1V2	V22	IIS4_WS				
Row W							
W1	RFE_GPI_7	W2	RFE_GPO_3	W5	RFE_GPI_0	W6	VSSM
W7	VSSC	W8	SPIFI_MOSI_SIO_ 0	W9	VDDIO_3V3	W10	VSSM
W12	VSSC	W13	VSSCWT	W14	SPI1_SCK	W15	IIS1_WS
W16	IIS6_SD1	W17	VSSC	W18	VDDIO_3V3	W21	IIS3_SD0
W22	IIS2_SD0						
Row Y							
Y1	RFE_GPO_2	Y2	RFE_GPI_2	Y21	IIS3_WS	Y22	IIS3_SCK
Row AA							
AA1	RFE_GPO_1	AA3	RFE_GPI_1	AA4	RFE_GPO_5	AA5	RFE_GPO_4
AA6	VDDM_1V2	AA7	VDDC_1V2	AA8	SPIFI_SIO_2	AA9	VSSIO
AA10	SPIFI_CS_N	AA11	VDDM_1V2	AA13	VDDC_1V2	AA14	VDDCWT_1V2
AA15	SPI1_MOSI	AA16	IIS1_SD0	AA17	IIS6_SCK	AA18	VDDC_1V2
AA19	IIS0_SCK	AA20	VSSIO	AA22	IIS2_WS		
Row AB							
AB2	RFE_GPO_0	AB3	RFE_GPI_4	AB4	RFE_GPO_6	AB5	RFE_GPI_5
AB6	SPIFI_MISO_SIO_ 1	AB7	SPIFI_SCK	AB8	I2C1_SDA	AB9	I2C1_SCL
AB10	SPIFI_SIO_3	AB11	GPIO_9	AB14	GPIO_2	AB15	SPI1_MISO
AB16	SPI1_CS_N	AB17	IIS1_SCK	AB18	IIS6_WS	AB19	IIS6_SD0
AB20	IIS0_WS	AB21	IIS0_SD1				

6.2 Pin description

Table 4. Pin description overview

Pin category	Table number
Secondary function	Table 5
Tertiary function	Table 6
Power supply	Table 7
Analog pins	Table 8
TDM interface pins	Table 9
Baseband interface pins	Table 10
Reset and general purpose	Table 11
SPI interface	Table 12
S/PDIF interface	Table 13
RFE general purpose pins	Table 14
I^{2}S-bus interface pins	Table 15
I^{2}C-bus interface pins	Table 16

Table 4. Pin description overview *...continued*

Pin category	Table number
Oscillator and clock	Table 17
JTAG pins	Table 18
Thermal pins	Table 19
Internal connected	Table 20

Table 5. Pin description - Secondary function of pins

Symbol	Pin	Description
BBIIS0_WS_IN	T1	baseband word select 0
BBIIS0_I_SD_IN	T2	baseband I-data 0
BBIIS1_I_SD_OUT	U1	baseband I-data 1
BBIIS0_Q_SD_IN	T4	baseband Q-data 0
BBIIS0_SCK_IN	U2	baseband serial clock 0
BBIIS1_Q_SD_OUT	V1	baseband Q-data 1
PWM_1	AB3	pulse width modulation input 1
PWM_0	AB4	pulse width modulation input 0
FS_SYS_OUT	AA4	system output clock
TDM0_SD_IN3	AA16	data input 0 TDM input 3
PCM_FSYNC	AB18	synchronous data frame sync
PCM_SCK	AA17	synchronous data serial clock
PCM_SD_1	W16	synchronous data input/output 1
PCM_SD_0	AB19	synchronous data input/output 0
TDM0_FSYNC	AB20	data output TDM output 0
TDM0_SCK	AA19	clock input TDM input
TDM0_SD_IN5	AB21	data input 0 TDM input 5
TDM0_SD_IN4	V19	data input 0 TDM input 4
TDM1_FSYNC	AA22	sync input TDM input 1
TDM0_SD_IN2	U19	data input 0 TDM input 2
TDM0_SD_IN1	W21	data input 0 TDM input 1
TDM0_SD_OUT5	W22	data output 0 TDM output 5
TDM1_SCK	R19	clock input TDM input
TDM0_SD_OUT4	U21	data output 0 TDM output 4
TDM1_SD_IN1	V22	data input 1 TDM input 1
TDM0_SD_OUT2	P22	data output TDM output 2
TDM1_SD_OUT1	N22	data output 1 TDM output 1
TDM0_SD_OUT3	M21	data output 0 TDM output 3
TDM0_SD_OUT1	M22	data output 0 TDM output 1
TDM0_SD_IN0	L22	data input 0 TDM input 0
TDM0_SD_OUT0	K22	data output 0 TDM output 0
TDM1_SD_OUT0	J22	data output 1 TDM output 0
TDM1_SD_IN0	J21	data input 1 TDM input 0

Table 6. Pin description - Tertiary function of pins

Symbol	Pin	Description
GPIO_3	AA5	general-purpose input output 3
GPIO_4	AB3	general-purpose input output 4
GPIO_5	AA4	general-purpose input output 5
GPIO_6	AB4	general-purpose input output 6
GPIO_7	U1	general-purpose input output 7
GPIO_8	AB5	general-purpose input output 8
GPIO_9	AB11	general-purpose input output 9
GPIO_10	H22	general-purpose input output 19
GPIO_11	V1	general-purpose input output 11
GPIO_12	W1	general-purpose input output 12
GPIO_13	T4	general-purpose input output 13
GPIO_14	T2	general-purpose input output 14

Table 7. Pin description - Power supplies

See Table 22 for limiting values

Symbol	Pin	Type[1]	Description
NC.	R2, R4	-	not connected
Digital supply pins			
VDDM_1V2	L21, AA6, AA11	P	supply voltage
VDDD_QPS_2V5	D13	P	QPS supply voltage
VDDD_DMUX_1V8	A11	P	DMUX supply voltage
VDDD_ADPLL_1V8	A10	P	PLL supply voltage
VDDIO_3V3	U4, W9, W18, D14, N19	P	I/O supply voltage
VDDC_1V2	N21, H21, AA7, AA13, AA18, V21, K21	P	core ground supply voltage
VDDCWT_1V2	P21, AA14	P	supply voltage
Digital ground pins			
VSSM	K19, W10, W6	G	ground supply
VSSIO	B15, R21, AA20, AA9, V2	G	I/O ground supply voltage

Table 7. Pin description - Power supplies *…continued*

See Table 22 for limiting values

Symbol	Pin	Type[1]	Description
VSSC	J19, L19, T19, W17, W12, W7, H19	G	ground supply
VSSCWT	M19, W13	G	ground supply
VSS_VREG	P19	G	regulator ground supply
VSSD_DMUX	B11	G	DMUX ground supply
VSSD_ADPLL	D10	G	PLL ground supply
Analog supply pins			
VDDA_AM	B1, D4	P	AM analog supply voltage
VDDA_MIX0	H2	P	MIX0 analog supply voltage
VDDA_FMDAB	H1	P	FM DAB analog supply voltage
VDDA_MIX1	J1	P	MIX1 analog supply voltage
VDDA_CODEC_3V3	B22	P	CODEC analog supply voltage
VDDA_PLL_1V2	A13	P	PLL analog supply voltage
VDDA_ADPLL_DCO_1V8	B9	P	ADPLL analog supply voltage
VDDA_XTAL_1V8	B8	P	XTAL PLL analog supply voltage
VDDA_ADC0_1V8	A6	P	ADC 0 analog supply voltage
VDDA_ADC1_1V8	A5	P	ADC 1 analog supply voltage
VDDA_ADPLL_1V8	A9	P	ADPLL analog supply voltage
VDDA_LOFACT_1V 8	B4	P	LOFACT analog supply voltage
VDDA_VREG_3V3	A2	P	analog voltage regulator supply
VREF_AM	E4	P	analog supply voltage
CODEC_VREFNEG_AD	B20	P	analog supply voltage
CODEC_VREFNEG	A20	P	analog supply voltage
CODEC_VREF	A21	P	analog supply voltage
Analog ground pins			
VSSA_VREG	D5, D6, A1, D9	G	analog ground supply
VSSA_AM	B2, D1, D2	G	analog ground supply
VSSA_FMDAB	M2, H4, G2, F4, G4	G	analog ground supply
VSSA_MIX0	J4	G	analog ground supply
VSSA_MIX1	K4	G	analog ground supply
VSSA_CODEC	E19	G	CODEC analog ground supply
VSSA_SUBA_COD EC	D18	G	analog ground supply
VSSA_PLL	B13	G	analog ground supply

Table 7. Pin description - Power supplies *...continued*

See Table 22 for limiting values

Symbol	Pin	Type[1]	Description
VSSA_SEALRING	D11, M4	G	analog ground supply
VSSA_ADPLL	B10	G	analog ground supply
VSSA_XTAL_PLL	B7	G	analog ground supply
VSSA_ADC0	B6	G	analog ground supply
VSSA_ADC1	B5	G	analog ground supply
VSSA_LOFACT	A4	G	analog ground supply
Regulator pins			
VREG_1V2_SENSE	T21	A	external sense pin
VREG_1V2_CONTR OL	U22	A	external supply control/status
VREG_1V8_SENSE	B3	A	external sense pin
VREG_1V8_CTRL	A3	A	external supply control/status

[1] Table 21 defines the pin type.

Table 8. Pin description - analog pins

See Table 11 for interface characteristics

Symbol	Pin	Type[1]	Description
ADC input			
AIN5_REF	F21	A	analog audio input 5 reference
AIN5	F22	A	analog input 5
AIN4_REF	E21	A	analog audio input 4 reference
AIN4	E22	A	analog input 4
AIN6_REF	G21	A	analog audio input 6 reference
AIN6	G22	A	analog input 6
AIN3_REF	D21	A	analog audio input 3 reference
AIN3	D22	A	analog input 3
AIN2	C22	A	analog input 2
AIN2_REF	C21	A	analog audio input 2 reference
AIN1_REF	B19	A	analog audio input 1 reference
AIN1	A19	A	analog input 1
AIN0	A18	A	analog input 0
AIN0_REF	B18	A	analog audio input 0 reference
AM section			
AM_IN	C1	A	AM tuner input
AM_CM	C2	A	AM external attenuation capacitance
DAB section			
FM0_DAB1_CM	F2	A	FM and DAB common mode
FM1_DAB0_CM	K2	A	FM and DAB common mode
DAB1_IN_M	F1	A	negative DAB1 tuner input
DAB1_IN_P	G1	A	positive DAB1 tuner input
DAB0_IN_M	L1	A	negative DAB0 tuner input

Table 8. Pin description - analog pins *...continued*
See Table 11 for interface characteristics

Symbol	Pin	Type[1]	Description
DAB0_IN_P	M1	A	positive DAB0 tuner input
FM section			
FM0_IN_M	E2	A	negative FM tuner input
FM0_IN_P	E1	A	positive FM tuner input
FM1_IN_P	J2	A	positive FM tuner input
FM1_IN_M	K1	A	negative FM tuner input
Analog test pins			
IC	L2	A	analog test bus 0
IC	L4	A	analog test bus 1

[1] Table 21 defines the pin type.

Table 9. Pin description - Time division multiplex interface
See Table 36 for interface characteristics

Symbol	Pin	Type[1]	Description
TDM0_SD_IN3	AA16	I	data input 0 TDM input 3[2]
TDM0_FSYNC	AB19	I/O	data output TDM output 0[2]
TDM0_SCK	AA19	I/O	clock input TDM input
TDM0_SD_IN5	AB21	I	data input 0 TDM input 5
TDM0_SD_IN4	V19	I	data input 0 TDM input 4
TDM1_FSYNC	AA22	I/O	sync input TDM input 1
TDM0_SD_IN2	U19	I	data input 0 TDM input 2
TDM0_SD_IN1	W21	I	data input 0 TDM input 1
TDM0_SD_OUT5	W22	O	data output 0 TDM output 5
TDM1_SCK	R19	I/O	clock input TDM input
TDM0_SD_OUT4	U21	O	data output 0 TDM output 4
TDM1_SD_IN1	V22	I	data input 1 TDM input 1
TDM0_SD_OUT2	P22	O	data output 0 TDM output 2
TDM1_SD_OUT1	N22	O	data output 1 TDM output 1
TDM0_SD_OUT3	M21	O	data output 0 TDM output 3
TDM0_SD_OUT1	M22	O	data output 0 TDM output 1
TDM0_SD_IN0	L22, W16	I	data input 0 TDM input 0
TDM0_SD_OUT0	AB19, K22	O	data output 0 TDM output 0
TDM1_SD_OUT0	J22	O	data output 1 TDM output 0
TDM1_SD_IN0	J21	I	data input 1 TDM input 0

[1] Table 21 defines the pin type.
[2] Secondary function.

Table 10. Pin description - Baseband interface

See Table 37 for interface characteristics

Symbol	Pin	Type[1]	Description
BBIIS0_WS	T1	O	baseband word select input/output
BBIIS0_I_SD	T2	O	baseband I-data input/output
BBIIS0_Q_SD	T4	O	baseband I-data input/output
BBIIS0_SCK	U2	O	baseband Q-data input/output
BBIIS1_Q_SD	V1, Y2	O	baseband Q-data input/output
BBIIS1_I_SD	U1, Y1	I	baseband I-data input/output
BBIIS1_WS	W2	O	baseband word select input/output
BBIS1_SCK	V4	O	baseband serial clock input/output

[1] Table 21 defines the pin type.

Table 11. Pin description - Reset and general-purpose pins

See Table 41 for interface characteristics

Symbol	Pin	Type[1]	Description
RESET			
RESET_N	P1	I	master reset input from host micro controller (active LOW)
RESET_N_OUT	P2	O	reset output (active LOW)
GPIO interface			
GPIO_0	P4	I/O	general-purpose input output 0
GPIO_1	R1	I/O	general-purpose input output 1
GPIO_2	AB14	I/O	general-purpose input output 2
GPIO_3	AA5	I/O	general-purpose input output 3
GPIO_4	AB3	I/O	general-purpose input output 4
GPIO_5	AA4	I/O	general-purpose input output 5
GPIO_6	AB4	I/O	general-purpose input output 6
GPIO_7	U1	I/O	general-purpose input output 7
GPIO_8	AB5	I/O	general-purpose input output 8
GPIO_9	AB11	I/O	general-purpose input output 9
GPIO_10	H22	I/O	general-purpose input output 10
GPIO_11	V1	I/O	general-purpose input output 11
GPIO_12	W1	I/O	general-purpose input output 12
GPIO_13	T4	I/O	general-purpose input output 13
GPIO_14	T2	I/O	general-purpose input output 14
GPIO_15	P2	I/O	general-purpose input output 15

[1] Table 21 defines the pin type.

Table 12. Pin description - Serial peripheral interface

Symbol	Pin	Type[1]	Description
SPIFI_MISO_SIO_ 1	AB6	I/O	quad SPI data output 1/master input
SPIFI_SCK	AB7	I/O	quad SPI serial clock output
SPIFI_SIO_2	AA8	I/O	quad SPI data output 2
SPIFI_MOSI_SIO_ 0	W8	I/O	quad SPI data output 0/master output
SPIFI_CS_N	AA10	I/O	quad SPI chip select 0
SPIFI_SIO_3	AB10	I/O	quad SPI data output 3
GPIO_9	AB11	I/O	general-purpose input output 9
SPI1_MISO	AB15	I/O	master input of SPI1 interface
SPI1_CS_N	AB16	I/O	chip select of SPI1 interface
SPI1_MOSI	AA15	I/O	master output of SPI interface
SPI1_SCK	W14	I/O	serial clock input of SPI1 interface
SPI0_CS_N	D15	I/O	chip select of SPI0 interface
SPI0_MOSI	A15	I/O	master output of SPI0 interface
SPI0_SCK	A14	I/O	serial clock input of SPI0 interface
SPI0_MISO	B14	I/O	master input of SPI0 interface

[1] Table 21 defines the pin type.

Table 13. Pin description - S/PDIF interface

See Table 44 for interface characteristics

Symbol	Pin	Type[1]	Description[2]
SPDIF_DIGITAL_IN	U19, L22	I	S/PDIF digital data input
SPDIF_DIGITAL_OUT	W22, K22	I	S/PDIF digital data output

[1] Table 21 defines the pin types.

[2] Tertiary function.

Table 14. Pin description - RFE general-purpose pins

Symbol	Pin	Type[1]	Description[2]
RFE_GPI_0	W5	I	RFE general-purpose input pin
RFE_GPI_1	AA3	I	RFE general-purpose input pin
RFE_GPI_2	Y2	I	RFE general purpose input pin
RFE_GPI_3	V4	I	RFE general-purpose input pin
RFE_GPI_4	AB3	I	RFE general-purpose input pin
RFE_GPI_5	AB5	I	RFE general-purpose input pin
RFE_GPI_6	U1	I	RFE general-purpose input pin
RFE_GPI_7	W1	I	RFE general-purpose input pin
RFE_GPO_0	AB2	O	RFE general-purpose output pin
RFE_GPO_1	AA1	O	RFE general-purpose output pin
RFE_GPO_2	Y1	O	RFE general-purpose output pin
RFE_GPO_3	W2	O	RFE general-purpose output pin

Table 14. Pin description - RFE general-purpose pins *…continued*

Symbol	Pin	Type[1]	Description[2]
RFE_GPO_4	AA5	O	RFE general-purpose output pin
RFE_GPO_5	AA4	O	RFE general-purpose output pin
RFE_GPO_6	AB4	O	RFE general-purpose output pin
RFE_GPO_7	V1	O	RFE general-purpose output pin

[1] Table 21 defines the pin type.

[2] Primary function.

Table 15. Pin description - I²S-bus interface
See Table 34 for interface characteristics

Symbol	Pin	Type[1]	Description[2]
IIS1_SCK	AB17	I/O	serial clock input/output of I²S-bus 1
IIS1_SD0	AB16	I/O	data input/output 0 of I²S-bus 1
IIS1_WS	W15	I/O	word select input/output of I²S-bus 1
IIS6_WS	AB18	I/O	word select input/output of I²S-bus 6
IIS6_SCK	AA17	I/O	serial clock input/output of I²S-bus 6
IIS6_SD1	W16	I/O	data input/output 1 of I²S-bus 6
IIS6_SD0	AB19	I/O	data input/output 0 of I²S-bus 6
IIS0_WS	AB20	I/O	word select input/output of I²S-bus 0
IIS0_SCK	AA19	I/O	serial clock input/output of I²S-bus 0
IIS0_SD1	AB21	I/O	data input/output 1 of I²S-bus 0
IIS0_SD0	V19	I/O	data input/output 0 of I²S-bus 0
IIS3_WS	Y21	I/O	word select input/output of I²S-bus 3
IIS2_WS	AA22	I/O	word select input/output of I²S-bus 2
IIS2_SD1	U19	I/O	data input/output 1 of I²S-bus 2
IIS3_SD0	W21	I/O	data input/output 0 of I²S-bus s 3
IIS3_SCK	Y22	I/O	serial clock input/output of I²S-bus 3
IIS2_SD0	W22	I/O	data input/output 0 of I²S-bus 2
IIS2_SCK	R19	I/O	serial clock input/output of I²S-bus 2
IIS4_SD3	U21	I/O	data input/output 3 of I²S-bus 4
IIS4_WS	V22	I/O	word select input/output of I²S-bus 4
IIS4_SD1	P22	I/O	data input/output 1 of I²S-bus 4
IIS4_SCK	N22	I/O	serial clock input/output of I²S-bus 4
IIS4_SD2	M21	I/O	data input/output 2 of I²S-bus 4
IIS4_SD0	M22	I/O	data input/output 0 of I²S-bus 4
IIS5_WS	L22	I/O	word select input/output of I²S-bus 5
IIS5_SCK	K22	I/O	serial clock input/output of I²S-bus 5
IIS5_SD1	J22	I/O	data input/output 1 of I²S-bus 5
IIS5_SD0	J21	I/O	data input/output 0 of I²S-bus 5

[1] Table 21 defines the pin type.

[2] Primary function.

Table 16. Pin description - I^{2}C-bus interface

See Table 40 for interface characteristics

Symbol	Pin	Type[1]	Description
I^{2}C-bus interface (master and slave)			
I2C1_SDA	AB8	I^{2}C	serial data of I^{2}C-bus 1
I2C1_SCL	AB9	I^{2}C	serial clock of I^{2}C-bus 1
I2C0_SDA	T22	I^{2}C	serial data of I^{2}C-bus 0
I2C0_SCL	R22	I^{2}C	serial clock of I^{2}C-bus 0

[1] Table 21 defines the pin type.

Table 17. Pin description - oscillator and clock

See Table 42 for interface characteristics

Symbol	Pin	Type[1]	Description
Oscillator			
XTAL_IN	A8	A	positive crystal buffered[2]
XTAL_OUT	A7	A	negative crystal buffered[2]
XTAL_BUF_P	D8	A	positive crystal buffered output[2]
XTAL_BUF_M	D7	A	negative crystal buffered output[2]
Clocks			
FS_SYS_OUT	AA4	I/O	audio clock output[3]

[1] Table 21 defines the pin type.

[2] Primary function.

[3] Secondary function.

Table 18. Pin description - JTAG

See Table 44 for interface characteristics

Symbol	Pin	Type[1]	Description
TDI	B16	I/O	JTAG test data input
TDO	B17	I/O	JTAG test data output
TRSTN	A16	I/O	JTAG test reset input (active LOW)
TMS	D16	I/O	JTAG test mode selection input
TCK	A17	I/O	JTAG test clock input

[1] Table 21 defines the pin type.

Table 19. Pin description - thermal pins

Symbol	Pin	Type	Description
Thermal	A12, A22, B12, B21, D12, D19, F6 to F17, F19, G6 to G17, G19, H6 to H17, J6 to J17, K6 to K17, L6 to L17, M6 to M17, N1, N2, N4, N6 to N17, P6 to P17, R6 to R17, T6 to T17, U6 to U17, W4, W11, W19, AA2, AA12, AA21, AB1, AB12, AB13, AB22	-	thermal connection

Table 20. Pin description - internal connected

See Table 37 for interface characteristics

Symbol	Pin	Type	Description
IC	L2, L4, and D17	-	internally connected; leave open

Table 21. Pin type description

Type	Description
A	analog
AI	analog input pin
AG	analog ground pin
AO	analog output pin
AP	analog power pin
AR	analog reference pin
G	ground pin
I	input
I/O	input or output
I^{2}C	I^{2}C-bus pin; 3.3 V tolerant
O	output
P	power supply pin

7. Functional description

7.1 Tuner description

The SAF400X tuner block diagram is given in Figure 3. Two IF data paths are supported consisting of an IF trans-impedance amplifier, wideband IF AD converter and primary decimation chain. The 2 IF data paths operate independent from each other. Both IF data paths can receive AM, FM, DAB Band III or weather band signals.

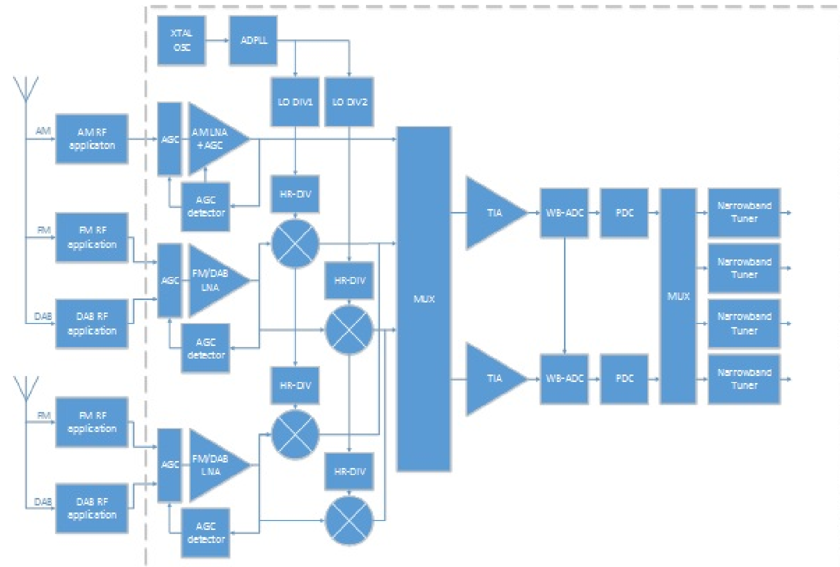


Fig 3. Dual tuner radio front-end of SAF400X

The SAF400X contains one AM RF input, two FM RF inputs and two DAB Band III / Weather band inputs.

The AM RF input is signal is processed by the AM LNA and provided to one of the two IF signal paths. The wideband ADC digitizes the complete AM band. After the first decimation stages in the primary decimation chain, a maximum number of three AM channels are selected in the narrowband tuner.

One FM RF input and one DAB RF input are connected to a combined FM/DAB LNA. This FM/DAB LNA processes either the FM or the DAB RF input signal.

In case of FM reception, a fixed LO frequency is used to convert one of the FM reception bands EU/US band, Japan band or OIRT band to the IF frequency range. This IF signal is provided to one of the two IF signal paths. With a second LO signal, another FM reception band can be converted to IF and provided to the other IF signal path. The wideband IF ADC digitizes the selected FM reception band. After the primary decimation chain, a maximum number of three FM channels within the selected FM reception band can be selected in the narrowband tuner.

In case of DAB reception, two different LO frequencies are used to cover the DAB Band III. One LO frequency is used to convert the lower part of the DAB Band III to the IF frequency range, the other LO frequency is used to convert the upper part of the DAB Band III. After frequency conversion, the IF signal is provided to one of the two IF signal paths for digitization, decimation and channel selection.

For analog AM/FM radio broadcasting, the selected AM or FM channels are demodulated for reception of audio signals, RDS (FM only), and signal quality information. In case of AM-HD, FM-HD, DRM or DAB digital radio reception, the baseband signal of the selected channel is provided to the digital radio processor for demodulation and decoding.

7.2 FM tuner to IF ADC input

An external wideband RF band pass filter is used to filter the RF antenna signal. It passes the complete FM band of interest and provides impedance transformation realizing the antenna impedance matching.

The output signal of the RF bandpass filter is provided to the FM AGC and the high dynamic range FM LNA of the SAF400X. The integrated AGC loop controls the attenuation of the FM AGC. The AGC range is 48 dB. The IC input impedance remains constant over the first 24 dB AGC range and is reduced for an AGC between 24 dB and 48 dB.

The signal from the LNA is converted to an IF signal using a complex mixer including image and harmonic LO rejection. The reception of the FM bands EU/US, Japan or OIRT each uses a different LO frequency. However within a reception band, the LO frequency is fixed. The IF frequency is in the range between 300 kHz and 23 MHz. The IF signal is amplified and digitized by the wideband IF ADC.

7.3 AM tuner to IF ADC input

An external high pass filter and an FM frequency band reject filter are used to filter the RF antenna signal. The high pass filter attenuates the 50 Hz/60 Hz signals from power supply lines. The band reject filter or FM intrusion filter attenuates the FM signals before entering the AM LNA, preventing inter modulation from two FM signals degrading AM reception.

After the external filtering, the RF signal is applied to the AM AGC and AM LNA of the SAF400X. The attenuation of the AM AGC and the gain of the AM LNA is controlled by the integrated AGC loop. The IC input impedance is constant over the first 39 dB of the AGC range and is reduced for higher AGC values.

The LNA output signal is amplified and digitized by the wideband ADC. As no frequency conversion is applied for AM-LW, MW, and SW reception, performance limitations due to reception of image and harmonic LO frequencies are avoided.

7.4 DAB tuner to IF ADC input

An external band pass filter selects the DAB Band III frequencies from the antenna signal and provides antenna impedance matching. After filtering, the RF signal is applied to the AGC and LNA. The integrated AGC loop controls the attenuation of the AGC. The IC input impedance is constant over the first 24dB of the AGC range and is reduced for AGC values between 24 dB and 36 dB.

A complex mixer converts the lower or the upper part of the DAB Band III to an IF signal. The IF signal is amplified and digitized by the wideband IF ADC.

7.5 WX tuner to IF ADC input

The DAB Band III tuner section can be used to receive weather band. The external band pass filter in application has to be extended below the DAB Band III frequencies in order to pass the weather band frequencies. After the AGC and LNA, a fixed LO signal is used to convert the weather band to IF. The IF signal is amplified and digitized by the IF ADC.

7.6 Tuning system

The tuning system provides a number of fixed LO frequencies for reception of the FM EU/US band, FM Japan band, FM OIRT band, the upper or lower part of the DAB Band III or the weather band. The LO signal from the tuning system is used to convert the selected RF frequency band to an IF signal fitting in the bandwidth of the wideband IF ADC. The LO signals are derived from a single fixed frequency oscillator by means of selecting a proper divider setting. The tuning PLL uses a 55.46667 MHz reference clock signal to generate this high frequency oscillator signal. The reference clock signal is generated by the crystal oscillator or provided by an external device.

7.7 Wideband IF ADC

The high dynamic range sigma-delta wideband IF ADC digitizes the RF frequencies from the AM-LW/MW/SW bands or the IF signals from the down converted FM bands, Weather band or DAB Band III. The bandwidth of the wideband IF ADC ranges from –23 MHz to +23 MHz and is extended to ±30 MHz for AM-SW. The bandwidth is wide enough to convert the complete AM band, the FM EU/US band, the FM Japan band, the FM OIRT band, weather band or half the DAB Band III. The wideband IF ADC provides I and Q bit streams which are decimated in the primary decimation chain.

7.8 Narrowband tuner

From the wideband signal provided by the IF ADC and Primary Decimation Chain, the narrow band tuner selects a single AM, FM, WX or DAB channel. A maximum of four narrow band channels can be selected. IQ correction is applied to optimize image rejection for FM, WX and DAB. The narrow band tuner applies filtering and decimation to appropriate bandwidths and sample rates for AM, FM, WX and DAB radio signal processing.

The FM Intermodulation Cancellation algorithm can be optionally applied. This algorithm cancels intermodulation components created by non-linearity of the wideband FM tuner, improving signal reception in strong signal conditions. The FM Intermodulation Cancellation algorithm is available for reception of analog FM and FM HD.

The AM Wideband Noise Cancellation (AM WNC) algorithm can be optionally applied to remove wideband noise components generated by electrical or hybrid cars from the desired signal. This algorithm uses the signal from a noise probe antenna connected to a separate receiver which is provided to the SAF400X by the IIPD interface. The AM Wideband Noise Cancellation algorithm is available for reception of analog AM as well as AM HD and DRM.

7.8.1 AM radio processing

The signal provided by the narrowband tuner is filtered to reject adjacent channels. The bandwidth of the channel filter can be programmed or controlled by an automatic bandwidth control algorithm (AM PACS). After this channel filtering, the signal is demodulated.

The AM noise blanker suppresses ignition noise pulses. It consists of an IF noise blanker in front of the channel filter and an audio noise blanker after AM demodulation. The device offers an optional feature, Impulsive Noise Concealment Algorithm (INCA) which can be

selected instead of the AM audio noise blanker. The INCA algorithm reconstructs the original waveform instead of blanking out the noise pulses. It improves the noise suppression performance and reduces the audio distortion.

Quality detectors are available to provide information about the quality of the signal reception:

- Radio Signal Strength Indication (RSSI) or field strength indication (level)
- Frequency offset detection
- AM modulation detection
- Adjacent channel or noise detection
- Co-channel detection
- Signal to Noise detection

The presence of a DRM signal can be detected by the DRM detector.

The AM weak signal handling improves the audio quality in weak or disturbed reception conditions by:

- Soft mute controlled by level and modulation
- High cut and Low cut controlled by level and modulation

7.8.2 FM radio processing

Phase diversity combines the signals provided by two narrowband tuners, each connected to a different wideband tuner and antenna input, achieving the best possible reception performance for different signal conditions. Phase diversity can also make use of one signal from an internal SAF400X narrowband tuner and one signal provided by an external tuner via the IIPD interface.

For single tuner reception, the adaptive filtering by the Channel Equalizer improves the reception performance in multipath, adjacent channel and weak signal conditions.

Before FM demodulation, the signal is filtered to reject adjacent channels. The bandwidth of the channel filter is controlled by an automatic bandwidth control algorithm (FM PACS). The selected bandwidth depends on the adjacent channel conditions and properties of the desired signal as modulation and field strength.

The improved multipath suppression algorithm reduces the audibility of multipath distortions by removing noise and distortion from the demodulated MPX output signal.

The FM noise blanker detects and blanks the ignition noise pulses. Instead of just blanking the ignition pulses, the Impulsive Noise Concealment Algorithm (INCA) can be selected for reconstructing the original waveform. This optional feature improves the noise suppression performance and reduces the audio distortion.

The FM Stereo Improvement (FMSI) is an advanced algorithm improving FM stereo reception. It improves stereo noise reduction and maintains stereo reception in signal conditions where conventional mono-stereo blend algorithms have blended over to mono.

Quality detectors are available to provide information about the quality of the signal reception:

- Radio Signal Strength Indication (RSSI) or field strength indication (Level)

- Frequency offset detection
- Multipath and adjacent channel detection by Ultrasonic Noise Detection (USN)
- Multipath detection by Wideband AM (WAM) detection
- FM frequency deviation detection
- Stereo pilot detection
- Fast quality change detection

The FM weak signal handling improves the audio quality in weak or disturbed reception conditions:

- Soft mute controlled by level, USN and WAM
- High cut and Low cut controlled by level, USN, WAM and modulation
- Stereo blend controlled by level, USN, WAM and modulation
- Stereo high blend controlled by level, USN, WAM and modulation

7.8.3 RDS/RBDS

An RDS demodulator and RDS decoder processes the data received from RDS and RBDS transmissions with excellent RDS sensitivity. RDS can be received simultaneous from three narrowband tuner signals.

7.8.4 RDS demodulator

The RDS demodulator includes optimized filtering and linear signal processing that allows very good RDS sensitivity. The MPX signal is filtered for selection of the 57 kHz RDS signal and data shaping. The RDS demodulator data is provided to the RDS decoder for further processing. To support available software stacks, the RDS demodulator data can also be read directly via the SPI bus.

7.8.5 RDS decoder

The RDS decoder provides synchronization to the block and group structure of the demodulated RDS data stream. When synchronized, the decoder delivers data in a fixed ABCD group order for easy software handling. In the background, synchronization search continues for fast correction on bit slip or other synchronization errors. Extended error detection and correction are included.

An SPI register indicates the availability of a new group. An interrupt signal ‘data available’ can be provided on a GPIO pin.

Data available is indicated whenever a new group is received, that is at reception of block D. For fast PI code reception, at synchronization start ‘data available’ is flagged on reception of the first PI code, such as block A or block C.

7.8.6 RDS full search

The SAF400X includes the special FULL SEARCH feature for improved RDS sensitivity reception. FULL SEARCH is an optimized RDS channel demodulation and decoder system. It uses soft decision and soft error detection techniques to achieve an improvement of RDS sensitivity at equal or better quality of output data compared to conventional RDS decoder systems.

7.8.7 Weather band radio processing

In weather band mode, the signal from the narrowband tuner is filtered and demodulated. The demodulated audio signal is filtered and the signal level is scaled.

Quality detectors are available to provide information about the quality of the signal reception:

- Radio Signal Strength Indication (RSSI) or field strength indication (Level)
- Frequency offset detection

The level information is used to control the soft mute in very weak reception conditions.

7.9 IIPD interface

The IIPD interface is a dedicated interface between NXP devices like e.g. SAF400X, SAF7770 or TEF7100. The IIPD interface is used to transfer a narrowband AM or FM baseband signal from one device (slave) to the other device (master). Example use cases are FM phase diversity with two tuners from different devices or AM wideband noise cancellation with one tuner connected to the main reception antenna and one tuner connected to the noise probe.

The IIPD interface between the SAF400X and/or SAF7770 devices can be configured as bi-directional interface with baseband signal transfer from slave to master device and tuner status information from the master to the slave device. For an IIPD interface between the SAF400X/SAF7770 and the TEF7100, the TEF7100 only provides data to the SAF400X/SAF7770.

7.10 Digital radio features

7.10.1 Baseband interfaces

In order to support tuner signal routing between different NXP car radio ICs, two I^2C-bus input interfaces are included to cope with down-mixed (I, Q) baseband signal pair streams. The two interfaces implement the following features:

- Split I/Q I^2S-bus signal-based input 24-bit I and Q data word serialized, word select, bit clock)
- Interface speed from 325 kS/s up to 2.6 MS/s to serve. For example:
  - 650 kS/s for HD Radio AM/FM Mode
  - 2.6 MS/s for additional DAB signal stream input
- Input and output using current mode

The interfaces can be used to implement AM and high performance FM-based digital radio transmission standards such as DRM and HD Radio, as well as DAB tuner signal transmission. The interface is typically used to connect to a TEF7100, SAF770X or SAF400X chip.

7.10.2 Digital front-end

The digital radio processing front end is used to convert the digitized radio frequency data streams and baseband I^2C-bus interface data streams into data packages. The data conversion suites distribution via the chips main control and data communication fabric.

- Channel filtering
- Sample rate conversion with bypass option
- Support for three parallel tuner (I, Q) paired data streams
- Direct memory access master capability into the chips main communication fabric

Next to data packaging a bypass-able sample rate conversion unit is implemented per data stream. In total, three parallel data streams are supported and packed into one time-multiplex data stream. The data stream is transmitted into the main processing system via direct memory access streaming interface with master capability.

7.10.3 Digital radio DSP for baseband processing

Any main baseband processing is designated to be done in software, enabling a flexible software defined radio approach to serve various digital radio standards. The main backbone for any processing is a vector DSP core. It includes infrastructure components such as tightly coupled memories, caches and user-defined instruction extensions suited to support digital radio reception algorithms.

The basic processor IO for any data stream can be done via an internal on chip bus. It is suited to consume processing data from the main memory or any other DMA client and to produce processed data into the next system unit.

A hardware accelerator is used to off-load basic stream decoding capabilities from the main radio processing system DSP. It includes the following functions:

- De-puncture unit
- Viterbi decoder
- De-scrambler unit
- Flexible / programmable de-interleaver data flow and control processor
- Multiple stream processing at small granularity
- Two direct memory access master units connected to the chips main communication fabric

7.10.4 Source decoding and control DSP

Any data/audio stream or any basic control processing is designated to perform in software. The main backbone for these tasks is a standard DSP core. It includes infra-structure components such as tightly coupled memories, caches and user-defined instruction extensions, especially suited to support audio processing and decoding algorithms.

The basic processor IO for any data stream can be done via an internal on-chip bus. It is suited to consume processing data from the main memory or any other DMA client and to produce processed data into the next system unit.

7.11 IC control unit

7.11.1 VREG_1V2

This voltage regulator generates the 1.2 V supply voltage used in SAF400x. The regulator circuitry consists of an internal control loop and an external NPN power transistor. Using this voltage regulator, the SAF400x requires just a single 3.3 V power supply.

7.11.2 VREG_1V8

This voltage regulator generates the 1.8 V supply voltage used in SAF400x. The regulator circuitry consists of an internal control loop and an external NPN power transistor. Using this voltage regulator, the SAF400x requires just a single 3.3 V power supply.

7.11.3 RESET

The reset generator controls the start-up sequence of all units. The generator takes care that all processing units will be set in a defined state during and after the reset phase.

POR (power-on reset) — also called cold boot.

Reset via RESET_N pin — an active low on RESET_N pin starts the sequence.

Watchdog reset — internally initiated reset on certain error conditions. During the watchdog reset, the boot process is halted. A reset via RESET_N pin or a power-on reset initiates the boot process. During a watchdog reset, the host can read the cause of reset via the SPI interface.

7.11.4 Security

The security module is used to manage key code and password storage and related security features including decryption to run protected audio codecs. It also includes the non-volatile storage for all related secure information.

- One device internal non-volatile memory for NXP-related information
- Programmable AES decryption engine
- Internal DMA flow control capability

Due to its independent DMA capabilities, the security engine does not require any data management support other than setting up the desired operation modes.

The following security mechanisms are supported in SAF400x:

- Secure boot
- Secure keycodes
- JTAG password protection

The secure boot mechanism of the SAF400x enables the different processor images to be encrypted. The encryption of the images is, typically, done offline, while the decryption is done during the SAF400x boot process, using an AES hardware accelerator. The image decryption process uses decryption keys that are programmed in OTP memory. The OTP memory is programmed by NXP and contains the NXP decryption keys for images provided by NXP, keycodes and JTAG password.

Several features of the SAF400x are protected by keycodes. The keycodes are subject to a commercial agreement and must be obtained via the NXP commercial department. The keycode is a bit-sequence, transferred via an SPI interface during the boot procedure and is, typically, sent by the host controller.

The JTAG interface of the SAF400x can be used to debug a program running on the Tensilica processors. However, the JTAG interface to the Tensilica processors is locked by default and a password is required to unlock it. The JTAG password can be obtained from the NXP commercial department.

7.11.5 I²C-bus

The I²C-bus is a communication interface between the SAF400x and other on-board devices (as example SAF7771). The I²C-bus interface can handle both data and control.

Switching between the different operational modes is handled internally.

- The I²C-bus interface (slave) can be used to control the device
- The I²C-bus interface (master) is available for control of other devices

The I²C-bus interface supports 400 kbit/s (fast mode) according to Ref. 3.

Exception to the I²C-bus specification: When SDA remains HIGH during this 9th clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. There are five conditions that lead to the generation of a NACK:

1. No receiver is present on the bus with the transmitted address so there is no device to respond with an acknowledge.
2. The receiver is unable to receive or transmit because it’s performing some real-time function and is not ready to start communication with the master.
3. During the transfer the receiver gets data or commands that it does not understand.
4. During the transfer, the receiver cannot receive any more data bytes.
5. A master-receiver needs to signal the end of the transfer to the slave transmitter

SAF400X does not support condition 4 from the spec by generating a NACK and to avoid data loss, clock stretching mechanism is used.

The two embedded I²C-bus communication units have the following features:

- Two standard I²C-bus units suited to run in fast mode at up to 400 kHz
- Master and slave operation capable
- Software configurable I²C-bus addresses
- Integrated FIFO to decouple incoming and outgoing data rates

These units are typically used to communicate to external tuner devices and system hosts. Both units require software support to run the required protocol or link layer services on the integrated I²C-bus units to allow full-blown communication.

7.11.6 Quad SPI

The SAF400X has one quad SPI interface. This interface is a master interface and is used to connect to flash with a maximum data rate of 400 Mbit per sec.

The embedded quad SPI communication interface support the following SPI formats:

- Motorola Serial Peripheral Interface (SPI)
- Texas Instruments Serial Protocol (SSP)
- National Semiconductor Microwire

This unit is used to communicate to on-board flash memories for fast download of main software image during boot. The unit require software support to run the required protocol or link layer services on the integrated SPI bus units to allow full-blown communication.

7.11.7 SPI

The SAF400X has two SPI interfaces. The SPI1 interface is used for control of the device. The SPI0 interface can be used for other control, like open core software control.

The two embedded SPI communication interfaces support the following SPI formats:

- Motorola Serial Peripheral Interface (SPI)
- Texas Instruments Serial Protocol (SSP)
- National Semiconductor Microwire

The following configurations and features are available in these systems:

- two master or slave unit combination for standard speed SPI traffic
- Full duplex protocol support
- Integrated FIFO to decouple incoming and outgoing data rates

These units are typically used to communicate to system host. They are also used to download the main software image during boot in a host controlled system. All units require software support to run the required protocol or link layer services on the integrated SPI bus units to allow full-blown communication.

7.11.8 GPIO MUX

A specific feature can be assigned to a GPIO. The features cover three different domains:

- Radio
- Audio
- Control

The following radio features use a GPIO pin:

- RDS data available indicator for the primary and secondary path (output)
- Quality status interrupt for the primary and secondary path (output)
- Fast quality change for the primary and secondary path (output)
- Scanning antenna control signal (output)
- DAB tuner control (input/output)

The following audio features use a GPIO pin:

- Click-clack (input)
- Clip connect limiters (input)

- De-emphasis (input)
- Fast mute (input)
- Digital radio blend (input)

The generic features include reading a specific GPI or writing to a specific GPO.

7.11.9 JTAG

The JTAG interface of the SAF400x can be used to debug a program running on the Tensilica processors. However, the JTAG interface to the Tensilica processors is locked by default and a password is required to unlock it. The JTAG password can be obtained from the NXP commercial department.

7.11.10 System booting

The SAF400X supports the following boot modes:

- Booting the firmware images from a serial flash connected to the quad SPI port
- Booting the firmware images from an external host processor via SPI_0 or SPI_1 port

The boot mode selection is possible via the GPIO-0 pin which is configured as a boot strap pin during power-on/reset. When GPIO-0 is driven active LOW, SAF400x loads the firmware from the external serial flash. Otherwise, it waits for the firmware to be loaded via the SPI port.

The boot process requires a secondary boot loader image to be loaded prior to any other firmware images. The firmware images including the secondary boot loader are based on a custom file format and is protected by means of encryption and signature. The flash file system is also proprietary.

During booting, the SPI slave interface is configured in Motorola format mode 1 (clock polarity low with clock phase on second edge) and supports a speed range of 100 KHz to 20 MHz with a recommended speed of 10 MHz.

The flash boot supports both quad mode SPI flashes and standard SPI flashes. The supported flash sizes are 8 Mbit to 128 Mbit. The initial flash read out happens with a clock speed of 2 MHz in standard SPI mode even if the flash supports quad mode. After identifying a secondary boot loader image in the flash, the flash read out switches to a configured speed in the flash image. The supported speeds for secondary boot loader image loading from flash are 22 MHz, 18.33 MHz, 15.7 MHz, 10 MHz, 5 MHz and 2 MHz. The secondary boot loader image loading always happens in standard mode. Further firmware image loading can happen in quad mode depending on the flash capability. With quad mode, higher clock speeds are configurable and the supported speeds are 110 MHz, 55 MHz and 22 MHz.

8. Limiting values

Table 22. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog supplies						
V_{DDA3V3}	analog supply voltage (3.3 V)	audio codec	–0.5	-	+3.9	V
V_{DDA1V8}	analog supply voltage (1.8 V)	RF	–0.5	-	+2.4	V
V_{DDA1V2}	analog supply voltage (1.2 V)	PLL	–0.5	-	+1.6	V
Digital supplies						
V_{DDD3V3}	digital supply voltage (3.3 V)	I/O	–0.5	-	+3.9	V
V_{DDD2V5}	digital supply voltage (2.5 V)	polyfuse	–0.5	-	+2.7	V
V_{DDA1V2}	digital supply voltage (1.2 V)	core and memory	–0.5	-	+1.6	V
Input voltages/current						
V_i	input voltage		–0.5	-	+3.9	V
V_{ESD}	electrostatic discharge voltage	human body model pass voltage level[1]				
		all pins	2000	-		V
		charge device model pass voltage level[2]				
		corner pins	750	-	-	V
		all other pins	500	-	-	V
Temperature						
T_{stg}	storage temperature	[3]	–55	-	+150	°C
T_{amb}	ambient temperature		–40	+25	+85	°C
T_j	junction temperature	[4]	–40	+25	+125	°C
Dissipation						
P_{tot}	total power dissipation		-	-	2500	mW
Thermal characteristics						
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	<tbd>	-	K/W

[1] Class 2 according to *AEC-Q100-002 Rev-E.*

[2] Class C4B according to *AEC-Q100-011 Rev-C.*

[3] Exposure for long time to very low or high temperature may affect product reliability.

[4] Range for correct functional behavior of product.

9. Recommended operating conditions

Table 23. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature						
T_{amb}	ambient temperature		-	25	-	°C
Power dissipation						
P_{tot}	total power dissipation	[1]	-	-	<tbd>	W

[1] Software release R<x>.

10. Thermal characteristics

Table 24. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	four-layer board [1][2][3][4]	<tbd>	K/W

[1] The overall $R_{th(j-a)}$ is based on JEDEC conditions and can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly, and all NC pins must be connected to the ground layer. An ample amount of copper area directly under the device with a number of through-hole plating, which connect to the ground layer (multiple-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. In addition, the use of soldering glue with a high thermal conductance after curing is recommended.

[2] Since a BGA package has different heat transfer coefficients in either direction, it is not recommended to use the above thermal resistance as an input to any thermal simulation but use a compact model instead. A model is available at NXP application and design in support on request.

[3] Simulation results assuming a four-layer board with a copper layer thickness of approximately 35 mm; size: <tbd> mm × <tbd> mm; thermal landing pattern connected to a large ground plane on the lower layers by multiple thermal vias; copper coverages approximately 90 % per layer.

[4] The number of thermal vias is <p> thermal with <d> mm diameter.

11. Characteristics

11.1 Static characteristics

Table 25. Current for each supply pin

Recommended operating conditions. Typ: T_{amb} = 25 °C; typical silicon, typical use case per pin. Max: T_{amb} = 85 °C; worst case silicon, worst case use case per pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
$V_{DDA(RF)(3V3)}$	RF analog supply voltage (3.3 V)		1.7	1.8	1.89	V
$V_{DDA(IF)(3V3)}$	IF analog supply voltage (3.3 V)		1.7	1.8	1.89	V
$V_{DDD(IO)(3V3)}$	input/output digital supply voltage (3.3 V)		3.0	3.3	3.5	V
$V_{DDA(CODEC)(3V3)}$	CODEC analog supply voltage (3.3 V)		3.0	3.3	3.5	V
$V_{DDA(PLL)(1V2)}$	PLL analog supply voltage (1.2 V)		1.14	1.2	1.26	V
$V_{DDD(C)(1V2)}$	core digital supply voltage (1.2 V)		1.14	1.2	1.26	V
$V_{DDD(MEM)(1V2)}$	memory digital supply voltage (1.2 V)		1.14	1.2	1.26	V
V_{QPS}	OTP programming voltage (2.5 V)		2.25	2.5	2.75	V
V_{SSD}	common ground		−0.5	0	0.5	V
Supply current						
$I_{DDA(RF)}$	RF analog supply current		-	-	<tbd>	mA
$I_{DDA(IF)}$	IF analog supply current		-	-	<tbd>	mA
$I_{DDD(IO)}$	input/output digital supply current		-	-	<tbd>	mA
$I_{DDA(CODEC)}$	CODEC analog supply current		-	-	<tbd>	mA
$I_{DDA(SPDIF)}$	S/PDIF analog supply current		-	-	<tbd>	mA
I_{DDD}	digital supply current		-	-	<tbd>	mA

Table 25. Current for each supply pin *…continued*

Recommended operating conditions. Typ: T_{amb} = 25 °C; typical silicon, typical use case per pin. Max: T_{amb} = 85 °C; worst case silicon, worst case use case per pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA(PLL)}$	PLL analog supply current		-	-	<tbd>	mA
$I_{DDD(C)}$	core digital supply current		-	-	<tbd>	mA
$I_{DDD(MEM)}$	memory digital supply current		-	-	<tbd>	mA

11.2 Radio characteristics

Table 26. FM radio characteristics

Recommended operating conditions: f_{RF} = 98.1 MHz; Δf = 22.5 kHz; f_{AF} = 1 kHz; 50 µs de-emphasis; IEC tuner filter 50 Ω / −6 dB dummy antenna. All signals in RMS at input dummy; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RF}	RF frequency	FM (OIRT) tuning range	64	-	74	MHz
		FM (US, Japan, EU) tuning range	76	-	108	MHz
$V_{i(sens)}$	input sensitivity voltage	$V_{i(RF)}$ for (S+N) / N = 26 dB; weak signal handling ON; channel equalizer ON	-	−4	-	dBµV
(S+N)/N	signal plus noise-to-noise ratio	mono; $V_{i(RF)}$ = 60 dBµV	65	70	-	dB
		stereo; $V_{i(RF)}$ = 60 dBµV	60	65	-	dB
$\alpha_{sup(AM)}$	AM suppression	$V_{i(RF)}$ = 60 dBµV; f_{AF} = 1 kHz; m = 30 %	65	70	-	dB
THD	total harmonic distortion	$V_{i(RF)}$ = 60 dBµV; f_{AF} = 1 kHz; mono; Δf = 75 kHz	-	0.01	0.1	%
		stereo L-only; Δf = 67.5 kHz	-	0.1	0.3	%
α_{image}	image rejection	$f_{RF(image)} = f_{RF(wanted)} \pm 2 \times f_{IF}$	80	-	-	dB
S	selectivity	$V_{RF(wanted)}$ = 20 dBµV; $\Delta f_{(wanted)}$ = 22.5 kHz for 0 dB reference; $f_{AF(wanted)}$ = 1 kHz; $f_{RF(unwanted)} = f_{RF(wanted)} \pm \delta f_{RF}$; $\Delta f_{(unwanted)}$ = 22.5 kHz; $f_{AF(unwanted)}$ = 1 kHz; increase $V_{RF(unwanted)}$ until SNR = 26 dB; S = $V_{RF(unwanted)}$ / $V_{RF(wanted)}$; channel equalizer ON				
		δf_{RF} = 100 kHz	60	70	-	dB
		δf_{RF} = 200 kHz	68	74	-	dB
		δf_{RF} = 300 kHz	74	78	-	dB
IP3	third-order intercept point	f_{RF} = 98.1 MHz; $f_{RF(unwanted)1}$ = 98.5 MHz; $f_{RF(unwanted)2}$ = 98.9 MHz	122	127	-	dBµV
$V_{i(RF)AGC(start)}$	start AGC RF input voltage	df = ±400 kHz	82	-	92	dBµV
		df = ±4 MHz	82	-	92	dBµV
$\alpha_{cr(AGC)}$	AGC control range		46	-	-	dB

Table 26. FM radio characteristics *…continued*

Recommended operating conditions: f_{RF} = 98.1 MHz; Δf = 22.5 kHz; f_{AF} = 1 kHz; 50 µs de-emphasis; IEC tuner filter 50 Ω / −6 dB dummy antenna. All signals in RMS at input dummy; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{cs}	channel separation	Δf = 67.5 kHz; f_{AF} = 1 kHz; Δf_{pilot} = 7.5 kHz; stereo L-only				
		$V_{i(RF)}$ = 20 dBµV; FMSI enabled	20	30	-	dB
		$V_{i(RF)}$ = 60 dBµV	50	-	-	dB
S_{RDS}	RDS sensitivity	Δf_{RDS} = 2 kHz; Δf_{FM} = 22.5 kHz; f_{AF} = 1 kHz; stereo; L = R				
		50% correct blocks without error correction	-	14	17	dBµV
		95% correct blocks without error correction	-	17.5	21	dBµV
N_{LEV}	LEV value	$V_{i(RF)}$ = 60 dBµV	57	60	63	dBµV
Dev	frequency deviation handling	THD = 3 %; f_{AF} = 1 kHz; Vdes = 80 dBµV	250	-	-	kHz
V_{FM_IN}	voltage	voltage on pin FM_IN	-	600	-	mV
R_i	input resistance	differential on FM_IN_P to FM_IN_M; f_{RF} = 100 MHz; AGC = 3	-	235	-	Ω
C_i	input capacitance	differential on FM_IN_P to FM_IN_M; f_{RF} = 100 MHz; AGC = 3	-	6.4	-	pF

Table 27. AM radio characteristics

Recommended operating conditions: m = 30 %; f_{AF} = 1 kHz; IEC tuner filter 15 pF / 60 pF dummy antenna. All signal in RMS at input dummy; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RF}	RF frequency	AM (LW) tuning range	144	-	288	kHz
		AM (MW) tuning range	522	-	1710	kHz
		AM (SW) tuning range	2300	-	27000	kHz
$V_{i(sens)}$	input sensitivity voltage	S/N = 26 dB; B_{audio} = 2 kHz; m = 30 %; weak signal handling on				
		AM (LW); f_{RF} = 207 kHz	-	39	-	dBµV
		AM (MW); f_{RF} = 990 kHz	-	33	-	dBµV
		AM (SW); f_{RF} = 6100 kHz	-	33	-	dBµV
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)}$ = 74 dBµV				
		AM (LW); f_{RF} = 207 kHz	57	60	-	dB
		AM (MW); f_{RF} = 990 kHz	62	65	-	dB
		AM (SW); f_{RF} = 6100 kHz	62	65	-	dB
THD	total harmonic distortion	$V_{i(RF)}$ = 60 dBµV				
		f_{AF} = 1 kHz; m = 80 %; f_{RF} = 207 kHz	-	0.1	0.3	%
		f_{AF} = 400 Hz; m = 80 %; f_{RF} = 990 kHz	-	0.1	0.3	%
		f_{AF} = 100 Hz; m = 80 %; f_{RF} = 6100 kHz	-	0.1	0.3	%

Table 27. AM radio characteristics *...continued*

Recommended operating conditions: m = 30 %; f_{AF} = 1 kHz; IEC tuner filter 15 pF / 60 pF dummy antenna. All signal in RMS at input dummy; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S_{stat}	static selectivity	single signal; δf_{RF} = 10 kHz; f_{tune} ± 10 kHz	80	90	-	dB
		single signal; δf_{RF} = 20 kHz; f_{tune} ± 20 kHz	90	-	-	dB
IP3	third-order intercept point	f_{RF} = 990 kHz; $f_{RF1(unwanted)}$ = 1030 kHz; $f_{RF2(unwanted)}$ = 1070 kHz	133	136	-	dBμV
		f_{RF} = 990 kHz; $f_{RF1(unwanted)}$ = 1290 kHz; $f_{RF2(unwanted)}$ = 1590 kHz;	133	136	-	dBμV
$V_{i(RF)AGC(start)}$	start AGC RF input voltage		90	-	103	dBμV
$\alpha_{cr(AGC)}$	AGC control range		54	60	-	dB
N_{LEV}	LEV value	f_{RF} = 1 MHz; m = 0 %; $V_{i(RF)}$ = 60 dBμV	57	60	63	dBμV
V_{FM_IN}	voltage	voltage on pin AM_IN	-	600	-	mV
R_i	input resistance	on pin AM_IN	-	2	-	MΩ
C_i	input capacitance	on pin AM_IN	-	150	-	pF

Table 28. Weather band

Recommended operating conditions; f_{RF} = 162.500 MHz; Δf = 1.5 kHz; f_{AF} = 400 Hz; 110 μs de-emphasis; IEC tuner filter 75 Ω/–6 dB dummy antenna. All signals in RMS at input dummy; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RF}	RF frequency		162.4	-	162.55	MHz
$V_{i(sens)}$	input sensitivity voltage	(S+N)/N = 26 dB	-	5	-	dBμV
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)}$ = 20 dBμV	-	41	-	dB
THD	total harmonic distortion	$V_{i(RF)}$ = 60 dBμV; Δf = 5 kHz; f_{AF} = 400 Hz	-	-	0.2	%
α_{image}	image rejection	$f_{RF(image)} = f_{RF(wanted)} \pm 2 \times f_{IF}$	80	-	-	dB
S	selectivity	δf_{RF} = 25 kHz	50	65	-	dB
		δf_{RF} = 50 kHz	60	70	-	dB

Table 29. DAB VHF band III characteristics

EEP3A protection profile.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RF}	RF frequency		167.392	-	239.968	MHz
$V_{i(sens)}$	input sensitivity voltage	R = 1/2; BER = 10^{-4}	-	–102	–100	dBm
ACR	adjacent channel rejection	R = 1/2; BER = 10^{-4}; $V_{i(RF,wanted)}$ = –70 dBm	45	55	-	dB

Table 29. DAB VHF band III characteristics *...continued*

EEP3A protection profile.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S_{fo}	far-off selectivity	R = 1/2; BER = 10^{-4}; $V_{i(RF,wanted)}$ = −70 dBm; Δf_{RF} = 5 MHz	65	70	-	dB
$A_{i(max)}$	maximum input voltage	R = 1/2; BER = 10^{-4}	-	-	10	dBm
V_{FM_IN}	voltage	voltage on pin DAB_IN	-	600	-	mV
R_i	input resistance	differential on DAB_IN_P to DAB_IN_M; f_{RF} = 200 MHz; AGC = 0	-	235	-	Ω
C_i	input capacitance	differential on DAB_IN_P to DAB_IN_M; f_{RF} = 200 MHz; AGC = 0	-	4	-	pF

Table 30. HD radio characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RF}	RF frequency	FM band tuning range	87.9	-	107.9	MHz
		AM band tuning range	530	-	1710	MHz
$V_{i(sens)}$	input sensitivity voltage	FM band; P1BER ≤ $5e^{-5}$; FM hybrid signal with a total band power of the specified level, single tuner	-	-	−92	dBm
		FM band; P1BER ≤ $5e^{-5}$; FM all digital signal with a total band power of the specified level, single tuner	-	-	−113	dBm
		AM hybrid clean signal, P1BER ≤ $1e^{-4}$	-	-	−98.5	dBm
		AM all digital signal, P1 BER ≤ $1e^{-4}$	-	-	−108.5	dBm
ACR	adjacent channel rejection	P1BER ≤ $5e^{-5}$; desired: FM hybrid signal; interferers: 15th and 30th adjacent (both−20 dBm), <tbd> FM source	50	-	-	dB
		P1BER ≤ $5e^{-5}$; desired: FM all digital signal; interferers: 15th and 30th adjacent (both−20 dBm), <tbd> FM source	<tbd>	-	-	dB
		P3BER ≤ $1e^{-4}$; desired: AM hybrid signal; peak power −62 dBm; interferer: upper 1st adjacent; hybrid signal	20	-	-	dB
		P3BER ≤ $1e^{-4}$; desired: AM all digital signal; peak power −70 dBm; interferer: lower 2nd adjacent; hybrid signal	20	-	-	dB

Table 30. HD radio characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{i(max)}$	maximum input power	P1BER and PIDS block errors 0 for a hybrid FM HD signal with a total band power of specified maximum level	−2	-	-	dBm
		P1BER and PIDS block errors 0 for all digital FM HD signal with a total band power of specified maximum level	−12	-	-	dBm
		hybrid HD AM signal; P1BER = 0, P3BER = 0, PIDS BLKER ≤ $5e^{-2}$	−26	-	-	dBm
		all digital HD AM signal; P1BER = 0, P3BER = 0, PIDS BLKER ≤ $5e^{-2}$	−26	-	-	dBm

Table 31. DRM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RF}	RF frequency	category LF tuning range	148.5	-	283.5	kHz
		category MF tuning range	525	-	1710	kHz
		category HF1 tuning range	2300	-	6200	kHz
		category HF2 tuning range	6200	-	30000	MHz
$V_{i(sens)}$	input sensitivity voltage	R = 1/2; BER = 10^{-4}				
		category LF; f_{RF} = 216 kHz	-	-	2	dBμV
		category MF; f_{RF} = 999 kHz	-	-	2	dBμV
		category HF1; f_{RF} = 4000 kHz	-	-	2	dBμV
		category HF2; f_{RF} = 19000 kHz	-	-	2	dBμV
ACR	adjacent channel rejection	desired signal at 18 dBμV; undesired first adjacent at 28 dBμV above desired signal level	35	-	-	dB
		desired signal at 18 dBμV; undesired second adjacent at 38 dBμV above desired signal level	44	-	-	dB
		desired signal at 18 dBμV; undesired third adjacent at 48 dBμV above desired signal level	53	-	-	dB
S_{fo}	far-off selectivity	R = 1/2; BER = 10^{-4}; $V_{i(RF,wanted)}$ = −80 dBm; Δf_{RF} = 400 kHz	70	-	-	dB
$A_{i(max)}$	maximum input voltage	reference at 8 dBμV; LW band, MW-band, SW1-band, SW2-band	100	-	-	dBm

Table 31. DRM characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<tbd>	blocker desensitization	desired signal at 11 dBμV; LW Band, MW-band, SW1-band; SW2-band	66	-	-	dB
<tbd>	receiver linearity	desired signal at 28 dBμV; LW Band, MW-band, SW1-band; SW2-band	60	-	-	dB
<tbd>	co-channel selectivity	desired signal at 28 dBμV; co-channel selectivity frequency offset in range of −5 kHz to +5 kHz	−5	-	-	dB

11.3 ADC characteristics

Table 32. Audio ADC characteristics (differential mode)

Recommended operating conditions: $V_{DDA(3V3)}$ = 3.3 V, $V_{DDD(3V3)}$ = 3.3 V, $V_{DDD(1V2)}$ = 1.2 V, f_s = 44.1 kHz in audio master mode and differential mode, T_{amb} = 25 °C. AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_i	input resistance		15	-	27	kW
V_i	input voltage	2 V mode; (THD+N)/S = −40 dB	-	-	2.2	V
		1 V mode; (THD+N)/S = −40 dB	-	-	1.1	V
N_O	output value	f_i = 1 kHz; V_i = 2 V for 2 volt mode	−4.9	-	−1.9	dBFS
		f_i = 1 kHz; V_i = 1 V for 1 volt mode	−4.9	-	−1.9	dBFS
$N_{O(unb)}$	unbalance output value	f_i = 1 kHz; V_i = 2 V for 2 volt mode or V_i = 1 V for 1 volt mode	−0.2	-	0.2	dB
CMRR	common-mode rejection ratio	f_i = 1 kHz; V_i = 35 mV; $R_{source} \leq 20\ \Omega$	55	-	-	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; V_{ripple} = 35 mV	60	-	-	dB
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	f_i = 1 kHz; V_i = 2 V for 2 volt mode	-	-	−80	dB
		f_i = 1 kHz; V_i = 1 V for 1 volt mode	-	-	−80	dB
		f_i = 1 kHz; V_i = 2 mV for 2 volt mode; A-weighted	-	-	−32	dB(A)
		f_i = 1 kHz; V_i = 1 mV for 1 volt mode; A-weighted	-	-	−32	dB(A)
$\alpha_{ct(ch)}$	channel crosstalk	f_i = 1 kHz; V_i = 2 V for 2 volt mode	-	-	−85	dB

Table 33. Audio ADC characteristics (pseudo differential and single ended mode)

Recommended operating conditions: $V_{DDA(3V3)}$ = 3.3 V, $V_{DDD(3V3)}$ = 3.3 V, $V_{DDD(1V2)}$ = 1.2 V, f_s = 44.1 kHz in audio master mode and pseudo differential and single ended mode, T_{amb} = 25 °C. AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_i	input resistance		15	-	27	kΩ
V_i	input voltage	2 V mode; (THD+N)/S = –40 dB	-	-	2	V
		1 V mode; (THD+N)/S = –40 dB	-	-	1.1	V
		0.5 V mode; (THD+N)/S = –40 dB	-	-	0.55	V
N_O	output value	f_i = 1 kHz; V_i = 2 V for 2 volt mode	–4.9	-	–1.9	dBFS
		f_i = 1 kHz; V_i = 1 V for 1 volt mode	–4.9	-	–1.9	dBFS
		f_i = 1 kHz; V_i = 0.5 V for 0.5 volt mode	–4.9	-	–1.9	dBFS
$N_{O(unb)}$	unbalance output value	stereo	–0.2	-	0.2	dBFS
CMRR	common-mode rejection ratio	f_i = 1 kHz; V_i = 35 mV; R_{source} ≤ 20 Ω; pseudo differential mode	55	-	-	dBFS
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; V_{ripple} = 35 mV	60	-	-	dB
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	f_i = 1 kHz; V_i = 2 V in 2 volt mode	-	-	–80	dB
		f_i = 1 kHz; V_i = 1 V in 1 volt mode	-	-	–80	dB
		f_i = 1 kHz; V_i = 2 mV in 2 volt mode; A-weighted	-	-	–35	dB(A)
		f_i = 1 kHz; V_i = 1 mV in 1 volt mode; A-weighted	-	-	–35	dB(A)
		f_i = 1 kHz; V_i = 0.5 mV in 0.5 volt mode	-	-	–80	dB
		f_i = 1 kHz; V_i = 0.5 mV in 0.5 volt mode; A-weighted	-	-	–29	dB(A)
$\alpha_{ct(ch)}$	channel crosstalk	f_i = 1 kHz; V_i = 2 V for 2 volt mode	-	-	–85	dB

11.4 I²S-bus timing specification

Table 34. I²S-bus timing specification

Recommended operating conditions; I²S pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{cy(clk)}$	clock time cycle	f_s = 8 - 96 kHz; asynchronous IIS	162.76	-	1953.13	ns
		f_s = 44.1 kHz; synchronous IIS	-	354.31	-	ns
		f_s = 48 kHz; synchronous IIS	-	325.52	-	ns
		f_s = 96 kHz; synchronous IIS	-	162.76	-	ns
δ	duty cycle		45	50	55	%
Output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	$V_{DDD(IO)3V3}$ − 0.4	-	$V_{DDD(IO)3V3}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	V_{SSD}	-	V_{SSD} + 0.4	V
C_L	load capacitance		-	50	-	pF
t_r	rise time	I_{OL} = 3 mA; C_L = 50 pF; f_s = 96 kHz	10	-	20	ns
		I_{OL} = 3 mA; C_L = 50 pF; f_s = 48 kHz or lower	25	-	46	ns
t_f	fall time	I_{OL} = 3 mA; C_L = 50 pF; f_s = 96 kHz	10	-	20	ns
		I_{OL} = 3 mA; C_L = 50 pF; f_s = 48 kHz or lower	25	-	46	ns
$t_{d(clk-WS)}$	clock to Word Select delay time	IIS master; V_{IL} = 0.8 V and V_{IH} = 2.0 V	0	-	10	ns
$t_{d(clk-data)}$	clock to data delay time	IIS master	0	-	10	ns
		IIS slave; f_s = 96 kHz	3	-	40	ns
		IIS slave; f_s = 48 kHz or lower	3	-	60	ns
Input signaling (3V3)						
V_{IH}	HIGH-level input voltage		2.0	-	$V_{DDD(IO)3V3}$ + 0.5	V
V_{IL}	LOW-level input voltage		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		0.1 × $V_{DDD(IO)3V3}$	-	-	V
$t_{su(WS)}$	Word Select set-up time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	2	-	-	ns
$t_{h(WS)}$	Word Select hold time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	8	-	-	ns
$t_{su(data)}$	data set-up time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	2	-	-	ns
$t_{h(data)}$	data hold time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	8	-	-	ns
$R_{pd(weak)}$	weak pull-down resistance		40	50	57	kΩ
C_i	input capacitance		-	8	10	pF

Table 34. I²S-bus timing specification *…continued*

Recommended operating conditions; I²S pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output signaling (current mode)						
I_{OH}	HIGH-level output current		–235	–360	–500	mA
I_{OL}	LOW-level output current		215	320	465	mA
$t_{d(clk-WS)}$	clock to Word Select delay time	IIS master; delay is measured at 50% point	0	-	10	ns
$t_{d(clk-data)}$	clock to data delay time	IIS master; delay is measured at 50% point	0	-	10	ns
		IIS slave; delay is measured at 50% point	12	-	30	ns
$V_{o(dc)}$	operating DC voltage		0.85	1.3	2.3	mV
Input signaling (current mode)						
I_{IH}	HIGH-level input current	input current to switch from LOW to HIGH (sourcing current)	80	-	1000	μA
I_{IL}	LOW-level input current	input current to switch from HIGH to LOW (sourcing current)	–20	-	–1000	μA
$t_{su(data)}$	data set-up time		2	-	-	ns
$t_{h(data)}$	data hold time		8	-	-	ns
$V_{i(dc)}$	operating DC voltage		0.85	1.3	1.5	V

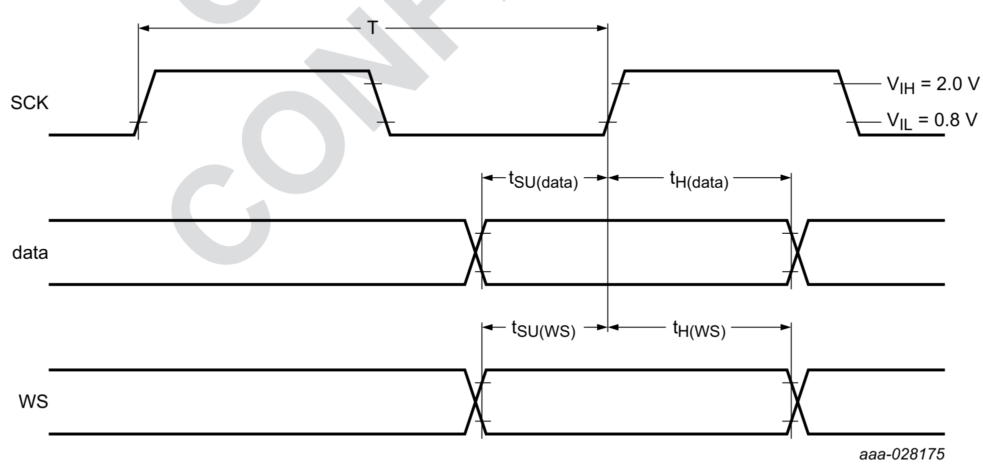


Fig 4. IIS receiver timing diagram

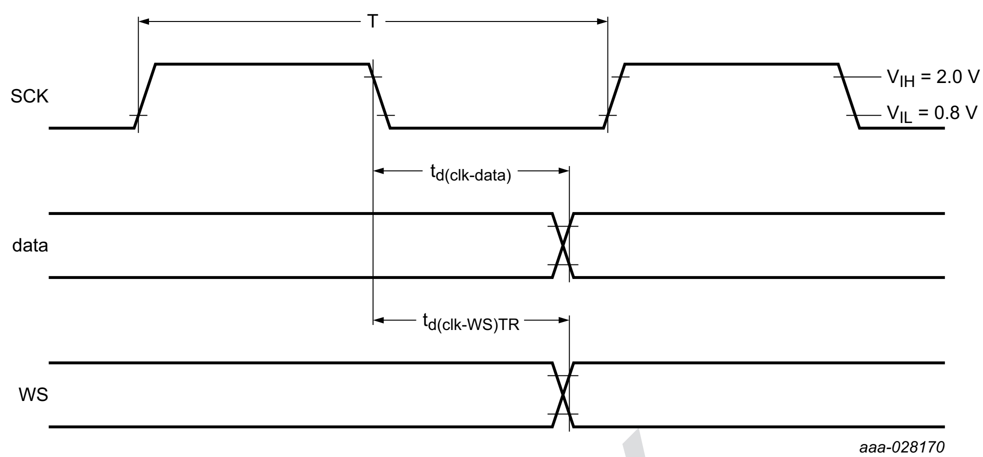


Fig 5. IIS transmitter diagram

11.5 PCM timing specification

Table 35. PCM characteristics

Recommended operating conditions; PCM pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified

Symbol	Parameter	Conditions Min	Min	Typ	Max	Unit
$t_{cy(clk)}$	clock time cycle	f_s = 8 kHz to 16 kHz	976.56	-	7812.5	ns
δ	duty cycle		45	50	55	%
Output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	$V_{DDD(IO)3V3} - 0.4$	-	$V_{DDD(IO)3V3}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	V_{SSD}	-	$V_{SSD} + 0.4$	V
C_L	load capacitance	-		50	-	pF
t_r	rise time	I_{OL} = 3 mA; C_L = 50 pF;	-	-	46	ns
t_f	fall time	I_{OL} = 3 mA; C_L = 50 pF;	-	-	46	ns
$t_{d(clk-framesync)}$	clock to frame sync delay time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	0	-	10	ns
$t_{d(clk-data)}$	clock to data delay time	PCM slave; V_{IL} = 0.8 V and V_{IH} = 2.0 V	3	-	60	ns
Input signaling (3V3)						
V_{IH}	HIGH-level input voltage		2.0	-	$V_{DDD(IO)3V3} + 0.5$	V
V_{IL}	LOW-level input voltage		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		$0.1 \times V_{DDD(IO)3V3}$	-	-	V
$t_{su(framesync)}$	frame sync set-up time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	5	-	-	ns
$t_{h(framesync)}$	frame sync hold time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	20	-	-	ns
$t_{su(data)}$	data set-up time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	5	-	-	ns

Table 35. PCM characteristics *...continued*

Recommended operating conditions; PCM pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified

Symbol	Parameter	Conditions Min	Min	Typ	Max	Unit
$t_{h(data)}$	data hold time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	20	-	-	ns
$R_{pd(weak)}$	weak pull-down resistance		40	50	57	kΩ
C_i	input capacitance	-	-	8	10	pF
Output signaling (current mode)						
I_{OH}	HIGH-level output current		−235	−360	−500	μA
I_{OL}	LOW-level output current		235	330	465	μA
$t_{d(clk-data)}$	clock to data delay time	PCM slave; delay is measured at 50% point	10	-	30	ns
$V_{o(dc)}$	operating DC voltage		0.85	1.3	2.3	V
Input signaling (current mode)						
I_{IH}	input current to switch from LOW to HIGH (sourcing current)		80	-	1000	μA
I_{IL}	input current to switch from HIGH to LOW (sourcing current)		−20	-	−1000	μA
$t_{su(data)}$	data set-up time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	5	-	-	ns
$t_{h(data)}$	data hold time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	20	-	-	ns
$V_{i(dc)}$	operating DC voltage		0.85	1.3	1.5	V

11.6 TDM timing specification

Table 36. TDM characteristics

Recommended operating conditions; TDM pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{cy(clk)}$	clock time cycle	f_s = 9 kHz - 96 kHz; asynchronous TDM		40.69	-	ns
		f_s = 44.1 kHz; synchronous TDM	-	88.58	-	ns
		f_s = 48 kHz; synchronous TDM	-	81.38	-	ns
δ	duty cycle		45	50	55	%
Output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	$V_{DDD(IO)3V3}$ − 0.4	-	$V_{DDD(IO)3V3}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	V_{SSD}	-	V_{SSD} + 0.4	V
C_L	load capacitance		-	50	-	pF

Table 36. TDM characteristics *…continued*
Recommended operating conditions; TDM pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	I_{OL} = 3 mA; C_L = 50 pF; f_s = 96 kHz	2	-	6	ns
		IOL = 3 mA; C_L = 50 pF; f_s = 48 kHz or lower	2	-	15	ns
t_f	fall time	I_{OL} = 3 mA; C_L = 50 pF; f_s = 96 kHz	2	-	6	ns
		I_{OL} = 3 mA; C_L = 50 pF; f_s = 48 kHz or lower	2	-	15	ns
$t_{d(clk-framesync)}$	clock to frame sync delay time		0	-	4	ns
$t_{d(clk-data)}$	clock to data delay time	TDM master; V_{IL} = 0.8 V and V_{IH} = 2.0 V	0	-	4	ns
		TDM slave; f_s = 96 kHz (rising edge); levels V_{IL} = 0.8 V and V_{IH} = 2.0 V;	6	-	17	ns
		TDM slave; f_s = 48 kHz or lower (rising edge); V_{IL} = 0.8 V and V_{IH} = 2.0 V;	11	-	26	ns
Input signaling (3V3)						
V_{IH}	HIGH-level input voltage		2	-	$V_{DDD(IO)3V3}$ + 0.5	V
V_{IL}	LOW-level input voltage		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		0.1 × $V_{DDD(IO)3V3}$	-	-	V
$t_{su(framesync)}$	frame sync set-up time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	6	-	-	ns
$t_{h(framesync)}$	frame sync hold time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	0	-	-	ns
$t_{h(data)}$	data hold time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	0	-	-	ns
$t_{su(data)}$	data set-up time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	6	-	-	ns
$R_{pd(weak)}$	weak pull-down resistance		40	50	57	kΩ
C_i	input capacitance		-	8	10	pF
Output signaling (current mode)						
I_{OH}	HIGH-level output current	f_s = 48 kHz or lower	-360	-550	-775	μA
I_{OL}	LOW-level output current	f_s = 48 kHz or lower	355	510	710	μA
$t_{d(clk-framesync)}$	clock to frame sync delay time	TDM master; delay is measured at 50% point	0	-	4	ns
$t_{d(clk-data)}$	clock to data delay time	TDM master; delay is measured at 50% point	0	-	4	ns
		TDM slave; delay is measured at 50% point (rising edge)	10	-	24	ns
$V_{i(dc)}$	operating DC voltage		0.85	1.3	2.3	V

Table 36. TDM characteristics *…continued*

Recommended operating conditions; TDM pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input signaling (current mode)						
I_{IH}	HIGH-level input current	input current to switch from LOW to HIGH (sourcing current)	80	-	1000	μA
I_{IL}	LOW-level input current	input current to switch from HIGH to LOW (sourcing current)	−20	-	−1000	μA
$t_{su(data)}$	data set-up time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	6	-	-	ns
$t_{h(data)}$	data hold time	V_{IL} = 0.8 V and V_{IH} = 2.0 V	0	-	-	ns
$V_{i(dc)}$	operating DC voltage		0.85	1.3	1.5	V

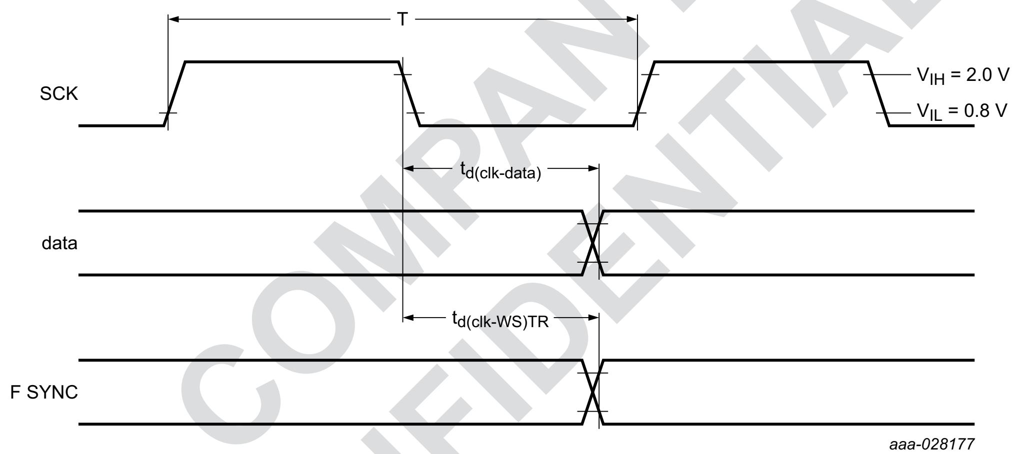


Fig 6. TDM master: Transmits on falling edge of the SCK

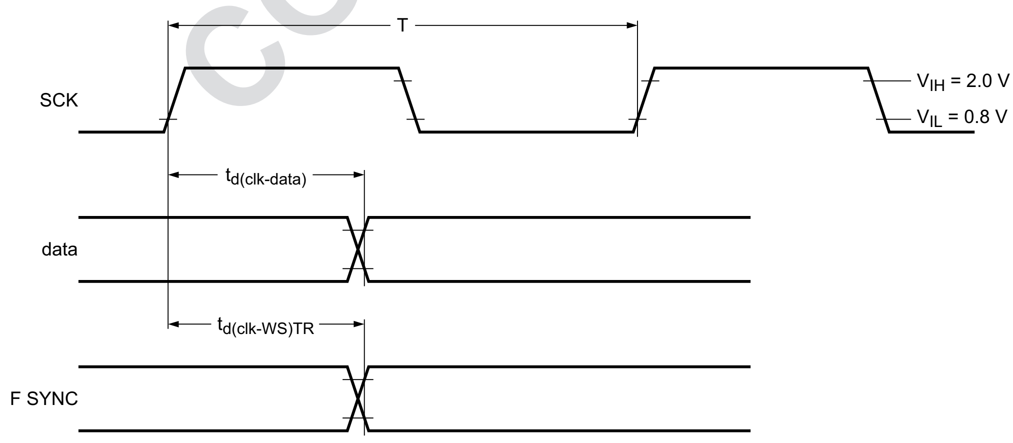


Fig 7. TDM slave: Transmits on falling edge of the SCK

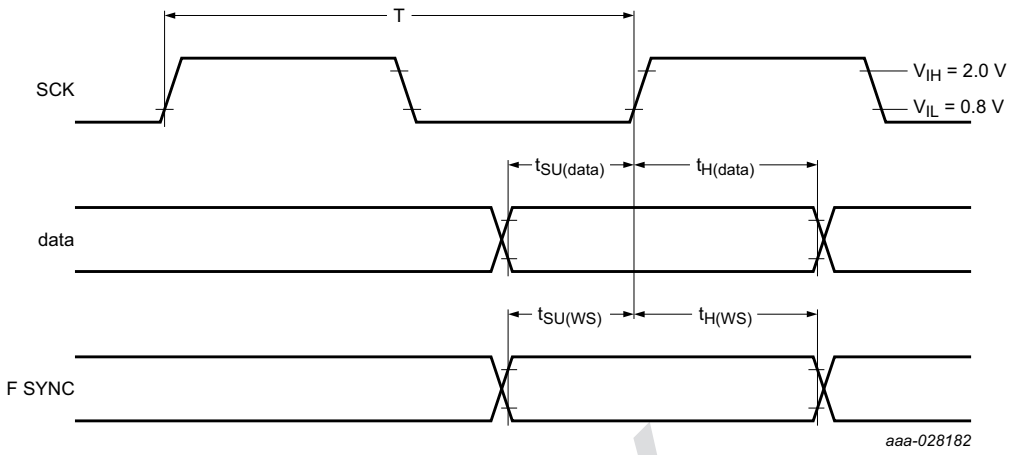


Fig 8. TDM receiver timing

11.7 Baseband interface

Table 37. Baseband interface (4-wires) characteristics

Recommended operating conditions. Pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{cy(clk)}$	clock cycle time	$f_{(clk)} = 1/t_{cy(clk)}$ [1]	16.03	-	96.15	ns
$t_{r(clk)}$	rise time	I_{OL} = 3 mA; C_L = 50 pF	-	0.15 × $t_{cy(CLK)}$	-	ns
$t_{f(clk)}$	fall time	I_{OL} = 3 mA; C_L = 50 pF	-	0.15 × $t_{cy(CLK)}$	-	ns
t_{BCLKH}	bit clock HIGH time		-	0.35 × $t_{cy(CLK)}$	-	ns
t_{BCLKL}	bit clock LOW time		-	0.35 × $t_{cy(CLK)}$	-	ns
δ	duty cycle		-	50	-	%
$t_{su(WS)}$	Word Select set-up time		0.2 × $t_{cy(clk)}$	-	-	ns
$t_{h(WS)}$	Word Select hold time		0.2 × $t_{cy(clk)}$	-	-	ns
$t_{S(data)}$	data set-up time		0.2 × $t_{cy(clk)}$	-	-	ns
$t_{h(data)}$	data hold time		0.2 × $t_{cy(clk)}$	-	-	ns
Output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	$V_{DDD(IO)3V3}$ − 0.4	-	$V_{DDD(IO)3V3}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	V_{SSD}	-	V_{SSD} + 0.4	V
C_L	load capacitance		-	50	-	pF
$t_{d(clk-WS)}$	clock to Word Select delay time		-	-	0.15 × $t_{cy(clk)}$	ns
$t_{d(clk-data)}$	clock to data delay time		-	-	0.15 × $t_{cy(clk)}$	ns
$t_{f(o)}$	output fall time	I_{OL} = 3 mA; C_L = 50 pF	-	0.15 × $t_{cy(BCLK)}$	-	ns

Table 37. Baseband interface (4-wires) characteristics *…continued*

Recommended operating conditions. Pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input signaling (3V3)						
V_{IH}	HIGH-level input voltage		2	-	$V_{DDD(IO)3V3}$	V
V_{IL}	LOW-level input voltage		–0.3	-	0.8	V
V_{hys}	hysteresis voltage		0.1 × $V_{DDD(IO)3V3}$	-	-	V
$V_{i(p-p)}$	peak-to-peak input voltage		-	50	-	mV
$R_{pu(weak)}$	weak pull-up resistance		40	50	57	kΩ
$R_{pd(weak)}$	weak pull-down resistance		40	50	57	kΩ
C_i	input capacitance		-	8	-	pF
Output signaling (current mode)						
I_{OH}	HIGH-level output current	V_{OH} = 1 V	+100	-	-	μA
I_{OL}	LOW-level output current	V_{OL} = 1 V	–100	-	-	mA
$V_{i(dc)}$	operating DC voltage		0.85	1.3	2.3	V
Input signaling (current mode)						
I_{IH}	HIGH-level input current		100	-	-	μA
I_{IL}	LOW-level input current		–100	-	-	μA
$V_{o(dc)}$	operating DC voltage		0.85	1.3	1.5	V

[1] HD Radio

[1] DRM.

[1] DAB.

11.8 SPI interface

Table 38. SPI interface characteristics

Recommended operating conditions; clock frequency of 10 MHz. Pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input signaling (3V3)						
V_{IH}	HIGH-level input voltage		2	-	$V_{DDD(IO)3V3}$ + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	-	+0.8	V
V_{hys}	hysteresis voltage		0.1 × $V_{DDD(IO)3V3}$	-	-	V
$R_{pu(weak)}$	weak pull-up resistance		40	50	57	kΩ
$R_{pd(weak)}$	weak pull-down resistance		40	50	57	kΩ
C_i	input capacitance		-	8	-	pF

Table 38. SPI interface characteristics *…continued*

Recommended operating conditions; clock frequency of 10 MHz. Pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(clk)}$	SCL clock frequency	slave mode	0	-	20	MHz
δ	duty cycle		45	50	55	%
$t_{su(data)}$	data set-up time	slave mode	10	-	-	ns
$t_{hd(data)}$	data hold time	slave mode	$0.5/f_{(clk)}$	-	-	ns
t_{SPILAG}	SPI enable lag time		$0.5/f_{(clk)}$	-	-	ns
$t_{SPILEAD}$	SPI enable lead time	non-delayed mode	$0.5/f_{(clk)}$	-	-	ns
$t_{WH(S)}$	chip select pulse width HIGH		$0.5/f_{(clk)}$	-	-	ns
Output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	$0.9 \times V_{DDD(IO)3V3}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	$0.1 \times V_{DDD(IO)3V3}$	V
C_L	load capacitance		-	15	-	pF
$t_{v(Q)}$	data output valid time	slave mode	-	-	20	ns
$t_{h(Q)}$	data output hold time	slave mode	$1/f_{(clk)}$	-	-	ns
$t_{r(o)}$	output rise time	slave mode	-	1.4	-	ns
$t_{f(o)}$	output fall time	slave mode	-	1.4	-	ns

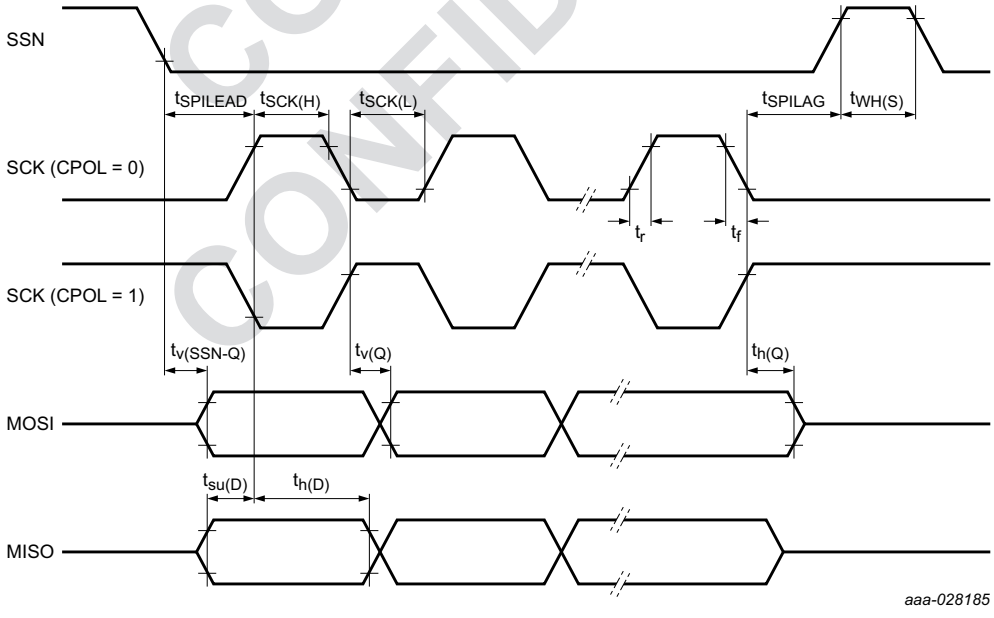


Fig 9. SPI master timing diagram (CPHA = 0)

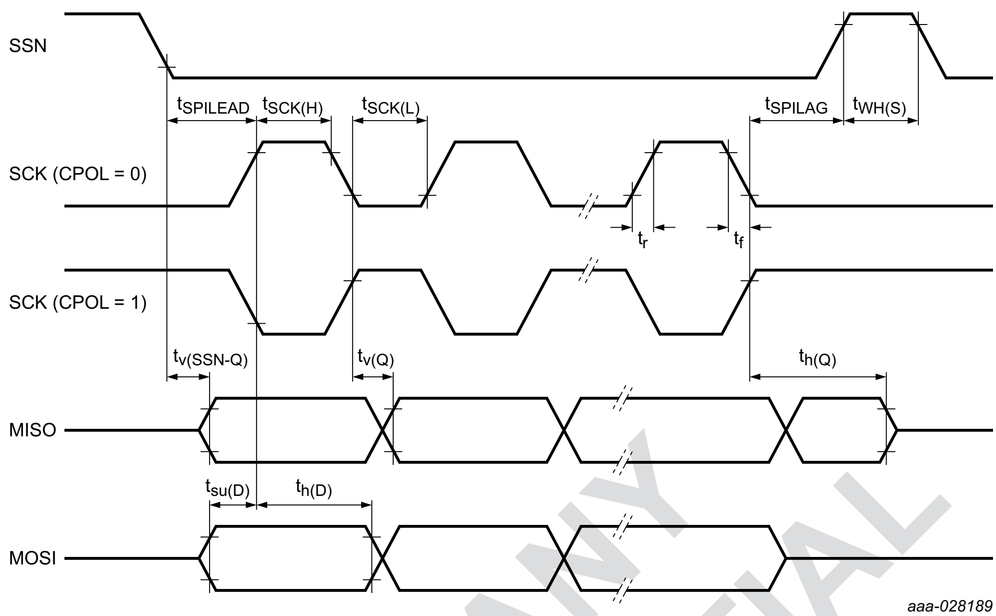


Fig 10. SPI slave timing (CPHA = 0)

11.9 Quad SPI interface

Table 39. Quad SPI interface characteristics

Recommended operating conditions; clock frequency of 10 MHz. Pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input signaling (3V3)						
V_{IH}	HIGH-level input voltage		2	-	$V_{DDD(IO)3V3}$ + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	+0.8	V
V_{hys}	hysteresis voltage		0.1 × $V_{DDD(IO)3V3}$	-	-	V
$R_{pu(weak)}$	weak pull-up resistance		40	50	57	kΩ
$R_{pd(weak)}$	weak pull-down resistance		40	50	57	kΩ
C_i	input capacitance		-	8	-	pF
Output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	0.9 × $V_{DDD(IO)3V3}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.1 × $V_{DDD(IO)3V3}$	V
C_L	load capacitance		-	15	-	pF
$f_{(clk)}$	SCL clock frequency		-	-	110	MHz
δ	duty cycle		45	50	55	%
t_{SPILAG}	SPI enable lag time		1.5 × T_{cyc}	-	-	ns
$t_{SPILEAD}$	SPI enable lead time		0.5 × T_{cyc}	-	-	ns

Table 39. Quad SPI interface characteristics *…continued*

Recommended operating conditions; clock frequency of 10 MHz. Pins can be configured as 3.3 V pins or as low-voltage pins; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SSN-Q)}$	SSN to data output		-	-	T_{cyc}	ns
$t_{v(Q)}$	data output valid time		0	-	1	ns
$t_{h(Q)}$	data output hold time		T_{cyc}	-	-	ns
$t_{su(D)}$	data input setup time		1	-	-	ns
$t_{h(D)}$	data input hold time		$0.5 \times T_{cyc}$	-	-	ns

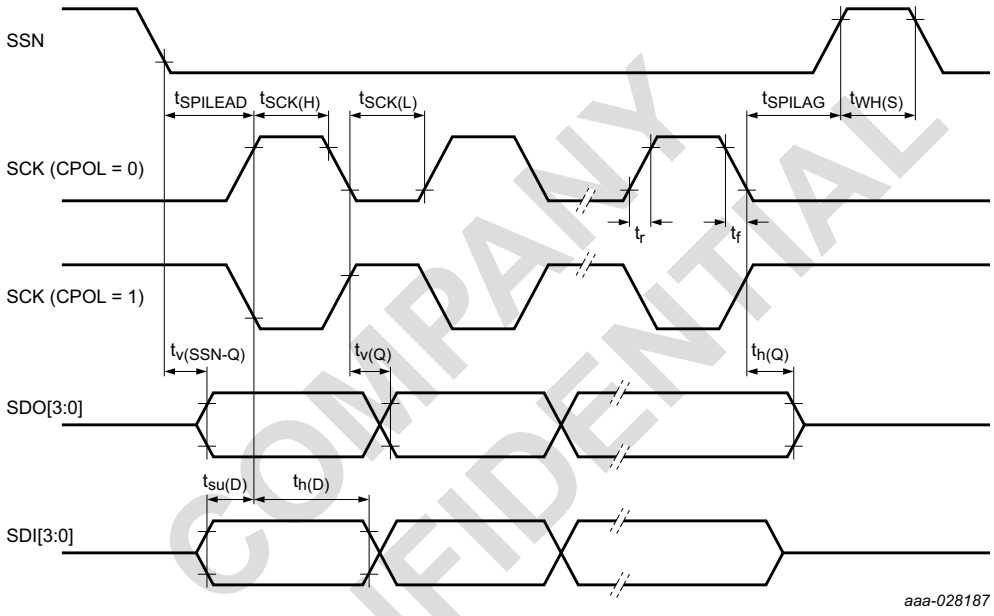


Fig 11. QuadSPI master timing diagram (CPHA = 0)

11.10 I²C-bus interfaces

Table 40. I²C-bus interface characteristics

The I²C-bus is 3.3 V tolerant; Recommended operating conditions; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	-	-	$V_{DDD(IO)3V3}$ + 0.5	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA; $V_{DDD(IO)}$ > 2 V	V_{SSD}	-	V_{SSD} + 0.4	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $f_{(scl)}$ = 400 kHz	3	-	-	mA
		V_{OL} = 0.6 V; $f_{(scl)}$ = 400 kHz	6	-	-	mA
C_b	capacitive load for each bus line		-	-	400	pF

Table 40. I²C-bus interface characteristics *…continued*

The I²C-bus is 3.3 V tolerant; Recommended operating conditions; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(scl)}$	SCL clock frequency	[1]	0	-	400	kHz
		[2]	0	-	100	kHz
t_{HIGH}	HIGH period of the SCL clock	$f_{(scl)}$ = 400 kHz	0.6	-	-	µs
		$f_{(scl)}$ = 100 kHz	4	-	-	µs
t_{LOW}	LOW period of the SCL clock	$f_{(scl)}$ = 400 kHz	1.3	-	-	µs
		$f_{(scl)}$ = 100 kHz	4.7	-	-	µs
t_r	rise time of both SDA and SCL signals	$f_{(scl)}$ = 400 kHz; application dependent	20	-	300	ns
		$f_{(scl)}$ = 100 kHz; application dependent	-	-	1000	ns
t_f	fall time of both SDA and SCL signals	C_b = 400 pF; $f_{(scl)}$ = 400 kHz; application dependent	20 × $V_{DDD(IO)3V3}$	-	300	ns
		C_b = 100 pF; $f_{(scl)}$ = 400 kHz; application dependent	-	-	300	ns
$t_{v(data)}$	data valid time	$f_{(scl)}$ = 400 kHz [3]	-	-	0.9	ns
		$f_{(scl)}$ = 100 kHz [3]	-	-	3.45	ns
$t_{v(data)ACK}$	data valid acknowledge time	$f_{(scl)}$ = 400 kHz [3]	-	-	0.9	ns
		$f_{(scl)}$ = 100 kHz [3]	-	-	3.45	ns
V_{nL}	noise margin at LOW level	$f_{(scl)}$ = 400 kHz [4]	0.1 × $V_{DDD(IO)3V3}$	-	-	V
V_{nH}	noise margin at HIGH level	$f_{(scl)}$ = 400 kHz [4]	0.2 × $V_{DDD(IO)3V3}$	-	-	V
Input signaling (3V3)						
V_{IH}	HIGH-level input voltage		0.7 × $V_{DDD(IO)3V3}$	-	$V_{DDD(IO)3V3}$ + 0.5	V
V_{IL}	LOW-level input voltage		−0.5	-	0.3 × $V_{DDD(IO)3V3}$	V
V_{hys}	hysteresis voltage		0.1 × $V_{DDD(IO)3V3}$	-	-	V
I_I	input current each I/O pin	0.1 × $V_{DDD(IO)3V3}$ < Vi < 0.9 × $V_{DDD(IO)3V3}$	−10	-	+10	µA
C_i	input capacitance		-	-	10	pF
$t_{su(data)}$	data set-up time	$f_{(scl)}$ = 400 kHz	100	-	-	ns
		$f_{(scl)}$ = 100 kHz	250	-	-	ns
$t_{hd(data)}$	data hold time	$f_{(scl)}$ = 400 kHz [3]	0	-	0.9	µs
		$f_{(scl)}$ = 100 kHz [3]	0	-	3.45	µs
$t_{hd(sta)}$	hold time (repeated) START condition	$f_{(scl)}$ = 100 kHz	0.6	-	-	µs
		$f_{(scl)}$ = 100 kHz	4	-	-	µs
$t_{su(sta)}$	set-up time for a repeated START condition	$f_{(scl)}$ = 400 kHz	0.6	-	-	µs
		$f_{(scl)}$ = 100 kHz	4.7	-	-	µs

Table 40. I²C-bus interface characteristics *…continued*

The I²C-bus is 3.3 V tolerant; Recommended operating conditions; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(sto)}$	set-up time for STOP condition	$f_{(scl)}$ = 400 kHz	0.6	-	-	µs
		$f_{(scl)}$ = 100 kHz	4	-	-	µs
$t_{(buf)}$	bus free time between a STOP and START condition	$f_{(scl)}$ = 400 kHz	1.3	-	-	µs
		$f_{(scl)}$ = 100 kHz	4.7	-	-	µs
t_{of}	output fall time from V_{IH} to V_{IL}	$f_{(scl)}$ = 400 kHz	20 × $V_{DDD(IO)3V3}$	-	250	ns
		$f_{(scl)}$ = 100 kHz	20 × $V_{DDD(IO)3V3}$	-	250	ns
t_{sp}	pulse width of spikes	$f_{(scl)}$ = 400 kHz	0	-	50	ns
		$f_{(scl)}$ = 100 kHz	-	-	<tbd>	ns
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $f_{(scl)}$ = 400 kHz	3	-	-	
		V_{OL} = 0.6 V; $f_{(scl)}$ = 400 kHz	6	-	-	

[1] Fast mode.

[2] Standard mode.

[3] The maximum must be less than the maximum of $t_{vd(data)}$ or $t_{vd(ack)}$ by a transition time. This maximum is only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[4] For each connected device included hysteresis

11.11 General purpose I/Os

Table 41. General purpose I/Os characteristics

Recommended operating conditions; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	2.4	-	$V_{DDD(IO)3V3}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	V_{SSD}	-	V_{SSD} + 0.4	V
I_{OSH}	HIGH-level short-circuit output current	output connected to ground	-	-	90	mA
I_{OSL}	LOW-level short-circuit output current	output connected to $V_{DDD(IO)3V3}$	-	-	87	mA
C_L	load capacitance		-	-	15	pF
t_r	rise time	I_{OL} = 3 mA; C_L = 15 pF	<tbd>	<tbd>	1.4	ns
t_f	fall time	C_L = 50 pF; $V_{DDD(IO)3V3}$	<tbd>	<tbd>	1.4	ns
Input signaling (3V3)						
V_{IH}	HIGH-level input voltage		2.0	-	$V_{DDD(IO)3V3}$	V
V_{IL}	LOW-level input voltage		−0.3	-	+0.8	V
V_{hys}	hysteresis voltage		0.1 × $V_{DDD(IO)3V3}$	-	-	V

Table 41. General purpose I/Os characteristics *...continued*

Recommended operating conditions; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{pu(weak)}$	weak pull-up resistance	I/O configured with pull-up	40	50	57	kΩ
$R_{pd(weak)}$	weak pull-down resistance	I/O configured with pull-down	40	50	57	kΩ
C_i	input capacitance		-	8	-	pF

11.12 Crystal oscillator

Table 42. Crystal oscillator characteristics

Recommended operating conditions; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{i(osc)}$	oscillator input frequency		-	55.46667	-	MHz
δ_{fi}	input frequency deviation		-	100	-	ppm
$V_{i(osc)p-p}$	oscillator input voltage peak-to-peak	slave mode	<tbd>	<tbd>	<tbd>	mV
$f_{o(osc)}$	oscillator output frequency		-	55.46667	-	MHz
δ_{fo}	output frequency deviation		-	100	-	ppm
$V_{o(osc)p-p}$	oscillator output voltage peak-to-peak	master mode	<tbd>	<tbd>	<tbd>	mV
$t_{jitter(osc)}$	jitter		<tbd>	<tbd>	<tbd>	ps

11.13 Reset input - RESET_N

Table 43. Reset interface characteristics

Recommended operating conditions; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.0	-	$V_{DDD(IO)3V3}$	V
V_{IL}	LOW-level input voltage		−0.3	-	+0.8	V
V_{hys}	hysteresis voltage		$0.1 \times V_{DDD(IO)3V3}$	-	-	V
$R_{pu(weak)}$	weak pull-up resistance		40	50	57	kΩ
$t_{w(rst)}$	reset pulse width		10	-	-	µs

11.14 S/PDIF timing specification

Table 44. Digital S/PDIF input and output characteristics

Recommended operating conditions; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	$V_{DDD(IO)3V3} - 0.4$	-	$V_{DDD(IO)3V3}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	V_{SDD}	-	$V_{SDD} - 0.4$	V
C_L	load capacitance		-	50	-	pF

Table 44. Digital S/PDIF input and output characteristics *…continued*

Recommended operating conditions; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	C_L = 50 pF	15	-	30	ns
t_f	fall time	C_L = 50 pF	15	-	30	ns
Output signaling (IEC60958)						
$V_{o(p-p)}$	peak-to-peak output voltage	SPDIF sink impedance is 75 Ω. SPDIF output external circuitry presented in Figure 3	200	-	600	mV
t_r	rise time	C_L = 50 pF	15	-	30	ns
t_f	fall time	C_L = 50 pF	15	-	30	ns
Input signaling (3V3)						
V_{IH}	HIGH-level input voltage	[1]	2.0	-	$V_{DDD(IO)3V3}$ + 0.8	V
V_{IL}	LOW-level input voltage		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		0.1 × $V_{DDD(IO)3V3}$	-	-	V
$R_{pd(weak)}$	weak pull-down resistance		40	50	57	kΩ
C_i	input capacitance		-	8	10	pF
Input signaling (IEC60958)						
$V_{i(p-p)}$	peak-to-peak input voltage	SPDIF sink impedance is 75 Ω. SPDIF output external circuitry presented in Figure 4	200	-	1000	mV

[1] In this context V_{DDDIO} abbreviates $V_{DDD(IO)(3V3)}$.

[2] Configured as 3.3 V pin.

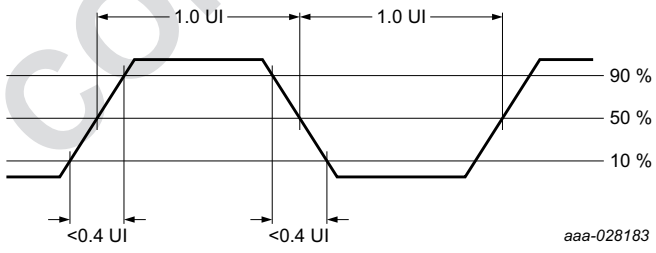


Fig 12. SPDIF rise and fall

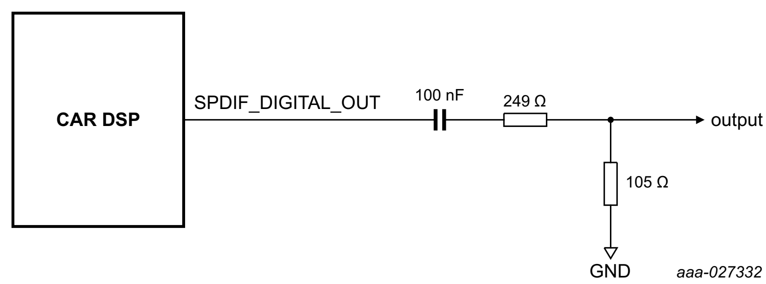


Fig 13. SPDIF digital output - IEC60958 mode

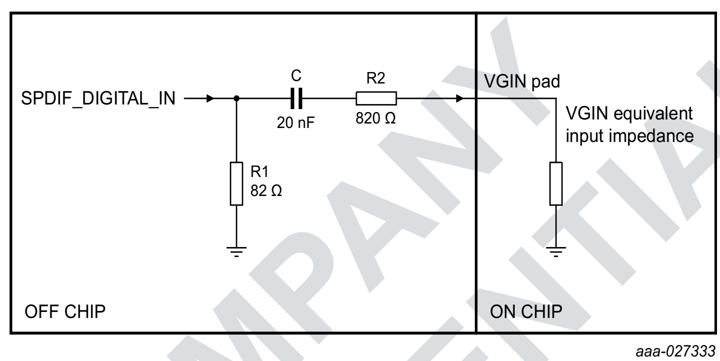


Fig 14. SPDIF digital input - IEC60958 mode

11.15 JTAG

Table 45. JTAG interface characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	0.9 × $V_{DDD(IO)3V3}$	-	$V_{DDD(IO)3V3}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	−0.3	-	0.1 × $V_{DDD(IO)3V3}$	V
C_L	load capacitance		-	50	-	pF
t_r	rise time	I_{OL} = 3 mA; C_L = 50 pF	-	5	-	ns
t_f	fall time	I_{OL} = 3 mA; C_L = 50 pF	-	5	-	ns
Input signaling (3V3)						
V_{IH}	HIGH-level input voltage		2	-	$V_{DDD(IO)3V3}$	V
V_{IL}	LOW-level input voltage		−0.3	-	+0.8	V
V_{hys}	hysteresis voltage		0.25	-	-	V
$R_{pu(weak)}$	weak pull-up resistance		40	50	57	kΩ
$R_{pd(weak)}$	weak pull-down resistance		40	50	57	kΩ
C_i	input capacitance		-	8	-	pF
$t_{cy(clk)}$	clock cycle time		50	-	-	ns

Table 45. JTAG interface characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WH}	pulse width HIGH		20	-	-	ns
t_{WL}	pulse width LOW		20	-	-	ns
$t_{su(data)}$	data input set-up time		-	5	-	ns
$t_{h(data)}$	data input hold time		-	5	-	ns
$t_{rst(L)}$	LOW-level reset time		500	-	-	ns
$t_{d(o)}$	output delay time		15	-	-	ns
t_{PHZ}	HIGH to OFF-state propagation delay		-	-	40	ns

11.16 FS_SYS_OUT characteristics

Table 46. FS_SYS_OUT characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	f_s = 44.1 kHz or 48 kHz		256 × f_s		kHz
δ	duty cycle			50		%
output signaling (3V3)						
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	$V_{DDD(IO)3V3}$ – 0.4		$V_{DDD(IO)3V3}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	V_{SSD}		V_{SSD} + 0.4	V
C_L	load capacitance			50		pF
t_r	rise time	I_{OL} = 3 mA; C_L = 50 pF; f_s = 44.1 kHz or 48 kHz		5		ns
t_f	fall time	I_{OL} = 3 mA; C_L = 50 pF; f_s = 44.1 kHz or 48 kHz		5		ns
output signaling (current mode)						
I_{OH}	HIGH-level output current	f_s = 44.1 kHz or 48 kHz	–360	–550	-775	µA
I_{OL}	LOW-level output current	f_s = 44.1 kHz or 48 kHz	355	510	710	µA
$V_{i(dc)}$	operating DC voltage		0.85	1.3	2.3	V

11.17 I2PD characteristics

Table 47. I2PD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{cy(clk)}$	clock cycle time	f_{clk} = 10.4 kHz		96.15		ns
$t_{cy(clk)}$	clock cycle time	f_{clk} = 20.8 kHz		48.08		ns
output signaling (current mode)						
I_{OH}	HIGH-level output current		–360	–550	-775	µA
I_{OL}	LOW-level output current		355	510	710	µA
$V_{i(dc)}$	operating DC voltage		0.85	1.3	2.3	V
input signaling (current mode)						

Table 47. I2PD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH-level output current		80		1000	µA
I_{OL}	LOW-level output current		−20		−1000	µA
$V_{o(dc)}$	operating DC voltage		0.85	1.3	2.3	V

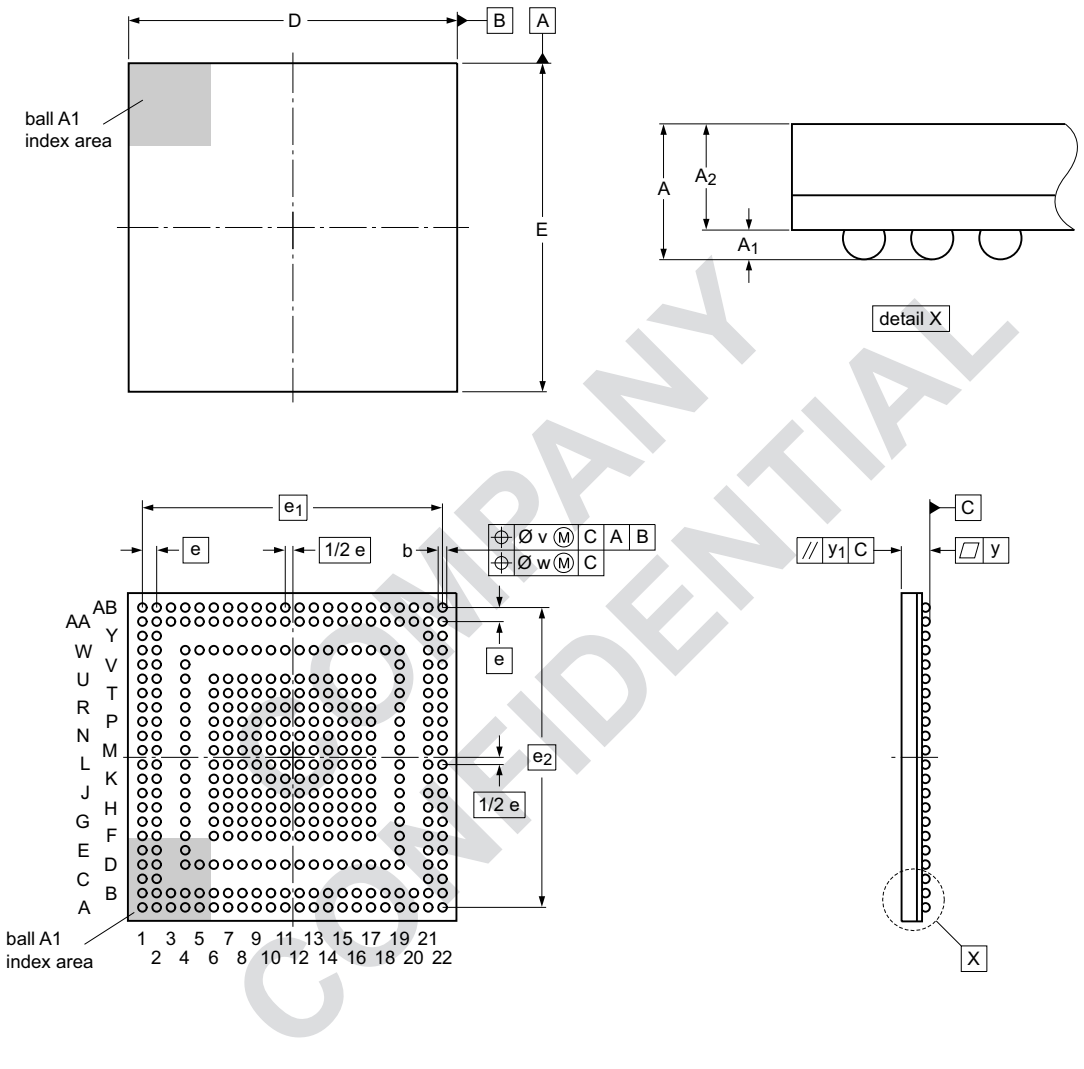
12. Test information

12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits,* and is suitable for use in automotive applications.

13. Package outline

LFBGA364: plastic low profile fine-pitch ball grid array package; 364 balls **SOT1457-1**



Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
max	1.45	0.35	1.10	0.45	15.1	15.1							
mm nom	1.30	0.30	1.00	0.40	15.0	15.0	0.65	13.65	13.65	0.15	0.08	0.1	0.1
min	1.20	0.25	0.95	0.35	14.9	14.9							

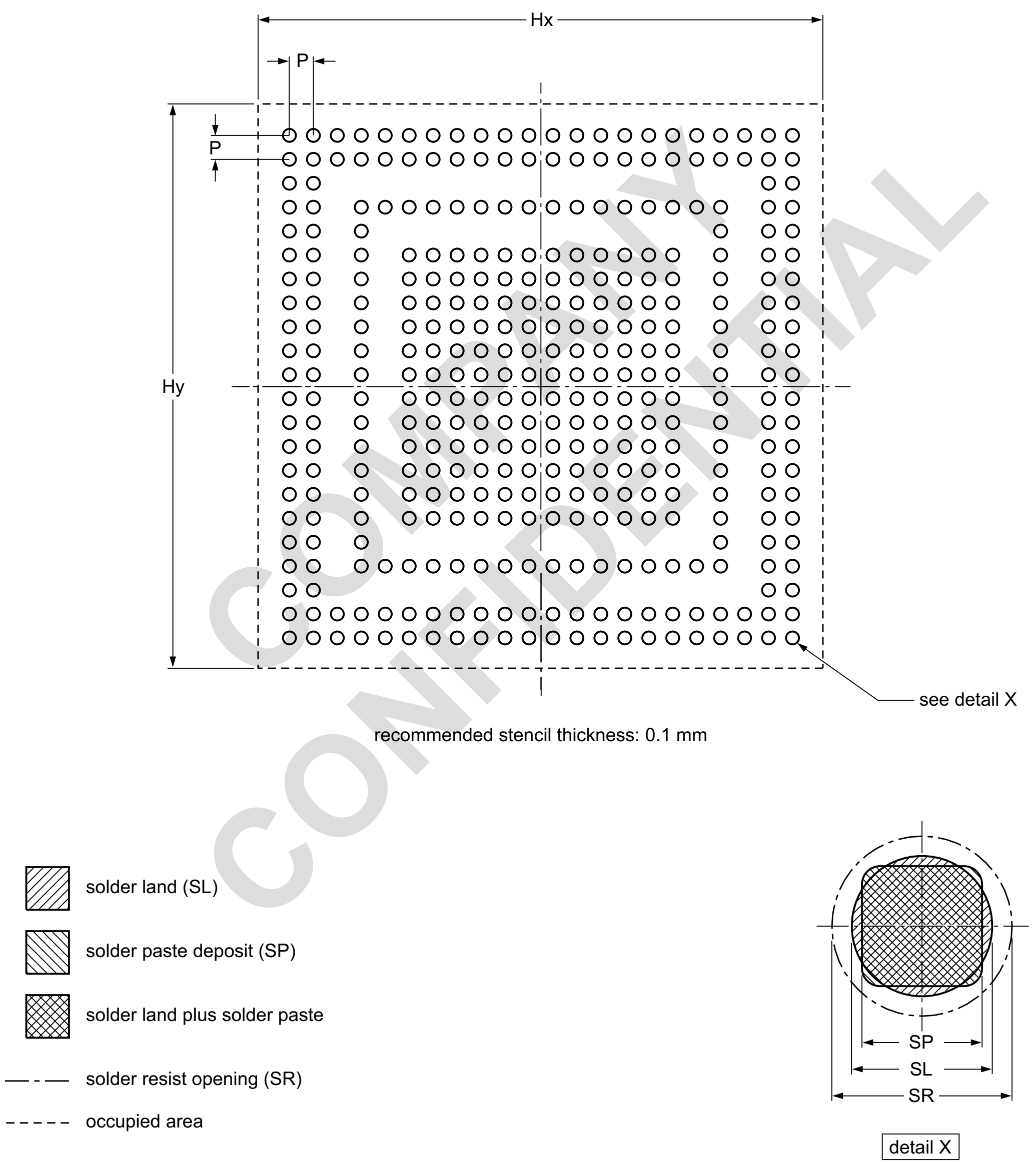
sot1457-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1457-1						~~15-10-20~~ 15-10-21

Fig 15. Package outline SOT1457-1 (LFBGA364)

14. Soldering

Footprint information for reflow soldering of LFBGA364 package **SOT1457-1**



Dimensions in mm

P	SL	SP	SR	Hx	Hy
0.65	0.35	0.30	0.45	15.3	15.3

Issue date ~~15-11-16~~ 15-11-18

sot1457-1_fr

Fig 16. Soldering footprint SOT1457-1 (LFBGA364)

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 48 and 49

Table 48. SnPb eutectic process (from J-STD-020D)

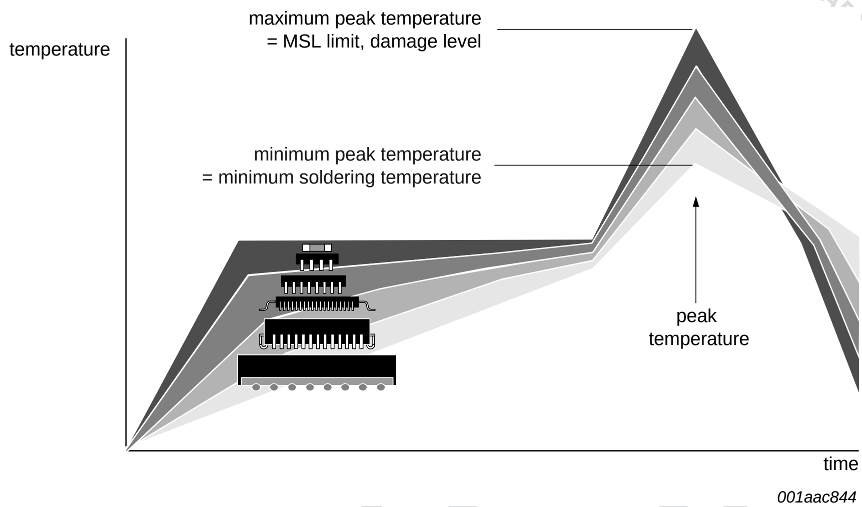
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 49. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.



MSL: Moisture Sensitivity Level

Fig 17. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

16. Abbreviations

Table 50. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ADPLL	All Digital Phase-Locked Loop
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
AM	Amplitude Modulation
API	Application Programmers Interface
APP	Audio Post Processing
AUX	Auxiliary
BBI	BaseBand Interface
BBP	BaseBand Processor
BPF	Band-Pass Filter
CD	Compact Disc
DAB	Digital Audio Broadcasting
DAC	Digital-to-Analog Converter
DCO	Digital Controlled Oscillator
DRM	Digital Radio Mondiale
DSP	Digital Signal Processor
FFS	Flash File System
FM	Frequency Modulation

Table 50. Abbreviations *...continued*

Acronym	Description
FS	Frame Sync
GPIO	General-Purpose Input Output
I/O	Input/Output
I/Q	In-phase/Quadrature-phase
I2C-bus	Inter-IC bus
I2S-bus	Inter-IC Sound bus
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response
JTAG	Joint Test Action Group
LNA	Low-Noise Amplifier
LO	Local Oscillator
LW	Long Wave
MPX	Multiplex
MSB	Most Significant Bit
MUX	Multiplexer
MW	Medium Wave
OEM	Original Equipment Manufacturer
OSC	Oscillator
OTP	One Time Programmable
PACS	Precision Adjacent Channel Suppression
PDC	Park Distance Control
PI	Program Identification
PLL	Phase-Locked Loop
RBDS	Radio Broadcast Data System
RDS	Radio Data System
RF	Radio Frequency
RFE	Radio Front End
RMS	Root Mean Square
RSSI	Received Signal Strength Indicator
SD	Sigma-Delta
S/PDIF	Sony/Philips Digital Interface
SPI	Serial Peripheral Interface
SRC	Sample Rate Converter
SW	Short Wave
TDM	Time Division Multiplex
USN	UltraSonic Noise
WAM	Wideband AM
WX	Weather Band
XTAL	Crystal

17. Glossary

FLASH memory — Non-volatile memory that can be electrically erased and programmed

Glue logic — Simple logic circuits used to connect together more complex circuits which are not perfectly compatible

HD Radio — Brand name of a digital transmission of audio on the FM and AM radio bands

Transceiver — An interface which transmits and receives data

18. References

[1] **IEC60958-1 Edition 2, Part 1: General Part —** Digital Audio Interface specification

[2] **IEC60958-3 Edition 2, Part 3: Consumer Applications —** Digital Audio Interface specification

[3] **UM10204: I2C-bus specification and user manual - v.5 —** Official I2C standard Document (available from NXP semiconductors, International Marketing and sales)

[4] **IEC61000-4-2 —** Electromagnetic compatibility (EMC) - Part 4-3: Testing and measurement techniques - Electrostatic discharge immunity test

[5] **AEC - Q100-Rev-H —** Automotive Electronics Council (AEC) - Failure mechanism-based stress test qualification for integrated circuits

[6] **AEC - Q100-004D —** Automotive Electronics Council (AEC) - IC Latch Up Test

[7] **AEC - Q100-002E —** Automotive Electronics Council (AEC) - Human Body Model (HBM) Electrostatic Discharge (ESD) Test

[8] **AEC - Q100-011C1 —** Automotive Electronics Council (AEC) - Charged Device Model (CDM) Electrostatic Discharge (ESD) Test

[9] **AN10365 —** Surface mount reflow soldering description

[10] **AN —** AN_SAF400xHV/N101

19. Revision history

Table 51. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAF400x_FAM v.1.0	<tbd>	Objective data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contact information

For more information, please visit: http://www.nxp.com

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