Preliminary Specification

On-Chip MRC & Dual DAB Front-End SoC Solution

PNS3030AD
DATA SHEET

PnpNetwork Technologies, Inc.

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(Version 0.02)

Note: This documentation is preliminary and subject to change. PnpNetwork Technologies, Inc. reserves the right to do any kind of modification in this datasheet regarding both hardware and software implementations without notice.

Revision History

Bars appearing in the left margin of the document as shown here indicate changes made to this document since the last revision issued.

Date	Revision	Description	Author
2019.06.26	Version 0.01	Initialization of document	Jeremy
2020.04.09	Version 0.02	Errata Correction - 1. Introduction - 2. Pin Information - 3. Pin Description - 4. Functional Description - 5. Peripheral Description	Jeremy

Contents

1. Introduction

1.1 Overview

PNS3030AD is a highly integrated SoC(System-on-Chip) DAB/DMB receiver. This device is composed of high performance RF front-end and demodulation part in a small-size single chip. This device supports various interfaces such as I2C, TSIF, SPI to make interface with external devices more flexible. With good sensitivity, high linearity, wide dynamic range, and low power consumption, PNS3030AD is the best solution for DAB/DMB application.

1.2 Features

- RF and Baseband one-chip solution
- Superior system performance
- Multi-standards support: DAB / DAB+ / DMB-A / T-DMB / HD-DMB(*1)
- Automatic RF channel setting
- Fast automatic channel acquisition and re-acquisition
- Outstanding SFN, Mobility, Adjacent and Co-channel rejection
- Ideal C/N Performance and Superior Fading Performance
- Support MRC diversity reception for high performance with dual antenna
- Embedded on-chip de-interleaving memory for full 1.824Mbps data rate
- FIC on-chip memory, access via HOST interfaces
- Decoding Information: FIC and MSC
- Variable HOST interfaces support: SPI, I2C and TSI interface
- Low power consumption: MAX 650mW (TBD)
- Compact package: 108-pin Fine pitch BGA(8×8mm^2, 0.65mm ball pitch) (TBD)
- System clock : 24.576Mhz

1.3 Applications

- Automotive Digital Radio System for receiving dual channel DAB signals
- Aftermarket car radio and audio system
- Boom Box and Audio component system
- Smart Speaker system for Digital Radio
- Kitchen Radio application

* Note 1: HD-DMB is required the proper CAS solution in HOST MCU processor for source decoding.

1.4 Ordering Information

Order Number		PNS3030AD
Package Information	Ball Pitch	0.65mm
	Body Size	8mm x 8mm x 1.2mm
	Ball Count (Type)	108 balls (FBGA)
Supply Voltage	Core	1.2V
	I/O	3.0V / 3.3V
Operation Temperature		-40 ~ +85°C
Storage Temperature		-50 ~ +150°C

Table 1-1 Ordering Information

Type number	Target Application	Internal tuner	Digital I/Q tuner Interface
PNS3030AD	[MRC Diversity Antenna] DAB 2-ch Receiver Front-End SOC for Audio & Data(*1) + BGS/Data(*2) or MRC Audio & Data mode	2 tuners : Band3+Band3	2
	[Single Antenna] DAB 2-ch Receiver Front-End SOC for Audio & Data mode + BGS/Data		

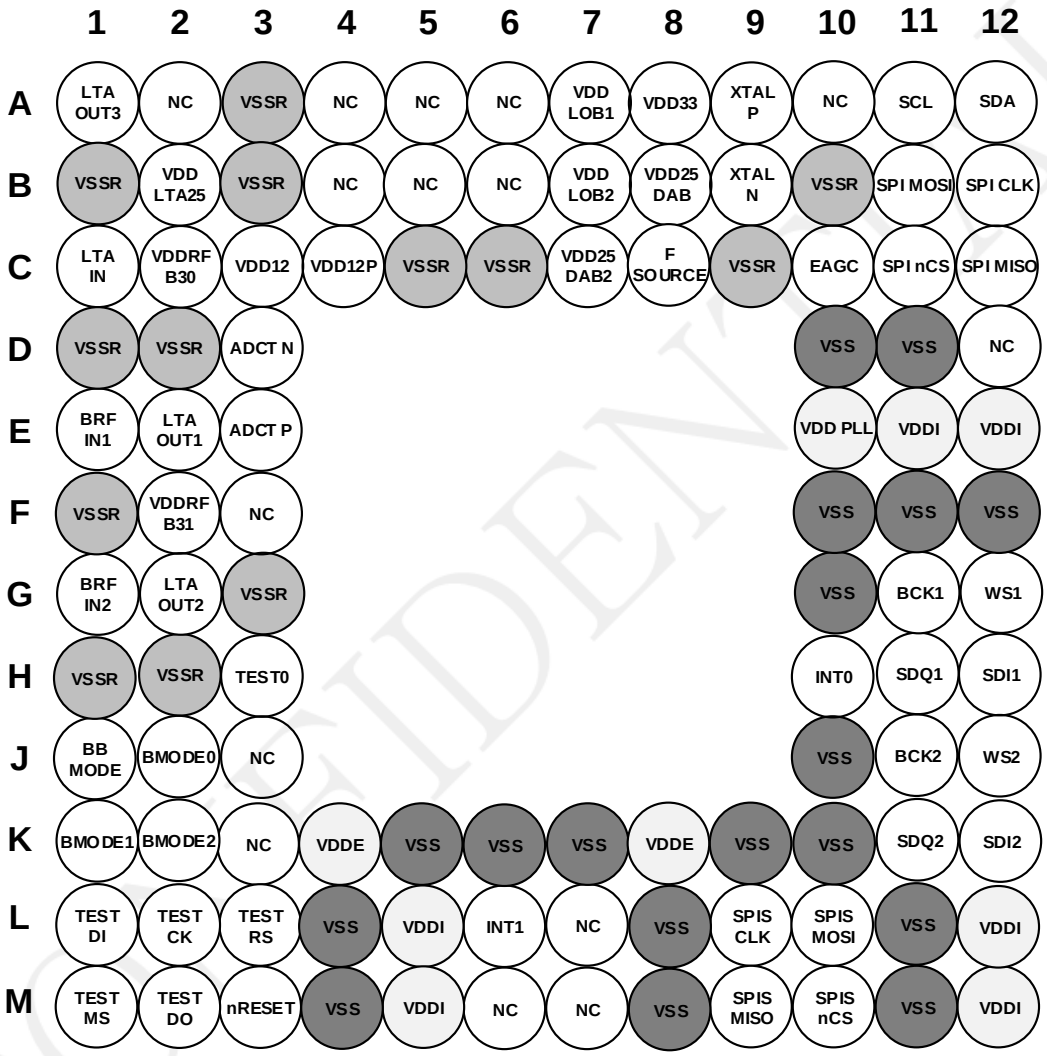
Table 1-2 Order type overview

* Note 1: “Audio & Data” means audio and data service are received simultaneous on the same frequency station.
* Note 2: “BGS/Data” means the separated tuner can be used for back ground scanning or data service on the other frequency stations time-dependently.

2. Pin Information

2.1 Pin Assignment

- Top View



PNS3030AD Pin assignment

3. Pin Descriptions

TYPE Description

I : Input, O : Output, IO : Bidirectional, AP : Analog Power, DP : Digital Power, DG : Digital Ground

- Baseband Pins

Pin	Symbol	Type	Function	Description
M6	NC	IO	-	Reserved for Future extension
L6	INT1	O	GPIO	External Interrupt Output[1] (Reserved for future)
A12	SDA	IO	I2C	I2C DATA (Slave)
A11	SCL	IO	I2C	I2C CLK (Slave)
H10	INT0	O	GPIO	External Interrupt Output[0]
L7	NC	IO	-	Reserved for Future extension
M7	NC	IO	-	Reserved for Future extension
M9	SPIS MISO	O	SPI	Secondary SPI MISO (Slave) (Reserved for future)
L10	SPIS MOSI	I	SPI	Secondary SPI MOSI (Slave) (Reserved for future)
L9	SPIS CLK	I	SPI	Secondary SPI CLK (Slave) (Reserved for future)
M10	SPIS nCS	I	SPI	Secondary SPI nCS (Slave) (Reserved for future)
C10	EAGC	O	Tuner IF	External AGC
B11	SPI MOSI	I	SPI	SPI MOSI (Slave)
B12	SPI CLK	I	SPI	SPI CLK (Slave)
C11	SPI nCS	I	SPI	SPI_nCS (Slave)
C12	SPI MISO	O	SPI	SPI_MISO(Slave)
G11	BCK1	I	Tuner IF	Digital I/Q Input BCL
G12	WS1	I	Tuner IF	Digital I/Q Input WS1
H11	SDQ1	I	Tuner IF	Digital I/Q Input Serial Data-Q 1
H12	SDI1	I	Tuner IF	Digital I/Q Input Serial Data-I 1
J11	BCK2	I	Tuner IF	Digital I/Q Input BCLK2
J12	WS2	I	Tuner IF	Digital I/Q Input WS2
K11	SDQ2	I	Tuner IF	Digital I/Q Input Serial Data-Q 2
K12	SDI2	I	Tuner IF	Digital I/Q Input Serial Data-I 2

- MODE & SYSTEM Pins

Pin	Symbol	Type	Function	Description
J2	BMODE0	I	MODE	Interface Mode Selection
K1	BMODE1	I	MODE-	Interface Mode Selection
K2	BMODE2	I	MODE	Interface Mode Selection
D12	NC	-	-	Reserved for Future extension
J1	BB MODE	I	MODE	BASEBAND Mode Selection
H3	TEST0	I	MODE	Digital Part Test Mode Selection
M3	nRESET	I	RESET	SYSTEM RESET IN
A9	XTAL P	I	CLOCK	Crystal Positive
B9	XTAL N	I	CLOCK	Crystal Negative
J3	NC	-	-	Reserved for Future extension
K3	NC	-	-	Reserved for Future extension
A10	NC	-	-	Reserved for Future extension
M2	TEST DO	IO	TEST	IC TEST Pin
L3	TEST RS	IO	TEST	IC TEST Pin
L1	TEST DI	IO	TEST	IC TEST Pin
M1	TEST MS	IO	TEST	IC TEST Pin
L2	TEST CK	IO	TEST	IC TEST Pin

- RF Pins (TBD)

Pin	Symbol	Type	Function	Description
A1	LTA OUT3	I	RF	LTA Output Buffer3
A2, A4, A5, A6	NC	-	-	Reserved for Future extension
B5, B6	NC	-	-	Reserved for Future extension
C1	LTA IN	I	RF	LTA Input
C8	F SOURCE	IO	RF	Reserved for Future extension
D3	ADCT N	IO	RF	ADC TEST Input Negative
E1	BRF IN1	I	RF	Band3 RF Input1
E2	LTA OUT1	O	RF	LTA Output Buffer1
E3	ADCT P	IO	RF	ADC TEST Input Positive
G1	BRF IN2	I	RF	Band3 RF Input2
G2	LTA OUT2	O	RF	LTA Output Buffer2

- Analog Power Pins (TBD)

Pin	Symbol	Type	Function	Description
A7	VDD LOB1	AP	POWER	RF & Analog Part Power Supply
A8	VDD33	AP	POWER	RF & Analog Part Power Supply
B2	VDD LTA25	AP	POWER	RF & Analog Part Power Supply
B4	NC	-	-	Reserved for Future extension
B7	VDD LOB2	AP	POWER	RF & Analog Part Power Supply
B8	VDD25 DAB	AP	POWER	RF & Analog Part Power Supply
C2	VDDRF B30	AP	POWER	RF & Analog Part Power Supply
C3	VDD12	AP	POWER	RF & Analog Part Power Supply
C4	VDD12P	AP	POWER	RF & Analog Part Power Supply
C7	VDD25 DAB2	AP	POWER	RF & Analog Part Power Supply
F2	VDDRF B31	AP	POWER	RF & Analog Part Power Supply
F3	NC	-	-	Reserved for Future extension
A3, B1, B3, B10, C5, C6, C9, D1, D2, F1, G3, H1, H2	VSSR	AP	POWER	RF & Analog Part Ground

- Digital Power Pins

Pin	Symbol	Type	Function	Description
E11, E12, L5, L12, M5, M12	VDDI	DP	POWER	Digital Power supply voltage for Core
K4, K8	VDDE	DP	POWER	Digital Power supply voltage for I/O
E10	VDD PLL	DP	POWER	Digital Power supply voltage for PLL
D10, D11, F10, F11, F12 G10, J10, K5, K6, K7, K9, K10, L4, L8, L11, M4, M8, M11	VSS	DG	POWER	Ground.

4. Functional Description

This chapter describes PNS3030AD internal structure, components and interfaces. The algorithms and architectures used in the PNS3030AD have been efficiently optimized in order to minimize hardware and chip area.

4.1 DAB Functions

- Support for DAB ETSI 300 401 v1.4.1 standard
- Multi-standards support in DAB Family: DAB/ DAB+/ DMB-A / T-DMB / HD-DMB
- Dual DAB demodulator support to receive the two ensembles in different frequency at once.
- Additional Back Scanning or Data service decoding by using dual demodulators
- All DAB transmission modes (I, II, III, and IV) support
- Low-IF (2.048 MHz) and Zero-IF support
- Fast automatic channel acquisition and re-acquisition
- EN 50248 performance environment compatible
- Dual AGC control for RF and IF amplifier, and WAGC/SLI to tuner
- Outstanding SFN, Mobility, Adjacent and Co-channel rejection
- Dynamic window positioning and channel tracking
- Internal digital AFC loop (no feedback to tuner)
- TII decoder can detect 5 signals
- Embedded on-chip de-interleaving memory for full 1.824Mbps data rate
- Relaxed crystal tolerance (±500ppm @ All modes, Not included RF part clock)

4.2 Tuner Interface Functions

- 2 x Digital I/Q interface support for External Tuner connection
- Support Split mode, Multiplexed mode, Analog/Digital mode, MSB bit shift mode
- Software and hardware switching of sample rates supported

4.3 Built-in RF tuners for DAB

- ❑ PNS3030AD support dual Band-3 RF tuners
- ❑ Supports Bands: 174~245MHz (Band-3)
- ❑ Low Noise Amplifier (LNA) with 4-gain modes
- ❑ RF automatics Gain Control
- ❑ Typical AGC dynamic range: Over 60dB
- ❑ Bandwidth adjustable band-pass filter
- ❑ I/Q Down Conversion Mixer to Baseband
- ❑ Low noise figure: 3 dB
- ❑ Low noise and Wide frequency range On-chip Voltage Controlled Oscillator (VCO)

4.4 Diversity Functions

- ❑ On-Chip MRC Diversity support for DAB family
- ❑ Better C/N performance and seamless switching between master and slave

4.5 Loop though Antenna

- ❑ VHF Band3 Band support
- ❑ Four RF output support with One Antenna input

4.6 I2C Functions

- ❑ Support 1x channels I2C (Slave mode)
- ❑ Detect/generate Start and Stop events
- ❑ Identify its slave (ID) address
- ❑ Identify the transfer direction (receive/transmit)
- ❑ Transfer data byte-wise according to the SCL clock line
- ❑ Generate an ACK signal following a byte receive
- ❑ Inspect an ACK signal following a byte transmit
- ❑ Generate vectored interrupt for receive and transmit events and receive/transmit/bus error exceptions
- ❑ Generate the clock signal (in Master mode)

4.7 SPI Functions

- ❑ 1 x /Slave Serial Peripheral Bus Interface
- ❑ 8- or 16-bits Programmable Data Length Per Chip Select
- ❑ Programmable Phase and Polarity Per Chip Select (master mode)
- ❑ Communication at up to main (clock/2) bps (slave), main (clock/2) bps(master mode)

5. *Peripheral Descriptions*

5.1 I2C Interface

The standard I2C protocol is used according to write operation or for a read operation with address table in below.

I2C Mode*1		MSB							LSB	Address [Hex]
BMODE[1:0] = [0,1]	Write Access	1	0	0	0	0	1	1	0	0x86
	Read Access	1	0	0	0	0	1	1	1	0x87
BMODE[1:0] = [1,1]	Write Access	1	1	0	1	0	0	0	0	0xD0
	Read Access	1	1	0	1	0	0	0	1	0xD1

Table 5-1. I2C Chip Address

Note *1 : I2C mode is selected in case of BMODE2=0

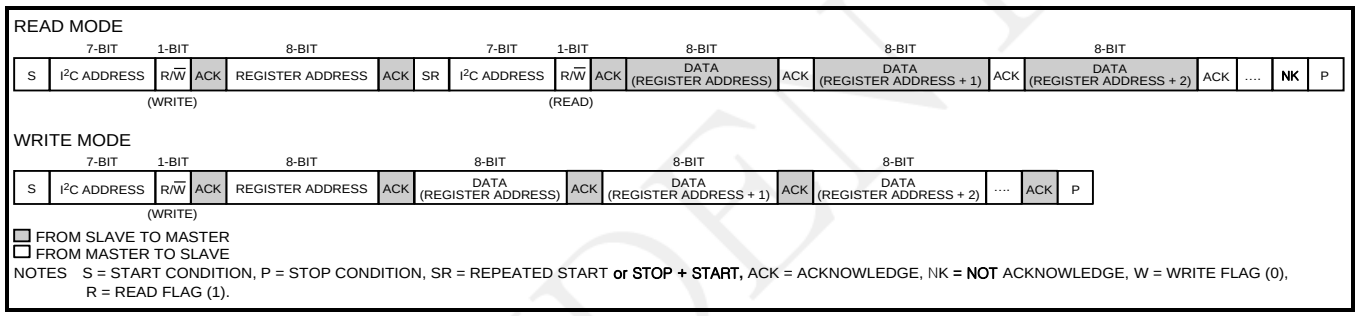


Figure5-1. I2C Write and Read Operations in Normal Mode

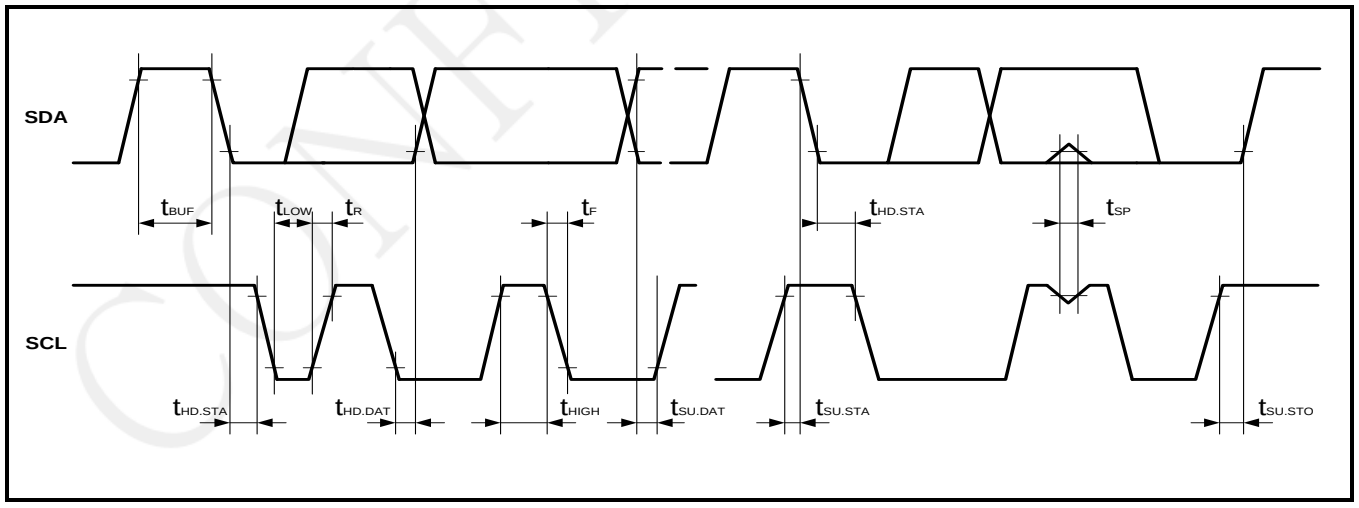


Figure5-2. I2C Timing Operation

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Low Level Input Voltage	Pull up to V_{DD}			$0.3V_{DD}$	V
V_{IH}	High Level Input Voltage		$0.7V_{DD}$			V
V_{OH}	High Level Output	Pull up to V_{DD}	2.4			V
V_{OL}	Low Level Output				0.45	V
I_{LK}	Input Leakage Current	V_{IN}= 0 to 3.3 V	-10		10	uA
C_{IN}	Input Capacitance	0		3.5		pF
I_{OL}	Output Sink Current	V_{OL}=0.45 V		4		mA
f_{SCLN}	SCL Clock Frequency	400kHz Mode	0		$f_{M\_CLK}/35$	kHz
f_{SCLS}		100kHz Mode	0		$f_{CLK\_IN}/10$	
t_{BUF}	Bus Free Time between a STOP and START Condition	400kHz Mode	1.3			uS
		100kHz Mode	4.7			
$t_{HD,STA}$	Hold Time(repeated) START Condition After this period, the first clock pulse is generated	400kHz Mode	0.6			uS
		100kHz Mode	4.0			
t_{LOW}	Low Period of the SCL Clock	400kHz Mode	1.3			uS
t_{HIGH}	High Period of the SCL Clock	100kHz Mode	0.6			
$t_{SU,STA}$	Setup Time for a repeated START Condition	400kHz Mode	0.6			uS
		100kHz Mode	4.7			
$t_{SU,STO}$	Setup Time for STOP Condition	400kHz Mode	0.6			uS
		100kHz Mode	4.0			
$t_{HD,DAT}$	Data Hold Time	400kHz Mode	0		0.9	uS
		100kHz Mode	0		3.45	
$t_{SU,DAT}$	Data Setup Time	400kHz Mode	0			nS
		100kHz Mode	0			
t_R, t_F	Rise and Fall Time of both SDA and SCL signals	400kHz Mode			300	nS
		100kHz Mode			300	

Table5-2. I2C Timing Characteristics

5.2 SPI Interface

This SPI (Serial Peripheral Interface) provides a duplex synchronous serial communication between the external MCU and demodulator. The SPI supports four different transfer formats with programmable polarity and phase. Figure5-3 shows four waveforms for SPI clock. The PNS3030AD uses SPI not only a simple peripheral interface but also as a host interface. The access byte sequence between the demodulator and an external MCU is similar to the standard I2C. Figure 5.4~5.7 shows byte sequences using SPI interface.

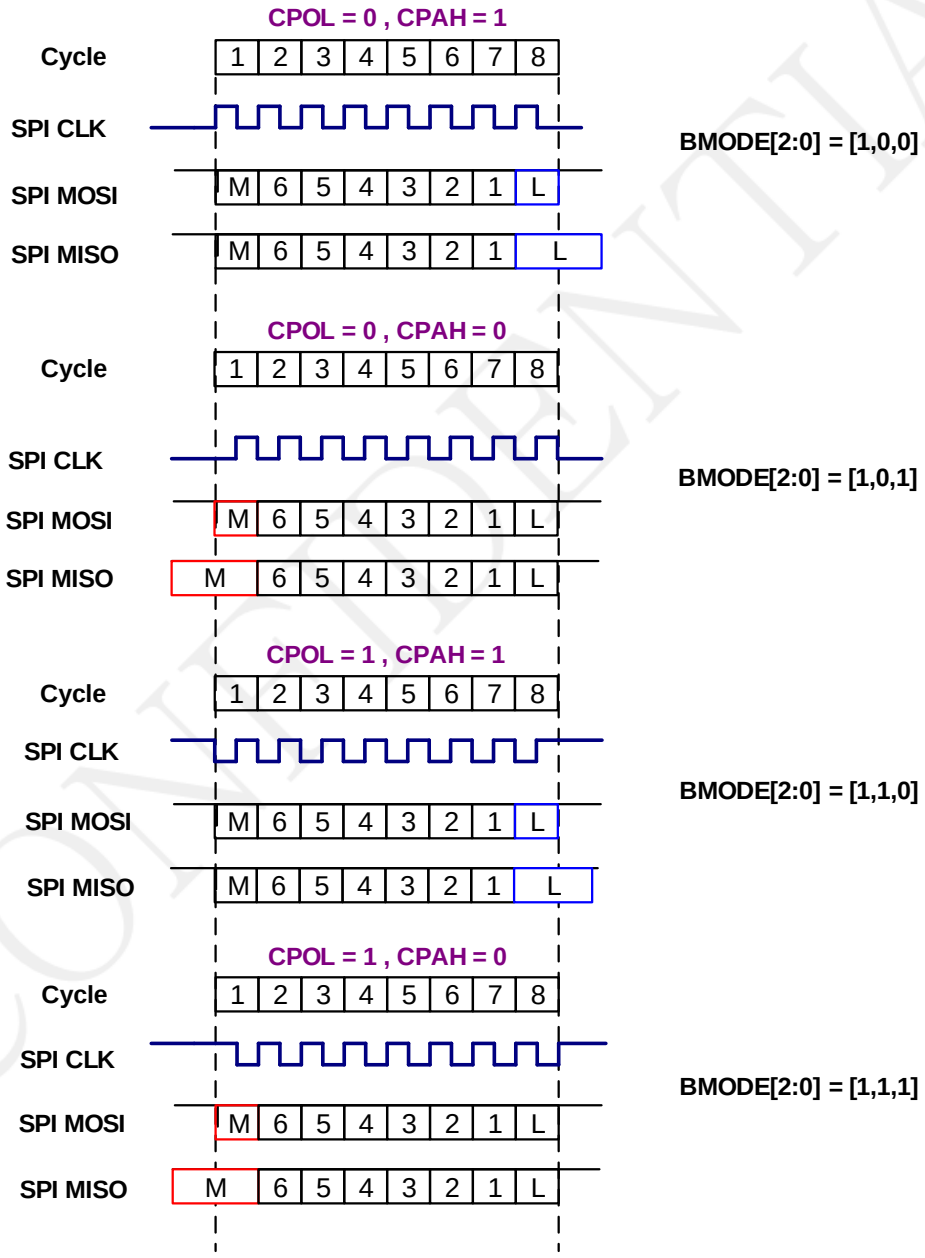


Figure 5-3. SPI Transfer Format

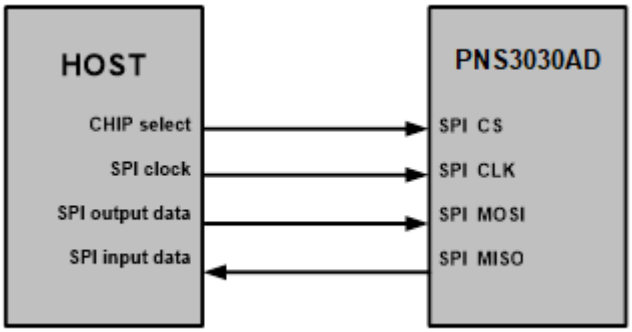


Figure 5-4. SPI Signal Connection Map

***Note**: After Power-On and starting the SPI communication, the SPI communication must be initialized by shaking the SPI_CS signal from Low to High. This SPI_CS signal toggling process is also needed after reset assertion.*

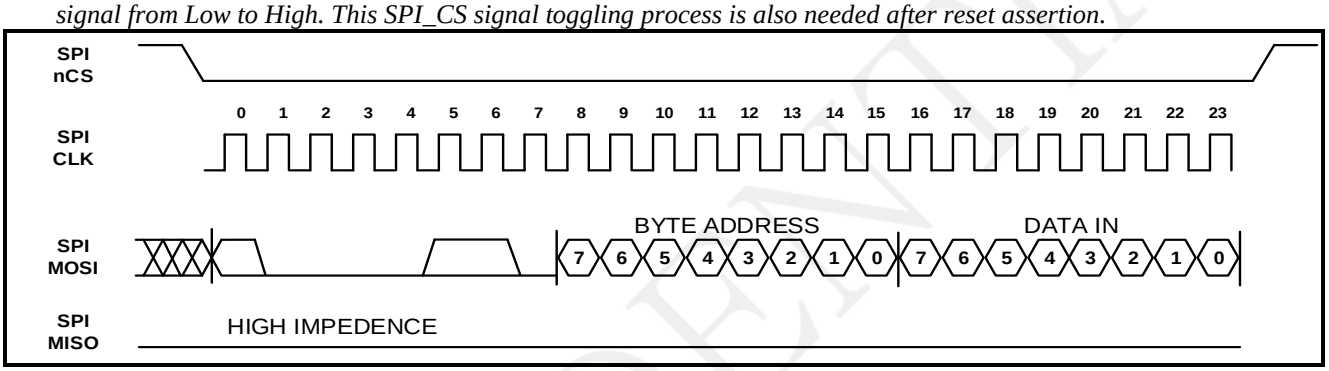


Figure 5-5. SPI Write Operation

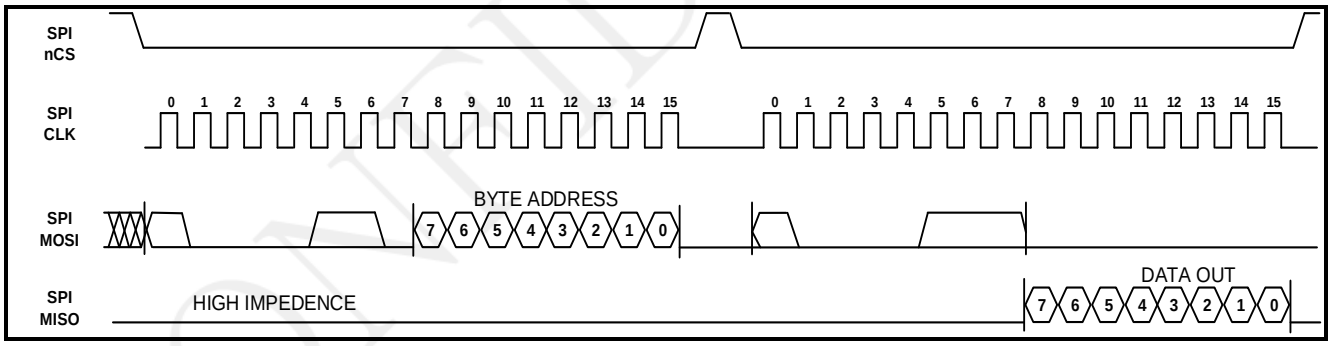


Figure 5-6. SPI Read Operation

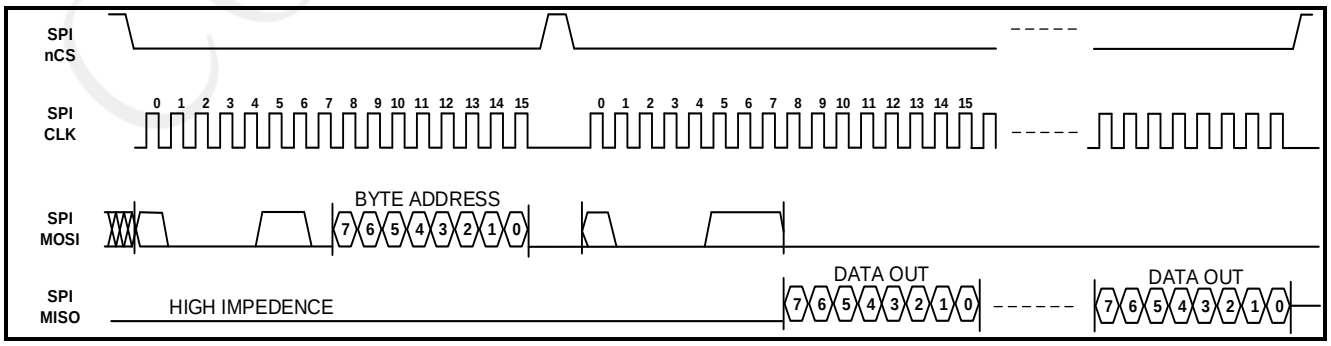


Figure 5-7. SPI Burst Read Operation

5.2.1 SPI Timing Diagram

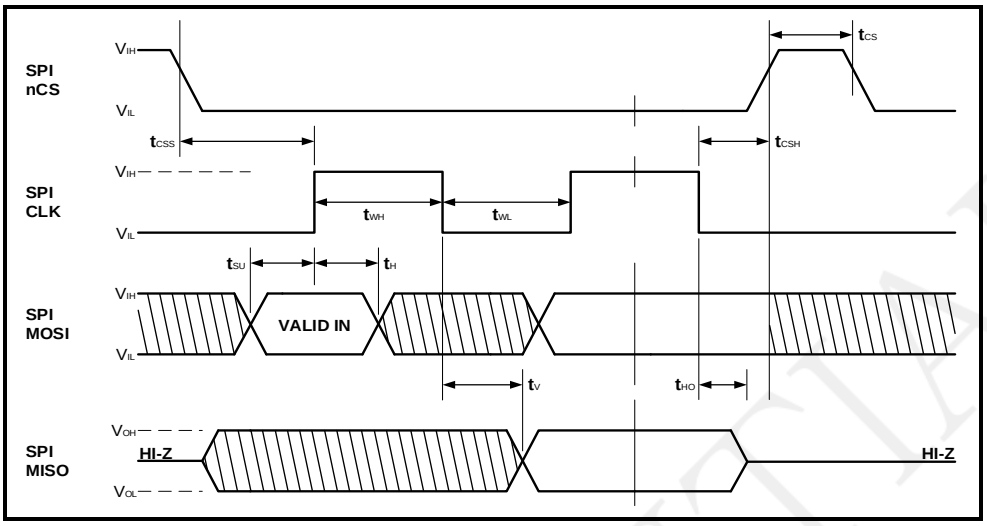


Figure 5-8. SPI Timing Diagram(TBD)

5.2.2 SPI Timing Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{CLKF}	CLK Clock Frequency	Normal Mode	0		12	MHz
f_{CLKS}		Standby Mode	0		12	MHz
t_{CS}	Minimum CS High Time		200			ns
t_{CSS}	CS Setup Time		100			ns
t_{CSH}	CS Hold Time		100			ns
t_{WH}	SCK High Time		122			ns
t_{WL}	SCK Low Time		65			ns
t_{SU}	Data In Setup Time		50			ns
t_{H}	Data In Hold Time		64			ns
t_{HD}	Hold Setup Time		100			ns

Table 5-3. SPI Timing (TBD)

5.3 Digital I/Q Interface

- Digital I/Q Interface is peripheral which delivers RF tuner's I & Q data from outside of chip and it support DMA. DMA reduces interrupt frequency to DSP core as a result DMA increases whole chip operation efficiency.

- Clock signals and data are delivered to outside device as BCLK, LRCK and Serial Data-I / Serial Data Data-Q

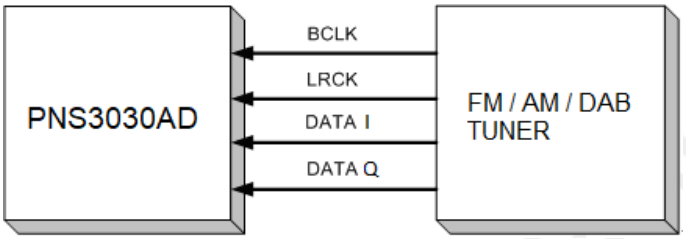


Figure 5-9. Digital I/Q Mode

- Support Split mode , Multiplexed mode

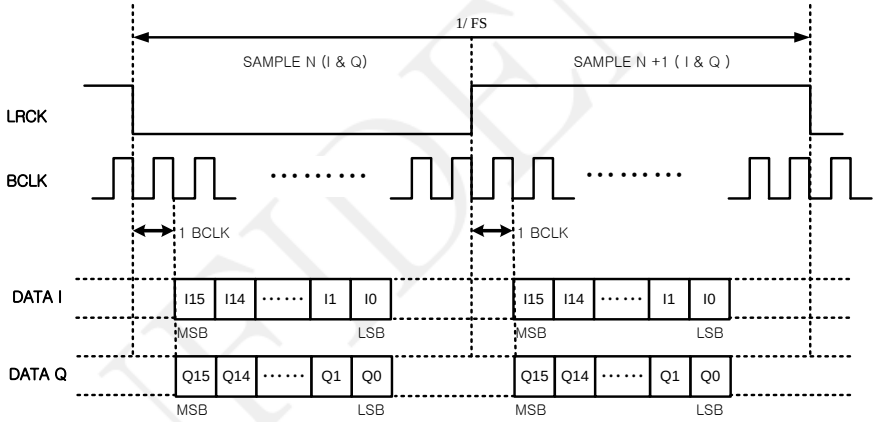


Figure 5-10. Digital IQ Split mode Timing Diagram

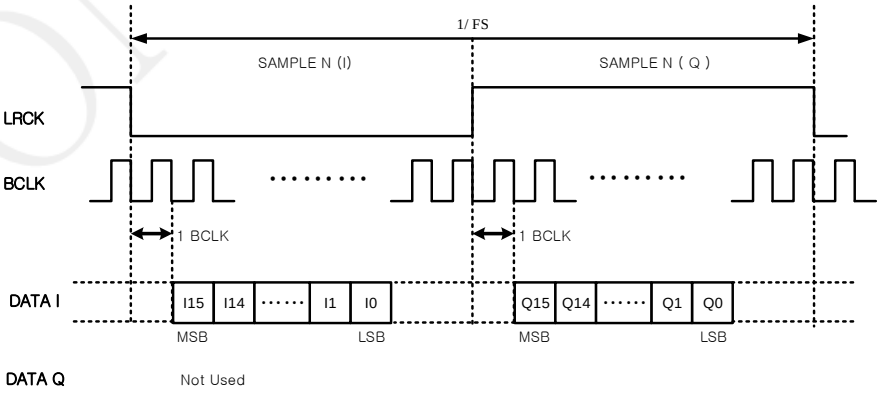


Figure 5-15 Digital I/Q Multiplexed mode Timing Diagram

5.4 Built-in RF tuners for DAB Band3

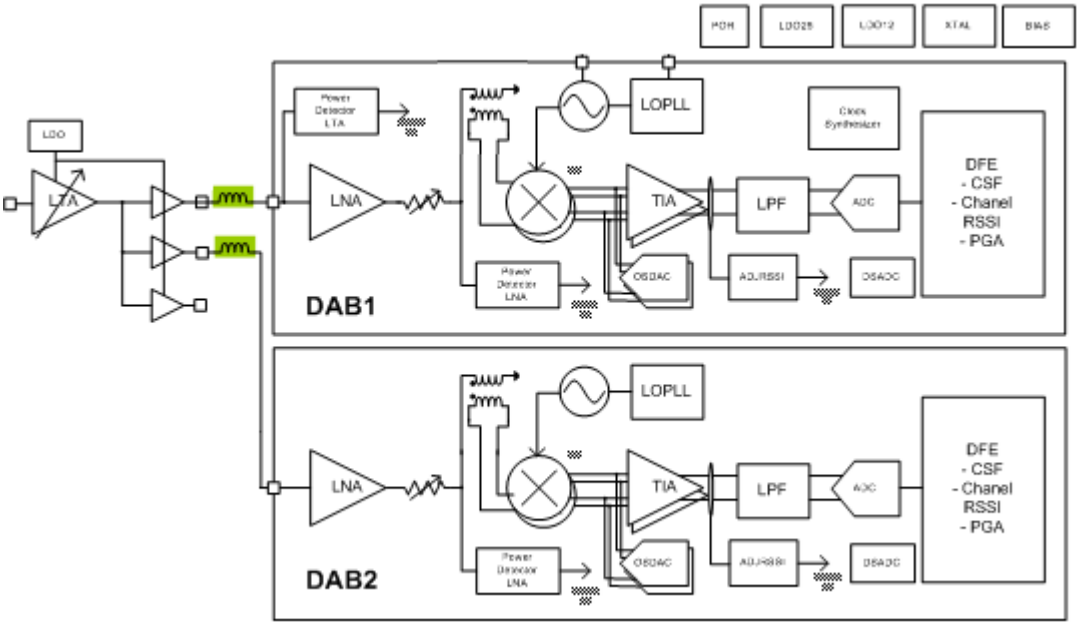


Figure 5-11. Built-in RF tuner Functional Block Diagram

The built-in RF tuners are highly integrated CMOS Receiver IP for DAB. The RF inputs can operate wideband range from 174MHz to 245MHz for DAB. The building blocks include LNA, RFPGA, I/Q down conversion mixer, bandwidth adjustable high-pass filter, baseband PGA, fractional-N frequency synthesizer with fully integrated VCO and LDO. The on-chip low phase noise VCO, along with the high-resolution fractional-N frequency synthesizer makes in-band phase noise low enough for reliable Radio applications.

6. Register Map Descriptions (TBD)

6.1 PNS3030AD TOP Register Descriptions (TBD)

This chapter will be updated later.

7. Electrical Characteristics

7.1 Absolute Maximum Rating

Operating the PNS3030AD under conditions that exceed those listed in Table 9-1 may result in damage to the device. Absolute maximum ratings are limiting values and are considered individually, while all other parameters are within their specified operating ranges. Functional operation of the PNS3030AD device under any of the conditions listed in Table 9-1 is not implied. Exposure to absolute maximum ratings for extended periods of time may affect the device's reliability.

Symbol	Description	Value	Units
T_J	Junction temperature	-40 to +125	°C
V_{VDDI}	Core Supply Voltage	-0.5 to + 1.4	V
V_{VDDE}	I/O Supply Voltage	-0.5 to + 3.6	V
V_{VDD33}	Analog I/O Supply Voltage	-0.5 to + 3.6	V
V_{VDD12} V_{VDD12P}	Analog Core Supply Voltage	-0.5 to + 1.4	V

Table 7-1 Absolute Maximum Ratings (TBD)

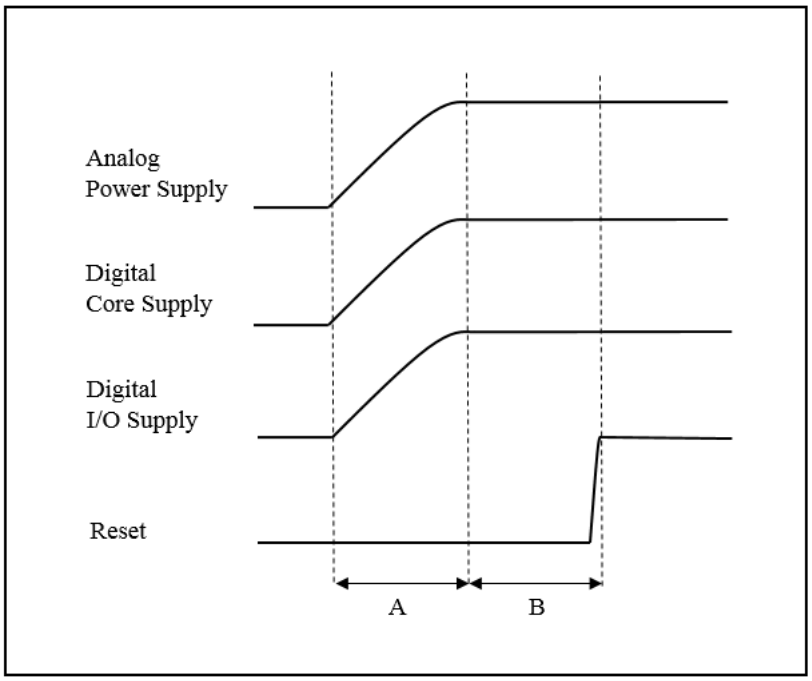
7.2 Recommended operating conditions

Symbol	Description	Min	Max	Units
T_{op}	Operation Temperature	-40	+85	°C
T_{STG}	Storage Temperature	-50	+150	°C
V_{VDDI}	Digital Core Supply Voltage	1.14	1.26	V
V_{VDDE}	Digital I/O Supply Voltage	2.97	3.63	V
V_{IH}	High Level Input voltage at I/O	0.7 * V_{VDDE}	V_{VDDE} +0.3	V
V_{IL}	Low Level Input voltage at I/O	V_{VDDE} -0.3	0.3 * V_{VDDE}	V
V_{HYS}	Input Hysteresis Voltage	0.4		V
V_{VDD12_RA}	RF & Analog Supply Voltage	1.14	1.26	V
V_{VDD_RA}	RF & Analog Supply Voltage	3.0	3.6	V

Table 7-2 Recommended Ratings (TBD)

7.3 Power-on and Reset Timing

Please refer to timing chart and table for proper power-on and IC reset.



Characteristic	Symbol	Min	Max	Unit
Power Supply Sequence	A	Don't Care	-	µs
Setup time for IC Reset	B	500	-	µs

Table 7-3 Power-on and Reset Timing

7.4 Power Consumption

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{VDD12-ALL}$	Supply Current for Core	$V_{VDD12ALL}$ = 1.2V Dual DAB Mode	-	166.0	-	mA
I_{VDDE}	Supply Current for IO	V_{VDDE} = 3.0V Dual DAB Mode	-	1.0	-	mA
I_{VDD_RA}	Supply Current for RF & Analog	V_{VDD_RA} =3.0V Dual DAB Mode	-	120.0	-	mA
P_{TPOW}	Total Power Consumption	Dual DAB Mode	-	562.2	-	mW

Table 7-4 Power Consumption (TBD)

8. *Package Dimension*

- The Package dimension of PNS3030AD

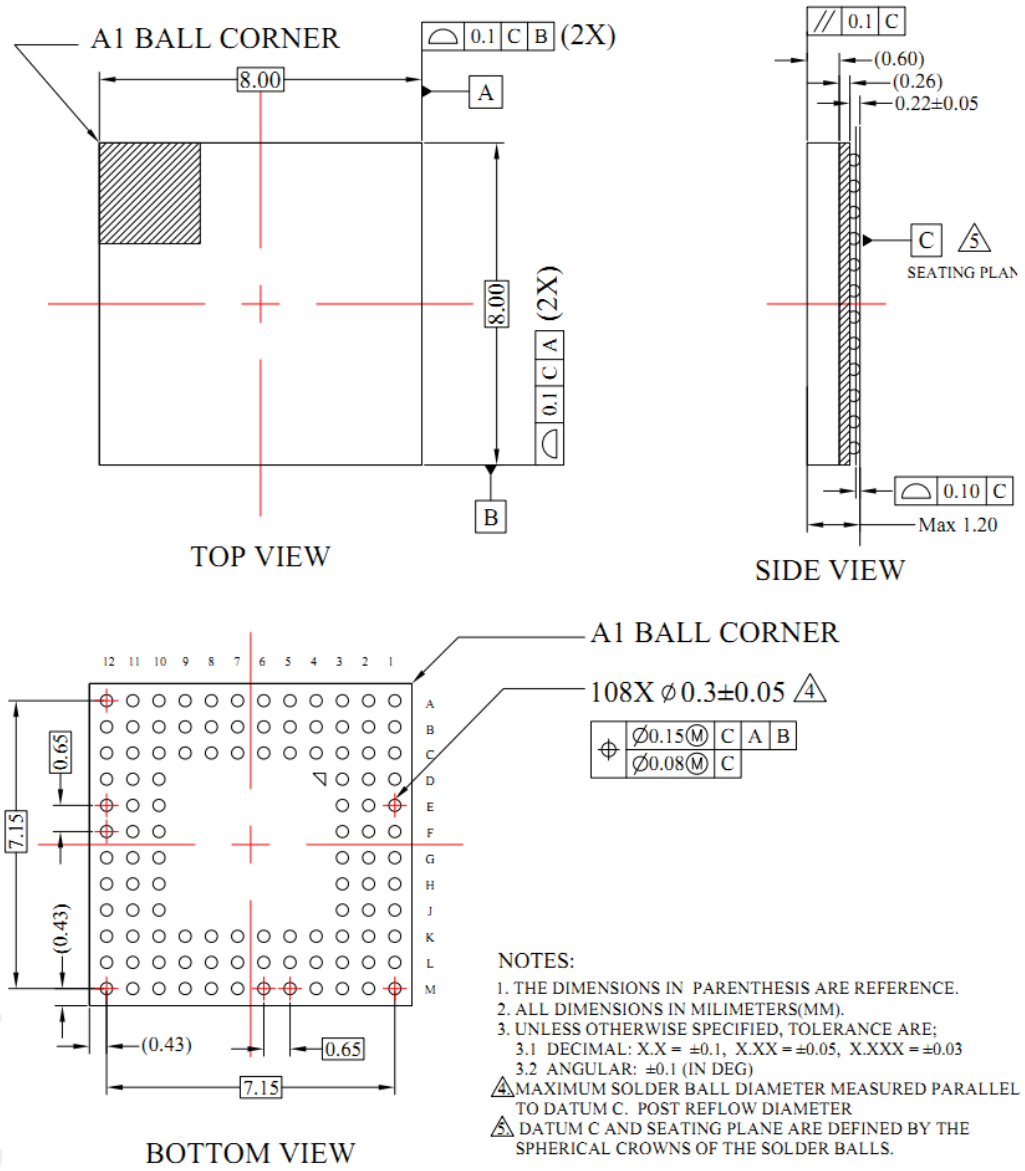


Figure 8.1 PNS3030AD Package Dimension

9. PCB Mounting Guidelines

Guidelines for mounting the PNS3030AD onto a printed circuit board (PCB) are presented in this part, including land pad and handling, SMT Process.

9.1 Board Pad Design

Item	Symbol	Recommendation
Pad pitch (mm)	PP	0.65
Pad diameter (mm)	PD	0.30
Solder mask open(mm)	MO	0.30

Table 9 -1 Board Pad Design

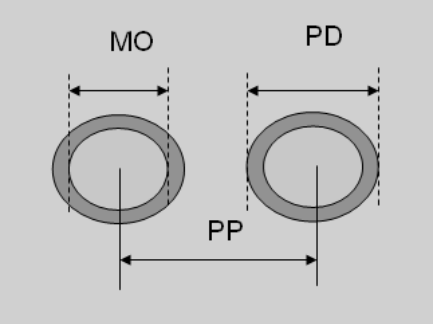


Figure 9-1 Pad design

9.2 Handling

Floor life time will be modified by environmental conditions other than 30'C/60%RH. If partial lots are used, the remaining SMD packages must be resealed or placed in safe storage within one hour of bag opening.

Refer to JEDEC spec (J-STD-033B) for details

Level	Floor life (out of bag) at factory Ambient 30'C/60%RH or as started
2	1 year
2a	4 weeks
3	168 hours
4	72 hours

Table 9 -2 Moisture classification level and floor life

9.3 DRYING

Component drying options for various moisture sensitivity levels and ambient humidity exposures of £≤ 60% RH are given in the following tables. Drying per an allowable option resets the floor life clock. If dried and sealed in an MBB with fresh desiccant, the shelf life is reset. Table 12-3 gives conditions for re-bake of SMD packages at a user site after the floor life has expired or other conditions have occurred to indicate excess moisture exposure.

PNS3030AD's condition: **Leve3, 9 hours, Bake @125℃**

Package Body Thickness	**Level**	**Bake @ 125°C**		**Bake @ 90°C ≤ 5% RH**		**Bake @ 40° C ≤ 5% RH**	
		Exceeding Floor Life by >72 hours	Exceeding Floor Life by ≤ 72 hours	Exceeding Floor Life by >72 hours	Exceeding Floor Life by ≤ 72 hours	Exceeding Floor Life by >72 hours	Exceeding Floor Life by ≤ 72 hours
	2						
≤ 1.4mm	2a	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	3	**9 hours**	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days

Table 9 -3 Reference Conditions for Drying Mounted or Un-mounted SMD Packages

9.4 SMT Process

- Screen print process

1. Type3 or type4 is recommended for solder paste.
2. No clean flux is recommended for lead-free condition.

- Component placement

Standard pick-and-place machines can be used for placing a package. The following methods can be used for recognition and positioning

1. Use ball inspection and compliant tip nozzle
2. It is recommended that the side-lighting option on pick and place machine
3. It is preferable to use IC placement/ fine pitch placement machines over chip-shooters for better accuracy.
4. Solder ball self-align when placed at an offset due to self-centering nature of it.
5. Little or no force needs to be exerted during placement to prevent damage to a part.
   It is recommended that balls be dipped into solder paste on PCB to greater than 20% of paste block height.

- Reflow and cleaning

1. Compatible with industry standard reflow process for both lead-free process.
2. Qualified for up to three reflow operation (260˚C peak) per J-STD-020.
3. Nitrogen gas is recommended (oxygen level<75ppm) to avoid oxidation or void formation.
4. Reflow profile depends on whole parts and board density.
5. Follow recommended recipe from paste manufacturer for reflow profile.

- Rework

The key features for rework are listed below.

1. Rework procedure used is identical to the one used for most BGA packages.
2. Rework reflow process should duplicate original reflow profile used for assembly.
3. Rework system should include localized convection heating element with profiling capacity, a bottom side pre-heater and a part pick and placer with image overlay.

9.5 The temperature profile of a reflow process

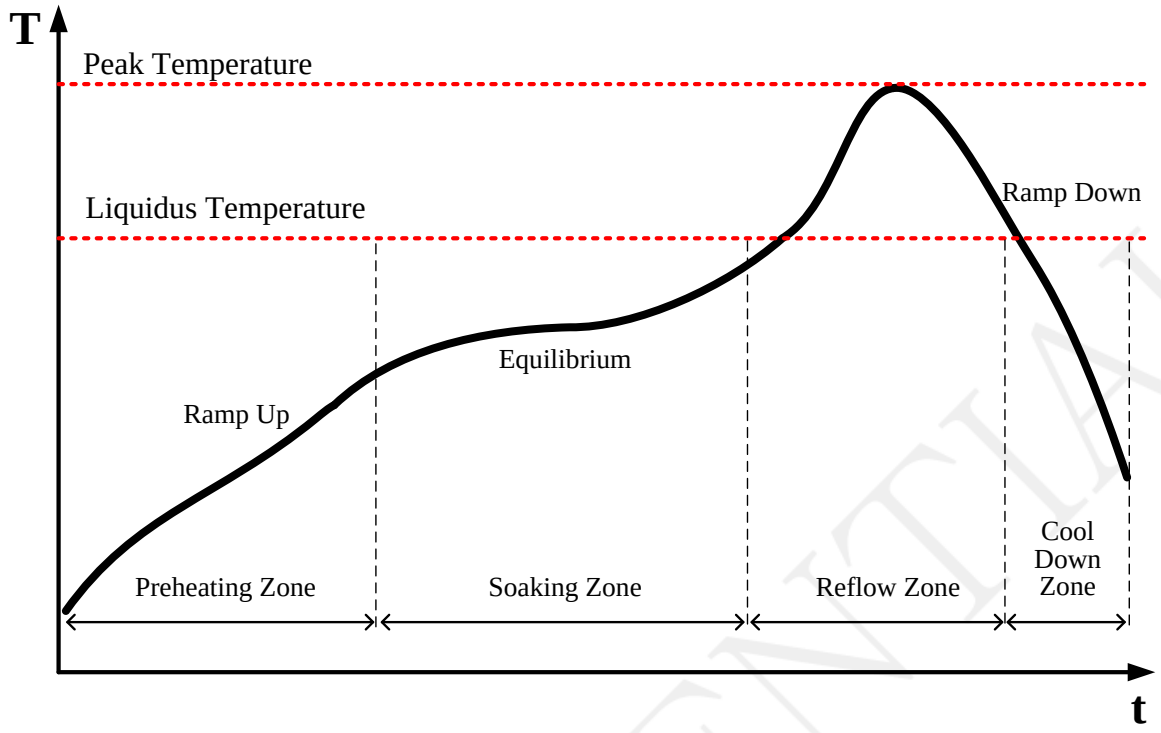


Figure 9-3 The temperature profile of a reflow process

Parameter	Tin-lead Alloy (SnPb or SnPbAg)	Lead-free Alloy (SnAgCu)	Main Requirements From
Preheating rate	2.5℃/sec	**2.5℃/sec**	Flux system(Solder paste)
Soaking temperature	140 ~ 170℃	**140 ~ 170℃**	Flux system(Solder paste)
Soaking time	80 second	**80 second**	Flux system(Solder paste)
Peak temperature	225℃	**245℃ ～ 260℃**	Alloy(Solder paste)
Reflow time over Liquidus	60 second	**60 or 90 second**	Alloy(Solder paste)
Liquidus temperature		**217℃or 219℃**	
Cool Down rate	2.5℃/sec	**2.5℃/sec**	

Table 9-4 The temperature profile of a reflow process

10. Part marking

- The marking information of PNS3030AD (TBD)

Line	Description	Image
1st	Company logo	
2nd	Device name*1	
3rd	Application name*2	
4th	Chip revision	
5th	Manufacturing date (KYYWW)*3	
6th (vertical)	Assembly lot number(CYWWPPTTT)*4	

*1 Device name : PNS3030AD

*2 Application name : WWR SoC

*3 Manufacturing date : KYYWW

- K : Site
- YYWW : Date code

*4 Assembly lot number : CYWWPPTTT

- C : Customer code
- Y : Years
- WW : Week
- PP : Package code
- TTT : Serial No.

Table 10-1 Marking Information: PNS3030AD(TBD)

PnpNetwork Technologies, Inc.
www.pnpnetwork.com
support@pnpnetwork.com
T : 82-2-2240-0800
3F, Fine Venture BLD, 41 , Seongnamdearo 925beangil, Bundang-gu, Seongnam-si, Gyeonggi-do, Korea 13496