Daimler NTG7

High

HARMAN

Country Specific Board
(refer to sheet – CSB)

SoC LGA Module

CAN[1]
CAN[0]
GPIOs
USB3_A [OTG]
USB3_C (Host)
HSIC
USB[A] 2.0
USB[C] 3.0
USB[B] 2.0
USB_3_PEX_C
PEX_A
GPIO Int
GPIO
MDIO
RGMII

USB3_A [OTG]
USB3_C (Host)
USB HSIC
USB[A] 2.0 OTG
USB[C] + USB 3.x Host USB3_C
USB[B] 2.0
USB_3_PEX_C
PEX_A
MDIO
RGMII
UART[C]
UART[A]
UART[B]
UART[D]

CAN[0]
CAN[1]
QSPI[0]
SDMMC_A
SDMMC_C
SDMMC D7 EMMC

JTAG
DAP[A]
DAP[B]
DAP[C]
DAP[D]
DAP[E]
DAP[F]
SPI[A]
SPI[B]
SPI[C]
SPI[D]
JTAG

102MHz
SDMMC_D
GPIO Int
GPIO Int
mmDP[0]
mmDP[1]
DP_AUX_CH[0]
DP_AUX_CH[1]
DSI2[A+B] x4
CSI2[A+B] x4
CSI2[C+D] x4
CSI2[E+F] x4
EMIFx128
I2C[A]
I2C[B]
I2C[C]
I2C[D]
I2C[PMU]
I2C[E]?
I2C[F]?
UFS x2
0: SATA_UFS /
1: Pex_B
I2C PMIC
UFS x2
GPIO
JTAG
SPI[A] Slave
SPI[B] master

nVidia
Parker
2x Denver2 @1.8GHz +
4x A57 @1.997GHz
GPU 1.148GHz
HSM

LPDDR4 RAM 16GB

TDM Nvidia/Valens:
* copy data outputs /clocks to both ports at Valens
* „wire-or" data inputs from both ports at Valens

256fs@48kHz

Base Board

QSPI NOR 64MB
S25FS512SFABHB213

HDMI
DDC
I2C
Lock
RGMII
MAX96947D GMSL2 w/ HDCP
HSVL
Central Display
Central Display
max 3187x1732@60Hz

HDMI
DDC
I2C
Lock
RGMII
MAX96945D GMSL2 w/o HDCP
HSVL
PIP Instrument Cluster
PIP
max 3304x2376@60Hz
IC
max 2400x900@60Hz

CSI2
I2C
RX
MAX96912H
Special Purpose Vehicle
max 1920x1080@60Hz

CSI2
CSI2
I2C
UART
RX
MAX96912H
ParkMan Surround View / RVC CAM
max 1920x3008@30Hz

I2C
Apple Auth 2.0c

8V5 Over coax
Only variant with RVC

I2C PMIC
UFS 256GB

Power Supply
KL30
KL31
HU CAN1
HU CAN2
PT CAN
ETH_Wup
Sub_Wup
Trace
TelMute
Car Connector
Level Shifter
Logger

JTAG SoC
UART SoC
Edge Conn

Multimedia Board

TV&Radio: 100MBit/s
3xGPIOs/ GNSS
USB PHY USB84604
I2C_A
HSDL: 1Gbit Eth + USB

Flash SoC
USB
DSRC
Ramses / MM-Box
USB 0.5A
USB 0.5A

WLAN 2.4/5G
ext
switch signal from µC
Switch
Diplex
WiFi/BT Module CWM-71-B225
BT4.1 WLAN 802.11ac BCM89359
PCIe
UART
PCM
BT / WLAN 5G

WLAN 2.4/5G
WiFi/BT Module CWM-71-55 (not for JPN)
WLAN BCM89359
PCIe
UART
PCM
Diplex

switch signal

16 Mbit Flash
USB+ / Ramses High
IntConn
I2C
Int
UART
HSDL
USB
SGMII
2 x TDM
VA6...

10x GPIOs/ Signals/ 3xADCs

to Central Display RGMII
USB 3 superspeed lane preparation VA60110

Mic Out
Ramses TEM

Ethernet vehicle 100BaseT1

BroadCom BCM89811 100Base-T1
MDIO
MII

ETH1
ETH3
MAC Adr. in RH850 E2P?
SGMII
MII
88EA6321
I2C
JTAG
MDIO
MII[5]

1000MBit/s

RGMII
SGMII
MDIO
RGMII
88EA6321
SGMII
1 x Phy
RGMII

B0

Ethernet SWDL (OBD) Star 2.x

E2P
E2P: Option Bringup,<C1

MII to IOC MUST be port 5 or 6 for remote management

1 mic w/ phantom from ext (decouple int. power!)

RTS/CTS 3Mbit/s
115kBit/s
64fs@8/16kHz
256fs @48kHz
10Mhz
UART/GNSS 115kBit/s

3-Axis Gyro SMI130
16 MB NOR Flash
GPIOs

TDM
SPI
SPI Slave
Audio DSP Griffin Lite ADI21571
Clock
MCK
JTAG
UART
OSC 24,567MHz
3MHz, CS
From C-Sample
Trace

TDM
SPI Slave
HSIC
INIC OS81118
USB
I2C
1x256fs @48khz
3x256fs @48khz

DAC AK4384
Pre-AMP
Class-D AMP TDF8534
2x ADC AK5720

ICC Mic 3,4
Tel Mic1,2/ ICC Mic1,2
Sub

JTAG DSP
UART IOC
JTAG IOC
Edge Conn

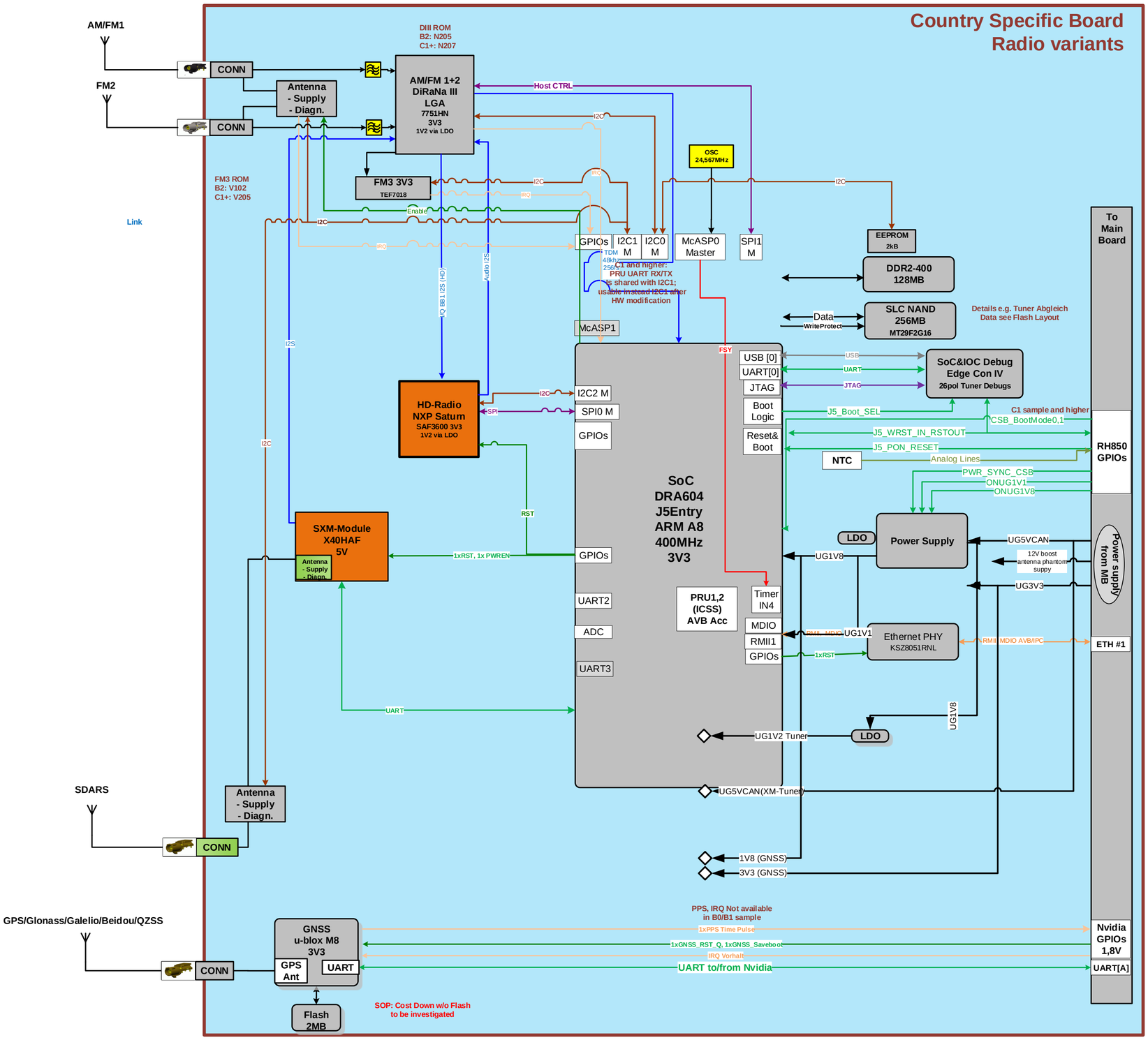
Freed up from C-Sample
1,5Mbit/s no RTS/CTS but 2x GPIO IRQ
115kBit/s
3MHz 1x CS + 1x GPIO IRQ

I2C
MII
MDIO
GPIO
ADC
ADC
ADC
Temp
Voltage
Current
SPI1-M
GPIO
PWM
UART
UART32
CAN1
GPIO
CAN2
GPIO
CAN3
GPIO
GPIO
GPIO
GPIO
GPIO
GPIO
RH850
F1H
R7F7015293ABG
120MHz
Dual Core
HSM
233Pin
512kB RAM
4MB Flash
64kB DataFlash
UART35
UART33
UART34
SPI2-M
JTAG
SPI0-M
EMIF
PWM
Counter
PWM
Counter
1MB RAM
Ext. FAN

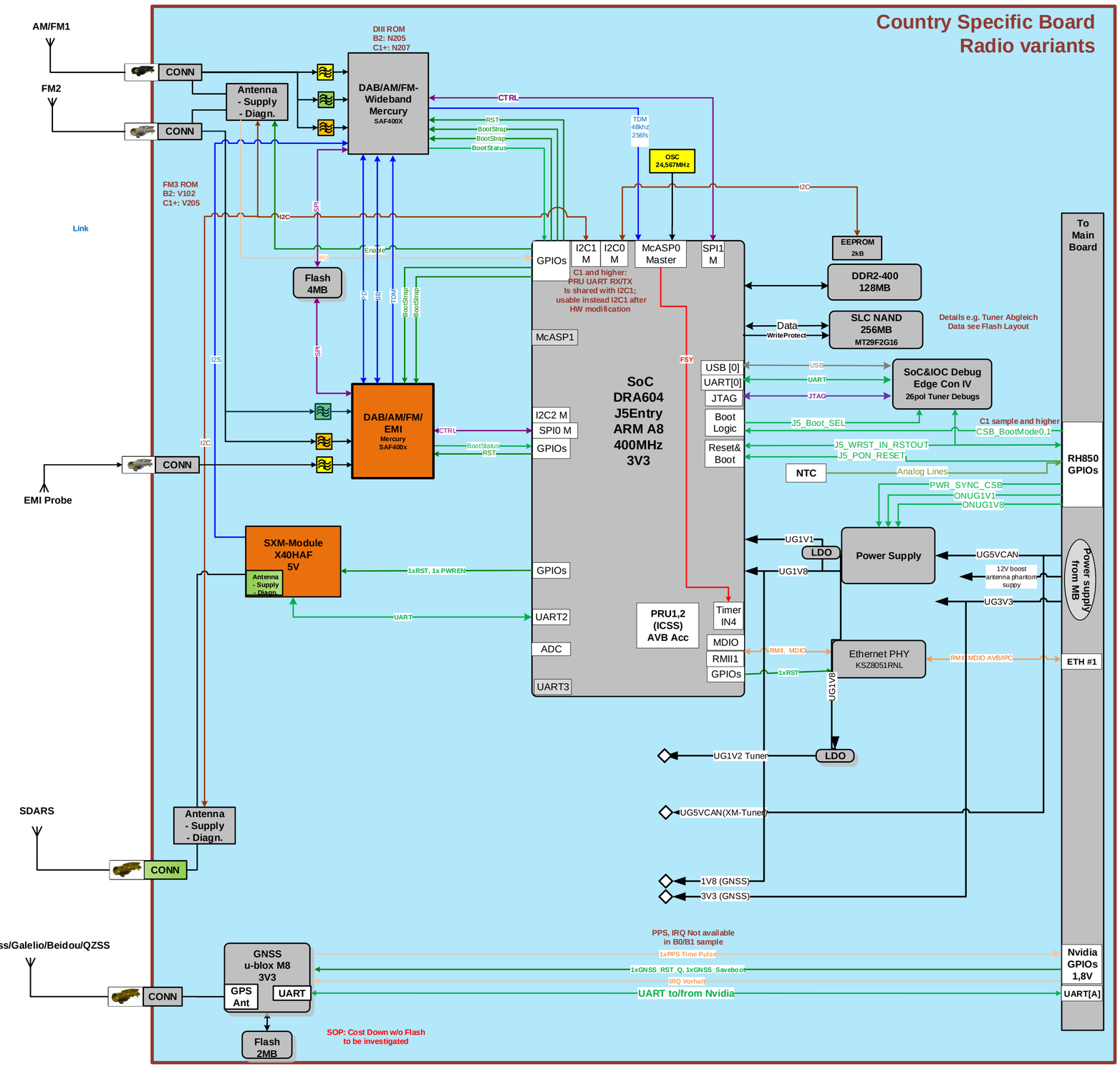
RX/TX CAN
INH CAN
RX/TX CAN
INH CAN
RX CAN
INH CAN
Ethernet Wakeup
Subwoof Wakeup
Int. FAN

memory
power
variant

HighMid.SDARS



HighMid.SDARS



High.DVB

Link

Country Specific Board TV variants

AM/FM1//ISDBT-SB/DAB1 (VHF)

FM2/DAB2//DVB-T2#2/ISDB-T#2 (UHF and VHF)

CONN1

CONN2

Antenna
- Supply0
- Diagn.

AM/FM 1+2
DiRaNa III
LGA
7751HN
3V3
1V2 via LDO

Host CTRL

I2C

RST

IRQ

Boot Status

TDM
48khz
256fs

FM3 3V3
TEF7018

LTE

VHF

Splitter

Splitter

Splitter

1xBLEND

Enable

IRQ

I2S

I2S

DAB 2
Max2173
3V3

I2C

FBB IF

IRQ

Switch0,1

SDRAM
16MB

DAB/DRM/HD
NXP Saturn
SAF360x 3V3
1V2 voa LDO

SPI CS0

I2C

GPIOs

I2C1 M

I2C0 M

TDM[1] M
12MBit/s

SPI[0] M
8Mbit/s

I2C5 M

GPIOs

SPI[2] 2xCS M
8MBit/s

I2C2 M

SoC

Intel
Broxton Low
2x 1600MHz
13000 DMIPs
HSM
1V8

GPIOs

EMIF

NVRAM

LGA
Module

LPDDR4
1024MB

PEMIC I2C

PWM

PMIC
Rohm

PMIC
SYNC

PMIC_
SYNC

GPIOs/
signals

PWM test point

1xRST/ 1xWAKE

PCIe[1]

PCIe

Intel Springville
I210-SC
3V3

4xGPIO

MDIO

SGMII
(IPC/AVB)

C1 sample
and higher

SGMII/
MDI
PHY

1pps, Test point, 4x MP

AVB synch test point

To
Main
Board

ETH #1

eMMC5[0]

Data

RST

eMMC5.0 NAND 8GB
MTFC 8G ACA ENS-K1 AIT
20 5.002861.046 1V8

Memory for Tuner
Abgleich in FS

QSPI[0]

QSPI

QSPI NOR 8 MB
N25Q064A11E12A0F 1V8

USB2.0 [2]

UART[2]

JTAG

SPI

USB

UART

JTAG

SPI

SoC&IOC Debug
Edge Con VII
30pol Tuner Debugs
incl. 14pol Micromatch

LS
1V8/
3V3

CAMERASB04

CAM

CIMaX+

USB CI+
For DVB

CONN

I2C

I2C

USB 3.0 NTG7 Vorhalt

USB

USB2.0

USB2.0
0.5A 3V3

USB 3.0[0]
OTG

FAULT

PWR_EN

SDIO
Acc

Temp
Sensor

GPIOs

SPI[1] M
10MBit/s

SDIO
4 Bit

GPIOs/
signals

7x Control Signals for
PowerOn/Boot/Reset/

3,3V

UG1V8

DC/DC

RH850
3,3V

5V

IRQ

ENABLE

1xPWR_EN

IRQ

SDIO

VHF

UHF

TV1
Dib50042
Master 1V8

PWR_SYNC_CSB
+ ONUG1V8

3,3V

Power
supply from
Main Board

Analog Lines

Power Supply

5V Tuner
Voltage

12V

DVB-T2#3/ISDBT#3 (UHF)

CONN3

LTE

VHF

UHF

TV2
Dib50042
Slave1

NTC

From C1 sample on

VHF

UHF

TV3
Dib50042
Slave2

UG1V8

SDARS//DVB-T2#1/ISDBT#1 (UHF)

Antenna
- Supply1
- Diagn.

CONN4

LTE

VHF

UHF

TV4
Dib50042
Slave3 (BG)

UG1V2 Tuner

LDO

GPS/Glonass/Galelio/Beidou/QZSS

CONN

GNSS
u-blox M8
3V3

GPS
Ant

UART

Flash
2MB

SOP: Cost Down w/o Flash
to be investigated

1xPPS Time Pulse

IRQ Vorhalt

UART to/from Nvidia

nVidia
GPIOs
1,8V

UART[A]

5V (GNSS Diagnosis)

1V8 (GNSS)

3V3 (GNSS)

High.DVB

Country Specific Board TV variants

AM/FM1//ISDBT-SB/DAB1 (VHF)

FM2/DAB2//DVB-T2#2/ISDB-T#2 (UHF and VHF)

CONN1

CONN2

Antenna - Supply0 - Diagn.

Splitter

DAB/AM/FM-Wideband Mercury SAF4000

Host CTRL

BootStatus

RST

BootStrap

BootStrap

TDM 48khz 256fs

LTE

VHF

Splitter

Splitter

SPI

Enable

IRQ

Flash 4MB

BB

BB

TDM

SPI

SPI

DAB/AM/FM/EMI Mercury SAF400x

BootStatus

RST

BootStrap

BootStrap

Link

EMI Probe

CONN

CAM

CIMaX+

USB CI+ For DVB

CONN

I2C

I2C

I2C3 M

USB 3.0 NTG7 Vorhalt

USB

USB2.0 0.5A 3V3

USB2.0

FAULT

PWR_EN

USB 3.0[0] OTG

GPIOs

SDIO Acc

Temp Sensor

SDIO 4 Bit

IRQ

ENABLE

5V

VHF

UHF

TV1 Dib50042 Master 1V8

1xPWR_EN

IRQ

SDIO

VHF

UHF

TV2 Dib50042 Slave1

LTE

VHF

UHF

TV3 Dib50042 Slave2

VHF

UHF

TV4 Dib50042 Slave3 (BG)

LTE

DVB-T2#3/ISDBT#3 (UHF)

CONN3

SDARS//DVB-T2#1/ISDBT#1 (UHF)

Antenna - Supply1 - Diagn.

CONN4

GPS/Glonass/Galelio/Beidou/QZSS

CONN

GNSS u-blox M8 3V3

GPS Ant

UART

Flash 2MB

SOP: Cost Down w/o Flash to be investigated

GPIOs

I2C1 M

I2C0 M

TDM[1] M 12MBit/s

SPI[0] M 8Mbit/s

I2C5 M

SPI[2] 2xCS M 8MBit/s

I2C2 M

GPIOs

SPI[1] M 10MBit/s

SoC

Intel Broxton Low 2x 1600MHz 13000 DMIPs HSM 1V8

GPIOs

EMIF

NVRAM

LGA Module

LPDDR4 1024MB

PEMIC I2C

PWM

PMIC Rohm

PMIC SYNC

GPIOs/ signals

PWM test point

1xRST/ 1xWAKE

PCIe[1]

PCIe

Intel Springville I210-SC 3V3

4xGPIO

MDIO

SGMII (IPC/AVB)

C1 sample and higher

SGMII/ MDI PHY

1pps, Test point, 4x MP

AVB synch test point

To Main Board

ETH #1

eMMC5[0]

Data

RST

eMMC5.0 NAND 8GB MTFC 8G ACA ENS-K1 AIT 20 5.002861.046 1V8

Memory for Tuner Abgleich in FS

QSPI[0]

QSPI

QSPI NOR 8 MB N25Q064A11E12A0F 1V8

USB2.0 [2]

UART[2]

JTAG

SPI

USB

UART

JTAG

SPI

SPI

SoC&IOC Debug Edge Con VII 30pol Tuner Debugs incl. 14pol Micromatch

LS 1V8/ 3V3

CAMERASB04

7x Control Signals for PowerOn/Boot/Reset/

RH850 3,3V

3,3V

UG1V8

DC/DC

PWR_SYNC_CSB + ONUG1V8

3,3V

Power Supply

5V Tuner Voltage

12V

Power supply from Main Board

Analog Lines

NTC

From C1 sample on

UG1V8

UG1V2 Tuner

LDO

1xPPS Time Pulse

IRQ Vorhalt

UART to/from Nvidia

5V (GNSS Diagnosis)

1V8 (GNSS)

3V3 (GNSS)

nVidia GPIOs 1,8V

UART[A]

High.DVB_ALT2

Country Specific Board TV variants

AM/FM1//ISDBT-SB/DAB1 (VHF)

FM2/DAB2//DVB-T2#2/ISDB-T#2 (UHF and VHF)

CONN1

CONN2

Antenna - Supply0 - Diagn.

Wideband Tuner DAB 1/2 Mercury SAF400X

Host CTRL

TDM 48khz 256fs

Bootstatus

RST

BootStrap

BootStrap

LTE

Splitter

Splitter

Splitter

Splitter

Link

TDM PD BB

Enable

GPIOs

I2C1 M

I2C0 M

TDM[1] M 12MBit/s

SPI[0] M 8Mbit/s

I2C5 M

GPIOs/ signals

PWM test point

1xRST/ 1xWAKE

PCIe[1]

PCIe

Intel Springville I210-SC 3V3

4xGPIO

MDIO

SGMII (IPC/AVB)

SGMII/ MDI PHY

C1 sample and higher

1pps, Test point, 4x MP

AVB synch test point

To Main Board

ETH #1

eMMC5.0 NAND 8GB MTFC 8G ACA ENS-K1 AIT 20 5.002861.046 1V8

eMMC5[0]

Data

RST

Memory for Tuner Abgleich in FS

QSPI[0]

QSPI

QSPI NOR 8 MB N25Q064A11E12A0F 1V8

SPI[2] 2xCS M 8MBit/s

I2C2 M

GPIOs

USB2.0 [2]

UART[2]

JTAG

SoC&IOC Debug Edge Con VII 30pol Tuner Debugs Incl. 14pol Micromatch

Wideband Tuner DAB 1/2 Mercury SAF4000

Host CTRL

BootStrap

BootStrap

RST

BootStatus

GPIOs

SoC TBD

EMIF

LPDDR 512MB

NVRAM

PEMIC I2C

Memory for PMIC Data C1 only!

Secific EEPROM 4kB

PWM

PMIC Rohm

PMIC SYNC

PMIC SYNC

CAMERASB04

EMI Probe

CAM

CIMaX+

USB CI+ For DVB

CONN

I2C

I2C

I2C M

Reset& Boot

USB

USB2.0

USB2.0 0.5A 3V3

FAULT

PWR_EN

GPIOs

SPI[1] M 10MBit/s

TS IF

Temp Sensor

GPIOs/ signals

7x Control Signals for PowerOn/Boot/Reset/

RH850 3,3V

ENABLE

IRQ

5V

3,3V

DC/DC

PWR_SYNC_CSB + QNUG1V8

IRQ

Analog Lines

3,3V

UG1V8

Power Supply

5V Tuner Voltage

12V

Power supply from Main Board

VHF

UHF

1xPWR_EN

TS IF

TS IF

DVB-T2#3/ISDBT#3 (UHF)

CONN3

LTE

TV1 SONY Rainbow

NTC

From C1 sample on

UG1V8

SDARS//DVB-T2#1/ISDBT#1 (UHF)

Antenna - Supply1 - Diagn.

CONN4

LTE

UG1V2 Tuner

LDO

GPS/Glonass/Galelio/Beidou/QZSS

GNSS u-blox M8 3V3

GPS Ant

UART

CONN

Flash 2MB

SOP: Cost Down w/o Flash to be investigated

1xPPS Time Pulse

IRQ Vorhalt

UART to/from Nvidia

nVidia GPIOs 1,8V

UART[A]

5V (GNSS Diagnosis)

1V8 (GNSS)

3V3 (GNSS)

High.DVB_CostDwn

Country Specific Board TV variants

AM/FM1//ISDBT-SB/DAB1 (VHF)

FM2/DAB2//DVB-T2#2/ISDB-T#2 (UHF and VHF)

CONN1

CONN2

Antenna - Supply0 - Diagn.

Wideband Tuner DAB 1/2 Mercury SAF400X

Host CTRL

OSC 24,567MHz

TDM 48khz 256fs

RST

IRQ

I2C

LTE

VHF

Splitter

Splitter

Splitter

Splitter

Link

TDM PD BB

Boot Mode

Boot Mode

Enable

GPIOs

I2C1 M

I2C0 M

McASP0 Master

SPI1 M

EEPROM 2kB

DDR2-400 128MB

SLC NAND 256MB MT29F2G16

Data

WriteProtect

C1 sample and higher

To Main Board

ETH #1

McASP1

FSY

SoC DRA604 J5Entry ARM A8 400MHz 3V3

USB [0]

UART[0]

JTAG

Boot Logic

Reset& Clock

USB

UART

JTAG

SoC&IOC Debug Edge Con IV

26pol Tuner Debugs

J5_Boot_SEL

CSB_BootMode0,1

J5_PORZ_IN

WRST_IN_RSTOUT

Analog Lines

RH850 3,3V

Wideband Tuner DAB 1/2 Mercury SAF400X

Host CTRL

SPI0 M

Boot Mode

Boot Mode

RST

IRQ

GPIOs

EMI Probe

UART3

UART2

I2C

I2C2 M

UG1V1

LDO

Power Supply

ONUG1V1

PWR_SYNC_CSB

UG1V8

ONUG1V8

PWR_SYNC_CSB + ONUG1V8

CAM

CIMaX+

USB CI+ For DVB

CONN

I2C

USB2.0

USB [1]

USB2.0 0.5...3V3

PWR_EN

FAULT

PRU1,2 (ICSS) AVB Acc

Timer IN4

MDIO

RMII1

GPIOs

SDIO 4 Bit

RMII, MDIO

1xRST

Ethernet PHY KSZ8051RNL

UG1V8

ENABLE

IRQ

UG1V8

5V

VHF

UHF

TV1 Dib50042 Master 1V8

1xPWR_EN

IRQ

SDIO

Analog Lines

3,3V

UG1V2 Tuner

LDO

Power Supply

Power supply from Main Board

5V Tuner Voltage

12V

DVB-T2#3/ISDBT#3 (UHF)

CONN3

VHF

UHF

LTE

TV2 Dib50042 Slave1

NTC

From C1 sample on

VHF

UHF

TV3 Dib50042 Slave2

SDARS//DVB-T2#1/ISDBT#1 (UHF)

Antenna - Supply1 - Diagn.

CONN4

VHF

UHF

LTE

TV4 Dib50042 Slave3 (BG)

GPS/Glonass/Galelio/Beidou/QZSS

CONN

GNSS u-blox M8 3V3

GPS Ant

UART

Flash 2MB

SOP: Cost Down w/o Flash to be investigated

1xPPS Time Pulse

IRQ Verhalt

UART to/from Nvidia

nVidia GPIOs 1,8V

UART[A]

5V (GNSS Diagnosis)

1V8 (GNSS)

3V3 (GNSS)

History

Initial: * F1H non-GW **Premium** version **R7F2015-29** with 576k 512k
* IOC: all required ports available, UART should not be overused due to interrupts (finally 2 UARTs used: RVC, Trace; [IPC to Msoc will be Ethernet)
* Later stage: UART IPC => Ethernet IPC

2017/03/02, V0.6	AM: MMB: open: exact SoC descriptions, flashing concept Valens/SoC: ok, PCIe for WiFi/UFS/M.2 for Xavier, **memory size UFS/eMMC**
2017/03/02, V0.7	AM: MMB: added Phys for new Mid-JPN variant
2017/03/03, V0.8	AM: MMB: USB OTG always for flashing, changed USB Inic to SPI Inic, changed low latency SoC-IOC from SPI to UART; open: switch configuration
2017/03/03, V0.9	AM: MMB: switch configuration from IOC and optional from Nvidia for MMB, optional E2P, added UART for flashing Valens (to be verified) debug
2017/03/03, V0.10	AM: mainboard: keep SPI IPC and share SPI between Inic/DSP (SWDL only); open: RAMSES / MMBOX I2S: preliminary
2017/03/06, V0.11	SvS: CSB: added UG 6V3 Power for SDARS, corrected GPIOS to Antenna Supply Diagnosis, added UG 5V GNSS Diagnosis, added LDO and UG 1V2 Tuner
2017/03/08, V0.12	SvS: CSB: corrected connection between tuner Ics, added BB.
2017/03/09, V0.13	SvS: CSB: added TV alternatives with Parrot O3+ and Sony Rainbow.
2017/03/10, V0.14	SvS: CSB TV: removed USB from JPN variants.
2017/03/10, V0.15	AM: MMB: used OTG to flash SoC (always there, to be verified), added I2S to MM-Box
2017/03/13, V0.16	SvS: CSB-TV: Corrected Merlin wiring.
2017/03/14, V0.17	SvS: CSB-TV: Replaced lines by connectors.
2017/03/15, V0.18	SvS: CSB-TV: Replaced Merlin by Mercury to ensure ISDB-Tsb and TV in parallel.
2017/03/29, V0.19	SvS: CSB-TV: Separated the different alternatives to separate sheets. Added cost down variant with J5 Entry instead of Intel APL.
2017/04/11, V0.20	AM: MMB: Maxim 96912H, added PMIC portion to LGA module, changed WiFi modules to CWM10/06
2017/04/13, V0.21	SvS: CSB: Changed tuner architecture back to NTG6 tuner architecture. Added CDR-Versions, added Mercury/Merlin for CDR.
2017/04/26, V0.22	SvS: CSB: Added variant SDARS+CDR with Mercury/Merlin.
2017/04/28, V0.23	AM: MMB: changed USB architecture: OTG to Valens (Apple Carplay), added USB switch(initial flash Nvdia), JPN variant purely optional; added co-driver display; Maxim: added phy's for RGMII connection display & lock status (additional Int GPIO for Nvidia needed: ok); added GPIO interrupts for Valens, **removed MDIO from Valens**; changed I2C architecture
2017/05/02, V0.24	AM: MMB: TDM signals Valens/Nvidia/DSP/Maxim
2017/05/03, V0.25	AM: MMB: corrected PCIe connections
2017/05/03, V0.26	AM: Main: provided eth Phy chip, USB mux, **SoC review**: redefined PCIe/USB, added UART debug
2017/05/04, V0.27	AM: main: marked 2nd SoC UART debug, **open: MDIO connections Valens / grafics**
2017/05/04, V0.28	AM: version **reviewed SW arch** Martin Binner, no changes, only highlights
2017/05/04, V0.29	AM: updated grafic resolutions based on HSVL architecture NTG7 V1.00 with EVA2 (DAI)
2017/05/11, V0.30	AM: Main: move Mic Ramses to ½, move OTG to external port
2017/05/30, V0.31	SvS: CSB: removed RH850, removed EEPROM, adjusted LS, corrected RAM.
2017/06/06, V0.32	AM: MMB: extended with variants premium, premium+, entry+, CR236, ports SoC-side Maxim CSI swapped
2017/06/07, V0.33	AM: MMB High variant – re-added SPV cam
2017/06/07, V0.34	AM: MMB: 4 antennas in all variants, diplexers fix
2017/06/08, V0.35	AM: removed non-Most layer (now: option for entry variants), added GPIO signals from to IOC for all variants
2017/06/12, V0.36	AM: added UART for DSP trace
2017/06/22, V0.37	AM: changed MMB USB B/C (as in NTG6@223)
2017/06/22, V0.38	SvS: CSB: Added page „CSB-Radio_Step2" with planned Step2 tuners; removed unnecessary pages.
2017/06/27, V0.39	AM: added I2C DDC from Maxim to I2C[A], corrected view for USB lines
2017/06/28, V0.40	SvS: CSB: Corrected Antenna circuit to latest plans from CoC Broadcast.
2017/06/29, V0.41	SvS: CSB: Added boot flash to Mercury tuners. Added FM-VICS to TV JPN Step2.
2017/06/29, V0.42	AM: extra I2C DDC removed (DDC only, no config port)
2017/07/03, V0.43	AM: finalized UART on IOC, UART to DSP after removal of UART IPC bulk communication to SoC
2017/07/04, V0.44	AM: I2C on serializer not available when connected via UART
2017/07/07, V0.45	AM: DSRC not optional in High-Variants, added High-Spped lane port descriptions Parker/Ohara; MDIO for B0 optional from IOC
2017/07/07, V0.46	AM: corrected display resolutions & deserializer type according Email Ellen Cho (DAI) 7.7. 9:20; **review B0 sample**
2017/07/07, V0.47	SvS: CSB: corrected findings from Daimler review.
2017/07/12, V0.48	SvS: CSB: Reviewed all relevant variants with CoC Tuner.
2017/07/13, V0.49	SvS: CSB: Corrected some more minor findings. Changed some connections to reduce crossings.
2017/07/13, V0.50	SvS: CSB: Corrected HF Splitters for CSB-TV.
2017/07/17, V0.51	AM: BB switch is MII to IOC, UART speed to WLAN is 3MBit, Valens memory is 16Mbit, sideband RGMII only for Premium(+), standard module is CWM-71-2**2**5 for all variants, SoC QSPI type changed / clock changed to 102MHz, DAP[E] potentially 2xI2C, UART to ethernet IPC change with C-sample (wording), added USB 3.x preparation for Valens 6010; **released for B0 sample**
2017/07/19, V0.52	USB[B] and USB[C] swapped for USB 3 Superspeed connectivity
2017/07/20, V0.53	AM: feedback from DAI review 0.51 (PiP resolution, SPV frequency, GPIO GNSS), removed x4 PCI in Xavier
2017/07/31, V0.54	AM: UART[E] marked for Xavier, debug interface DIRECTDC; swapped UART[B/C] for Xavier ➔ debug is [C] for Xavier; Central Display / PIP => 60Hz; corrected HSIO Xavier; updated performance settings for Nvidia SoC (still in review!) – **corrections for released B0 sample**

Export HU variants to Pdf (with history)