Marvell® Brightlane™ 88Q1110/88Q1111

Automotive 100BASE-T1 Ethernet Transceiver

Datasheet

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PRODUCT OVERVIEW

The Marvell® Brightlane™ 88Q1110/88Q1111 device is a single pair Ethernet physical layer transceiver (PHY) designed for automotive applications. The transceiver implements the Ethernet physical layer portion of the 100BASE-T1 standard as defined by the IEEE 802.3bw task force. It is manufactured using a standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on a single balanced twisted pair.

The 88Q1110 device supports reduced pin count GMII (RGMII), reduced pin count MII (RMII), and media independent interface (MII) for direct connection to a MAC or switch port. The 88Q1111 device supports Serial GMII (SGMII) for direct connection to a MAC or switch port. SGMII operates at 1.25 Gbps over a single differential pair, reducing power and number of I/Os used on the MAC interface.

The device integrates media dependent interface (MDI) termination resistors into the PHY. This resistor integration simplifies board layout and reduces board cost by reducing the number of external components.

The device has an integrated linear voltage regulator to generate all required voltages. The device can run off a single 3.3V supply. The device supports 1.8V, 2.5V, and 3.3V LVCMOS I/O standards.

88Q1110/88Q1111 device is designed to support the passing and reporting for CRC errors for preemption frames per IEEE 802.3br-2016.

The device uses advanced mixed-signal processing to perform equalization, echo, data recovery, and error correction at a 100 Mbps data rate. The device achieves robust performance and exceeds automotive electromagnetic interference (EMI) requirements in noisy environments with very low power dissipation.

This 88Q1110 is compatible to the footprint of Marvell 88Q1010 100BASE-T1 and 88Q2110 100/1000BASE-T1 Ethernet PHY transceivers.

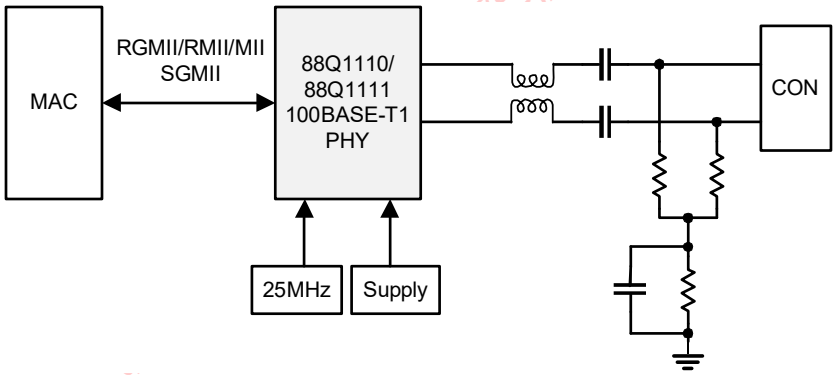
Features

- General
  - Single-port 100BASE-T1 PHY, IEEE 802.3bw compliant
  - RGMII / RMII / MII system interface with 1.8V / 2.5V / 3.3V I/Os (88Q1110 device)
  - Serial GMII (SGMII) system interface with 1.8V / 2.5V / 3.3V I/Os (88Q1111 device)
  - MDC/MDIO management interface
  - Supports synchronous Ethernet (SyncE)
  - Supports 802.1AS – precision time protocol (PTP)
  - Supports Wake on LAN (WoL) event detection
  - Supports one-step PTP
  - Integrated filter network for reduced BOM cost and board space
  - Integrated temperature sensor
  - OPEN Alliance TC1 and TC10 support
  - AEC-Q100 automotive standard compliant
  - Supports Automotive Grade 1 (-40 °C to +125 °C)
- Diagnostics
  - Advanced diagnostic features including dynamic channel, harness defect detection, link quality, polarity detection & correction.
  - Integrated VCT for cable diagnostics
  - Supply undervoltage detection with safe-mode behavior.
  - Build-in packet generator and receive error counter.
  - Internal loopback mode for diagnostics.
- Power
  - Integrated LDO for 3.3V only operation
  - Ultra-low power at 100 mW
  - Low power mode with energy detect at 30 µA
- Package
  - 40-QFN, 6.0×6.0 mm, 0.5 mm pitch (88Q1110 with RGMII/xMII)
  - 40-QFN, 6.0×6.0 mm, 0.5 mm pitch (88Q1111 with SGMII)

Applications

- Automotive infotainment systems
- Advanced driver assist systems
- Automotive diagnostics
- Body electronics

Figure 1: Block Diagram



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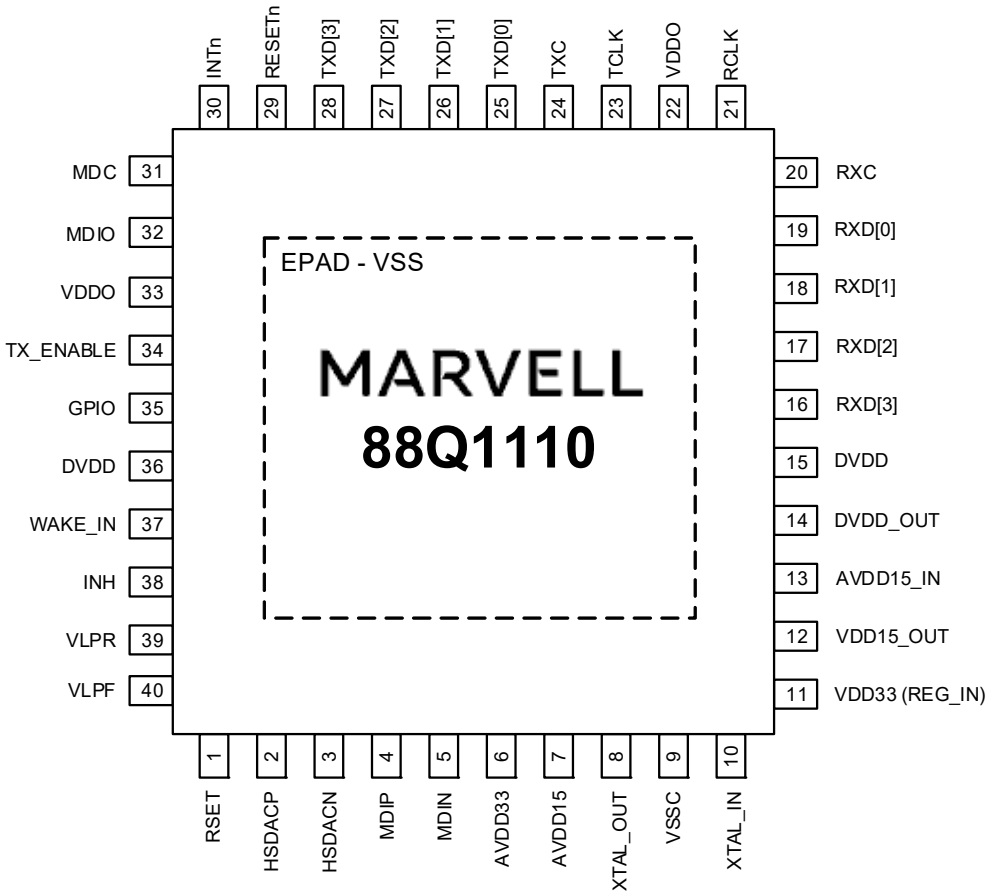
1.1 88Q1110 Pinout

The 88Q1110 device is a 100BASE-T1 Ethernet transceiver with an RGMII/RMII/MII MAC interface.

Figure 2: 88Q1110 Device 40-Pin QFN Package (Top View)



1.2 88Q1110 Pin Descriptions

Table 1: 88Q1110 Pin Type Definitions

Pin Type	Definition
A	Analog
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.2.1 88Q1110 Media Dependent Interface

Table 2: 88Q1110 Media Dependent Interface

Pin #	Pin Name	Pin Type	During Reset	Description
5 4	MDIN MDIP	I/O	Tri-state	Media Dependent Interface. In 100BASE-T1, MDIN/P are used for transmit and receive.

1.2.2 88Q1110 Host Interface

The host interfaces support 100BASE-T1 mode of operation.

Table 3: 88Q1110 Host Interfaces

Pin #	Pin Name	Pin Type	During Reset	Description
23	TCLK[1]	I/O	Tri-state	• When MII is used, this pin is an output that drives out a 25 MHz clock with ± 50 ppm tolerance. • When RGMII is used, this pin is an input. It should be driven with a 25 MHz clock with ± 50 ppm tolerance. • When RMII is used, this pin is not used. Connect to VSS.
24	TXC	I	I	• When MII is used, this pin's signal should be presented for sampling with the positive edge of TCLK. • When RGMII is used, this pin's signal must be presented according to the RGMII timing mode requirements. • When RMII is used, this pin's signal should be presented based on the 50 MHz clock from RCLK.
28 27 26 25	TXD[3] TXD[2] TXD[1] TXD[0]	I	I	• When MII is used, the signals for these pins should be presented for sampling with the positive edge of TCLK. • When RGMII is used, the signals for these pins must be presented according to RGMII timing mode requirements. Data is presented for sampling with the rising edge of TCLK only. • When RMII is used, only TXD[1:0] are used. Connect TXD[3:2] to VSS. Two-bits are input every 20 ns based on the 50 MHz clock from RCLK.
21	RCLK	I/O	Tri-state	• When MII is used, this pin is an output that drives out a 25 MHz clock with ± 50 ppm tolerance used by a connected MAC. • When RGMII is used, this pin is an output that drives out a 25 MHz clock with ± 50 ppm tolerance used by a connected MAC. • When RMII is used, this pin outputs a 50 MHz clock used by the PHY for the RX and TX datapaths and a connected MAC. • RCLK follows XTAL ppm (i.e., if XTAL has 100 ppm, RCLK is also 100 ppm).

Table 3: 88Q1110 Host Interfaces (Continued)

Pin #	Pin Name	Pin Type	During Reset	Description
20	RXC	I/O	Tri-state	• When MII is used, this pin's signal is presented for sampling with the positive edge of RCLK. • When RGMII is used, this pin's signal is presented according to the RGMII timing mode requirements. • When RMII is used, this pin's signal is presented for sampling with the positive edge of RCLK.
16 17 18 19	RXD[3] RXD[2] RXD[1] RXD[0]	I/O	Tri-state	• When MII is used, the signals for these pins are presented for sampling with the positive edge of RCLK. • When RGMII is used, the signals for these pins are presented according to RGMII timing mode requirements. Data is presented for sampling with the rising edge of RCLK only. • When RMII is used, only RXD[1:0] are used for RMII. Two-bitdata are output every 20 ns based on the 50 MHz clock from RCLK. RXD[3:2] can be left floating.

1. This pin is an output pin on the MII interface.

1.2.3 88Q1110 Management Interface

Table 4: 88Q1110 Management Interface

Pin #	Pin Name	Pin Type	During Reset	Description
31	MDC	I	I	Management Interface Clock. This pin is MDC. A continuous clock stream is not required for MDC. The maximum frequency allowed is 12.5 MHz.
32	MDIO	I/O	I	Management Interface Data. This pin is MDIO and requires a pull-up resistor with a resistance from 1.5 kΩ to 10 kΩ.

1.2.4 88Q1110 Tx Enable/GPIO/LED/Interrupt/SyncE Clock Interface

Table 5: 88Q1110 Tx Enable/GPIO/LED/Interrupt Interface

Pin #	Pin Name	Pin Type	During Reset	Description
34	TX_ENABLE	I/O	Tri-state with PU	Tx Enable/GPIO/LED. This pin is an input by default and used to implement a feature that allows blocking Tx packets. For details, see Section 2.2.5, Tx Disable Feature, on page 43. This pin can be used as a GPIO or LED pin.
35	GPIO	I/O	Tri-state with PU	PHYAD[2] Configuration/GPIO/LED Output/SyncE Recovered Clock Output.
30	INTn	O	Tri-state	Interrupt output.

1.2.5 88Q1110 Clock/Configuration/Reset/I/O

Table 6: 88Q1110 Clock/Configuration/Reset/I/O

Pin #	Pin Name	Pin Type	During Reset	Description
10	XTAL_IN	I	I	Reference Clock. 25 MHz ± 100 ppm tolerance crystal reference or oscillator input. When XTAL_IN is driven directly from the oscillator or clock buffer, AC couple this pin with a 0.1 nF capacitor. **NOTE:** The XTAL_IN pin is not 2.5V/3.3V tolerant. For information on how to convert a 2.5V/3.3V clock source to a 1.5V clock, see the *Oscillator Level Shifting* application note (MV-S301630-00).
8	XTAL_OUT	O	Independent of Reset	Reference Clock. 25 MHz ± 100 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected to a crystal, connect this pin to VSS through a 0.1 uF ceramic capacitor.
9	VSSC	Analog GND	Analog GND	XTAL ground.
29	RESETn	I	Low	Hardware Reset, active-low. 0 = Reset 1 = Normal operation

1.2.6 88Q1110 Control and Reference

Table 7: 88Q1110 Control and Reference

Pin #	Pin Name	Pin Type	During Reset	Description
1	RSET	A	A	Constant Voltage Reference. For this pin, an external 4.99 kΩ 1% resistor connection to VSS is required.

1.2.7 88Q1110 Test

Table 8: 88Q1110 Test

Pin #	Pin Name	Pin Type	During Reset	Description
3 2	HSDACN HSDACP	A, O	Tri-state	Test Pins. Used to bring out TX_TCLK for IEEE test modes. Connect these pins with a 50Ω termination resistor to VSS for IEEE testing. If IEEE testing is not done, these pins can be left floating.

1.2.8 88Q1110 Power, Ground, and Internal Regulators

Table 9: 88Q1110 Power, Ground, and Internal Regulators

Pin #	Pin Name	Pin Type	During Reset	Description
7	AVDD15	Analog Power	Analog Power	Analog Supply – 1.5V[1]. AVDD15 can be supplied externally with 1.5V, or via the 1.5V internal regulator.
6	AVDD33	Analog Power	Analog Power	Analog Supply – 3.3V.
11	VDD33 (REG_IN)	Analog Power	Analog Power	Analog Supply for the internal regulator – 3.3V. If the internal regulator is not used, this pin must be left floating (No Connect).
13	AVDD15_IN	Analog Power	Analog Power	Power Regulator Input – 1.5V. AVDD15_IN is a supply input for the internal DVDD regulator. If internal regulators are in use, this should be connected to VDD15_OUT. If internal regulators are not used, this pin should be left floating (No Connect)
12	VDD15_OUT	Analog Power	Analog Power	Regulator Output – 1.5V. If the internal regulator is used, this pin must be connected to a 1.5V power plane that connects to AVDD15.This should also be connected to AVDD15_IN. If an external supply is used, this pin must be left floating (No Connect).
14	DVDD_OUT	Power	Power	Regulator Output – 1.05V. If the internal regulator is used, this pin must be connected to a 1.05V power plane that connects to DVDD. If the external supply is used, this pin must be left floating (No Connect).
22 33	VDDO	Power	Power	3.3V or 2.5V or 1.8V Digital I/O Supply[2]. VDDO must be supplied externally.
15 36	DVDD	Power	Power	Digital Core Supply – 1.05V. DVDD can be supplied externally with 1.05V or via the 1.05V internal regulator.
E-PAD	VSS	GND	GND	Ground to Device. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. For the exact location and dimensions of the E-PAD, see Section 6, Package Mechanical Dimensions, on page 261.

1. AVDD15 supplies the XTAL_IN and XTAL_OUT pins.
2. VDDO supplies the MDC, MDIO, RESETn, INTn, TX_ENABLE, GPIO, and the host interface pins.

1.2.9 88Q1110 Low Power Signal Detect (LPSD)

Table 10: 88Q1110 Low Power Signal Detect

Pin #	Pin Name	Pin Type	During Reset	Description
38	INH	A, O	O	Output collector to control enable of the external regulator. In order to draw minimal current in deep sleep, INH has two states. 'HIGH' to drive the external regulator(s) enables signal (on), and tristate when in deep sleep. An external 10 kohm pull-down is required at INH. This pin should be left floating when LPSD is not used.
39	VLPR	Analog Power	Analog Power	Regulated supply derived from battery. This supplies the energy detect sensing circuit, and the INH I/O.
40	VLPF	Analog	Analog	Connect to external battery circuit. Refer to Figure 17 on page 58 and Figure 18 on page 59 for details. This pin should be left floating when LPSD is not used.
37	WAKE_IN	A, I	I	Used for local wake-up. This pin should be left floating when LPSD is not used.

1.3 88Q1110 Pin Assignment List – Alphabetical by Signal Name

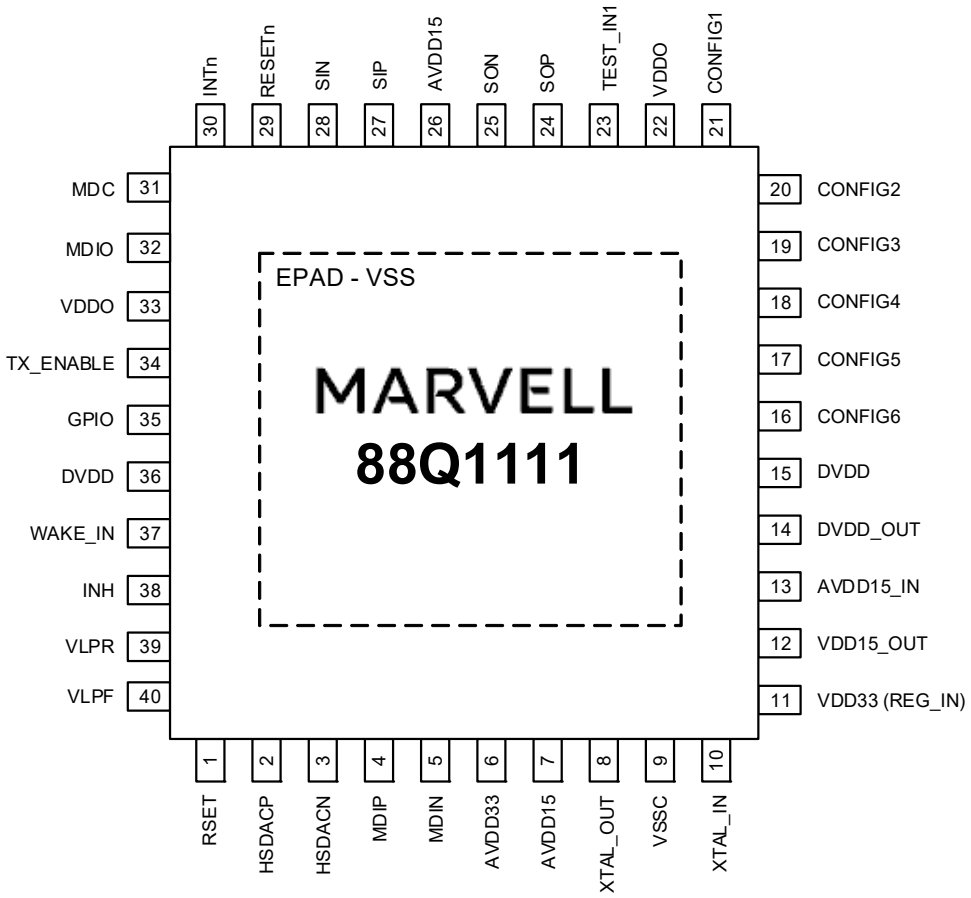
Table 11: 88Q1110 Pin Assignment List – Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
7	AVDD15	17	RXD[2]
13	AVDD15_IN	16	RXD[3]
6	AVDD33	23	TCLK
15	DVDD	34	TX_ENABLE
36	DVDD	24	TXC
14	DVDD_OUT	25	TXD[0]
35	GPIO	26	TXD[1]
3	HSDACN	27	TXD[2]
2	HSDACP	28	TXD[3]
38	INH	12	VDD15_OUT
30	INTn	11	VDD33 (REG_IN)
31	MDC	22	VDDO
5	MDIN	33	VDDO
32	MDIO	40	VLPF
4	MDIP	39	VLPR
21	RCLK	E-PAD	VSS
29	RESETn	9	VSSC
1	RSET	37	WAKE_IN
20	RXC	10	XTAL_IN
19	RXD[0]	8	XTAL_OUT
18	RXD[1]	--	--

1.4 88Q1111 Pinout

The 88Q1111 device is a 100BASE-T1 Ethernet transceiver with an SGMII MAC interface.

Figure 3: 88Q1111 Device 40-Pin QFN Package (Top View)



1.5 88Q1111 Pin Descriptions

Table 12: 88Q1111 Pin Type Definitions

Pin Type	Definition
A	Analog
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.5.1 88Q1111 Media Dependent Interface

Table 13: 88Q1111 Media Dependent Interface

Pin #	Pin Name	Pin Type	During Reset	Description
5 4	MDIN MDIP	I/O	Tri-state	Media Dependent Interface. In 100BASE-T1, MDIN/P are used for transmit and receive.

1.5.2 88Q1111 Host Interface

The host interface supports 100BASE-T1 mode of operation.

Table 14: 88Q1111 SGMII Interface

Pin #	Pin Name	Pin Type	During Reset	Description
24	SOP	A, O	O	SGMII Transmit Data. Positive
25	SON	A, O	O	SGMII Transmit Data. Negative
27	SIP	A, I	I	SGMII Receive Data. Positive
28	SIN	A, I	I	SGMII Receive Data. Negative

1.5.3 88Q1111 Management Interface

Table 15: 88Q1111 Management Interface

Pin #	Pin Name	Pin Type	During Reset	Description
31	MDC	I	I	Management Interface Clock. This pin is MDC. A continuous clock stream is not required for MDC. The maximum frequency allowed is 12.5 MHz.
32	MDIO	I/O	I	Management Interface Data. This pin is MDIO and requires a pull-up resistor with a resistance from 1.5 kΩ to 10 kΩ.

1.5.4 88Q1111 Tx Enable/GPIO/LED/Interrupt/SyncE Clock Interface

Table 16: 88Q1111 Tx Enable/GPIO/LED/Interrupt Interface

Pin #	Pin Name	Pin Type	During Reset	Description
34	TX_ENABLE	I/O	Tri-state with PU	Tx Enable/GPIO/LED. This pin is an input by default and used to implement a feature that allows blocking Tx packets. For details, see Section 2.2.5, Tx Disable Feature, on page 43. This pin can be used as a GPIO or LED pin.
35	GPIO	I/O	Tri-state with PU	PHYAD[2] Configuration/GPIO/LED Output/SyncE Recovered Clock Output.
30	INTn	O	Tri-state	Interrupt output.

1.5.5 88Q1111 Clock/Configuration/Reset/I/O

Table 17: 88Q1111 Clock/Configuration/Reset/I/O

Pin #	Pin Name	Pin Type	During Reset	Description
10	XTAL_IN	I	I	Reference Clock. 25 MHz ± 100 ppm tolerance crystal reference or oscillator input. When XTAL_IN is driven directly from the oscillator or clock buffer, this pin should be AC coupled with a 0.1 nF capacitor. **NOTE:** The XTAL_IN pin is not 2.5V/3.3V tolerant. For information on how to convert a 2.5V/3.3V clock source to a 1.5V clock, see the *Oscillator Level Shifting* application note (MV-S301630-00).
8	XTAL_OUT	O	Independent of Reset	Reference Clock. 25 MHz ± 100 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected to a crystal, it should be connected to ground through a 0.1 uF ceramic capacitor.
9	VSSC	Analog GND	Analog GND	XTAL ground.
16	CONFIG6	I/O	Tri-state	Global hardware configuration.
17	CONFIG5	I/O	Tri-state	
18	CONFIG4	I/O	Tri-state	
19	CONFIG3	I/O	Tri-state	
20	CONFIG2	I/O	Tri-state	
21	CONFIG1	I/O	Tri-state	
29	RESETn	I	Low	Hardware Reset, active-low. 0 = Reset 1 = Normal operation

1.5.6 88Q1111 Control and Reference

Table 18: 88Q1111 Control and Reference

Pin #	Pin Name	Pin Type	During Reset	Description
1	RSET	A	A	Constant Voltage Reference. For this pin, an external 4.99 kΩ 1% resistor connection to VSS is required.

1.5.7 88Q1111 Test

Table 19: 88Q1111 Test

Pin #	Pin Name	Pin Type	During Reset	Description
3 2	HSDACN HSDACP	A, O	Tri-state	Test Pins. Used to bring out TX_TCLK for IEEE test modes. Connect these pins with a 50Ω termination resistor to VSS for IEEE testing. If IEEE testing is not done, these pins can be left floating.
23	TEST_IN1	I	I	Test pin.

1.5.8 88Q1111 Power, Ground, and Internal Regulators

Table 20: 88Q1111 Power, Ground, and Internal Regulators

Pin #	Pin Name	Pin Type	During Reset	Description
7 26	AVDD15	Analog Power	Analog Power	Analog Supply – 1.5V[1]. AVDD15 can be supplied externally with 1.5V, or via the 1.5V internal regulator.
6	AVDD33	Analog Power	Analog Power	Analog Supply – 3.3V.
11	VDD33 (REG_IN)	Analog Power	Analog Power	Analog Supply for the internal regulator – 3.3V. If the internal regulator is not used, this pin must be left floating (No Connect).
13	AVDD15_IN	Analog Power	Analog Power	Power Regulator Input – 1.5V. AVDD15_IN is a supply input for the internal DVDD regulator. If internal regulators are in use, this should be connected to VDD15_OUT. If internal regulators are not used, this pin should be left floating (No Connect)
12	VDD15_OUT	Analog Power	Analog Power	Regulator Output – 1.5V. If the internal regulator is used, this pin must be connected to a 1.5V power plane that connects to AVDD15. This should also be connected to AVDD15_IN. If an external supply is used, this pin must be left floating (No Connect).
14	DVDD_OUT	Power	Power	Regulator Output – 1.05V. If the internal regulator is used, this pin must be connected to a 1.05V power plane that connects to DVDD. If the external supply is used, this pin must be left floating (No Connect).
22 33	VDDO	Power	Power	3.3V or 2.5V or 1.8V Digital I/O Supply[2]. VDDO must be supplied externally.
15 36	DVDD	Power	Power	Digital Core Supply – 1.05V. DVDD can be supplied externally with 1.05V or via the 1.05V internal regulator.
E-PAD	VSS	GND	GND	Ground to Device. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. For the exact location and dimensions of the E-PAD, see Section 6, Package Mechanical Dimensions, on page 261.

1. AVDD15 supplies the XTAL_IN and XTAL_OUT pins.
2. VDDO supplies the MDC, MDIO, RESETn, INTn, TX_ENABLE, GPIO, and the host interface pins.

1.5.9 88Q1111 Low Power Signal Detect (LPSD)

Table 21: 88Q1111 Low Power Signal Detect

Pin #	Pin Name	Pin Type	During Reset	Description
38	INH	A, O	O	Output collector to control enable of the external regulator. In order to draw minimal current in deep sleep, INH has two states. 'HIGH' to drive the external regulator(s) enables signal (on), and tristate when in deep sleep. An external 10 kohm pull-down is required at INH. This pin should be left floating when LPSD is not used.
39	VLPR	Analog Power	Analog Power	Regulated supply derived from battery. This supplies the energy detect sensing circuit, and the INH I/O.
40	VLPF	Analog	Analog	Connect to external battery circuit. Refer to Figure 17 on page 58 and Figure 18 on page 59 for details. This pin should be left floating when LPSD is not used.
37	WAKE_IN	A, I	I	Used for local wake-up. This pin should be left floating when LPSD is not used.

1.6 88Q1111 Pin Assignment List – Alphabetical by Signal Name

Table 22: 88Q1111 Pin Assignment List – Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
7	AVDD15	4	MDIP
26	AVDD15	29	RESETn
13	AVDD15_IN	1	RSET
6	AVDD33	28	SIN
21	CONFIG1	27	SIP
20	CONFIG2	25	SON
19	CONFIG3	24	SOP
18	CONFIG4	23	TEST_IN1
17	CONFIG5	34	TX_ENABLE
16	CONFIG6	12	VDD15_OUT
15	DVDD	11	VDD33 (REG_IN)
36	DVDD	22	VDDO
14	DVDD_OUT	33	VDDO
35	GPIO	40	VLPF
3	HSDACN	39	VLPR
2	HSDACP	E-PAD	VSS
38	INH	9	VSSC
30	INTn	37	WAKE_IN
31	MDC	10	XTAL_IN
5	MDIN	8	XTAL_OUT
32	MDIO	--	--

2 PHY Functional Specifications

The device is a 100BASE-T1 Ethernet transceiver. Figure 4 shows the functional block diagram of the device.

Note Refer to Product Overview for a list of features supported by the device.

Figure 4: 88Q1110 Device Functional Block Diagram

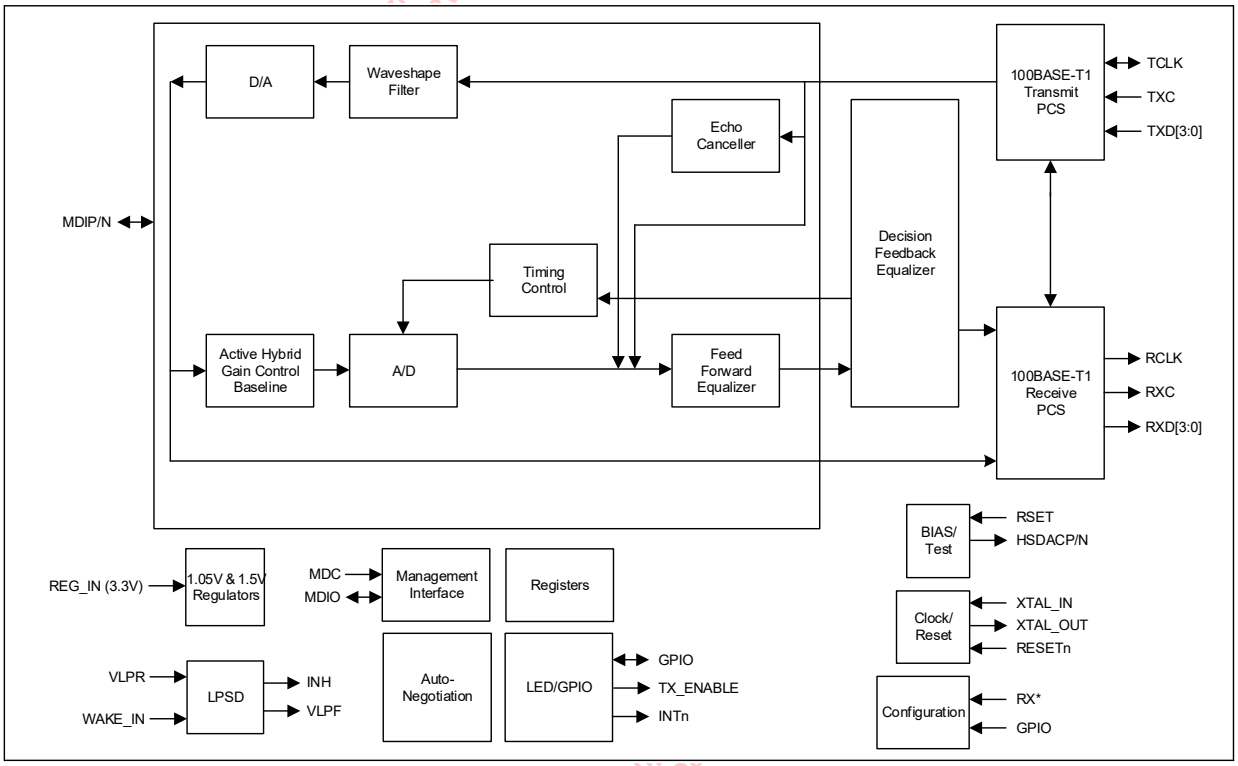
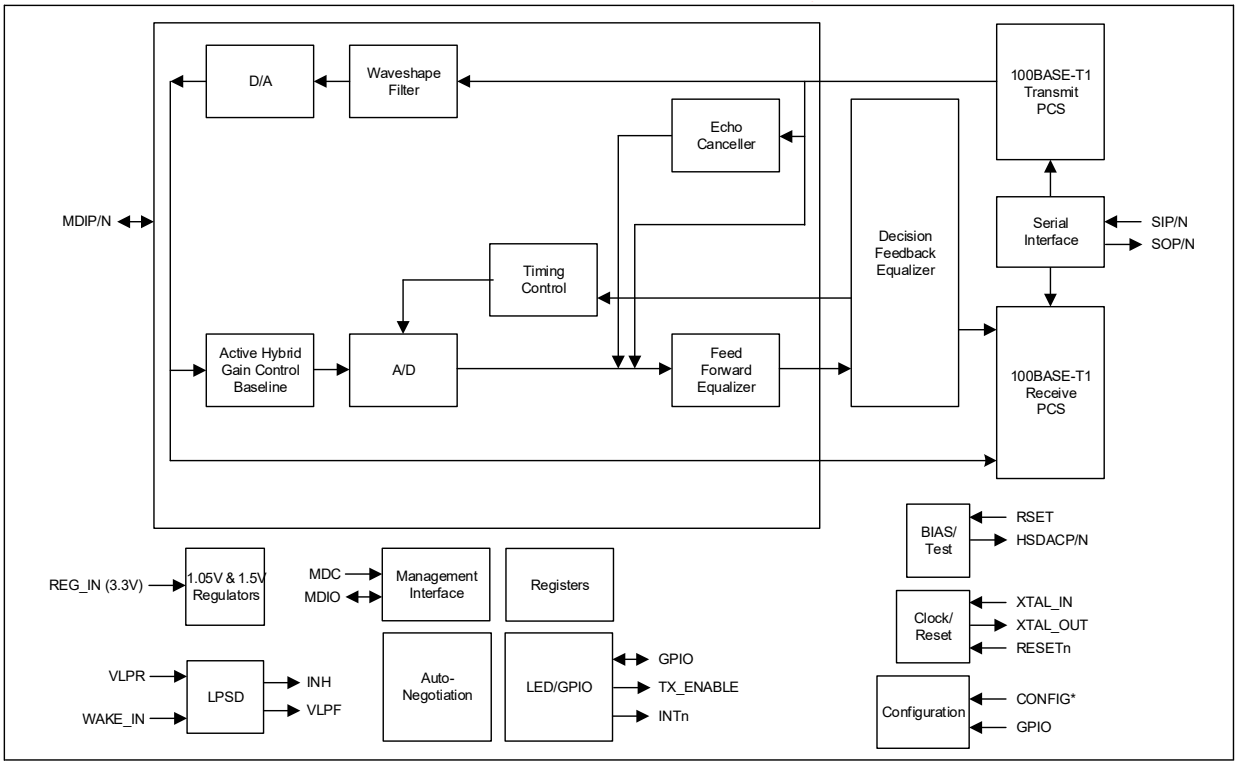


Figure 5: 88Q1111 Device Functional Block Diagram



2.1 Copper Media Interface

The copper interface consists of the MDIP/N pins that connect to the physical media for 100BASE-T1 mode of operation per IEEE 802.3bw standard.

2.1.1 Transmit Side Network Interface

The device integrates MDI interface termination resistors. The IEEE 802.3 specification requires that both sides of a link have termination resistors to prevent reflections. The resistors must be very accurate to meet the strict IEEE and OPEN Alliance PSD and MDI return loss requirements.

The device incorporates a transmit DAC to generate filtered 3-level pulse amplitude modulation (PAM3) symbols. The transmit DAC performs signal wave shaping in conjunction with slew rate control to reduce the emission. In addition, transmitter integrates low pass filter to meet OPEN Alliance EMC requirement, as well as radiated emission at higher frequency band, without extra external circuits.

2.1.1.1 Receive Side Network Interface

The device incorporates an advanced high-speed ADC on the receive channel with greater resolution than the ADC used in the reference model of the IEEE 802.3ab standard committee. Higher resolution ADC results in better SNR, and therefore lower error rates. Patented architectures and design techniques result in high differential and integral linearity, high power supply noise rejection, and low metastability error rate. The ADC samples the input signal at 66.67 MHz

Residual echo not removed by the hybrid and echo due to patch cord impedance mismatch, patch panel discontinuity, and variations in cable impedance along the twisted pair cable result in drastic SNR degradation on the receive signal. The device employs a fully developed digital echo canceller to adjust for echo impairments from more than 15 meters of cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

2.2 System Interfaces

The 88Q1110 device supports three System interfaces: RGMII, MII and RMII. The 88Q1111 device supports SGMII as the System interface. The 88Q1110 device interface desired may be selected by configuration.

Two RGMII modes can be configured to select the data/clock timing relation. The default of registers 4.8000.3:2 will be set correctly by configuration to select the delay of TCLK and RCLK. For more flexibility, the delay of TCLK and RCLK can also be controlled by reprogramming register 4.8000.3:2. For detailed timing requirement for all modes, see Section 5.7, MAC Interface Timing, on page 251.

Table 23: Modes

Mode	Description	4.8000.1:0	4.8000.3:2
RGMII (mode1)	TCLK (input) transitions at the same time as TXD/TXC. RCLK (output) transitions when RXD/RXC is stable. TCLK and RCLK are 25 MHz. DDR interface.	01	11
RGMII (mode2)	TCLK (input) transitions when TXD/TXC is stable. RCLK (output) transitions when RXD/RXC is stable. TCLK and RCLK are 25 MHz. DDR interface.	11	10
MII	Both TCLK and RCLK are 25 MHz. Data should be latched at rising edge of clocks.	00	Don't care
RMII	RCLK is 50 MHz output and is used for both Tx and Rx; data should be latched at rising edge of RCLK.	10	Don't care

The slew rate/drive strength of the RX pins (RXD[3:0], RXC, and RCLK) and the TCLK pin (in MII mode, when it is used as an output) can be controlled via register 4.8001.11:4.

Table 24: RGMII Output Pin Control

Register Bits	Field	Type	Description
4.8001.11:8	PMOS Value control	R/W	Control drive strength and slew rate value of RGMII pads
4.8001.7:4	NMOS Value control	R/W	Control drive strength and slew rate value of RGMII pads

If the device is configured to RMII mode, the default for 4.8100.11:4 is 1010_1010; otherwise, it is 1001_1001.

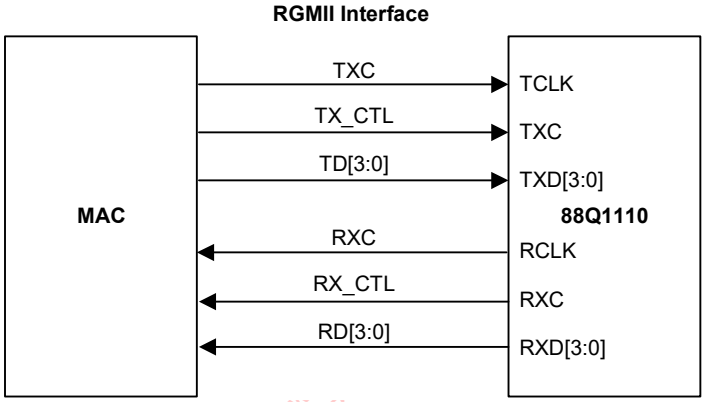
2.2.1 RGMII Interface

The device supports an RGMII interface that operates at 100 Mbps. Four RGMII timing modes, with different receive clock to data timing and transmit clock to data timing, can be programmed by setting register 4.8000.3:2. For timing details, see Section 5.7.2, RGMII 100 Mbps Input Timing, on page 251 or Section 5.7.3, RGMII 100 Mbps Output Timing, on page 253.

Table 25: RGMII Signal Mapping

Device Pin Name	RGMII Spec Pin Name	Description
TCLK	TXC	25 MHz transmit clock with ±50 ppm tolerance.
TXC	TX_CTL	Transmit Control Signals. TX_EN is encoded on the rising edge of TCLK. TX_ER XOR'ed with TX_EN is encoded on the falling edge of TCLK.
TXD[3:0]	TD[3:0]	TXD[3:0] are synchronous with the rising edge of TCLK.
RCLK	RXC	25 MHz receive clock derived from the received data stream.
RXC	RX_CTL	Receive Control Signals. RX_DV is encoded on the rising edge of RCLK. RX_ER XOR'ed with RX_DV is encoded on the falling edge of RCLK.
RXD[3:0]	RD[3:0]	RXD[3:0] are synchronous with the rising edge of RCLK.

Figure 6: RGMII Signal Diagram



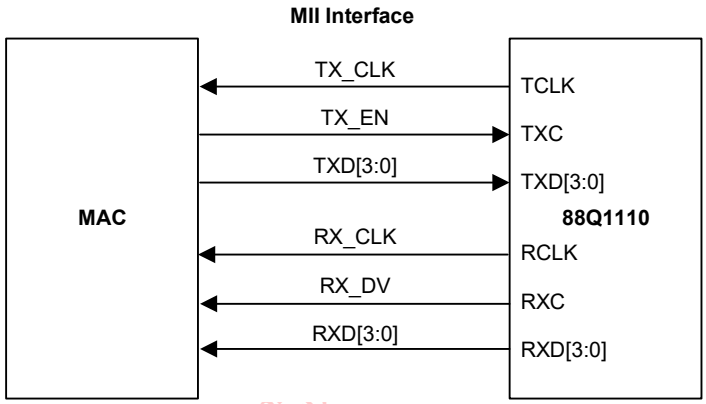
2.2.2 MII Interface

Table 26 indicates the signal mapping of the 88Q1110 device to the MII interface. TX_ER, RX_ER, CRS, and COL, which are specified in IEEE802.3 Clause 22, are not implemented.

Table 26: MII Signal Mapping

Device Pin Name	MII Spec Pin Name	Description
TCLK	TX_CLK	25 MHz transmit clock.
TXC	TX_EN	Transmit Enable Signal. This signal is synchronous with respect to the rising edge of TCLK.
TXD[3:0]	TXD[3:0]	Transmit Data. TXD[3:0] are synchronous with respect to the rising edge of TCLK.
RCLK	RX_CLK	25 MHz receive clock derived from the received data stream.
RXC	RX_DV	Receive Data Valid. This signal is synchronous with respect to rising edge of RCLK
RXD[3:0]	RXD[3:0]	Receive Data. RXD[3:0] are synchronous with respect to the rising edge of RCLK.

Figure 7: MII Signal Diagram



Note

During the transition from link change, a dead time for a maximum duration of 1.5 clock cycles may occur on RCLK and TCLK to ensure a glitch-free clock.

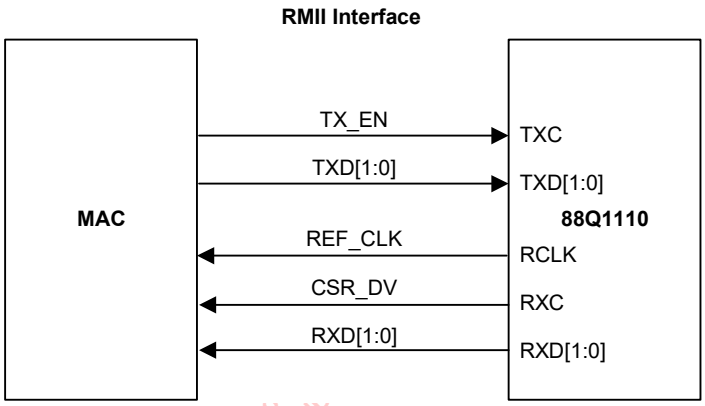
2.2.3 RMII Interface

RMII interface is also supported by the device. 2-bit data are transferred with respect to a 50 MHz REF_CLK on all rising edges. However, the 50 MHz REF_CLK is output from the device, rather than sourced externally from a MAC or system board as described in the RMII specification.The mapping of the signals is listed in Table 27.

Table 27: RMII Interface

Device Pin Name	RMII Pin Name	Description
TXC	TX_EN	Transmit Enable Signal. This signal is synchronous with respect to the rising edge of RCLK.
TXD[1:0]	TXD[1:0]	Transmit Data. TXD[1:0] are synchronous with respect to the rising edge of RCLK
RCLK	REF_CLK	Output 50 MHz reference clock for both Rx and Tx.
RXC	CRS_DV	Carrier Sense/Receive Data Valid. This signal is synchronous with respect to the rising edge of RCLK.
RXD[1:0]	RXD[1:0]	Receive Data. RXD[1:0] are synchronous with respect to the rising edge of RCLK.

Figure 8: RMII Interface



2.2.4 SGMII Interface

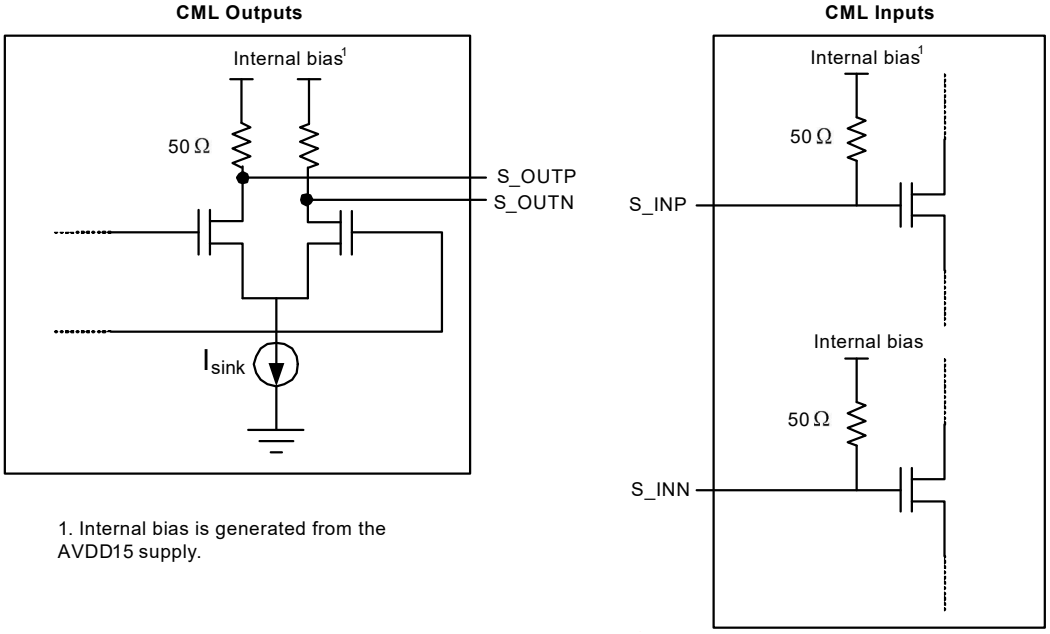
The device supports the SGMII specification revision 1.8. This interface supports a 100 Mbps mode of operation.

2.2.4.1 1.25 GHz SERDES Interface

The 1.25 GHz SERDES supports the SGMII mode at the line side.

The input and output buffers of the 1.25 GHz SERDES interface are internally terminated by 50Ω impedance. No external terminations are required. The output swing can be adjusted by programming register 31.801A.2:0. The 1.25 GHz SERDES I/Os are current mode logic (CML) buffers. CML I/Os can be used to connect to other components with PECL or LVDS I/Os.

Figure 9: CML I/Os



1. Internal bias is generated from the AVDD15 supply.

2.2.4.2 SGMII Link and Status

Two registers are available to determine whether the SGMII achieved link and sync. Status Register 31.8011.5 indicates that the SERDES locked onto the incoming KDKDKD… sequence. Register 31.8011.10 indicates whether a link is established on the SERDES. If SGMII Auto-Negotiation is disabled, then register 31.8011.10 has the same meaning as register 31.8011.5. If SGMII Auto-Negotiation is enabled, then register 31.8011.10 indicates whether SGMII Auto-Negotiation successfully established the link.

2.2.5 Tx Disable Feature

The device supports a Tx Disable feature (TX_ENABLE pin). If the pin input is LOW, then Tx packets will be stopped after link up, but Rx packets are still received normally. The link will stay up, and only idles will be sent out the Tx media side. There is an internal pull-up, which will disable this feature if the pin is left floating. A HIGH value from the pull-up or if driven externally will allow packets to flow by default.

To disable this feature completely and use this pin for LED or GPIO functions, write register 3.8640.0 = 0. This will change the pin to an output, and the link status will light up the LED without additional programming.

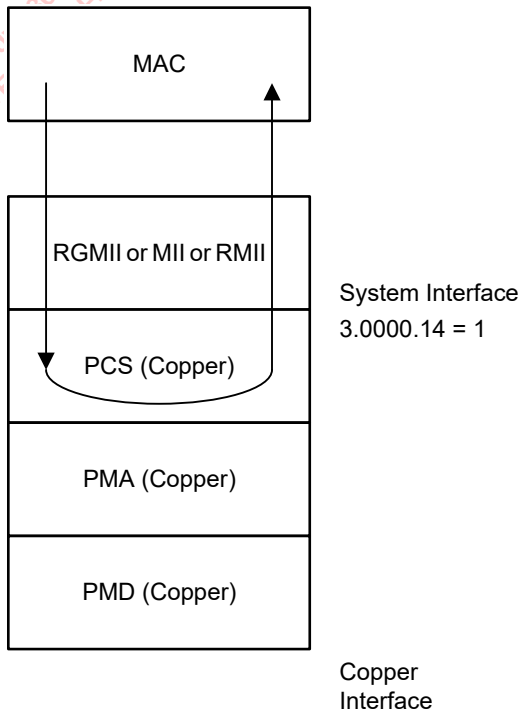
2.3 Loopback

The device implements various loopback paths.

2.3.1 System Interface Loopback

The functionality, timing, and signal integrity of the system interface can be tested by placing the device in system interface loopback mode. This can be accomplished by setting register 3.0000.14 = 1. In this loopback mode, the data received from the MAC is not transmitted out on the copper interface. Instead, the data is looped back and sent to the MAC. During loopback, copper link will be lost and packets will not be received.

Figure 10: MAC Interface Loopback Diagram – Copper Media Interface

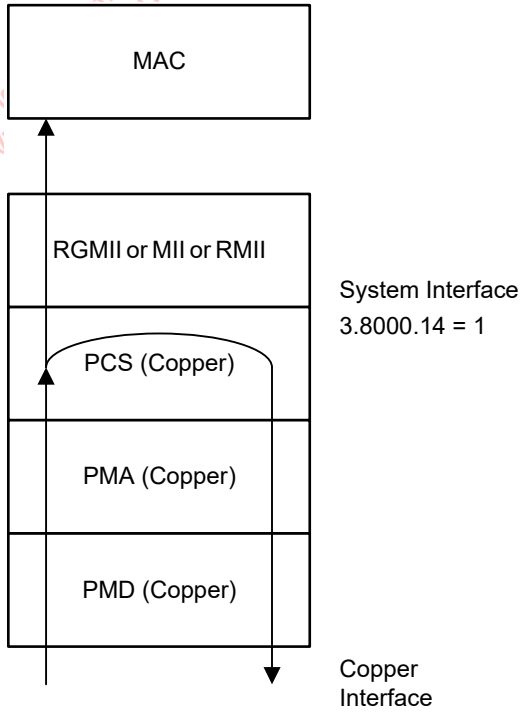


2.3.2 Line Loopback

Line loopback allows a link partner to send frames into the device to test the transmit and receive data path. Frames from a link partner received by the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during line loopback. This allows the link partner to receive its own frames.

Before enabling the line loopback feature, the PHY must first establish link to another PHY link partner. Once link is established, the line loopback mode can be enabled. Register 3.8000.14 = 1 enables the line loopback on the copper interface.

Figure 11: Copper Line Loopback Data Path

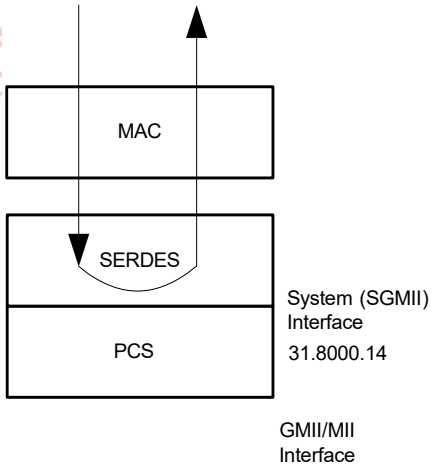


2.3.3 Synchronous SERDES Loopback

The 1.25 GHz SERDES can loop back the raw 10 bit symbol at the receiver back to the transmitter. In this mode of operation, the received data is assumed to be frequency locked with the transmit data output by the PHY. No frequency compensation is performed when the 10 bit symbol is looped back. This mode facilitates testing using data that does not consist of 8B/10B symbols such as PRBS.

The 1.25 GHz SERDES synchronous loopback is enabled by setting register 31.8010.12 = 1 and 31.8010.8 = 0.

Figure 12: Synchronous SERDES Loopback Diagram



2.4 Resets

The 88Q1110/88Q1111 device Reset can be enabled by Hardware or Software, as detailed in the sections below.

2.4.1 Hardware Reset

The 88Q1110/88Q1111 device is forced into Reset mode when the RESETn pin is held LOW. Note that RESETn must be held low for at least ten 25 MHz clocks at power up and 1 ms if asserted during normal operation. Refer to Section 5.6.1, Reset Timing, on page 247.

All register bits are reset to their default values in Reset mode.

2.4.2 Software Reset

The copper circuit is reset via registers 1.0000.15, 3.0000.15, 7.0200.15. The RGMII circuit is reset via register 4.8000.15 and the SGMII circuit is reset via register 31.8000.15. The reset in one circuit does not directly affect another circuit.

All reset registers are self-clear.

Table 28: Reset Control Bits

Reset Register	Register Effect	Functional Block
1.0000.15	Software Reset for Registers in Device 1	Copper
3.0000.15	Software Reset for Registers in Device 3	Copper
7.0200.15	Software Reset for Registers in Device 7	Copper
4.8000.15	Software Reset for Registers in Device 4	RGMII
31.8000.15	Software Reset for Registers in Device 31	SGMII

2.4.3 Undervoltage Protection

The 88Q1110/88Q1111 device monitors the status of the supply voltages continuously, after this monitoring is enabled by setting the corresponding bits (4.8700.3:0) to 1. Once any of the following supply voltages, DVDD, AVDD33, AVDD15 or VDDO drops below the specified minimum operating levels an undervoltage (UV) event is flagged. The 88Q1110/88Q1111 device transitions to a Fail-safe mode (known as Standby mode) automatically. A UV_Error interrupt is generated if enabled programming 4.8703, and the source is indicated in the Interrupt Status register, 4.8704. The device will also flag in 4.8704 when the associated supply voltages exceed their specified minimum undervoltage recovery voltages and set an interrupt if enabled.

A Hardware Reset must be issued when a UV event is flagged in order to resume normal operation.

When the VLPR voltage drops there are two interrupts to detect this. One to indicate that VLPR dropped but not far enough to cause a reset to the LPSD circuit and one to indicate that VLPR is back up.

Once the interrupts or status are seen for a non-VLPR UV event, a hardware reset should be issued; however, for a VLPR UV event this is not recommended.

The interrupt enable bits are defined in Table 29, and the interrupt status bits are defined in Table 30

Table 29: Undervoltage Interrupt Enable
Device 4, Register 0x8703

Bits	Field	Mode	HW Rst	SW Rst	Description
11	VLPR Up Enable	R/W	0x0	Retain	1 = Enable Interrupt when VLPR is above the required voltage threshold for Normal Operation
10:6	Reserved	R/W	0x00	Retain	
5	FIRSTBOOT Enable	R/W	0x0	Retain	1 = Enable Interrupt for FIRSTBOOT event
4	VLPR Down Enable	R/W	0x0	Retain	1 = Enable Interrupt when VLPR is below the required voltage threshold for Normal Operation

Table 30: Undervoltage Interrupt Status
Device 4, Register 0x8704

Bits	Field	Mode	HW Rst	SW Rst	Description
11	VLPR Up	RO, LH	0x0	Retain	1 = VLPR is above the required voltage threshold for Normal Operation
10:6	Reserved	RO, LH	0x00	Retain	
5	FIRSTBOOT Event	RO, LH	0x0	Retain	1 = FIRSTBOOT event happened
4	VLPR Down	RO, LH	0x0	Retain	1 = VLPR is below the required voltage threshold for Normal Operation

When the VLPR voltage drops low enough and then rises back up again, the LPSD block will reset and a FIRSTBOOT status bit will set to 1. It will clear if read. Also the INTn bit must be enabled. Note that even after a read, the FIRSTBOOT interrupt status bit will be set again if there is HW reset or POR as long as there is no Deep Sleep entered prior to that.

The interrupt for FIRSTBOOT is programmed using the FIRSTBOOT Enable bit, as defined in Table 31. The FIRSTBOOT Event bit (defined in Table 32) indicates that a A FIRSTBOOT Event has happened.

Table 31: FIRSTBOOT Interrupt Enable
Device 4, Register 0x8703

Bits	Field	Mode	HW Rst	SW Rst	Description
5	FIRSTBOOT Enable	R/W	0x0	Retain	1 = Enable Interrupt for FIRSTBOOT event

Table 32: FIRSTBOOT Event Status
Device 4, Register 0x8704

Bits	Field	Mode	HW Rst	SW Rst	Description
5	FIRSTBOOT Event	RO, LH	0x0	Retain	1 = FIRSTBOOT event happened

2.5 Power Management

The device supports several advanced power management modes that conserve power.

2.5.1 Low Power Modes

Two low power modes are supported in the device:

- IEEE Compliance Power Down mode
- OPEN Alliance TC10 100BASE-T1 Port Sleep Mode

2.5.1.1 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting register 1.0000.11 or 3.0000.11 for RGMII (88Q1110 device) and 31.8000.11 for SGMII (88Q1111 device). In this mode, the PHY does not respond to any system interface signals (that is, the RGMII/MII//RMII signals for the 88Q1110 device and the SGMII input signals for the 88Q1111 device), except the MDC/MDIO. It also does not respond to any activity on the copper media.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the media. It can only wake up by setting registers 1.0000.11 and 3.0000.11= 0 for RGMII (88Q1110 device) and 31.8000.11 = 0 for SGMII (88Q1111 device).

Table 33: Power Down Control Bits

Reset Register	Register Effect
1.0000.11	RGMII/Copper Power Down
3.0000.11	RGMII/Copper Power Down
31.8000.11	SGMII Power Down

2.5.1.2 OPEN Alliance TC10 Sleep Mode

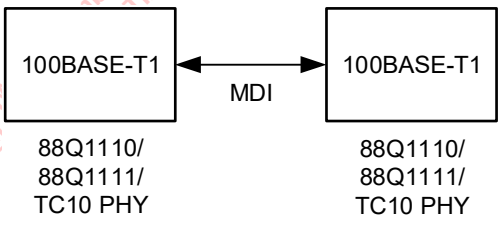
The 88Q1110/88Q1111 device can operate in a low power sleep mode with minimal standby current from the battery voltage with the main supply shut off. During this mode, the device can continuously monitor for a pulse presented at the local wake-up pin, and respond to this wake-up pulse command as specified in OPEN Alliance Sleep/Wake Specification.

TC10 Sleep/Wake Configurations

- **Stand-alone TC10 Capable PHY to Stand-alone TC10 Capable PHY**

  The Sleep/Wake between two TC10 capable stand-alone PHYs, such as the 88Q1110/88Q1111 device, are accomplished through MDI. Either of the devices can initiate a sleep request via register write.

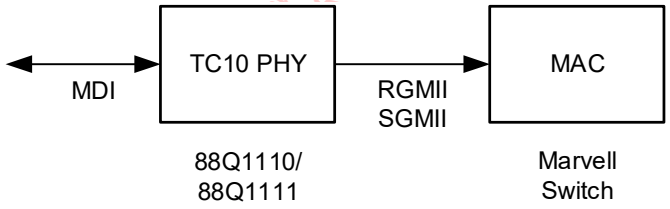
Figure 13: TC10 Sleep/Wake



- **External TC10 Capable PHY with TC10 Capable MAC (Switch)**

  For extended applications of PHYs connected with a Marvell Automotive switch, the Switch level awareness of the Sleep/Wake events are required so that the Switch can determine if the Switch is ready to allow itself to enter sleep. The in-band communication from PHY to MAC (i.e., Switch) to convey sleep state is available to achieve this notification.

Figure 14: In-band TC10 Relay to MAC (Switch) Interface

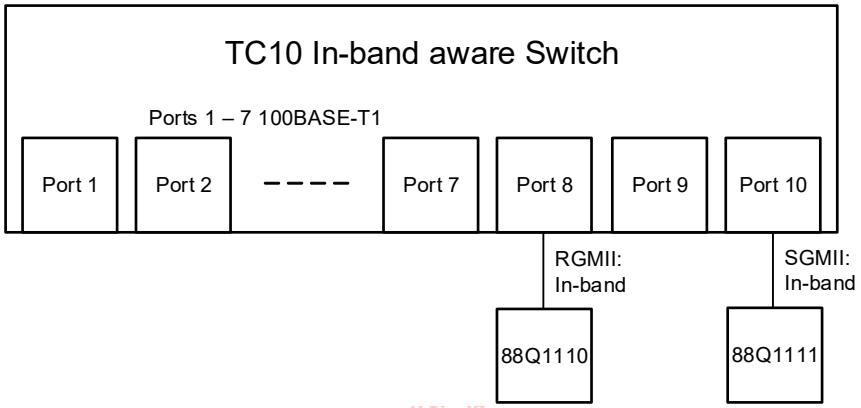


- **Multiple TC10 Capable PHYs Integrated/External in a Switch Application**

  In the case of a Switch application, although a port and its link partner may agree to enter TC10 deep sleep state (where power to the Device is totally removed), the Switch and remaining PHY ports may not be ready to enter the deep sleep state. Therefore, the PHY port will enter a low power state similar to IEEE power down while the remaining Switch and others stay active.

  When all ports have agreed to enter the TC10 Deep Sleep state with their link partner, the Switch can then decide to enter the Deep Sleep state taking away power to the Switch.

Figure 15: MAC (Switch) Interface In-band TC10 Relay



In-band Wake/Sleep Embedded IDLES

This feature has a way to send Sleep/Wake (per the OA TC10 specification) commands and messages embedded in the idles of the 88Q1110/88Q1111 device SGMII and RGMII Host interfaces. Note that MII and RMII do not support this feature since RGMII will always be supported along with them in the same Host interface for Marvell PHYs. The commands or messages conveyed in one idle group is known as a Command Idle Codegroup (CIC).

The following CICs are defined for each Host interface:

RGMII mode - 2 4-bit nibbles presented at each clock edge that are paired together to form a byte.

SGMII mode - 1 KD idle codegroup if the disparity following these is negative and 2 KD idle codegroups if the disparity following the first is positive.

For RGMII mode, the CICs replace normal idles when the in-band status is allowed to be sent (RX_DV and RX_ER are low or TX_EN and TX_ER are low) and each upper data nibble match one of the CIC 4-bit command values defined in Table 34 and Table 35.

Table 34: RGMII Coding- For Legacy in-band Status and the New Sleep/Wake Command Mapping for the PHY

Command Number	RX_CTL	GMII_RX_DV	GMII_RX_ER	Command to Send?	Output from PHY RXD[7:4]	Output from PHY RXD[3:0]	Command/Status
0	0, 0	0	0	No	0000	Xxxx	No Command is Sent
1	0, 0	0	0	No	0001	0110	RGMII Interface Ready
2-15	0, 0	0	0	Yes	xxxx & ! (0000 | 0001)	in-band Status	Command is Sent with in-band Status
2	0, 0	0	0	Yes	0010	in-band Status	PHY Sleep In Progress
4	0, 0	0	0	Yes	0100	in-band Status	PHY Wake Request
6	0, 0	0	0	Yes	0110	in-band Status	PHY Sleep Aborted or Failed
7	0, 0	0	0	Yes	0111	in-band Status	PHY Sleep Complete Remote
8	0, 0	0	0	Yes	1000	in-band Status	PHY Sleep Complete Local
10-15	0, 0	0	0	Yes	1010 – 1111	in-band Status	Reserved

Table 35: RGMII Coding- For Legacy in-band Status and the New Sleep/Wake Command Mapping for the Switch

Command Number	TX_CTL	GMII_TX_EN	GMII_TX_ER	Command to Send?	Output from Switch TXD[7:4]	Output from Switch TXD[3:0]	Command/Status
0	0	0	0	No	0000	0000	No Command is Sent
1	0	0	0	No	0001	0110	RGMII Interface Ready
3	0	0	0	Yes	0011	0000	Switch Sleep Request
5	0	0	0	Yes	0101	0000	Switch Wake Request

Table 35: RGMII Coding- For Legacy in-band Status and the New Sleep/Wake Command Mapping for the Switch (Continued)

Command Number	TX_CTL	GMII_TX_EN	GMII_TX_ER	Command to Send?	Output from Switch TXD[7:4]	Output from Switch TXD[3:0]	Command/Status
9	0	0	0	Yes	1001	0000	Switch Power Removal Request
10-15	0	0	0	Yes	1010 – 1111	0000	Reserved

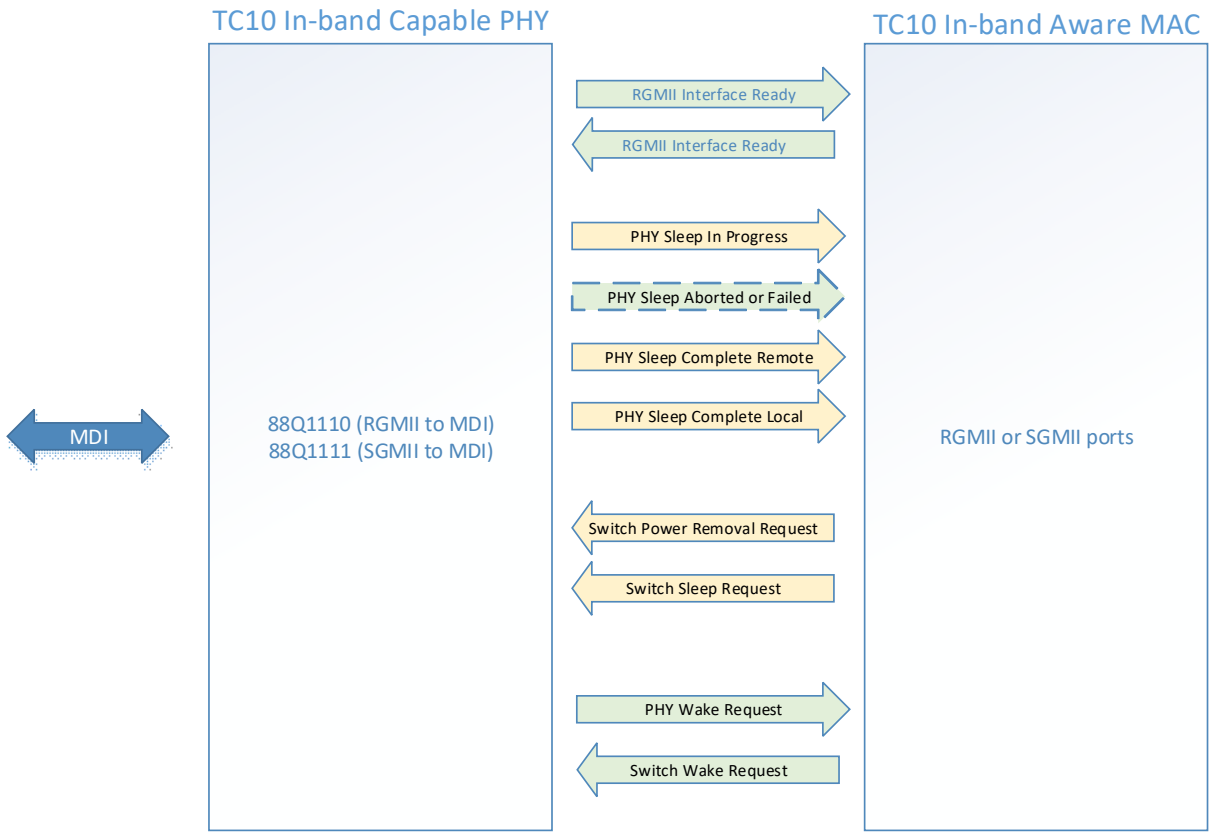
For SGMII, the CICs replace normal idles in an IPG.

Table 36 lists the commands passed through the SGMII interface between the PHYs and Switch:

Table 36: Commands Passed through SGMII code group (8-bit)

Command Number	Command Name	CIC Disparity Inverting D Codegroups (8-bit)	Hex Value
0	Reserved	0010_0000	20
1	Reserved	0010_0001	21
2	PHY Sleep In Progress	0010_0010	22
3	Switch Sleep Request	0000_0011	03
4	PHY Wake Request	0010_0100	24
5	Switch Wake Request	0000_0101	05
6	PHY Sleep Aborted or Failed	0000_0110	06
7	PHY Sleep Complete Remote	0000_0111	07
8	PHY Sleep Complete Local	0010_1000	28
9	Switch Power Removal Request	0000_1001	09
10	Reserved	0000_1010	0A
11	Reserved	0000_1011	0B
12	Reserved	0000_1100	0C
13	Reserved	0000_1101	0D
14	Reserved	0000_1110	0E
15	Reserved	0010_1111	2F

Figure 16: In-band Communication Transaction



Enter Sleep Modes

There are two low power or sleep modes.

- The traditional LPSD mode, known as the Deep Sleep Mode, where the device has supply power completely removed.
- T1 Port Sleep Mode, where the Device still has power but in a low power state. (similar to IEEE power down)

The following are ways to request that the 88Q1110/88Q1111 device power down in the T1 Port Sleep Mode:

1. The link partner sends a low power sleep command (LPS), which is a specific scrambled idles message included in the normal 100BASE-T1 idles to the 88Q1110/88Q1111 device. This initiates a sleep handshake with it to confirm both would like to be in the T1 Port Sleep Mode low power state. A register bit (3.8702.0) is programmed to 1 to initiate a sleep request, which will initiate a sleep handshake with the link partner
2. A sleep request is received at the Host interface from the Switch, which initiates the sleep handshake with the link partner. This can be the result of a sleep request being forwarded from 1 port to the others.

There are two ways to request a Deep Sleep Mode entry:

1. Write register bit (3.8700.0) to 1. This puts the device in Deep Sleep Mode immediately, without doing a TC10 sleep handshake with the Link Partner.

2. A Switch Power Removal Request. This gives the 88Q1110/88Q1111 device permission to go into Deep Sleep. This is only allowed when all devices are in the T1 Port Sleep Mode first and then they receive this power removal permission. The Switch can instead not grant permission for a PHY to have power removed and it would itself not go into Deep Sleep. Note that there is a register bit that can prevent the Switch from going into Deep Sleep if this is desired by the user.

A sleep handshake may be aborted if Register 3.8702.4 is set. If a sleep request is received when the PHY and its copper link partner have link up, then the PHY will send an LPS to the link partner and try to initiate a sleep handshake. If link is not up and the PHY is not in a low power state then the PHY will wait for link to be up before sending the sleep request (LPS). The wait time is 195 ms by default. After this time the sleep request in dropped.

Sleep Handshake

The sleep handshake scheme between the 88Q1110/88Q1111 device and a connected Switch is used when the sleep handshake is initiated, completed, and the LPSD logic removes power.

1. The 88Q1110/88Q1111 device sends a command to the Switch to tell the Switch to stop TX traffic. The command to do this is “PHY Sleep in Progress”.
2. Once the Switch receives this command, the Switch immediately stops TX traffic if no packet is being sent or as soon as the current packet finishes (i.e., if there is one being transmitted).
3. If the TX traffic has stopped, the 88Q1110/88Q1111 device will be able to complete the sleep handshake after both the 88Q1110/88Q1111 device and its LP go into the SLEEP_SILENT state. After this, the 88Q1110/88Q1111 device and its LP go into the T1 Port Sleep Mode.
4. If the TX traffic has not stopped from the Switch, or activity from the LP has not stopped while the 88Q1110/88Q1111 device and LP are in the SLEEP_SILENT state, then the sleep request fails.
5. If the sleep handshake has completed, then the 88Q1110/88Q1111 device tells the Switch that it is sleeping and ready to have power removed by the LPSD circuit if confirmed by the Switch. One of these two commands is sent:
   a) A command called “PHY Sleep Complete Remote” is sent if the sleep request was sent in from the LP. This tells the Switch that the sleep request should be forwarded to the other ports that the Switch logic indicates should receive forwarded sleep commands.
   b) A command called “PHY Sleep Complete Local” is sent if the sleep request was sent in from the Switch. This command indicates that the Switch should not forward the sleep request since it initiated it.
6. If the sleep request is aborted or failed, then a different embedded command called “PHY Sleep Aborted or Failed” is forwarded to the Switch.
7. When the “PHY Sleep In Progress” command is received from the PHY, the Switch starts a timer that expires after 20 ms. If there is no “PHY Sleep Aborted or Failed” or “PHY Sleep Completed Local/Remote” command sent from the PHY after 20 ms, then the Switch should stop the flow control. This is added for safety reasons to prevent flow control (and the prevention of TX packets from being sent) from being stuck indefinitely.
8. If the sleep handshake is aborted or failed but the “Sleep Aborted or Failed” command is not seen by the Switch and the link is still up, then traffic should be allowed to pass.
9. If the sleep handshake is completed and the “Sleep Complete Remote/Local” command is not seen by the Switch then after 20 ms, the Switch will no longer expect this command. The link should drop and this will prevent the traffic from flowing.
10. If a wake request comes in when the PHY is in SLEEP SILENT state, then the sleep handshake is failed and a “Sleep Aborted or Failed” command is sent and sleep is terminated. If the wake request comes during a state after the SLEEP SILENT state, then the wake request is processed normally.
11. If the sleep handshake is finished and one of the two commands in #5 has been sent to the Switch, then the Switch will send the command “Switch Power Removal Request” to the 88Q1110/88Q1111 device to communicate “drop INH” and remove power (which must happen

within another 8 ms) if the Switch is OK with this power removal. Once started, the command sequence for power removal can be interrupted by a wake request regardless of what is seen at the Host interfaces. If the 88Q1110/88Q1111 device is able to initiate an LPSD power removal, and once the device is in the LPSD Deep Sleep Mode, only a pulse sent into the WAKE_IN pin for a local wake up or activity on the copper media side (Analog receiver) for a remote wake up can wake up the 88Q1110/88Q1111 device. Anything else getting power from a regulator controlled by the 88Q1110/88Q1111 device INH output also will wake up. Note that a local or remote wakeup may be disabled by programming the corresponding register bits in the 3.87xx space in the PHY:

- 3.8701.12 disables the LPSD Local Wake Up
- 3.8701.11 disables the LPSD Remote Wake Up

12. If the Switch is not OK with power removal, it will not send the “Switch Power Removal Request” command. The 88Q1110/88Q1111 device and its LP stay in the T1 Port Sleep Mode. For example, if a wake request is seen if from any source, then the Switch cannot initiate an LPSD power removal.
13. The Switch cannot force a power removal before either the sleep handshake finishes or the sleep handshake has failed.
14. By default, the 88Q1110/88Q1111 device does not get itself out of the T1 Port Sleep Mode.
15. One of the following actions must be done to get the 88Q1110/88Q1111 device out of the T1 Port Sleep Mode if desired:

    a) The 88Q1110/88Q1111 device Wake Request register bit is written to by the Switch.
    b) The Switch can send the “Switch Wake Request” command to have the 88Q1110/88Q1111 device wake up from the T1 Port Sleep Mode.
    c) A pulse can be sent in the WAKE_IN pin.

After power is reapplied, the Switch automatically sends wake requests to whatever ports are designated to have these requests forwarded to them; however, if the PHY receives a remote wake request from the copper media side or from a register bit setting, then the PHY must send a wake request to the Switch and the Switch needs to relay this according to its forwarding logic.

The Switch can enable flow control after it has power reapplied. Link toggling from 0 to 1 tells the Switch that it can send traffic to the PHY TX side. If link drops, then flow control is enabled; therefore, flow control may be enabled by the Switch when it receives a “Sleep in Progress” command or when link goes down.

2.5.1.3 Wake from Sleep

As an IEEE and OPEN Alliance TC10 compliant 100Base-T1 Ethernet PHY, the 88Q1110/88Q1111 supports wake-up using a Wake-up Pulse (WUP) or supports using a Wake-up Request (WUR) to notify others to potentially wake up Devices further within a network.

Wake-up

The 88Q1110/88Q1111 can be woken up by a local wake-up pin, a wake-up request command or a wake-up pulse from link partner. Upon detection, a wake-up interrupt may be generated, and the wake-up source is flagged in the Wake-up Status Register. The source bits are cleared when device is in reset mode.

Local Wake-up

When the Device is in low power mode, a positive pulse presented at the WAKE_IN pin meeting the minimum duration time ($t_{localwkup}$) triggers a local wake-up.

Remote Wake-up Indication During Link-up by Wake-Up Request (WUR)

A WUR command is encoded in the scrambler stream as defined in Section 7.3 of OPEN TC10 Sleep/Wake-up Specification when a wake request is received after link up and therefore Device is not in a low power mode. A minimum of 64-bits of Wake-up Request encoded idles are needed for a successful detection and passing of the wake request to the other parts of the network.

Remote Wake-up by Wake-Up Pulse (WUP)

WUP are link training codes transmitted from the link partner over a passive link. The activity on the MDI lines will be detected as a remote wake-up. The wake-up pulse has a duration of 1ms (+/- 0.3ms) to allow for a reliable detection.

Low Power Sleep

Low Power Sleep (LPS) is encoded in the scrambler stream as defined in Section 7.3 of OPEN Sleep/Wake-up Specification. 64 bits of LPS encoded idles must be sent for a sleep request to be successfully detected by the link partner.

In-band WUP, WUR and LPS Commands

Optionally, wake-up request commands and low power sleep commands may be embedded into the RGMII and SGMII interface if such a feature is enabled through register write.

WUP are link training codes transmitted from the link partner over a passive link. The activity on the MDI lines will be detected as a remote wake-up. The wake-up pulse has a duration of 1ms (+/- 0.3ms) to allow a reliable detection.

In-band command and status feature is disabled upon initial network power up or if it was not enabled before going to sleep.

TC10 Sleep/Wake-up Enable

The TC10 Sleep/Wake-up feature for the Device is enabled via the configuration pin. If the RCLK pin floats an internal pull-up will enable this feature. An external pull-down will disable the feature.

Enabling Wake Sources out the GPIO Pin

Register 4.821B.0 as shown in Table 37, enables the Wake source requests. The 88Q1110/88Q1111 device can output wake requests from various sources as described in Table 38.

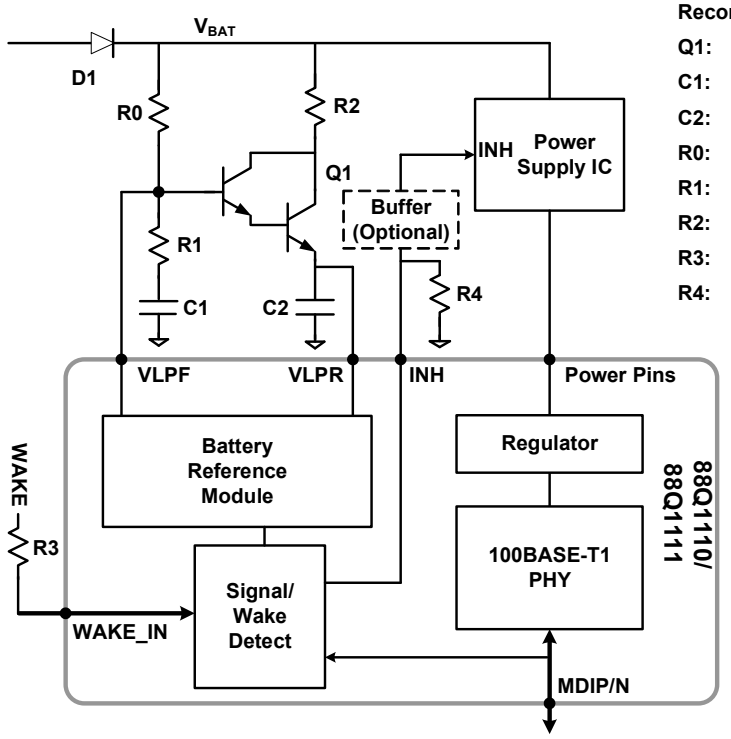
Table 37: GPIO Control Register for Wake Sources
Device 4, Register 0x821B

Bits	Field	Mode	HW Rst	SW Rst	Description
0	Enable the selected wake source to the GPIO Pin	R/W	0x0	Retain	1 = Bring out the selected wake source to the GPIO pin

Table 38: Wake Sources

Source	Register to Enable	Description of Source
WAKE_REQ register	4.FD20.8	The register bit that when written to requests a wake.
LPSD_LOCAL_WAKE	4.FD20.6	The wake status from the Analog when the WAKE_IN pin is asserted during Deep Sleep.
LPSD_LOCAL_WAKE_ RAW	4.FD20.4	The wake status from the Analog when the WAKE_IN pin is asserted during the T1 Port Sleep Mode.
WAKE_FWD	4.FD20.7	The wake request that is forwarded from a connected Switch via the Host side.
LPSD_REMOTE_WAKE/ SDET	4.FD20.5	The wake request from the Link Partner at the line side when link is down and the DUT is sleeping in Deep Sleep or T1 Port Sleep Mode.
WUR_RECV	4.FD20.3	The wake request from the Link Partner at the line side when link is up.

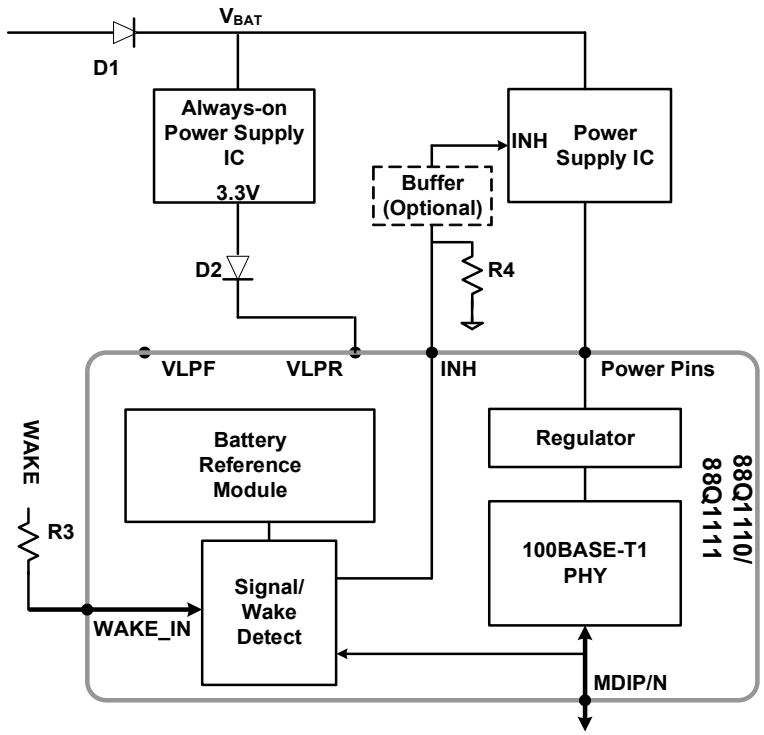
Figure 17: LPSD Block Diagram - V_{BAT} Option 1



Recommended components:

Q1:	BCV47 (NPN)
C1:	2.7 nF
C2:	2.2 uF
R0:	2 Mohm
R1:	100 kohm
R2:	200 ohm
R3:	25 kohm (not needed if WAKE VIH ≤ 3.3V)
R4:	10 kohm

Figure 18: LPSD Block Diagram - V_{BAT} Option 2



Recommended components:

R3: 25 kohm

R4: 10 kohm

Electrical Characteristics

Table 39: LPSD Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{BAT}	Battery Voltage	--	6	12	28	V
$I_{STANDBY}$	Standby current	Battery voltage = 12V[1]	--	--	35	µA
$T_{MDI,LAT}$	Latency from MDI signals to INH assertion	Normal link	--	--	20	µs
$T_{WAKE,PW}$	WAKE_IN Pin Pulse Width to wake-up LPSD	--	30[2]	--	--	µs
I_{INH}	INH Pin Source Current	--	--	--	0.4	mA
V_{INH}	INH Pin Output High Voltage	--	2.0	--	3.63	V

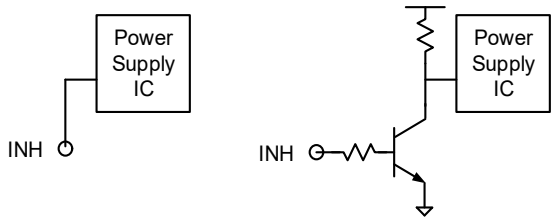
1. Current will be higher for battery voltages above 12V (e.g., up to 45 uA for 24V battery voltage)
2. = Default value.

Application Notes

- WAKE_IN voltage level:
  a) WAKE_IN can be directly driven up to a nominal 3.3V level.
  b) WAKE_IN can be driven to battery supply level through a series 25 kΩ resistor.
- INH output:
  Power supply IC EN/INH pin can be driven by 88Q1110/88Q1111 INH pin in typical cases. For example configurations, see Figure 19.

  If on-chip regulator not used, INH output needs to control EN input of all power supply ICs that power the device.

Figure 19: INH Output Example Configurations



Active (power on) High – Output high level at 2.0V – 3.63V @ < 0.4mA load

Active (power on) Low

- Wake-up application scenarios – four cases of wake-up schemes can be supported:
  - Case 1: Local wake-up and remote wake-up.
    WAKE_IN from host controller. 3.3V or VBAT level can be accepted.
    For VLPR, VLPF, and INH, see Figure 17 and Figure 18.
  - Case 2: No local wake-up. Remote wake-up support.
    WAKE_IN = VSS. For VLPR, VLPF, and INH, see Figure 17 and Figure 18.
    Or use case 1 configuration, but use registers to program.
  - Case 3: Local wake-up only. No remote wake-up.
    Use case 1 configuration. Use register programming to disable remote wake-up.
  - Case 4: No local wake-up. No remote wake-up.
    WAKE_IN = VSS or NC. VLPR, VLPF, and INH = NC.

2.6 Status of Functional Blocks in Each Device Mode

Table 40: Status of Functional Block in Each Mode

Functional Block Pin(s)	Reset	Standby/ Fail-safe	Normal Operation	Open Alliance Sleep[1]	IEEE Copper Power Down	IEEE SGMII Power Down
MDI	Off	Off	On	Off[2]	Off	On
RGMII/MII/RMII	Off	Off	On	Off	On	On
SGMII	Off	Off	On	Off	On	Off
Crystal	On	On	On	Off	On	On
Regulator	On	On	On	Off	On	On
RESETn	On	On	On	Off	On	On
MDC/MDIO	Off	On	On	Off	On	On
TX_DISABLE	Off	Off	On	Off	Off	On
WAKE_IN	Off	Off	On	On	Off	On
INH	On	On	On	On	On	On
INTn	Off	Off	Off	Off	Off	Off

1. This mode is the Power Removed LPSD Deep Sleep mode.
2. Only remote wake-up function is available.

2.7 Wake on Lan (WOL) Event Detection

The device supports the detection and reporting of Wake On LAN (WOL) events. There are two types of events:

- Magic Packet Event
- Link Change Event

WOL related registers are grouped in 4.8215 to 4.8219. (Table 183 to Table 187).

Register 4.8213.15 indicates whether any of the events have been detected or not. If 4.8213.15 = 1, then at least one of the two types of events have been detected. Setting 4.8212.15 to 1 will enable an interrupt to be generated which can be sent out the INTn pin.

2.7.1 Magic Packet Event

If any of the frames received by the device contain 6 bytes of FF followed by 16 iterations of the destination address programmed in Register 4.8217, 4.8218, and 4.8219, then such a frame is considered to be a Magic Packet and a Magic Packet Event has happened. Magic Packet detection can be enabled/disabled by 4.8215.14. Register 4.8216.14 will be set to 1 when a Magic Packet Event has happened and can be cleared by setting 4.8215.12.

2.7.2 Link Change Event

If the link status changes from link down to up, then a Link Change Event has happened. This detection can be enabled/disabled by 4.8215.13. Register 4.8216.13 will be set to 1 when a Link Change Event has happened and can be cleared by setting 4.8215.12 to 1.

2.8 Advanced Virtual Cable Tester®

The device's Advanced VCT feature uses time domain reflectometry (TDR) to determine the quality of the cables, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. The device transmits a signal of known amplitude (+1V) down the single pair of an attached cable. It will conduct the cable diagnostic test on MDIP/N. The transmitted signal will continue down the cable until it reflects off of a cable imperfection.

The VCT test is initiated by setting register 3.8517.15 to 1. This bit will self clear when the test is completed. Register 3.8517.14 will be set to a 1 indicating that the TDR results in the registers are valid.

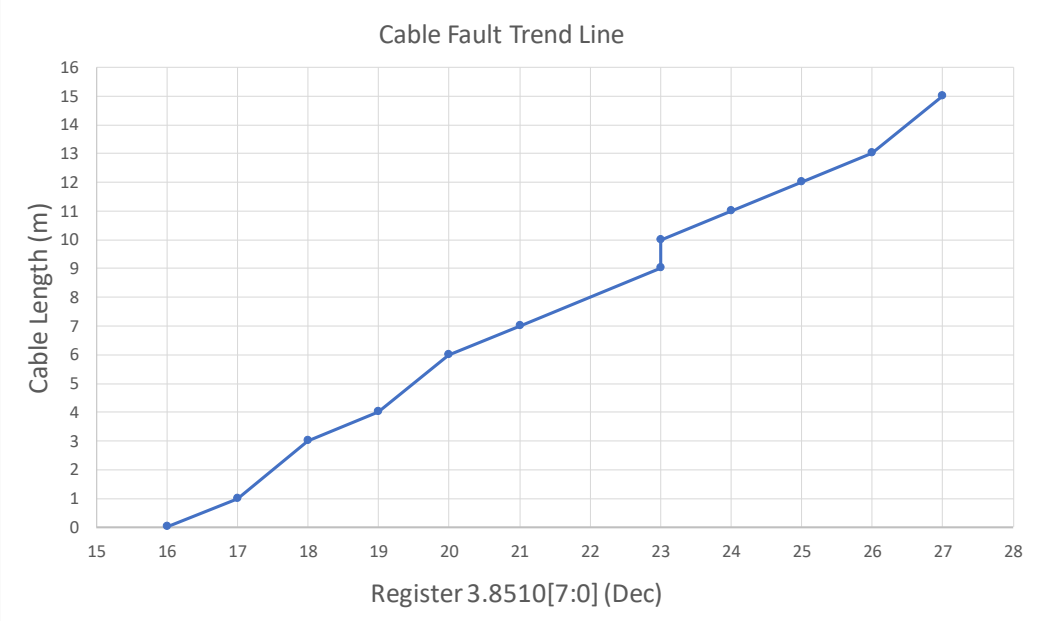
Each time the VCT test is enabled, the results seen on the single channel are reported in register 3.8510.

2.8.1 Maximum Peak

The Maximum Peak method is used for TDR testing. For this method, the maximum peak above a certain threshold is reported. Pulses are sent out.

The results are stored in register 3.8510. Bits 7:0 report the distance of the peak. The distance can be converted to using the trend line in Figure 20. Bits 14:8 report the reflected amplitude. Bit 15 reports whether the reflected amplitude was positive or negative. When bits 15:8 return a value of 0x80, it means there was no peak detected above the threshold. If bits 15:8 return a value of 0x00 then the test failed.

Figure 20: TDR Trend Line



If 3.8510.15 is 1, this indicates the cable is open, otherwise if 3.8510.15 is 0, this indicates the cable is shorted. If the TDR test fails, it might be caused by 1 wire of a twisted pair being cut. To diagnose this case, set 3.851D.15 = 1 and run the TDR test again to check if there is an open on one wire of the pair.

2.8.2 Pulse Amplitude and Pulse Width

The transmitted pulse amplitude and pulse width can be adjusted via registers 3.851C.9:8 and 3.851C.11:10 respectively. They should normally be set to full amplitude and full pulse width.

2.8.3 Drop Link

When register 3.851C.12 is set to 0 the circuit will wait 1.5 seconds to break the link before starting VCT™. When set to 1 this delay is bypassed.

2.9 Packet Generator and Packet Checker

2.9.1 CRC Error Counter and Packet Counter

The cyclic redundancy check (CRC) counter and packet counters, normally found in MACs, are available in the device. The error counter and packet counter features are enabled through register writes, and each counter is stored in eight register bits.

To enable the counters to count, set register 3.8610.4 to a one.

To read the CRC counter and packet counter, read register:

- 3.8614 (Packet count is stored in these bits)
- 3.8615 (CRC error count is stored in these bits)

The CRC counter and packet counter do not clear on a read command. To clear the counters, write register 3.8612. 4 = 1 (this bit is a self-clear bit). Disabling the counters by writing register 3.8610.4 = 0 will also reset the counters.

2.9.2 Packet Generator

The device contains a very simple packet generator. Write to register 3.8610.3 to enable the packet generator.

Once enabled, fixed length packets of 64 or 1518 bytes (including CRC) will be transmitted, separated by 12 bytes of inter-packet gap (IPG).The preamble length will be 8 bytes. The payload of the packet is either a fixed 5A, A5, 5A, A5 pattern, a pseudo random pattern, or a constant payload of 0 or 1. A correct IEEE CRC is appended to the end of the packet. An error packet can also be generated.

The registers are as follows:

- 3.8610.2 Payload Type
  - 0 = Pseudo random
  - 1 = Fixed 5A, A5, 5A, A5, …
- 3.8610.1 Packet Length
  - 0 = 64 bytes
  - 1 = 1518 bytes
- 3.8610.0 Error Packet
  - 0 = Good CRC
  - 1 = Symbol error and corrupt CRC
- 3.8611 Packet Burst Size
  - 0x0000 = Continuous
  - 0x0001 to 0xFFFF = Burst 1 to 65535 packets
- 3.8613.15 Packet Generator Constant Payload Enable
  - 1 = Payload of packet is controlled by register 3.8613.14 when packet generator is enabled
  - 0 = Payload of packet is controlled by register 3.8610.2 when packet generator is enabled
- 3.8613.14 Packet Generator Constant Payload Value
  - 1 = All 1s in the payload when register 3.8613.15 = 1
  - 0 = All 0s in the payload when register 3.8613.15 = 1

2.10 Automatic Polarity Detection and Correction

The device, when configured as SLAVE in 100BASE-T1 mode, has the capability to automatically detect the polarity on the receive side when a polarity swap is observed. In addition to this, when a polarity flip is observed, it will also invert the polarity on its transmit side if this is enabled.

If 100BASE-T1 link is established, then register 3.8009.1 records the real time status of the polarity.

3.8009.1 Polarity (real time)

1 = Reversed

0 = Normal

Polarity correction feature is disabled by default and can be enabled by programming register 3.8000.9 to 1.

2.11 Link Disconnect Counter

The link disconnect counter increments every time the link transitions from up to down. 3.8020.7:0 is used as the counter. It clears on read and will not roll over when it reaches 0xFF.

2.12 GPIO

The GPIO and TX_ENABLE pins can be used for GPIO functionality. Registers 3.8302 to 3.8312 control the operation of the GPIO/TX_ENABLE pins. Register 3.8304.11 is used to configure the GPIO pin for GPIO functionality and register 3.8304.3 is used to program the TX_ENABLE pin for GPIO functionality. These register bits should be programmed to 1 in order to configure the respective pin for GPIO functionality. Register bits 3.8303.0 and 3.8303.1 control the direction of these pins. When they are programmed to 0, these pins are used as input pin. Otherwise, these are used as output pins.

When the GPIO/TX_ENABLE pins are in input mode, the register bits 3.8302.1:0 can be used to read the state of these pins. 3.8302.1 indicates the state of the TX_ENABLE pin, and 3.8302.0 indicates the state of the GPIO pin. In input mode, an interrupt can also be generated depending on the value of the GPIO/TX_ENABLE pins. Registers 3.8304.10:8 and 3.8304.2:0 can be used to select when an interrupt should be generated. The interrupt status is stored in register 3.8301.1:0.

When the GPIO/TX_ENABLE pins are configured in output mode, register bits 3.8302.1:0 are used to drive the state of these pins. The value written to the 3.8302.1 register bit will be driven on the TX_ENABLE pin, and the value written to the 3.8302.0 register bit will be driven on the GPIO pin. By default the GPIO pin is programmed to be used for LED functionality.

2.13 LED

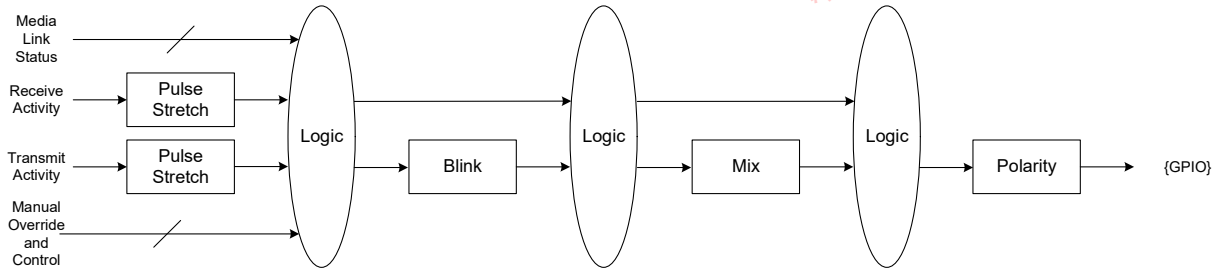
The TX_ENABLE and GPIO pins can be used to drive LED. Register 3.8304.11 is used to program the GPIO pin for LED functionality, and by default the GPIO pin is programmed for LED functionality. Register 3.8304.3 is used to program the TX_ENABLE pin for LED functionality. These register bits should be programmed to 0 in order to configure the respective pin for LED functionality.

In general, 3.8310.7:4 controls the LED functionality for the GPIO pin, and 3.8310.3:0 controls the LED functionality for the TX_ENABLE pin. These are referred to as single LED modes.

However, there are some LED modes where the GPIO and TX_ENABLE pins operate as a unit. These are entered when 3.8310.3:2 are set to 11. These are referred to as dual LED modes. In dual LED modes, register 3.8310.7:4 have no meaning when 3.8310.3:2 are set to 11.

Figure 21 shows the general chaining of function for the LEDs. The various functions are described in the following sections.

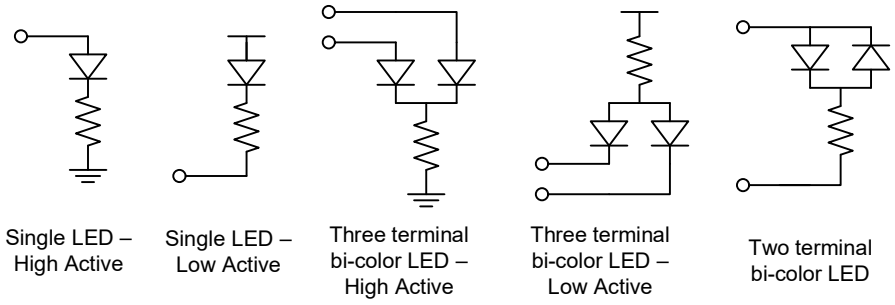
Figure 21: LED Chain



2.13.1 LED Polarity

There are a variety of ways to hook up the LEDs. Some examples are shown in Figure 22. In order to make things more flexible, registers 3.8311.3:2 and 3.8311.1:0 specify the output polarity for the LEDs. The lower bit of each pair specifies the On (active) state of the LED, either high or low. The upper bit of each pair specifies whether the Off (inactive) state of the LED should be driven to the opposite level of the On state or Hi-Z.

Figure 22: Various LED Hookup Configurations



2.13.2 Pulse Stretching and Blinking

Register 3.8312.14:12 specifies the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require blinking instead of a solid on. Register 3.8312.10:8 specifies the blink rate. Note that the pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse.

The stretched/blinked output will then be mixed if needed (for details, see Section 2.13.3) and then inverted/Hi-Z according to the polarity described in Section 2.13.1.

2.13.3 Bi-Color LED Mixing

In the dual LED modes, the mixing function allows the two colors of the LED to be mixed to form a third color. Register 3.8311.15:12 controls the amount to mix in the GPIO pin. Register 3.8311.11:8 controls the amount to mix in the TX_ENABLE pin. The mixing is determined by the percentage of time the LED is on during the active state. The percentage is selectable in 12.5% increments.

Note that there are two types of bi-color LEDs. There is the three terminal type and the two terminal type. For example, the third and fourth LED block from the left in Figure 22 illustrate three terminal types, and the one on the far right is the two terminal type. In the three terminal type, both of the LEDs can be turned on at the same time. Hence the sum of the percentage specified by 3.8311.15:12 and 3.8311.11:8 can exceed 100%. However, in the two terminal type the sum should never exceed 100% since only one LED can be turned on at any given time.

The mixing only applies when register 3.8310.3:0 are set to 11xx. There is no mixing in single LED modes.

2.13.4 Modes of Operation

The GPIO/TX_ENABLE pins relay some modes of the PHY so that these modes can be displayed by the LEDs. Most of the single LED modes are self-explanatory from the register map. The non-obvious ones are covered in this section.

2.13.4.1 Compound LED Modes

Compound LED modes are defined in Table 41.

Table 41: Compound LED Status

Compound Mode	Description
Activity	Transmit Activity OR Receive Activity

2.13.4.2 Speed Blink

When 3.8310.3:0 is set to 0010, the TX_ENABLE pin takes on the following behavior.

The TX_ENABLE pin outputs the sequence shown in Table 42, depending on the status of the link. The sequence consists of eight segments. If a 100 Mbps link is established, the TX_ENABLE pin outputs 2 pulses, and no link 0 pulses. The sequence repeats over and over again indefinitely.

The odd numbered segment pulse duration is specified in register 3.8312.1:0. The even numbered pulse duration is specified in register 3.8312.3:2.

Table 42: Speed Blinking Sequence

Segment	100 Mbps	No Link	Duration
1	On	Off	3.8312.1:0
2	Off	Off	3.8312.3:2
3	On	Off	3.8312.1:0
4	Off	Off	3.8312.3:2
5	Off	Off	3.8312.1:0
6	Off	Off	3.8312.3:2
7	Off	Off	3.8312.1:0
8	Off	Off	3.8312.3:2

Table 43: Speed Blink

Register	Pin	Definition
3.8312.3:2	Pulse Period for Even Segments	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
3.8312.1:0	Pulse Period for Odd Segments	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

2.13.4.3 Manual Override

When registers 3.8310.7:6 and 3.8310.3:2 are set to 10, the LEDs are manually forced. Registers 3.8310.5:4 and 3.8310.1:0 then select whether the LEDs are to be on, off, Hi-Z, or blink.

If bi-color LEDs are used, the manual override will select only one of the two colors. In order to get the third color, mixing MODE 1 and MODE 2 should be used (Section 2.13.4.4).

2.13.4.4 MODE 1, MODE 2, MODE 3, MODE 4

MODE 1 to 4 are dual LED modes. These are used to mix to a third color using bi-color LEDs.

When 3.8310.3:0 is set to 11xx, then one of the four modes are enabled:

- MODE 1 – Solid mixed color.
  The mixing is discussed in Section 2.13.3.
- MODE 2 – Blinking mixed color.
  The mixing is discussed in Section 2.13.3. The blinking is discussed in section Section 2.13.2.
- MODE 3 – Behavior according to Table 44.
- MODE 4 – Behavior according to Table 45.

Table 44: MODE 3 Behavior

Status	GPIO	TX_ENABLE
100 Mbps Link – No Activity	Solid Mix	Solid Mix
100 Mbps Link – Activity	Blink Mix	Blink Mix
No Link	Off	Off

Table 45: MODE 4 Behavior

Status	GPIO	TX_ENABLE
100 Mbps Link – No Activity	Solid On	Off
100 Mbps Link – Activity	Blink	Off
No Link	Off	Off

2.14 Synchronous Ethernet (SyncE) Clock

The GPIO pin can output a 25 MHz SyncE clock that can be used to clock other digital logic. This clock should not be used as an input to devices that require a higher quality clock.

Register 3.8000.6 is used to enable/disable the SyncE clock output on the GPIO pin. When 3.8000.6 is 1, the GPIO pin is used to output the SyncE clock. When 3.8000.6 is 0, the GPIO pin is used for GPIO/LED functionality. The default value of 3.8000.6 is 0 on power on reset or hardware reset.

2.14.1 Hardware Reset State

When hardware reset is asserted, the SyncE clock will not be output.

2.15 Interrupt

Interrupt function is brought out to the chip's INTn pin. Register 3.8312.11 selects the polarity of the interrupt signal when it is active, where 3.8312.11 = 1 means it is active low and 3.8312.11 = 0 means it is active high.

Registers 3.8012 and 3.8212 are the Interrupt Enable registers for the copper media.

Registers 3.8013 and 3.8213 are the Interrupt Status registers for the copper media.

Registers 3.8300 and 3.8301 are the Interrupt Enable and the Interrupt Status registers for the GPIO functionality of the GPIO/TX_ENABLE pins.

Register 4.8212 is the Interrupt Enable register for the Host side.

Register 4.8213 is the Interrupt Status register for the Host side.

There are force and polarity bits for INTn pin. See Table 46. By default, the INTn pin is tristated. This can be disabled by programming Register 3.8305.4 to 1.

Table 46: Interrupt Control

Register	Function
3.8312.15	Force Interrupt
3.8312.11	Set Polarity

2.16 Manual Impedance Calibration

Manual NMOS and PMOS settings are available. If the printed circuit board (PCB) traces are different from 47.3Ω, the output impedance of the MAC interface I/O buffers can be programmed to match the trace impedance. Users can adjust the NMOS and PMOS driver output strengths to perfectly match the transmission line impedance and eliminate reflections completely.

2.16.1 Manual Settings to the Calibration Registers

To use manual calibration, write to the following registers:

Write to register 4.8001.11:8 = b'PPPP and register 4.8001.7:4 = b'NNNN to adjust the PMOS and NMOS fingers accordingly, where

- PPPP is the 4-bit value for the PMOS strength.
- NNNN is the 4-bit value for the NMOS strength.

PPPP or NNNN will depend on the PCB used. A value of 1111 enables all the fingers for maximum drive strength and for minimum impedance. A value of 0000 turns all fingers off for minimum drive strength and for maximum impedance. Figure 23 shows an example of a signal output that needs to be cleaned up. Through manual calibration, the reflections can be eliminated as shown in Figure 24.

Figure 23: Signal Reflections, Using the 50Ω Setting, 60Ω Line

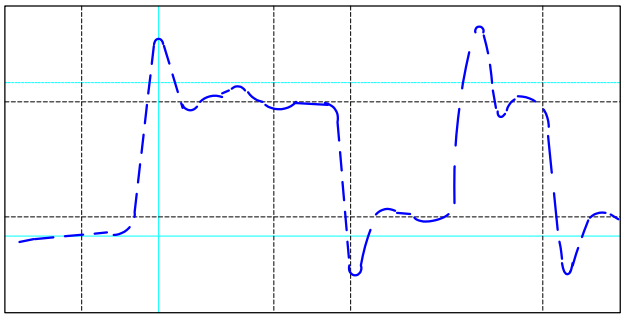
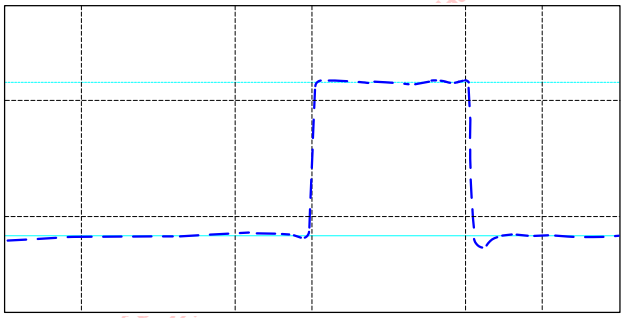


Figure 24: Clean Signal after Manual Calibration for the 60Ω



2.17 Configuring the 88Q1110 Device

The device can be configured in two ways:

- Hardware configuration strap options (unmanaged applications)
- MDC/MDIO register writes (managed applications)

The Master/Slave configuration bits can be overwritten by software. PHYAD, RGMII/RMII/MII cannot be overwritten.

2.17.1 Hardware Configuration

After the de-assertion of RESETn, the device will be hardware configured.

The device is configured through the GPIO, RXD[3:0], RXC, and RCLK pins as shown in the Table 47.

Table 47: 88Q1110 Configuration Pin Mapping

Configuration	88Q1110 Pin	Sampled Bit Definition	Register Affected	Pull-Up in Pad
PHYADR[0]	RXD[0]	PHYAD bit 0	None	Yes
PHYADR[1]	RXD[1]	PHYAD bit 1	None	Yes
PHYADR[2]	GPIO	PHYAD bit 2	None	Yes
Master/Slave Configuration	RXD[2]	Auto-Negotiation Off 0 - Master 1 - Slave	1.0834.14, 7.0202.12	Yes
Mode	{RXC, RXD[3]}	11 - MII 10 - RGMII mode 1 01 - RMII 00 - RGMII mode 2	None	Yes
TC10 Sleep/Wake-up	RCLK	0 - Disable the TC10 Sleep/Wake-up feature 1 - Enable the TC10 Sleep/Wake-up feature	3.8707.0	Yes

The RXD[0], RXD[1], and GPIO pins are used to configure PHYAD[0], PHYAD[1], and PHYAD[2], respectively. For a PHYAD of 0, these pins should be left floating. In order to configure a 1 on the PHYAD[0]/PHYAD[1]/PHYAD[2] bits, the corresponding RX*/GPIO pins must have a pull-down resistor (4.7 kΩ) added to them externally. The mapping is shown in Table 48.

Table 48: {GPIO, RXD[1:0]} to PHYAD[2:0] Mapping for Configuration

GPIO Pin	RXD[1] Pin	RXD[0] Pin	PHYAD[2:0] Value
Unconnected	Unconnected	Unconnected	000
Unconnected	Unconnected	4.7 kΩ Pull-Down Resistor	001
Unconnected	4.7 kΩ Pull-Down Resistor	Unconnected	010
Unconnected	4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	011
4.7 kΩ Pull-Down Resistor	Unconnected	Unconnected	100

Table 48: {GPIO, RXD[1:0]} to PHYAD[2:0] Mapping for Configuration (Continued)

GPIO Pin	RXD[1] Pin	RXD[0] Pin	PHYAD[2:0] Value
4.7 kΩ Pull-Down Resistor	Unconnected	4.7 kΩ Pull-Down Resistor	101
4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	Unconnected	110
4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	111

The RXD[2] pin is used to configure the Master/Slave Configuration. The configuration value is set depending on what is connected to the RXD[2] pin soon after the de-assertion of hardware reset. The mapping is shown in Table 49.

Table 49: RXD[2] Mapping for Configuration

RXD[2]/CONFIG5 Pin	Value	Configuration Definition
Unconnected	1	Slave
4.7 kΩ Pull-Down Resistor	0	Master

The RXC and RXD[3] pins are used to configure the system interface in RGMII/MII/RMII mode. The configuration value is set depending on what is connected to the RXC and RXD[3] pins soon after the de-assertion of hardware reset. The mapping is shown in Table 50. The 88Q1110 device supports four RGMII timing modes. RGMII timing modes 1 and 2 are configured directly via the configuration pins.

Table 50: RXC and RXD[3] Mapping for Configuration

RXC	RXD[3] Pin	Value	Configuration Definition
4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	00	RGMII Mode 2
4.7 kΩ Pull-Down Resistor	Unconnected	01	RMII
Unconnected	4.7 kΩ Pull-Down Resistor	10	RGMII Mode 1
Unconnected	Unconnected	11	MII

RGMII Mode 1

TCLK transitions the same time as TXD/TXC. Rx clock transitions when RXD/RXC is stable.

RGMII Mode 2

TCLK transitions when TXD/TXC is stable. Rx clock transitions when RXD/RXC is stable.

The RCLK pin is used to configure the TC10 Sleep/Wake-up feature in the device either when the chip powers up or after hardware reset. The configuration value is set depending on what is connected to the RCLK pin soon after the deassertion of hardware reset. The mapping is shown in Table 51. Once the chip is in the TC10 Sleep/Wake-up mode via this configuration pin, a write of 0 to register 3.8707.0 takes the chip out of TC10 Sleep/Wake-up mode and enables normal operation. A write of 1 to this register bit reenables the TC10 Sleep/Wake-up feature.

Table 51: RCLK Mapping for Configuration

RCLK	Value	Configuration Definition
Unconnected	1	Enable the TC10 Sleep/Wake-up feature
4.7 kΩ Pull-Down Resistor	0	Disable the TC10 Sleep/Wake-up feature.

2.18 Configuring the 88Q1111 Device

The device can be configured in two ways:

- Hardware configuration strap options (unmanaged applications)
- MDC/MDIO register writes (managed applications)

The Master/Slave configuration bits can be overwritten by software. PHYAD cannot be overwritten.

2.18.1 Hardware Configuration

After the de-assertion of RESETn, the device will be hardware configured.

The device is configured through the GPIO, CONFIG3, CONFIG4, CONFIG5, and CONFIG1 pins as shown in the Table 52.

Table 52: 88Q1111 Configuration Pin Mapping

Configuration	88Q1111 Pin	Sampled Bit Definition	Register Affected	Pull-Up in Pad
PHYADR[0]	CONFIG3	PHYAD bit 0	None	Yes
PHYADR[1]	CONFIG4	PHYAD bit 1	None	Yes
PHYADR[2]	GPIO	PHYAD bit 2	None	Yes
Master/Slave Configuration	CONFIG5	Auto-Negotiation Off 0 - Master 1 - Slave	1.0834.14, 7.0202.12	Yes
TC10 Sleep/Wake-up	CONFIG1	0 - Disable the TC10 Sleep/Wake-up feature 1 - Enable the TC10 Sleep/Wake-up feature	3.8707.0	Yes
Reserved	CONFIG2, CONFIG6	The sampled value must be 10, so the CONFIG2 pin must be floating and the CONFIG6 pin must have a pull-down added.	None	Yes

The CONFIG3, CONFIG4, and GPIO pins are used to configure PHYAD[0], PHYAD[1], and PHYAD[2], respectively. For a PHYAD of 0, these pins should be left floating. In order to configure a 1 on the PHYAD[0]/PHYAD[1]/PHYAD[2] bits, the corresponding CONFIG*/GPIO pins must have a pull-down resistor (4.7 kΩ) added to them externally. The mapping is shown in Table 53.

Table 53: {GPIO, CONFIG[4:3]} to PHYAD[2:0] Mapping for Configuration

GPIO Pin	CONFIG4 Pin	CONFIG3 Pin	PHYAD[2:0] Value
Unconnected	Unconnected	Unconnected	000
Unconnected	Unconnected	4.7 kΩ Pull-Down Resistor	001
Unconnected	4.7 kΩ Pull-Down Resistor	Unconnected	010
Unconnected	4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	011
4.7 kΩ Pull-Down Resistor	Unconnected	Unconnected	100
4.7 kΩ Pull-Down Resistor	Unconnected	4.7 kΩ Pull-Down Resistor	101
4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	Unconnected	110
4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	111

The CONFIG5 pin is used to configure the Master/Slave Configuration. The configuration value is set depending on what is connected to the CONFIG5 pin soon after the de-assertion of hardware reset. The mapping is shown in Table 54.

Table 54: CONFIG5 Mapping for Configuration

CONFIG5 Pin	Value	Configuration Definition
Unconnected	1	Slave
4.7 kΩ Pull-Down Resistor	0	Master

The CONFIG2 and CONFIG6 pins are not used for configuration; however, the CONFIG2 pin must be floating and the CONFIG6 pin must have a pull-down added. The CONFIG1 pin is used to configure the TC10 Sleep/Wake-up feature in the device either when the chip powers up or after hardware reset. The configuration value is set depending on what is connected to the CONFIG1 pin soon after the deassertion of hardware reset. The mapping is shown in Table 55. Once the chip is in the TC10 Sleep/Wake-up mode via this configuration pin, a write of 0 to register 3.8707.0 takes the chip out of TC10 Sleep/Wake-up mode and enables normal operation. A write of 1 to this register bit reenables the TC10 Sleep/Wake-up feature.

Table 55: CONFIG1 Mapping for Configuration

RCLK	Value	Configuration Definition
Unconnected	1	Enable the TC10 Sleep/Wake-up feature
4.7 kΩ Pull-Down Resistor	0	Disable the TC10 Sleep/Wake-up feature.

2.18.2 Software Configuration – Management Interface

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3u Clause 45 MDIO protocol. MDC is the management data clock input, and it can run from DC to a maximum rate of 12.5 MHz. At high MDIO fanouts, the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO pin requires a pull-up resistor in a range from 1.5 kΩ to 10 kΩ that pulls the MDIO high during the idle and turnaround phases of read and write operations.

Bits 2, 1 and 0 of the PHY address are configured during the hardware reset sequence. PHY address bits[4:3] are set to 00 internally in the device. For more information on how to configure this, see Section 2.17 and Section 2.18.

2.18.2.1 Clause 45 Register Access

Typical read and write operations on the management interface are shown in Figure 25 and Figure 26. All the required serial management registers are implemented as well as several optional registers.

Figure 25: Typical MDC/MDIO Read Operation

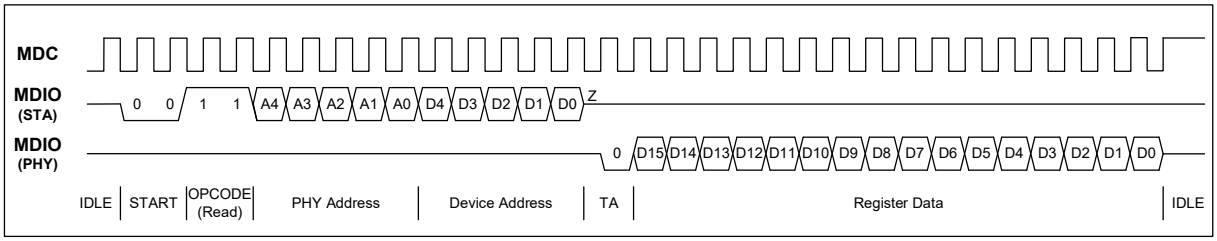
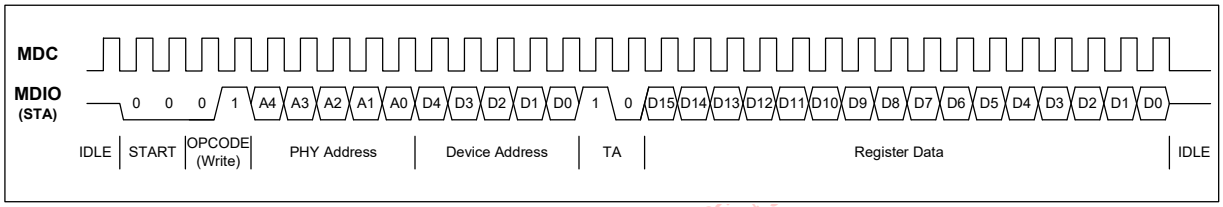


Figure 26: Typical MDC/MDIO Write Operation



The MDIO interface frame structure is compatible with the one defined in Clause 22 such that the two management interfaces can co-exist on the same MDIO bus.

The extensions for Clause 45 MDIO indirect register accesses are specified in Table 56.

Table 56: Extensions for Management Frame Format for Indirect Access

Frame	PRE	ST	OP	PHYAD	DEVADR	TA	ADDRESS/DATA	Idle
Address	1...1	00	00	PPPPP	DDDDD	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	DDDDD	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z
Read Increment	1...1	00	10	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z

The MDIO implements a 16-bit address register that stores the address of the register to be accessed. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, post-read-increment-address cycles, the field contains the data for the register. At power up and reset, the contents of the register are undefined.

Write, read, and post-read-increment-address frames access the address register, though write and read frames do not modify the contents of the address register.

2.18.2.2 Clause 22 MDIO Register Access Method

The 88Q1110 device supports Clause 22 MDIO manageable devices (MMD) extension registers to access Clause 45 MMD registers, using register 13 and 14 as specified in the IEEE Annex 22D.

Table 57: XMDIO MMD Control Register
Device 0, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Function	R/W	0	0	11 = Data, post increments on writes only 10 = Data, post increment on reads and writes 01 = Data, no post increment 00 = Address
13:5	Reserved	RO	0	0	Reserved
4:0	DEVAD	R/W	0	0	Device Address

Table 58: XMDIO MMD Address Data Register
Device 0, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Address Data	R/W	0	0	If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register

For example, to write single Clause 45 register, perform the following accesses:

1. To Register 13, write 00 (address) to bit 15:14 and the device address value to bit 4:0;
2. To Register 14, write the address value;
3. To Register 13, write 01 (Data, no post increment) to bit 15:14 and the same device address value to bit 4:0;
4. To Register 14, write the content of the MMD's selected register.

Step 1 and Step 2 can be skipped if the MMD's address register was previously configured.

2.18.2.3 New Clause 22 MDIO Register Access Method

The 88Q1110 device now supports a third type of register access method. With this method, Clause 22 Extension Registers are used to support traditional Clause 22 register accesses.

This register access method uses XMDIO MMD Registers 13 and 14 as described by IEEE Annex 22D, but in a different way. Registers 13 and 14 are still indirect registers; however, Register 13.4:0 (DEVAD) must be 00000 in order to enable/use this method. Once DEVAD is written with 00000, both of the following must be done:

- Register 14.15:5 must be written with the upper 11 bits of the Clause 45 16-bit register address of the registers in the 88Q1110/88Q1111 device's Clause 45 space to be accessed.
- Register 14.4:0 must be written with the Clause 45 Device Address (for 88Q1110 Device Addresses include 1, 3, 4, and 7; for 88Q1111 the Device Addresses also include 31).

Table 59: XMDIO MMD Control Register
Device 0, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0	0	Reserved
4:0	New Access Enable	R/W	0	0	00000: Enables the new Clause 22 register access method.

Table 60: XMDIO MMD Address Data Register
Device 0, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Upper Register Address	R/W	0	0	Upper 11 bits of the device's Clause 45 16-bit register address
4:0	DEVAD	R/W	0	0	Clause 45 Device Address

Then, once this Device Address and the upper 11 bits are in Register 14, Clause 22 accesses may be issued where the 5-bit register address of the Clause 22 frame is the lower 5 bits of the Clause 45 16-bit address. As long as the Device Address and the upper 11 bits do not change, Clause 22 accesses to registers may be issued without any extra writes to Register 14.

Also, if Registers 13 and 14 are changed for the IEEE Annex 22D access method (and, for example, the Device Address in Register 13 is not 00000), then if a Clause 22 access comes in for a register other than Register 13 or 14, this will go through with the Device Address and upper 11 bits entered previously in Register 14 when Register 13.4:0 was 00000. The lower 5 bits of the address used will be the 5-bit register address in the Clause 22 frame that just came in.

To avoid conflicts with the indirect registers, any registers that have a Clause 45 16-bit address with the lower 5 bits = 0x0D (13) or 0x0E (14) are remapped, so that the lower 5 bits are neither 13 nor 14. Table 61 shows the remapping.

Note that readPlus register 4.8E0E has been remapped to 4.8E1E. Because Register 4.8E0F is associated with Register 4.8E0E, it has been remapped too; its new address is 4.8E1F.

Table 61: Remapped Registers

Current Clause 45 Address	New Clause 45 Address
3.850D	3.851D
3.851E	3.8020
3.850E	3.851E
4.880D	4.881D
4.880E	4.881E
4.890D	4.891D
4.890E	4.891E
4.8C0E	4.8C1E
4.8D0D	4.8D1D
4.8D0E	4.8D1E
4.8E0E	4.8E1E
4.8F0D	4.8F1D
4.8F0E	4.8F1E
7.020D	7.021D

For this new Clause 22 access method, registers 1.000E and 7.000E cannot be accessed since the lower 5 bits are 0x0E (14). They cannot be remapped either since they are defined by IEEE. Instead, registers 1.0002 or 7.0002 may be accessed.

PTP register addresses have been changed as follows (compared to E151xP registers):

- To access register 4.8C09 (page 12, register 9), now address 4.8D00 must be used (which used to access page 13, register 0).
- To access register 4.8C0A (page 12, register 10), now address 4.8D01 must be used (which used to access page 13, register 1).
- To access register 4.8C0B (page 12, register 11), now address 4.8D02 must be used (which used to access page 13, register 2).
- To access register 4.8D00 (page 13, register 0), now address 4.8C09 must be used (which used to access page 12, register 9).
- To access register 4.8D01 (page 13, register 1), now address 4.8C0A must be used (which used to access page 12, register 10).
- To access register 4.8D02 (page 13, register 2), now address 4.8C0B must be used (which used to access page 12, register 11).

2.18.2.4 Preamble Suppression

The device is permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

2.19 Temperature Sensor

The device features an internal temperature sensor. The sensor is enabled through register 3.861B.15:14.

The following register provides the temperature reading of the sensor:

- Average temperature reading (register 3.861B.7:0)

The temperature for the above register is given by (3.861B.7:0 - 75), in degrees Celsius.

There are two different modes to enable the temperature sensor reading:

- Programmable temperature sensor sampling rate
- Fixed temperature sensor sampling rate (where the sampling rate is 1 second)

Programmable Temperature Sensor Sampling Rate

This mode is enabled by setting register 3.861B.15:14 to 2'b01. The sampling rate is then provided through register 3.861B.10:8. The number of samples to obtain the average temperature reading is provided through register 3.861B.12:11. For debug purposes, there is an average test mode, where the number of samples is fixed at 16. This can be enabled by setting register 3.861A.14 to 1'b1. Note that this register has priority over what is programmed in register 3.861B.12:11.

Fixed Temperature Sensor Sampling Rate

This mode is enabled by setting register 3.861B.15:14 to 2'b00. The sampling rate is fixed at 1 second. The number of samples to obtain the average temperature reading is provided through register 3.861B.12:11. For debug purposes, there is an average test mode, where the number of samples is fixed at 16. This can be enabled by setting register 3.861A.14 to 1'b1. Note that this register has priority over what is programmed in register 3.861B.12:11.

2.20 Regulators and Power Supplies

The 88Q1110/88Q1111 devices have built-in regulators to support single rail operation from a 3.3V source. These internal regulators generate 1.5V and 1.05V. The integrated regulators greatly reduce the PCB BOM cost. If regulators are not used then an external 1.5V and 1.05V supply are needed. The following tables list the valid combinations of regulator usage.

The VDDO supply can operate at 1.8V/2.5V/3.3V supplies.

Note

- If VDDO is tied to either 1.8V or 2.5V, then the I/Os are not 3.3V tolerant.
- AVDD15 is tied to 1.5V, so the XTAL_IN pin is not 2.5V/3.3V tolerant.

Table 62: Power Supply Options – Integrated Regulator (REG_IN)

Functional Description	AVDD33	AVDD15	DVDD	Setup
Supply Source	3.3V	1.5V from Internal Regulator	1.05V from Internal Regulator	Single 3.3V external supply Internal regulator enabled

Table 63: Power Supply Options – External Supplies

Functional Description	AVDD33	AVDD15	DVDD	Setup
Supply Source	3.3V	1.5V from External	1.05V from External	3.3V, 1.5V, 1.05V external supplies Internal regulator disabled.

Table 64: Power Supply Options – External 1.5V, Integrated Regulator (REG_IN) Supplies Only 1.05V

Functional Description	AVDD33	AVDD15	DVDD	Setup
Supply Source	3.3V	1.5V from External	1.05V from Internal Regulator	Internal regulator enabled, but only for 1.05V. 1.5V external: VDD33 supplied. VDD15_OUT connects to AVDD15_IN, but does not connect to AVDD15 (AVDD15 supplied externally). DVDD_OUT connects to DVDD.

Table 65: Power Supply Options – External 1.05V, Integrated Regulator (REG_IN) Supplies Only 1.5V

Functional Description	AVDD33	AVDD15	DVDD	Setup
Supply Source	3.3V	1.5V from Internal Regulator	1.05V from External	Internal regulator enabled but only for 1.5V. 1.05V supplied externally: VDD33 supplied, VDD15_OUT connects to AVDD15_IN and AVDD15. DVDD_OUT is not connected to DVDD. Also need to supply DVDD for bypass caps externally.

2.20.1 AVDD15

AVDD15 is used as the 1.5V analog supply.

It is used as a 1.5V analog supply for the XTAL_IN/OUT pins. AVDD15 can be supplied externally with 1.5V, or via the 1.5V regulator.

2.20.2 AVDD15_IN

AVDD15_IN is the internal regulator 1.5V input and is a supply for the DVDD regulator. If the internal regulator is used, this input should connect to VDD15_OUT. If the internal regulator is not used, this input should float.

2.20.3 AVDD33

AVDD33 is used as a 3.3V analog supply.

2.20.4 DVDD

DVDD is used as the 1.05V digital supply. DVDD can be supplied externally with 1.05V, or via the internal 1.05V regulator.

2.20.5 VDD33 (REG_IN)

VDD33 (REG_IN) is used as the 3.3V supply to the internal regulator that generates the 1.5V for AVDD15 and 1.05V for DVDD. If the 1.5V and 1.05V regulators are not used, VDD33 (REG_IN) must be left floating.

2.20.6 VDD15_OUT

VDD15_OUT is the internal regulator 1.5V output. This must be connected to 1.5V power plane that connects to AVDD15. If an external supply is used to supply AVDD15, VDD15_OUT must be left floating.

2.20.7 DVDD_OUT

DVDD_OUT is the internal regulator 1.05V output. When internal regulator is used, DVDD_OUT must be connected to the DVDD plane. If an external supply is used to supply DVDD, DVDD_OUT must be left floating.

2.20.8 VDDO

VDDO supplies all digital I/O pins which use LVCMOS I/O standards. The supported voltages are 1.8V, 2.5V or 3.3V. For operation in 2.5V mode, the user must set Register 4.8214.15 to 1.

Note LEDs cannot be used for VDDO = 1.8V operation.

2.20.9 Power Supply Sequencing

On power-up, no special power supply sequencing is required.

2.21 Precision Time Protocol (PTP) Time Stamping Support

Precision Timing Protocol (PTP) is used by IEEE specifications to determine the time of day for systems across a network. The IEEE specifications are IEEE 802.1AS, IEEE 1588 version 1, and IEEE 1588 version 2. The PTP protocol is typically used in audio video bridging (PTP) applications, or industrial and test automation applications.

The fundamental concept is to be able to time stamp the PTP frames with high precision as close to the physical wires as possible. As such, doing the time stamping in the PHY increases the accuracy compared to doing it in the MAC or higher layers since the MAC interface FIFOs can add up to ±2 bytes of uncertainty.

The PTP core in the device consists of two sub-cores, namely the Packet Time Stamping and the Time Application Interface (TAI). The time stamping core supports time stamping of frame formats as defined in IEEE 802.1AS, IEEE 1588v1, and IEEE 1588v2 frames.

2.21.1 PTP Control

To support the PTP Time Stamping function, the device has three pins that are global to the entire PHY:

- PTP Event Request input pin (the LED/GPIO[1] pin is used for this purpose)
- PTP Trigger Generate output pin (the LED/GPIO[1] pin is used for this purpose)
- Interrupt pin

2.21.1.1 PTP Event Request

The PTP Event Request input pin can be configured to capture an external event (referred to as EventReq) and record the time at which the event occurred using the PTP Global Time Register (PTP Global Time Register – registers 4.8C1E and 4.8C0F). Users must program 3.8630.7:4 to select whether LED or GPIO are used to enable this function. The definition of an external event is a low-to-high transition or a high-to-low transition on the LED/GPIO pin. Register 4.8C00 bit 13 (Event Phase) selects which transition (rising or falling) is used. The event time is captured in EventCapRegister (Event Capture Register – registers 4.8D01 and 4.8D02). This field is validated by the EventCapValid bit (TAI Global Configuration Register – register 4.8D00).

2.21.1.2 PTP Trigger Generate

The PTP Trigger Generate output pin is used to output an external signal (referred to as TrigGenResp) when the internal Time of Day counter matches a value programmed into a PHY register. When there is a match, this output will go from low to high or from high to low, based on register 4.8C00 bit 12 (TrigPhase). The LED or GPIO pin is used for this function. It is selected by setting register 3.8630.7:4 selection. The trigger output can also be a pulse or a clock, depending on what is programmed in register 4.8C00, bit 1 (TrigMode).

2.21.1.3 PTP Control Register

The PTP circuit timestamps packets as it passes through the PHY. The register control to this function can be accessed via registers 4.88xx to 4.8Fxx. The PTP circuit can be powered down when it is not used via register 3.8630.9. When register 3.8630.9 is set to 1, the registers in 4.88xx to 4.8Fxx are not accessible since the entire circuit is powered down.

By default, register 3.8630.9 is set to 1. It must be set to 0 to enable PTP.

For the register description, see Table 160, PTP Control Register, on page 150.

1. Refer to Section Table 5:, 88Q1110 Tx Enable/GPIO/LED/Interrupt Interface, on page 23 or Section Table 16:, 88Q1111 Tx Enable/GPIO/LED/Interrupt Interface, on page 30 for further details on LED/GPIO pin.

2.21.2 Packet Time Stamping

2.21.2.1 Time Stamping without Hardware Acceleration

The device supports two sets of hardware arrival time stamp registers to be able to capture two different PTP event messages' time stamp before the CPU reads the time stamp registers out of the device. For every incoming PTP message type, either PTPArr0Time (PTP Arrival 0 Time Registers – registers 4.880A and 4.880B) or PTPArr1Time (PTP Arrival 1 Time Registers – registers 4.881D and 4.881E) can be chosen by configuring TSArrPtr (PTP Global Configuration Register 2 – register 4.8E02). The SequenceID from the PTP Common header is captured as part of Arrival 0, Arrival 1, and/or Departure time stamp register sets, so the software can correlate the collected time stamps with the received or transmitted PTP event message. The hardware can be enabled to generate an interrupt upon capturing the time stamp information by writing a 0x1 to the interrupt enable register bits PTPArrIntEn (PTP Port Configuration Register 2 – register 4.8802) for incoming PTP event messages or PTPDepIntEn (PTP Port Configuration Register 2 – register 4.8802) for outgoing PTP event messages. In addition to generating an interrupt on the interrupt pin, an interrupt status (PTPArr0IntStatus, PTPArr1IntStatus, and PTPDepIntStatus) gets generated, which indicates if there were to be an error related to the time stamp register. The interrupt status gets set to 0x1 when the time stamp counter gets overwritten before the previous time stamp registers have been read out. The interrupt status gets set to a 0x2, when a time stamp could not be captured for a PTP event message because DisTSOverwrite (PTP Port Configuration Register – register 4.8800) is set to 0x1.

Given that the device registers are accessed in units of 16 bits, to retain the entire 32-bit time stamp and the associated error messages and the SequenceID for a given PTP frame, the hardware treats the Arrival 0 block registers (registers 4.8808 to 4.890B), Arrival 1 block registers (registers 4.880C, 4.881D, 4.881E, and 4.880F), and Departure block registers (registers 4.8900 to 4.8903) as a group and atomic operations are supported for these block of registers.

It is important to note that the device does not alter the contents of any PTP packet in either ingress or egress direction. Time stamping at the device level does not involve adding a time stamp to a packet or changing its CRC. It also does not involve the device looking at time stamps that are embedded within a packet. The PHY does not add any additional latency when the PTP function is enabled. The PHY only identifies that a packet is a PTP frame and records the enter and exit time. The PHY does this by parsing the packet for certain fields as described in later sections. If the packet is identified as such a PTP packet, the device loads the value of an internal "time of day counter" to a register showing the time for the first byte or SFD of the packet. The device then can inform the CPU or the PTP higher level firmware/software that such an event happened by activating an interrupt pin. The CPU can then read the relevant registers to find out if the event was in the Rx or TX direction and the value of the "time of day counter" when the event happened.

Using the above time information and following the PTP protocol, the CPU or higher level entity can then determine the offset in time of day between a Grand Master Clock and the SLAVE node, as well as the frequency difference between the Grand Master Clock and the SLAVE clock in case they are not frequency-locked. These calculations are above the PHY level. The PHY provides full flexibility by allowing its time of day counter to be adjusted based on the CPU's calculations, as well as a totally new time of day value to be entered. The CPU can also use the time information provided by the PHY to create PTP packets that inform the link partners or the Grand Master when the packets had arrived or left the port in question.

The maximum jitter associated with capturing the time stamps collected by the logic is one TSClkPer (TAI Global Configuration Register 1 – register 4.8C01). Note that there are inherent delay variations introduced in PHY layer pipelines both in receive and transmit direction, which add to the overall jitter of the time stamps collected by the hardware and frequency/phase computations done in PTP protocol software.

For achieving higher accuracies in terms of PTP, it is recommended that an external clock device is used to adjust the time stamping clock with the frequency/phase offset information computed in PTP protocol software. The frequency and/or phase adjusted clock can in turn be fed back into the device to be used by the time stamping logic.

2.21.2.2 Time Stamping with Hardware Acceleration

Hardware acceleration is available and can be turned on to offload the CPU from processing time stamp information.

Without the hardware acceleration, PTP frames are detected and the time stamp information is extracted and placed in registers so there is no alteration of any frames. A CPU or a higher level entity will need to access the relevant registers to obtain the time stamp information.

With the hardware acceleration, time stamp information is inserted directly into the PTP frame before it is transmitted to the CPU. Therefore, the CPU can obtain the time stamp information once the frame is received and does not need to access registers. In this case, PTP frames are being modified and additional latency is introduced due to the frame buffering and time stamp insertion.

Frames Involved

Hardware acceleration is achieved by modifying the seven frames mentioned earlier based on the mode of operation. Table 66 lists the fields of each of these frames.

Table 66: List of Frame's Fields

# Octet	Sync	Follow_Up	Delay_Req	Delay_Resp	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_ Follow_Up
6	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr
6	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr
2	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType
	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion
1	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType
1 2	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength
1	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber
1	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField
8	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField
4	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID
2	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID
1	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField
1	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval
10	OriginTS - 1588 Rsvd – 802.1AS	Precise OriginTS	OriginTS	ReceiveTS	OriginTS - 1588 Rsvd – 802.1AS	ReqReceiptTS	Response OriginTS
10		TLV – 802.1AS		ReqPortID	Rsvd	ReqPortID	ReqPortID
22	-		-	-	-	-	-

Data Receive Path

To accelerate the frames in hardware, the egress port needs information from the ingress port. The frame's ingress time stamp value is needed at the egress port to calculate the frame's residence time in the switch. When event frames ingress the switch, the hardware needs to embed the arrival time into the frame (in the 4 bytes RSVD location). In addition to the arrival time, in some cases, the correction field needs to be updated with the mean path delay and the delay asymmetry values at the ingress port.

Table 67: Receive Path Frame Modifications

Receive path
Fields highlighted in
Gray – Decode these fields in hardware (to determine if it is a supported PTP frame)
Blue – Modify these fields of the frame (as needed) in hardware
Green – Capture these fields of the frame in hardware to use for comparisons of associated frames

# Octet	Sync	Follow_Up	Delay_Req	Delay_Resp	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_ Follow_Up
6	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr
6	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr
2	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType
	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion
1	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType
1	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP
2	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength
1	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber
1	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField
8	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField
4	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID
2	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID
1	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField
1	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval
10	OriginTS -1588 / Rsvd –802.1AS	Precise OriginTS	OriginTS	ReceiveTS	OriginTS -1588 / Rsvd –802.1AS	ReqReceiptTS	Response OriginTS
10		TLV – 802.1AS		ReqPortID	Rsvd	ReqPortID	ReqPortID
22	-		-	-	-	-	-

Data Transmit Path

Hardware acceleration involves modifying some of the frame's fields at the egress port. The required information is extracted from the frames and used to update them before transmitting the frames. The ingress time value should be extracted from the reserved location and the field zeroed out. Correction field will be updated on top of any modifications made at the ingress port.

Table 68: Transmit Path Frame Modifications

Transmit path
Fields highlighted in
Gray – Decode these fields in hardware (to determine if it is a supported PTP frame)
Blue – Modify these fields of the frame (as needed) in hardware
Green – Capture these fields of the frame in hardware to use for comparisons of associated frames
Red – Hardware can't modify these fields. The modification has to be done by software (after checking for associated frames)

# Octet	Sync	Follow_Up	Delay_Req	Delay_Resp	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_ Follow_Up
6	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr
6	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr
2	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType
1	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType
1	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP
2	MessageLength	Message Length	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength
1	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber
1	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField
8	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField
4	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID
2	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID
1	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField
1	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval
10	OriginTS -1588 Rsvd –802.1AS	Precise OriginTS	OriginTS	ReceiveTS	OriginTS -1588 Rsvd –802.1AS	ReqReceiptTS	Response OriginTS
10		TLV – 802.1AS		ReqPortID	Rsvd	ReqPortID	ReqPortID
22	-		-	-	-	-	-

Frame Ingress Path Modification

When a frame ingresses a port, decoding its header determines if it is a PTP frame. If hardware acceleration is enabled (HA bit register 4.8802), then IEEE 1588/802.1AS layer 2 frames of know time domains (PTP Global – register 4.8F02) and version number (PTP Global – register 4.8E07) are accelerated in hardware. The event frame's ingress time (IntPTPTime Register PTP Global – register 4.8E07) is placed in the 4 bytes of reserved space in the frame (bytes 17–20). The correction field of the frames is updated with MeanPathDelay and IngressDelayAsymmetry values whenever applicable, based on the mode of operation as described on "Equations Defining Frame Field Values" on page 95.

When a frame contains unknown domain number, unknown message type, or unsupported version number, it cannot be accelerated by hardware. In such cases, the event frame's arrival time (domain specific time or the hardware timer value) is embedded into the frame itself based on the ArrTSMode register value (PTP Port – register 4.8802) so that the CPU has the ingress time information. If the ArrTSMode value is zero, the frame's arrival time is placed in the status registers (PTP Port – registers 4.8808 to 4.880F, 4.881D, 4.881E, and 4.8900).

A latency of about 8 byte times is introduced in the data path to achieve the hardware acceleration. Switching between bypass mode (no acceleration) and hardware acceleration mode should be done only when the port is idle to avoid corrupting the frames.

Frame Transmit Path Modification

When a frame egresses a port, decoding its header determines if it is a PTP frame. If hardware acceleration is enabled (HA bit register 4.8802), then IEEE 1588/802.1AS layer 2 frames of know time domains (register 4.8F02) and version number (register 4.8E07, index 0x0) are accelerated in hardware. These frames could be coming from an ingress port (hardware accelerated at ingress) or from the CPU port (CPU needs to place the needed info into the frames).

The event frame's ingress time (IntPTPTime Register – register 4.8E07) is extracted from the 4 bytes of reserved space in the frame (bytes 17–20) for use in further calculations and the reserved bytes zeroed out (unless KeepRxData bit of action vectors is set). The OriginTS field and the Correction field of the frames are updated whenever applicable, based on the mode of operation as described on "Equations Defining Frame Field Values" on page 95.

A latency of about 12 byte times is introduced in the data path to achieve the hardware acceleration. Switching between bypass mode (no hardware acceleration) and hardware acceleration mode should be done only when the port is idle to avoid corrupting the frames.

Sync – Follow_Up Frames

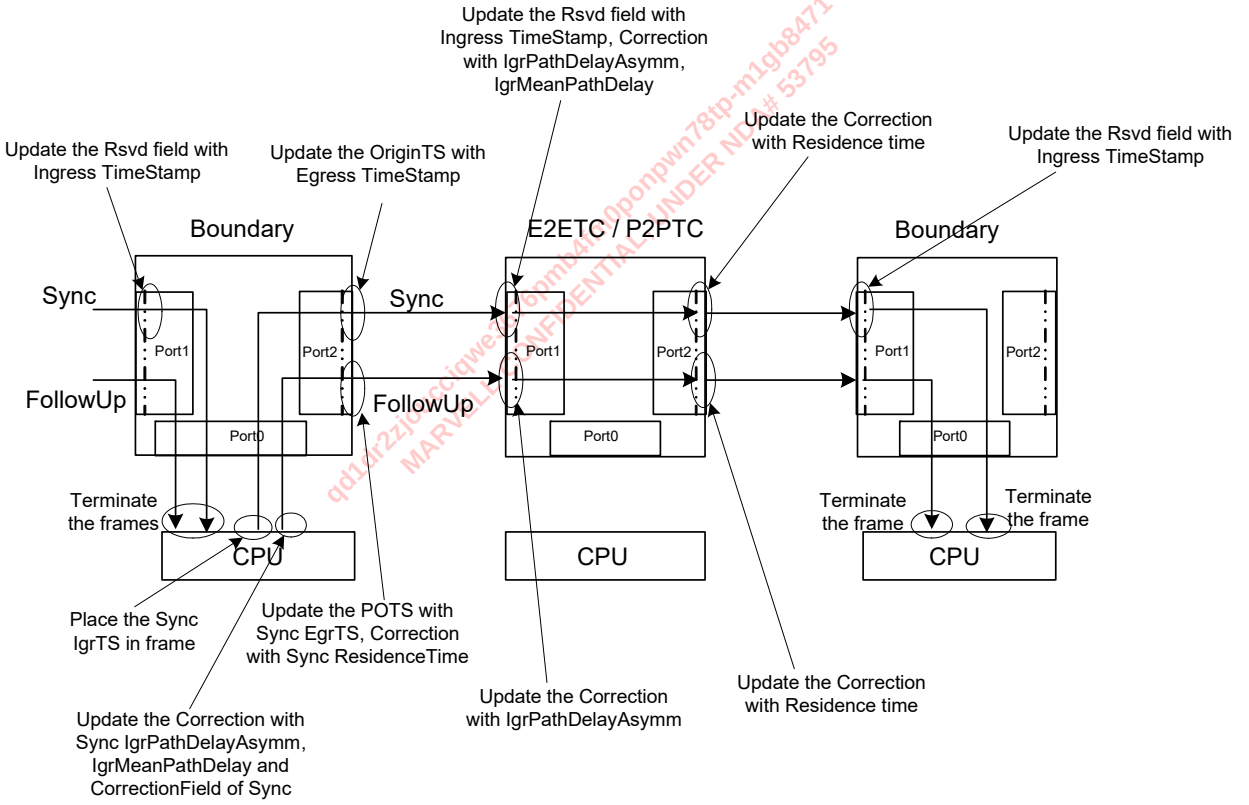
Sync and FollowUp frames travel in the same direction—from master to the slave. These frames contain master's timing information. A FollowUp frame and Sync frame are said to be associated frames if their SourcePortID and the SeqID match. A FollowUp frame should be modified only after checking its SourcePortID and SeqID against the previously received Sync frame to ensure that the associated frames are modified correctly. The fields to be updated in the FollowUp frame are ahead of the SourcePortID and the SeqID fields. The 'compare and then modify' method results in a long latency. Thus, the 'modify and then compare' method is used to avoid the latency, FollowUp frames are modified on the fly even before checking their SourcePortID and SeqID. After such modifications, when the SourcePortID and SeqID fields are reached in the frame, they are compared with that of the previous Sync frame. If they do not match, the FCS value of the FollowUp frame is purposefully corrupted before transmitting the frame.

At ingress, the hardware inserts the receive time into the Sync frames. The CorrectionField of the Sync and FollowUp frames is updated with MeanPathDelay and IngressDelayAsymmetry values whenever applicable, based on the mode of operation.

At the egress port, the Sync frame's ingress time is extracted from the reserved bytes (bytes 17–20 of PTP header) and the field is zeroed out before being transmitted (unless KeepRxData bit of action vectors is set). The Sync frame's OriginTS and CorrectionField are modified based on the equations matrix. The residence time of the Sync frame is saved to be used in updating the CorrectionField of the FollowUp frame when applicable. The FollowUp frame's preciseOriginTS and CorrectionField are modified on the egress path based on the equations matrix.

Figure 27 lists all possible modifications needed on Sync and FollowUp frames. However, it should be noted that the changes described in the figure do not all occur at the same time. Based on the mode, the device is in i.e. one-step, two-step, IEEE1588 etc. only some of the changes will be made at a time.

Figure 27: Sync-FollowUp Frame's Hardware Acceleration Path



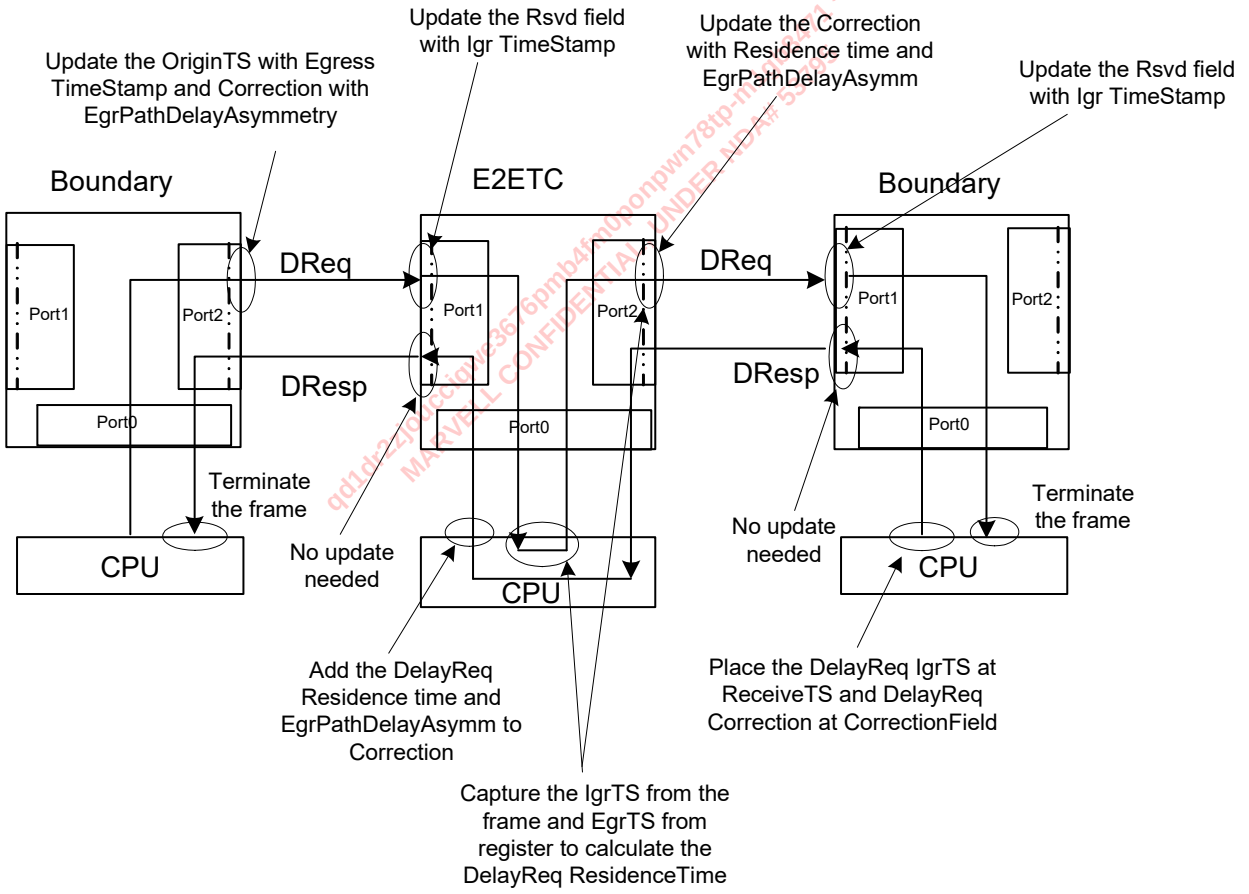
Delay_Request – Delay_Response Frames

DelayReq and DelayResp frames travel in opposite directions. DelayReq frame is sent by the slave and DelayResp frame is sent by the master port. At ingress, the hardware inserts the receive time into the DelayReq frames before sending them to the CPU. At egress port, the DelayReq frame's ingress time is extracted from the reserved bytes (bytes 17–20 of PTP header) and the field is zeroed out before being transmitted (unless KeepRxData bit of action vectors is set). The DelayReq frame's OriginTS and CorrectionField are modified based on the equations matrix. DelayReq frame's egress time is placed into the status registers so that the CPU can extract this information and use it to update the DelayResp frame.

A DelayReq frame and DelayResp frame are said to be associated frames if their SourcePortID and the SeqID match. A DelayResp frame should be modified with information from previously received DelayReq only after matching its SourcePortID and SeqID to ensure that they are associated frames. However, the hardware at egress port of DelayResp frame does not have the SourcePortId or SeqID values of the received DelayReq frame (opposite direction). Thus, the CPU needs to check SourcePortId and SeqId of the frames and add in the correct DelayReq frame's information (residence time, CorrectionField value and EgrPathDelayAsymm) to the DelayResp frames before transmission. The hardware does not modify/accelerate the DelayResp frames at egress.

Figure 28 lists all possible modifications needed on DelayReq and DelayResp frames. However, it should be noted that the changes described in the figure do not all occur at the same time. Based on the mode, the device is in i.e. one-step, two-step, IEEE1588 etc. only some of the changes will be made at a time.

Figure 28: DelayReq-DelayResp Frame's Hardware Acceleration Path



PDelayRequest, PDelayResponse, and PDelayResponseFollowUp Frames

PDelayReq frame is sent by the initiator to the responder. At ingress, the hardware inserts the receive time into the PDelayReq frames before sending them to the CPU. At egress port, the PDelayReq frame's ingress time is extracted from the reserved bytes (bytes 17–20 of PTP header) and the field is zeroed out before being transmitted (unless KeepRxData bit of action vectors is set). The PDelayReq frame's OriginTS and CorrectionField are modified based on the equations matrix. PDelayReq frame's egress time is placed into the status registers so that the CPU can extract this information and use it to update the PDelayResp/ PDelayRespFollowUp frame.

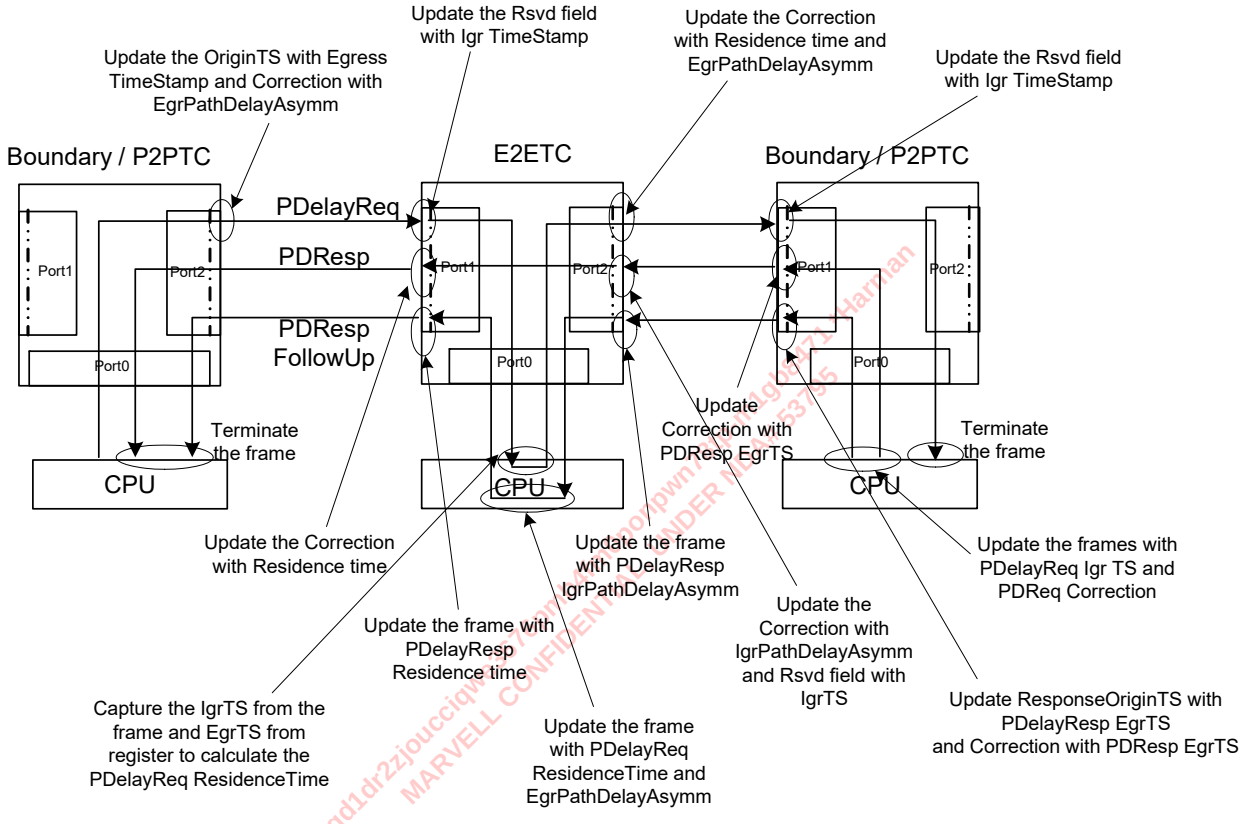
The PDelayResp frame is sent by the responder to the initiator, that is, in opposite direction than the PDelayReq frame. At ingress, the hardware inserts the receive time into the PDelayResp frames. A PDelayReq frame and PDelayResp frame are associated frames if the SourcePortID and SeqID of PDelayReq frame matches with the ReqPortID and the SeqID of PDelayResp frame. A PDelayResp frame should be modified only after checking its ReqPortID and SeqID against the SourcePortId and SeqID of previously received PDelayReq frame to ensure that the associated frames are modified correctly. However, the hardware at egress port of PDelayResp frame does not have the SourcePortId or SeqID values of the received PDelayReq frame (opposite direction). Thus, the CPU needs to match the frames and add in the correct PDelayReq frame's information to the

PDelayResp frames before transmission. The CorrectionField value of PDelayReq needs to be added to the CorrectionField of PDelayResp frames when applicable. The CPU should place the PDelayReq frame's IgrTS in the 4 reserved bytes (bytes 17–20 of PTP header) of PDelayResp frames when applicable. At egress, the hardware extracts this information and updates the PDelayResp frame's ReqReceiptTS and CorrectionField based on the equation's matrix.

PDelayResp and PDelayRespFollowUp frames travel in the same direction, from the responder to the initiator. A PDelayRespFollowUp frame and PDelayResp frame are associated with each other if their ReqPortID and the SeqID match. A PDelayRespFollowUp frame should be modified only after checking its ReqPortID and SeqID against the previously received PDelayResp frame to ensure that the associated frames are modified correctly. The fields to be updated in the PDRespFollowUp frame are ahead of the ReqPortID and the SeqID fields. The 'compare and then modify' method results in a long latency. Thus, the 'modify and then compare' method is used to avoid the latency, PDelayRespFollowUp frames are modified on the fly even before checking their ReqPortID and SeqID. After such modifications, when the ReqPortID and SeqID fields are reached in the frame, they are compared with that of the previous PDelayResp frame. If they do not match, the FCS value of the PDelayRespFollowUp frame is purposefully corrupted before transmitting the frame. Similar to the PDelayResp frame's case, the hardware depends on the CPU to make PDelayReq related timing information changes to PDelayRespFollowUp whenever applicable.

Figure 29 lists all possible modifications needed on PDelayReq, PDelayResp, and PDelayRespFollowUp frames. However, it should be noted that the changes described in the figure do not all occur at the same time. Based on the mode the device is in i.e. one-step, two-step, IEEE1588 etc. only some of the changes will be made at a time.

Figure 29: PDelayReq, PDelayResp, PDelayRespFollowUp Frame's Hardware Acceleration Path



Equations Defining Frame Field Values

The tables below describe the equations that govern the frame field values based on various configurations supported.

Table 69: Sync Frame Equations Implemented

1. The boxes filled in red depict the special cases where the device works differently than described in the IEEE specification. The text describes the device's behavior in those cases.
2. The text highlighted in light grey is the ingress path function that is not performed in hardware. The frame is sent to CPU and it should take care of this portion.
3. The text highlighted in green is the information that CPU is required to supply the hardware in the egress path. That portion needs to be placed in the frame by the software.
4. Rest of the portion is done in hardware (combination of the ingress path and egress path)

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Sync	**One Step**	**1588**	**OriginTS** = SyncEgrTS **CorrectionField** = Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField + IgrMeanPathDelay + ResidenceTime + IgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField + ResidenceTime + IgrPathDelayAsym
	Two Step w/Rx **Two Step Flag = False**	**1588**	N/A	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx **Two Step Flag = True**	**1588**	**OriginTS** = Rx's OriginTS (0 or estimate SyncEgrTS) OR SyncEgrTS (Program action reg bit) **CorrectionField** = Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
		802.1 AS	**OriginTS** - NA **CorrectionField** = Rx's CorrectionField (0) *i.e., frame not modified*	N/A	N/A

Table 70: FollowUp Frame Equations Implemented

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
FollowUp	**One Step**	**1588**	N/A	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = False	**1588**	N/A	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = True	**1588**	**PreciseOriginTS** = SyncEgrTS **Correction** = Rx's CorrectionField (0 – CorrectionField Sync)	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField + ResidenceTime + IgrMeanPathDelay + IgrPathDelayAsym	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField + ResidenceTime + IgrPathDelayAsym
		802.1 AS	**PreciseOriginTS** = (a) If GrandMaster: SyncEgrTS (b) If not the GrandMaster: Rx's PreciseOriginTS **Correction** = (a) If GrandMaster: Rx's CorrectionField (0) (b) If not the GrandMaster: Rx's CorrectionField + ResidenceTime + PropagationDelay (MeanPathDelay) + IgrPathDelayAsym	N/A	N/A

Table 71: DelayReq and DelayResp Frame Equations Implemented

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Delay Req	**One Step**	**1588**	**OriginTS** = Rx's OriginTS (0 /estimate DelayReqEgrTS) OR DelayRespEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	Discard	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField + ResidenceTime - EgrPathDelayAsym
	Two Step w/Rx Two Step Flag = False	**1588**	**OriginTS** = Rx's OriginTS (0 /estimate DelayReqEgrTS) OR DelayRespEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	Discard	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = True	**1588**	**OriginTS** = Rx's OriginTS (0 /estimate DelayReqEgrTS) OR DelayRespEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	Discard	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
		802.1 AS	N/A	N/A	N/A
Delay Resp	**One Step**	**1588**	**ReceiveTS** = DelayReqIgrTS **Correction** = 0 + CorrectionField DelayReq *i.e., frame not modified*	Discard	**ReceiveTS** = Rx's ReceiveTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = False	**1588**	**ReceiveTS** = DelayReqIgrTS **Correction** = 0 + CorrectionField DelayReq *i.e., frame not modified*	Discard	**ReceiveTS** = Rx's ReceiveTS **Correction** = Rx's CorrectionField + ResidenceTime DelayReq – EgrPathDelayAsym of DelayReq *i.e., frame not modified*
	Two Step w/ Rx Two Step Flag = True	**1588**	**ReceiveTS** = DelayReqIgrTS **Correction** = 0 + CorrectionField DelayReq *i.e., frame not modified*	Discard	**ReceiveTS** = Rx's ReceiveTS **Correction** = Rx's CorrectionField + ResidenceTime DelayReq – EgrPathDelayAsym of DelayReq *i.e., frame not modified*
		802.1 AS	N/A	N/A	N/A

Table 72: PDelayReq Frame Equations Implemented

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Pdelay Req	**One Step**	**1588**	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField + Residence Time PdelayReq – EgrPathDelayAsym
	Two Step w/Rx Two Step Flag = False	**1588**	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = True	**1588**	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
		802.1 AS	**OriginTS** = NA **Correction** = Rx's CorrectionField (0) *i.e., frame not modified*	N/A	N/A

Table 73: PDelayResp Frame Equations Implemented

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Pdelay Resp	**One Step**	**1588**	**ReqReceiptTS** = Rx's ReqReceiptTS (0) **Correction** = CorrectionField of PdelayReq + (PDRespEgrTS – PDReqIgrTS) **Rsvd** = PDReqIgrTS **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = Rx's ReqReceiptTS (0) **Correction** = CorrectionField of PdelayReq + (PDRespEgrTS – PDReqIgrTS) **Rsvd** = PDReqIgrTS **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = Rx's ReqReceiptTS **Correction** = Rx's CorrectionField + ResidenceTime Pdelay_Resp + IgrPathDelayAsym
	Two Step w/Rx **Two Step Flag = False**	**1588**	N/A	N/A	**ReqReceiptTS** = Rx's ReqReceiptTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx **Two Step Flag = True**	**1588**	**ReqReceiptTS** = (a) Rx's ReqReceiptTS (0) OR (b) ReqReceiptTS (PDelayReqIgrTS) **Correction** = (a) Rx's CorrectionField (0) OR (b) Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = (a) Rx's ReqReceiptTS (0) OR (b) ReqReceiptTS (PDelayReqIgrTS) **Correction** = (a) Rx's CorrectionField (0) OR (b) Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = Rx's ReqReceiptTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
		802.1 AS	**ReqReceiptTS** = Rx's ReqReceiptTS (PDelayReqIgrTS) **Correction** = Rx's CorrectionField (0) *i.e., frame not modified*	N/A	N/A

Table 74: PDelayRespFollowUp Frame Equations Implemented

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Pdelay Resp FollowUp	**One Step**	**1588**	N/A	N/A	**ResponseOriginTS** = Rx's ResponseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = False	**1588**	N/A	N/A	**ResponseOriginTS** = Rx's ResponseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = True	**1588**	**ResponseOriginTS** = (a) Rx's ResponseOriginTS (0) OR (b) PdelayRespEgrTS **Correction** = Correction Field PdelayReq + (a) PdelayRespEgrTS-PdelayReqIgrTS OR (b) 0 **Rsvd** = (a) PdelayReqIgrTS	**ResponseOriginTS** = (a) Rx's ResponseOriginTS (0) OR (b) PdelayRespEgrTS **Correction** = Correction Field PdelayReq + (a) PdelayRespEgrTS-PdelayReqIgrTS OR (b) 0 **Rsvd** = (a) PdelayReqIgrTS	**ResponseOriginTS** = Rx's ResponseOriginTS **Correction** = Rx's Correction field + Residence Time of PdelayReq + Residence Time of PdelayResp + IgrPathDelayAsym of PDelayResp – EgrPathDelayAsym of PDelayReq
		802.1 AS	**ResponseOriginTS** = PdelayRespEgrTS **Correction** = Rx's Correction field (0)	N/A	N/A

The PdelayResp and PdelayRespFollowUp frames follow either scheme (a) or (b), based on the register selection.

2.21.3 Time Application Interface (TAI)

The Precision Time Protocol provides both frequency and time of day with respect to the PTP Grand Master for the entire PTP network. In a given endpoint device (media talker or a media listener), once the PTP Grand Master aware clock and time are available, it needs to be transported over to the rest of the subsystem without loss of accuracy. For example, if a Digital Video Recorder (DVR) is the end device, the network clock and time need to be transported to the video SoC and/or storage SoC and to the host processor seamlessly. This ensures that when the media is played out of the DVR, the network time aware presentation time of the content is required to be carried through.

The TAI "Timing Interface Block" supports features required for the above purpose. This block utilizes two signals to offer various services. One signal is called EventRequest input signal, and the second is called TriggerGenerate output signal.

Using the above signals, there are several functions that this block supports:

- An event pulse capture function.
- Multiple event counter function.
- A trigger pulse generate function with pulse width control.
- A trigger clock generate function with digital clock compensation.
- A multi-PTP device time sync function.

2.21.3.1 Event Pulse Capture Interface

In many IEEE 1588 applications like industrial automation etc., it is important to precisely capture the time at which a particular event has happened. The event is defined by a low-to-high or high-to-low transition on an external signal called EventRequest. The event time is captured in EventCapRegister (registers 4.8D01 and 4.8D02). This field is validated by EventCapValid bit (TAI Global Configuration – register 4.8D00).

The captured event time register needs to be read out by the software and the valid bit needs to be cleared before the hardware captures another event. If there were to be two back-to-back events before the software read the results of the first event, an error indication is set in EventCapErr (TAI Global Configuration – register 4.8D00). If the user chooses that the hardware rather overwrite the Event capture register, then it can be configured by setting a 0x1 to EventCapOv (TAI Global Configuration – register 4.8C00).

Once an event has been captured, the software can optionally (EventCapIntEn – register 4.8C00) be interrupted and an EventInt (register 4.8C09) bit is also set.

The maximum jitter associated with capturing the EventRequest signal pulse is one TSClkPer (TAI Global Configuration – register 4.8C01). The minimum pulse width of the EventRequest signal needs to be 1.5 times the TSClkPer (TAI Global Configuration – register 4.8C01). In order for the hardware logic to detect distinct events on the EventRequest signal, the minimum gap between two events needs to be 150 ns plus 5 times the TSClkPer amount.

2.21.3.2 Multiple Event Counter Function

Similar to the Event Pulse capture interface described above, if multiple events need to be captured for an application to detect how many times a particular event is happening on the EventRequest input signal, EventCtrStart (TAI Global Configuration Register – register 4.8C00) needs to be set to 0x1 and EventCapOv (TAI Global Configuration Register – register 4.8C00) needs to set to 0x1.

The Multiple Event Counter function is capable of capturing up to 255 events in EventCapCtr (TAI Global Configuration – register 4.8C09).

The maximum jitter associated with capturing the EventRequest signal pulse is one TSClkPer (TAI Global Configuration – register 4.8C01). The minimum pulse width of the EventRequest signal needs to be 1.5 times the TSClkPer (TAI Global Configuration – register 4.8C01). In order for the hardware logic to detect distinct events on the EventRequest signal, the minimum gap between two events needs to be 150 ns plus 5 times the TSClkPer amount.

Note

In the multiple event counter mode, the EventCapRegister (registers 4.8D01 and 4.8D02) indicate the time stamp value for the last captured event register.

2.21.3.3 Trigger Pulse Generate Function

In many PTP applications, the time of day computed in PTP needs to be distributed in some form to the rest of the node. One commonly used method is to generate a pulse whenever the PTP Global Time matches a certain configured value. The pulse gets output on a TrigGenResp output signal.

The above function can be achieved by:

a) Configuring the TrigMode (TAI Global Configuration Register 4.8C00) to 0x1 and
b) Configuring the time amount when the pulse needs to be generated in TrigGenAmt (TAI Global Configuration Registers 4.8C02 and 4.8C03) and
c) Configuring the TrigGenReq (TAI Global Configuration Register 4.8C00) to 0x1

The PTP Global Timer gets compared to the TrigGenAmt, and upon a match a pulse signal gets generated on the TrigGenResp output signal.

Optionally after generating the TrigGenResp pulse, the CPU can be notified by setting TrigGenIntEn (TAI Global Configuration Register 4.8C00), and along with the pulse output the TrigGenInt bit (PTP Status Register - Register 4.8E08) gets set. Upon receiving the interrupt, it is the CPU's job to clear the interrupt bit.

The pulse width of the output signal can be controlled by PulseWidth (TAI Global Configuration Register 4.8C05). Do not set the PulseWidth to a zero value.

2.21.3.4 Trigger Clock Generate Function

Similar to the trigger pulse generation function described above, the same set of registers can be used to generate a periodic clock. The value specified in TrigGenAmt (TAI Global Configuration Register 4.8C02 and 4.8C03) is used to generate the base period of the clock output. For this functional mode, the TrigMode (TAI Global Configuration Register 4.8C00) needs to be set to 0x0 and TrigGenReq (TAI Global Configuration Register 4.8C00) needs to be set to 0x1.

The output clock can be compensated by configuring field TrigClkComp (TAI Global Configuration Register 4.8C04) and TrigClkCompSubps (TAI Global Configuration Register 4.8C05). This field specifies the remainder amount for the clock that is being generated with the period specified by TrigGenAmt. The TrigClkComp amount gets constantly accumulated and when this accumulated amount exceeds the value specified in TSClkPer, a TSClkPer gets added to the output clock momentarily to compensate for the remainder accumulated over time.

A start time for the clock may be chosen (TAI Global Registers 4.8C09 and 4.8C0A and Register 4.8C0A). Also, a compensation direction may be chosen by indicating the amount to add or subtract in register 4.8C04, bit 15 (TrigCompDir).

Note TrigGenAmt should be set to no less than 2 times the TSCLKPer amount.

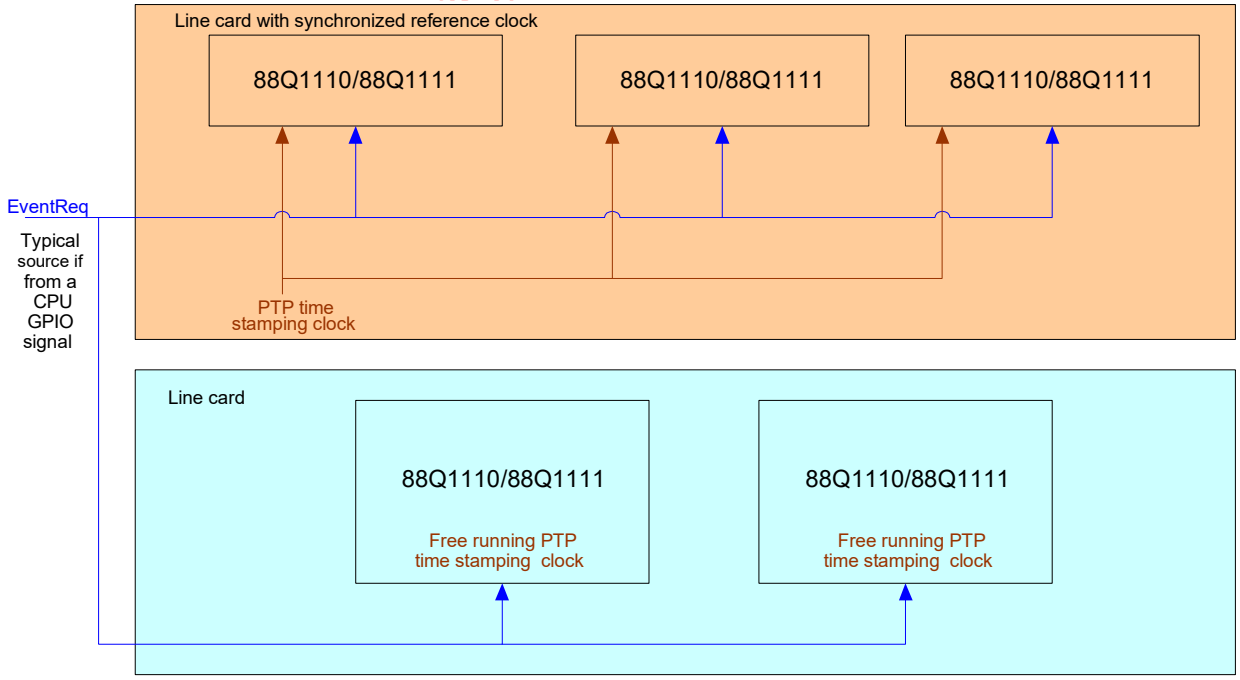
2.21.3.5 Multi-PTP Device Time Sync Function

When PTP is enabled on devices on enterprise, service provider line cards and/or chassis, it is important for various PTP capable devices on the system to have the common notion of PTP Global Time. Typically, a central processing card is present in these chassis, which runs the PTP software for the entire chassis, and all the data line cards send the PTP frames and the time stamp information to the central PTP software entity. Given that there can be so many ports on each line card and each of the line cards may be plugged into the chassis at different times, the PTP Global

Time counter value in each of the PTP devices on the line cards may not be synchronized. Thus, the hardware needs to provide a sure short way for all the PTP capable devices across various line cards, regardless of when the line cards have been powered on, to be synchronized to the same PTP Global Time so that the PTP protocol software does not have to remember the offsets with respect to the PTP Grand Master and also with respect to each of these devices.

The background for this feature is that the PTP nodes derive the time of day via PTP message exchange. The derived time of day consists of 64 bits of seconds and 32 bits of nanoseconds. The PTP slave nodes are expected to derive the frequency and phase offset information with respect to the PTP Grand Master node. The derived offset information is used to periodically adjust various device PTP global timer values. For multi-PTP (Marvell devices only) capable devices, the goal is to synchronize all the nodes with a common 32-bit nanoseconds field and also adjust the nanoseconds field with the computed PTP Grand Master offset information.

Figure 30: Multiple Devices Across Multiple Line Cards Connected by an EventReq Input Signal



This feature is enabled by setting MultiPTPSyncMode (TAI Global Configuration Register 4.8C00) to 0x1. Note that once this bit is enabled, the functions EventRequest and TriggerGen are disabled.

When MultiPTPSyncMode is 0x1, a low-to-high or high-to-low transition on the EventRequest signal triggers transfer of TrigGenAmt to the PTP Global Timer register. At the timer of the low-to-high or high-to-low transition for further software time correlation, the EventCapTime register is also updated with the value of the PTP Global Time before it gets overwritten.

Note that even though the above schema ensures that the PTP Global Time register value is synchronized, the following are possible sources of jitter associated from a system level (which can be avoided):

a) The reference clock sources for various PTP devices that support the multi-sync EventReq interface on the same line card and/or across line cards may not be synchronized.

b) The added delays in the clock path between various PTP devices that support the multi-sync EventReq interface on the same line card and/or across line cards.
c) Inherent operating system related jitter from the point a command is issued to when it actually gets executed in hardware. This is applicable for EventReq pulse generation from a GPIO as well. This tends to be more predictable with real time operating systems.

One guaranteed method to avoid the above mentioned jitter factors a and b is by using a flip-flop with the EventReq as the data input and PTP time stamping clock as the clock input into the flop and the flop output gets distributed with matched delays across various PTP devices that support the multi-sync EventReq. One method to reduce the operating system associated uncertainties, is to choose an operating system in which the scheduler tasks are predictable down to 1's of nanoseconds accuracy.

2.21.4 ReadPlus Command

The PTP Global Time Registers are used as 32-bit global timer value that is running off of the free running PHY clock. A Read from the PTP Global Time Registers must be done with the ReadPlus command. ReadPlus can only be used after powering up the PTP Block. Otherwise, it will return 0. A Read directly to the PTP Global Time Registers without using the ReadPlus command will return 0. The PTP Global Time Registers value can be loaded directly by writing back-to-back to the PTP Global Time Register Byte 3 & 2 – register 4.8C0F first followed by PTP Global Time Register Byte 1 & 0 – register 4.8C1E. ReadPlus can read up to 4 consecutive registers.

Shown below are the formula to program PTP ReadPlus Command Register 0x8E1E and the examples of PTP registers that need ReadPlus commands. The only exception is that PTPAddr for PTP Event Capture Time register does not follow this formula, as shown in example below.

PTPAddr[3:0] = Lower 4 bits of the register address to be read:

PTPReg = 0x0 (4.88xx – 4.89xx)

PTPAddr[4] = '0' (4.88xx)

PTPAddr[4] = '1' (4.89xx)

PTPReg = 0xE (4.8Cxx – 4.8Dxx)

PTPAddr[4] = '0' (4.8Cxx)

PTPAddr[4] = '1' (4.8Dxx)

PTPReg = 0xF (4.8Exx- 4.8Fxx)

PTPAddr[4] = '0' (4.8Exx)

PTPAddr[4] = '1' (4.8Fxx)

For example,

1. Write to Register 4.8E1E = 0x8E0E (ReadPlus command for PTP Global Time Register 4.8C1E to 4.8C0F)
2. Read from Register 4.8E1F (PTP Global Time Register bits [15:0])
3. Read from Register 4.8E1F (PTP Global Time Register bits [31:16])

1. Write to Register 4.8E1E = 0x8F10 (ReadPlus command for TOD Load Point Register 4.8F00 to 4.8F02)
2. Read from Register 4.8E1F (PTP TOD Load Point Register bits [15:0])

3. Read from Register 4.8E1F (PTP TOD Load Point Register bits [31:16])
4. Read from Register 4.8E1F (PTP TOD Control Register 4.8F02)

1. Write to Register 4.8E1E = 0x8F13 (ReadPlus command for TOD Nano Register 4.8F03 to 4.8F04)
2. Read from Register 4.8E1F (PTP TOD Nano Register bits [15:0])
3. Read from Register 4.8E1F (PTP TOD Nano Register bits [31:16])

1. Write to Register 4.8E1E = 0x8F15 (ReadPlus command for TOD Sec Register 4.8F05 to 4.8F07)
2. Read from Register 4.8E1F (PTP TOD Sec Register bits [15:0])
3. Read from Register 4.8E1F (PTP TOD Sec Register bits [31:16])
4. Read from Register 4.8E1F (PTP TOD Sec Register bits [47:32])

1. Write to Register 4.8E1E = 0x8F18 (ReadPlus command for 1722 Nano Register 4.8F08 to 4.8F0B)
2. Read from Register 4.8E1F (PTP 1722 Nano Register bits [15:0])
3. Read from Register 4.8E1F (PTP 1722 Nano Register bits [31:16])
4. Read from Register 4.8E1F (PTP 1722 Nano Register bits [47:32])
5. Read from Register 4.8E1F (PTP 1722 Nano Register bits [63:48])

1. Write to Register 4.8E1E = 0x8F1C (ReadPlus command for TOD Comp Register 4.8F0C to 4.8F1D)
2. Read from Register 4.8E1F (PTP TOD Comp Register bits [15:0])
3. Read from Register 4.8E1F (PTP TOD Comp Register bits [31:16])

1. Write to Register 4.8E1E = 0x8E0A (ReadPlus command for Event Capture Register 4.8D01 and 4.8D02)
2. Read from Register 4.8E1F (PTP Event Capture Register bits [15:0])
3. Read from Register 4.8E1F (PTP Event Capture Register bits [31:16])

1. Write to Register 4.8E1E = 0x8008 (ReadPlus command for Arrival 0 Register 4.8808 to 4.880B)
2. Read from Register 4.8E1F (PTP Arrival 0 Register 4.8808)
3. Read from Register 4.8E1F (PTP Arrival 0 Time Register bits [15:0])
4. Read from Register 4.8E1F (PTP Arrival 0 Time Register bits [31:16])
5. Read from Register 4.8E1F (PTP Arrival 0 SeqID Register 4.880B)

1. Write to Register 4.8E1E = 0x800C (ReadPlus command for Arrival 1 Register 4.880C, 4.881D, 4.881E, 4.880F)
2. Read from Register 4.8E1F (PTP Arrival 1 Register 4.880C)
3. Read from Register 4.8E1F (PTP Arrival 1 Time Register bits [15:0])
4. Read from Register 4.8E1F (PTP Arrival 1 Time Register bits [31:16])
5. Read from Register 4.8E1F (PTP Arrival 1 SeqID Register 4.880F)

1. Write to Register 4.8E1E = 0x8010 (ReadPlus command for Departure Register 4.8900 to 4.8903)
2. Read from Register 4.8E1F (PTP Departure Register 4.8900)
3. Read from Register 4.8E1F (PTP Departure Time Register bits [15:0])
4. Read from Register 4.8E1F (PTP Departure Time Register bits [31:16])
5. Read from Register 4.8E1F (PTP Departure SeqID Register 4.880F)

Note

These registers need to use the ReadPlus command; otherwise, the read-back value is not correct:

-
- 4.8F00 to 4.8F1F (PTP Global Time Array Registers)
- 4.8C1E and 4.8C0F (PTP Global Time [31:0])
- 4.8D01 and 4.8D02 (Event Capture Time [31:0])
- 4.8808 to 4.880B (PTP Arrival 0)
- 4.880C, 4.881D, 4.881E and 4.880F (PTP Arrival 1)
- 4.8900 to 4.8903 (PTP Departure)

2.22 Advanced PHY Diagnostics Features

The 88Q1110/88Q1111 device supports advanced diagnostic features as specified in “Advanced Diagnostic Features for Automotive Ethernet PHYs” by OPEN Alliance.

Table 75: Supported Advanced PHY Diagnostic Features

Group	Group Name	Parameter	Parameter Name	Description	Support
DCQ	Dynamic Channel	MSE	Mean Square Error	The MSE (Mean Square Error) value of the symbol detection shall be determined in a standardized way	Yes
		SQI	Signal Quality Index	A classification of the signal quality in 8 stages (3 bit) shall be carried out	Yes
		pMSE	peak MSE	To identify short time noise (pulses) a peak MSE value shall be provided (for 100BASE-T1)	Yes
HDD	Harness Defect Detection	OS	OPEN/SHORT detection	Cable-Harness errors (short circuit or open line) shall be detected	Both bus wires OPEN Bus wires SHORT One bus wire OPEN Both bus wires SHORT to GND/VBAT
LQ	LinkQuality	LTT	Link-training time	The time of the last link training shall be stored	Yes
		LRT	Local Receiver Time	The timing of the local receiver shall be stored	Yes
		RRT	Remote Receiver Time	The timing of the remote receiver shall be stored	Yes
		LFL	Link Failures and Losses	Number of link losses since the last power cycle shall be stored	Yes
		COM	Communication ready	Optimized Link Status information. Signals when communication is possible	Yes
POL	Polarity detection/ correction	DET	Polarity detect	According to the IEEE specifications of 100BASE-T1	Yes
		COR	Polarity correct	According to the IEEE specifications of 100BASE-T1	Yes

2.23 Electromagnetic Compatibility (EMC) Performance

2.23.1 EMC Overview

The 88Q1110/88Q1111 device is designed to have low emission and high immunity performance. It also provides high ESD tolerance level per various industry standards.

2.23.1.1 Emission

- Ultra-low emission at GPS bands.
- Meets corresponding OPEN Alliance TC1 specification.

2.23.1.2 Immunity

- 200 mA BCI extended to 500MHz.
- Tolerates narrow band interference up to 100-140V/m electronic field strength across 0.5-3GHz frequency band.
- Meets corresponding OPEN Alliance TC1 specification.

2.23.1.3 Electrostatic Discharge

- Human Body Model (HBM): ±2kV, ±6kV (MDI pins)
- Charged Device Model (CDM): ±500V for all pins except corner pins. ±750V for corner pins.
- Meets corresponding OPEN Alliance TC1 specification.

3 General Registers

Table 76 defines the register types used in the register map.

Table 76: Register Types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs.
RES	Reserved. All reserved bits are read as zero unless otherwise noted.
Retain	The register value is retained after software reset is executed.
RO	Read only.
ROC	Read only clear. After read, register field is cleared.
R/W	Read and Write with initial value indicated.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, register field is cleared to zero.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete.
Update	Value written to the register field does not take effect until soft reset is executed.
WO	Write only. Reads from this type of register field return undefined data.
NR	Non-Rollover Register

3.1 PHY MDIO Registers

The device supports Clause 45 XMDIO register access protocol. The device also supports:

- Clause 22 MDIO access to registers in Clause 45 XMDIO register space using registers 13 and 14 as specified in the IEEE Annex 22D
- New Clause 22 MDIO access to registers in Clause 45 XMDIO register space, using register 13 and 14 as specified in the IEEE Annex 22D, but in a different way

3.2 PMA/PMD Registers

Table 77: PMA/PMD – Registers Register Map

Register Name	Register Address	Table and Page
PMA/PMD Control 1	Device 1, Register 0x0000	Table 78, p. 111
PMA/PMD Status 1	Device 1, Register 0x0001	Table 79, p. 112
PMA/PMD Device Identifier 1	Device 1, Register 0x0002	Table 80, p. 112
PMA/PMD Device Identifier 2	Device 1, Register 0x0003	Table 81, p. 112
PMA/PMD Speed Ability	Device 1, Register 0x0004	Table 82, p. 113
PMA/PMD Devices in Package 1	Device 1, Register 0x0005	Table 83, p. 113
PMA/PMD Devices in Package 2	Device 1, Register 0x0006	Table 84, p. 114
10G PMA/PMD Control 2	Device 1, Register 0x0007	Table 85, p. 114
PMA/PMD Status 2 Register	Device 1, Register 0x0008	Table 86, p. 115
PMD Transmit Disable Register	Device 1, Register 0x0009	Table 87, p. 116
PMD Receive Signal Detect Register	Device 1, Register 0x000A	Table 88, p. 116
PMA/PMD Extended Ability Register	Device 1, Register 0x000B	Table 89, p. 116
PMA/PMD Device Identifier 1	Device 1, Register 0x000E	Table 90, p. 117
PMA/PMD Device Identifier 2	Device 1, Register 0x000F	Table 91, p. 117
PMA/PMD Extended Ability Register	Device 1, Register 0x0012	Table 92, p. 117
100BASE-T1 PMA/PMD Control Register	Device 1, Register 0x0834	Table 93, p. 118
100BASE-T1 PMA/PMD Test Control Register	Device 1, Register 0x0836	Table 94, p. 118

Table 78: PMA/PMD Control 1
Device 1, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x1	0x1	This register will soft reset the copper unit. 1 = Reset 0 = Normal
14	Reserved	R/W	0x0	0x0	Set to 0
13	Speed Select	RO	0x1	Retain	bit 6, bit 13 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Bits 5:2 determine speed
12	Reserved	R/W	0x0	0x0	Set to 0
11	Low Power	R/W	See Descr.	0x0	This register will power down the copper unit. At HW reset, this register gets default value from p*_phy_pwrdn_a 1 = Power down 1 = Low Power mode 0 = Normal
10:7	Reserved	R/W	0x0	0x0	Set to 0s
6	Speed Select	RO	0x0	Retain	bit 6, bit 13 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Bits 5:2 determine speed
5:2	Speed Select	RO	0x3	0x3	0011 = Operation at 100 Mbps
1	Reserved	R/W	0x0	0x0	Set to 0
0	PMA Loopback	R/W	0x0	0x0	1 = PMA transmit loopback transmit data to PMA receive 0 = Normal operation

Table 79: PMA/PMD Status 1
Device 1, Register 0x0001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	Set to 00000000
7	Fault	RO	0x0	0x0	1 = Fault condition 0 = No fault condition Bit 1.0001.7 = 1.0008.11 OR 1.0008.10
6:3	Reserved	RO	0x0	0x0	Set to 0000
2	Link Status	RO, LL	0x0	0x0	1 = PMA/PMD link up 0 = PMA/PMD link down Bit 1.0001.2 is the inverse of 1.0008.10
1	Low Power Ability	RO	0x1	0x0	1 = PMA/PMD supports Low Power
0	Reserved	RO	0x0	0x0	Set to 0

Table 80: PMA/PMD Device Identifier 1
Device 1, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	Marvell OUI is 00:0A:C2 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit18

Table 81: PMA/PMD Device Identifier 2
Device 1, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	0x02	0x02	Organizationally Unique Identifier bits 19:24 00 0010 ^.....^ bit 19...bit24
9:4	Model Number	RO	110010	110010	Represents Automotive PHY products.
3:0	Revision Number	RO	0001	0001	Identifies the revision of the Device.

Table 82: PMA/PMD Speed Ability
Device 1, Register 0x0004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	Set to 000000000
6	10M Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 10 Mbps
5	100M Capable	RO	0x1	0x1	1 = PMA/PMD is capable of operating at 100 Mbps
4	1000M Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 1000 Mbps
3:1	Reserved	RO	0x0	0x0	Set to 000
0	10G Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 10 Gbps

Table 83: PMA/PMD Devices in Package 1
Device 1, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	Set to 00000000
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-Negotiation present in package
6	Reserved	RO	0x0	0x0	Set to 0
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS present in package 0 = DTE XS not present in package
4	PHY XS Present	RO	0x0	0x0	1 = PHY XS present in package 0 = PHY XS not present in package
3	PCS Present	RO	0x1	0x1	1 = PCS present in package 0 = PCS not present in package
2	WIS Present	RO	0x0	0x0	1 = WIS present in package 0 = WIS not present in package
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD present in package 0 = PMA/PMD not present in package
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package

Table 84: PMA/PMD Devices in Package 2
Device 1, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Vendor Specific Device 2 Present	RO	0x0	0x0	1 = Vendor-specific device 2 present 0 = Vendor-specific device 2 not present
14	Vendor Specific Device 1 Present	RO	0x0	0x0	1 = Vendor-specific device 1 present 0 = Vendor-specific device 1 not present
13:0	Reserved	RO	0x0000	0x0000	Set to 00000000000000

Table 85: 10G PMA/PMD Control 2
Device 1, Register 0x0007

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	R/W	0x000	0x000	Set to 000000000000
5:0	PMA/PMD Type	R/W	0x3D	0x3D	111101 = 100BASE-T1 001110 = 100BASE-TX 001101 = 1000BASE-KX 001100 = 1000BASE-T 001011 = 10GBASE-KR 001010 = 10GBASE-KX4 001001 = 10GBASE-T 001000 = 10GBASE-LRM 000111 = 10GBASE-SR 000110 = 10GBASE-LR 000101 = 10GBASE-ER 000100 = 10GBASE-LX4 000011 = 10GBASE-SW 000010 = 10GBASE-LW 000001 = 10GBASE-EW 000000 = 10GBASE-CX4 This register is ignored by the PHY. Actual PMA/PMD used is determined by auto-negotiations, or PHY mode select.

Table 86: PMA/PMD Status 2 Register
Device 1, Register 0x0008

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Device Present	RO	0x2	0x2	10 = Device responding at this address 11 = No device responding at this address 01 = No device responding at this address 00 = No device responding at this address
13	Transmit Fault Ability	RO	0x0	0x0	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path
12	Receive Fault Ability	RO	0x1	0x1	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path
11	Transmit Fault	RO,LH	0x0	0x0	1 = Fault condition on transmit path 0 = No fault condition on transmit path
10	Receive Fault	RO,LH	0x0	0x0	1 = Fault condition on receive path 0 = No fault condition on receive path
9	Extended Abilities	RO	0x0	0x0	1 = PMA/PMD has extended abilities listed in register 1.11 0 = PMA/PMD does not have extended abilities
8	PMD Transmit Disable Ability	RO	0x0	0x0	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path
7	10GBASE-SR Ability	RO	0x0	0x0	1 = PMA/PMD is able to perform 10GBASE-SR 0 = PMA/PMD is not able to perform 10GBASE-SR
6	10GBASE-LR Ability	RO	0x0	0x0	1 = PMA/PMD is able to perform 10GBASE-LR 0 = PMA/PMD is not able to perform 10GBASE-LR
5	10GBASE-ER Ability	RO	0x0	0x0	1 = PMA/PMD is able to perform 10GBASE-ER 0 = PMA/PMD is not able to perform 10GBASE-ER
4	10GBASE-LX4 Ability	RO	0x0	0x0	1 = PMA/PMD is able to perform 10GBASE-LX4 0 = PMA/PMD is not able to perform 10GBASE-LX4
3	10GBASE-SW Ability	RO	0x0	0x0	1 = PMA/PMD is able to perform 10GBASE-SW 0 = PMA/PMD is not able to perform 10GBASE-SW
2	10GBASE-LW Ability	RO	0x0	0x0	1 = PMA/PMD is able to perform 10GBASE-LW 0 = PMA/PMD is not able to perform 10GBASE-LW
1	10GBASE-EW Ability	RO	0x0	0x0	1 = PMA/PMD is able to perform 10GBASE-EW 0 = PMA/PMD is not able to perform 10GBASE-EW
0	Loopback Ability	RO	0x1	0x1	1 = PMA has the ability to perform a local loopback function 0 = PMA does not have the ability to perform a local loopback function

Table 87: PMD Transmit Disable Register
Device 1, Register 0x0009

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RO	0x0000	0x0000	Always read 0
0	Global PMD Transmit Disable	R/W	0x0	Retain	1 = Transmitter disable 0 = Transmitter enable

Table 88: PMD Receive Signal Detect Register
Device 1, Register 0x000A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RO	0x0000	0x0000	
0	Global PMD Receive Signal Detect	RO	0x0	Retain	1 = Signal detected on receive 0 = Signal not detected on receive

Table 89: PMA/PMD Extended Ability Register
Device 1, Register 0x000B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	Always read 0
11	BASE-T1 Extended Abilities	RO	0x1	0x1	1 = PMA/PMD has BASE-T1 extended abilities listed in register 1.18
10	40G/100G Extended Abilities	RO	0x0	0x0	0 = PMA/PMD does not have 40G/100G extended abilities listed in register 1.13
9	P2MP Ability	RO	0x0	0x0	0 = PMA/PMD does not have P2MP abilities listed in register 1.12
8	10BASE-T	RO	0x0	0x0	0 = PMA/PMD is not able to perform 10BASE-T
7	100BASE-TX	RO	0x0	0x0	0 = PMA/PMD is not able to perform 100BASE-TX
6	1000BASE-KX	RO	0x0	0x0	0 = PMA/PMD is not able to perform 1000BASE-KX
5	1000BASE-T	RO	0x0	0x0	0 = PMA/PMD is not able to perform 1000BASE-T
4	10GBASE-KR	RO	0x0	0x0	0 = PMA/PMD is not able to perform 10GBASE-KR
3	10GBASE-KX4	RO	0x0	0x0	0 = PMA/PMD is not able to perform 10GBASE-KX4
2	10GBASE-T	RO	0x0	0x0	0 = PMA/PMD is not able to perform 10GBASE-T
1	10GBASE-LRM	RO	0x0	0x0	0 = PMA/PMD is not able to perform 10GBASE-LRM
0	10GBASE-CX4	RO	0x0	0x0	0 = PMA/PMD is not able to perform 10GBASE-CX4

Table 90: PMA/PMD Device Identifier 1
Device 1, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	Marvell OUI is 00:0A:C2 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit18

Table 91: PMA/PMD Device Identifier 2
Device 1, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	0x02	0x02	Organizationally Unique Identifier bits 19:24 00 0010 ^.....^ bit 19...bit24
9:4	Model Number	RO	110010	110010	Represents Automotive PHY products.
3:0	Revision Number	RO	0001	0001	Identifies the revision of the Device.

Table 92: PMA/PMD Extended Ability Register
Device 1, Register 0x0012

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RO	0x0000	0x0000	Set to 000000000000
0	100BASE-T1 Ability	RO	0x1	0x1	1 = PMA/PMD is able to perform 100BASE-T1 0 = PMA/PMD is not able to perform 100BASE-T1

Table 93: 100BASE-T1 PMA/PMD Control Register
Device 1, Register 0x0834

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MASTER-SLAVE Manual Configuration Enable	R/W	0x1	0x1	Value always 1, writes ignored
14	MASTER-SLAVE Configuration Value	R/W	Value configured.	Retain	1 = Configure PHY as Master 0 = Configure PHY as Slave
13:4	Reserved	RO	0x000	0x000	Set to 000000000000
3:0	Type Selection	R/W	0x0	0x0	0000 = 100BASE-T1

Table 94: 100BASE-T1 PMA/PMD Test Control Register
Device 1, Register 0x0836

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	100BASE-T1 Test Mode Control	R/W	0x0	0x0	11x = Reserved 101 = Test mode 5 100 = Test mode 4 011 = Reserved 010 = Test mode 2 001 = Test mode 1 000 = Normal operation
12:0	Reserved	R/W	0x0000	0x0000	Set to 000000000000

3.3 Control Registers

Table 95: Control Registers – Register Map

Register Name	Register Address	Table and Page
Copper Control Register 1	Device 3, Register 0x0000	Table 96, p. 122
Copper Control Register 2	Device 3, Register 0x8000	Table 97, p. 122
100BASE-T1 Status Register	Device 3, Register 0x8008	Table 98, p. 123
100BASE-T1 Status Register	Device 3, Register 0x8009	Table 99, p. 124
PHY Status	Device 3, Register 0x800A	Table 100, p. 124
PHY REM/LOC Counters	Device 3, Register 0x800B	Table 101, p. 125
Copper Specific Interrupt Enable Register	Device 3, Register 0x8012	Table 102, p. 125
Copper Interrupt Status Register	Device 3, Register 0x8013	Table 103, p. 126
Interrupt Status Register	Device 3, Register 0x8017	Table 104, p. 126
Link Drop Counter	Device 3, Register 0x8020	Table 105, p. 127
MAC Specific Control Register	Device 3, Register 0x8210	Table 106, p. 127
MAC Specific Interrupt Enable Register	Device 3, Register 0x8212	Table 107, p. 128
MAC Specific Status Register	Device 3, Register 0x8213	Table 108, p. 128
Tx FIFO Overflow/Underflow Counter	Device 3, Register 0x8214	Table 109, p. 128
Counter Control Register	Device 3, Register 0x8220	Table 110, p. 129
Bad Link Counter	Device 3, Register 0x8221	Table 111, p. 129
Bad SSD Counter	Device 3, Register 0x8222	Table 112, p. 129
Bad ESD Counter	Device 3, Register 0x8223	Table 113, p. 130
Rx Error Counter	Device 3, Register 0x8224	Table 114, p. 130
Receiver Status	Device 3, Register 0x8230	Table 115, p. 131
Link Training Time	Device 3, Register 0x8231	Table 116, p. 131
Local Receiver Time	Device 3, Register 0x8232	Table 117, p. 132
Remote Receiver Time	Device 3, Register 0x8233	Table 118, p. 132
Link Failures and Losses	Device 3, Register 0x8234	Table 119, p. 132
Communication Ready Status	Device 3, Register 0x8235	Table 120, p. 133
Mean Square Error (DCQ.MSE)	Device 3, Register 0x8236	Table 121, p. 133
Worst Case Mean Square Error (WC_DCQ.MSE)	Device 3, Register 0x8237	Table 122, p. 133
Peak Mean Square Error	Device 3, Register 0x8238	Table 123, p. 134
DCQ MSE enable	Device 3, Register 0x8239	Table 124, p. 134
Interrupt Enable	Device 3, Register 0x8300	Table 125, p. 134
Interrupt Status	Device 3, Register 0x8301	Table 126, p. 134
GPIO/LED Control	Device 3, Register 0x8302	Table 127, p. 135
GPIO/LED Control	Device 3, Register 0x8303	Table 128, p. 135
GPIO/LED Control	Device 3, Register 0x8304	Table 129, p. 135
GPIO/LED Control	Device 3, Register 0x8305	Table 130, p. 136
LED Function Control Register	Device 3, Register 0x8310	Table 131, p. 138
LED Polarity Control Register	Device 3, Register 0x8311	Table 132, p. 139

Table 95: Control Registers – Register Map

Register Name	Register Address	Table and Page
LED Timer Control Register	Device 3, Register 0x8312	Table 133, p. 140
TDR Threshold of Negative Threshold	Device 3, Register 0x850B	Table 134, p. 140
TDR Threshold of Negative Threshold	Device 3, Register 0x850C	Table 135, p. 141
TDR Result	Device 3, Register 0x8510	Table 136, p. 141
Advanced VCT Wait for Time Up for pwr_mgt	Device 3, Register 0x8511	Table 137, p. 141
Advanced VCT Wait for 3 us Before Sending Out New Pulse	Device 3, Register 0x8512	Table 138, p. 141
100BASE-T Pair Swap and Polarity	Device 3, Register 0x8515	Table 139, p. 141
Advanced VCT Control	Device 3, Register 0x8517	Table 140, p. 142
Advanced VCT Sample Point Distance	Device 3, Register 0x8518	Table 141, p. 142
Advanced VCT Cross Pair Positive Threshold	Device 3, Register 0x8519	Table 142, p. 143
Advanced VCT Same Pair Impedance Positive Threshold 0 and 1	Device 3, Register 0x851A	Table 143, p. 143
Advanced VCT Same Pair Impedance Positive Threshold 2 and 3	Device 3, Register 0x851B	Table 144, p. 143
Advanced VCT Same Pair Impedance Positive Threshold 4 and Transmit Pulse Control	Device 3, Register 0x851C	Table 145, p. 144
TDR Threshold of Negative Threshold	Device 3, Register 0x851D	Table 146, p. 144
DSP VCT	Device 3, Register 0x8580	Table 147, p. 145
Copper Port Packet Generation	Device 3, Register 0x8610	Table 148, p. 145
Copper Port Packet Size	Device 3, Register 0x8611	Table 149, p. 146
Checker Control	Device 3, Register 0x8612	Table 150, p. 146
Pktgen Control	Device 3, Register 0x8613	Table 151, p. 146
Copper Port Packet Counters	Device 3, Register 0x8614	Table 152, p. 147
Copper Port CRC Counters	Device 3, Register 0x8615	Table 153, p. 147
BIST Control	Device 3, Register 0x8617	Table 154, p. 147
BIST Status	Device 3, Register 0x8618	Table 155, p. 147
BIST Counters	Device 3, Register 0x8619	Table 156, p. 148
Misc Test	Device 3, Register 0x861A	Table 157, p. 148
Temperature Sensor 1	Device 3, Register 0x861B	Table 158, p. 148
Temperature Sensor 2	Device 3, Register 0x861C	Table 159, p. 149
PTP Control Register	Device 3, Register 0x8630	Table 160, p. 150
PTP Control Register2 mac_address[15:0]	Device 3, Register 0x8631	Table 161, p. 150
PTP Control Register3 mac_address [31:16]	Device 3, Register 0x8632	Table 162, p. 151
PTP Control Register 4 mac_address [47:32]	Device 3, Register 0x8633	Table 163, p. 151
PTP Control Register 5 other fields	Device 3, Register 0x8634	Table 164, p. 151
DISABLE_IN Control Register	Device 3, Register 0x8640	Table 165, p. 151
LPSD Control Register	Device 3, Register 0x8700	Table 166, p. 152
LPSD Control Register 2	Device 3, Register 0x8701	Table 167, p. 152
Sleep/Wake Request	Device 3, Register 0x8702	Table 168, p. 153
Sleep Status	Device 3, Register 0x8703	Table 169, p. 153

Table 95: Control Registers – Register Map

Register Name	Register Address	Table and Page
Wakeup Status	Device 3, Register 0x8704	Table 170, p. 154
Sleep/Wakeup Interrupt Status	Device 3, Register 0x8705	Table 171, p. 154
Sleep/Wakeup Interrupt Enable	Device 3, Register 0x8706	Table 172, p. 155
Sleep/Wakeup Configuration	Device 3, Register 0x8707	Table 173, p. 155
Sleep/Wakeup Interrupt Status 2	Device 3, Register 0x870A	Table 174, p. 156
Sleep/Wakeup Interrupt Enable 2	Device 3, Register 0x870B	Table 175, p. 156

Table 96: Copper Control Register 1
Device 3, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Reset	R/W, SC	0x0	SC	Copper Software Reset Affects dev1, dev3, dev7 register. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. 1 = Enable loopback 0 = Disable loopback
13	Speed MSB	RO	0x0	0x0	Always 0
12	Reserved	RO	Always 0	Always 0	
11	Port Power Down	R/W	See Descr.	0x0	0 = Power up 1 = Power down
10:7	Reserved	RO	Always 000000	Always 000000	
6	Speed LSB	RO	0x1	0x1	Always 1
5:0	Reserved	RO	Always 000000	Always 000000	

Table 97: Copper Control Register 2
Device 3, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	
14	Copper Line Loopback	R/W	0x0	0x0	1 = Enable loopback of MDI to MDI 0 = Normal operation
13:10	Reserved	R/W	0x0	Retain	
9	PCS Automatic Polarity Detection	R/W	0x0	Retain	When this bit is a 1 and the PCS is slave, the PCS Rx will detect the polarity, and if there is a polarity swap, the Tx polarity will be reversed. The detected Rx polarity status is shown in register 3.8009.1.
8	Reserved	R/W	0x0	Retain	
7	SyncE Link Down Disable	R/W	0x0	Retain	Selects what the SyncE clock output is during link down. 1 = SyncE clock is low 0 = SyncE clock is the local 25 MHz clock

Table 97: Copper Control Register 2
Device 3, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
6	SyncE CLK Enable	R/W	0x0	Retain	1 = Enable SyncE CLK to go out on the GPIO pin 0 = Disable SyncE
5:2	Reserved	R/W	0x0	Retain	
1	Tx Polarity Reversal Enable	R/W	0x0	Retain	1 = Tx PCS polarity is reversed 0 = Tx PCS Polarity is not reversed
0	Disable Jabber	R/W	0x0	Retain	1 = Disable jabber function 0 = Enable jabber function

Table 98: 100BASE-T1 Status Register
Device 3, Register 0x8008

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Master/Slave Configuration Fault	RO	0x0	0x0	1 = Master/Slave configuration fault detected 0 = No Master/Slave configuration fault detected
14	Master/Slave Configuration Resolution	RO	0x0	0x0	1 = Local PHY configuration resolved to Master 0 = Local PHY configuration resolved to Slave
13	Local Receiver Status	RO	0x0	0x0	1 = Local receiver OK 0 = Local receiver is not OK
12	Remote Receiver Status	RO	0x0	0x0	1 = Remote receiver OK 0 = Remote receiver not OK
11:10	Reserved	RO	Always 000000	Always 000000	
9	Copper Link Status	RO, LL	0x0	0x0	This register bit indicates when the link was down since the last read. For the current link status, either read this register back-to-back or read register 3.8009.2 (Copper Link Real Time). 1 = Link is up 0 = Link is down
8	Jabber Detect	RO, LH	0x0	0x0	1 = Jabber condition detected 0 = Jabber condition not detected
7:0	Idle Error Count	RO, ROC	0x00	Retain	Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.

Table 99: 100BASE-T1 Status Register
Device 3, Register 0x8009

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	Always 0	Always 0	
4	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
3	Autoneg Resolved	RO	0x0	0x0	1 = Resolved 0 = Not resolved
2	Copper Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
1	Polarity (real time)	RO	0x0	0x0	1 = Reversed 0 = Normal
0	Jabber (real time)	RO	0x0	0x0	1 = Jabber 0 = No jabber

Table 100: PHY Status
Device 3, Register 0x800A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Idle Error	RO, ROC	0x00	Retain	Idle Error Counter This register reports the idle error count since the last time the register was read. The counter pegs at 0xFF and does not roll over. Same as 3.8008.7:0.
7	DSP SNR Margin OK	RO	0x0	Retain	1 = OK
6	Descram-bler/Polar-ity/Alignment Status	RO	0x0	Retain	1= OK
5	Scrambler Status (to PHY CTRL)	RO	0x0	Retain	1 = OK (only valid for Master)
4	Polarity (Real Time)	RO	0x0	Retain	1 = Polarity swapped
3	PHY_CTRL in SEND_N state	RO	0x0	Retain	1 = PHY_CTRL in SEND_N state
2	Link Status(Real Time)	RO	0x0	Retain	1 = Link OK
1	Remote Receiver Status	RO	0x0	Retain	1 = OK
0	Local Receiver Status	RO	0x0	Retain	1 = OK

Table 101: PHY REM/LOC Counters
Device 3, Register 0x800B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	REM_RCVR_ NOT_OK counter	RO, ROC	0x00	Retain	This register reports the number of times the REM_ RCVR_STATUS was NOT_OK since the last time the register was read. The counter pegs at 0xFF and does not roll over
7:0	LOC_RCVR_ NOT_OK counter	RO, ROC	0x00	Retain	This register reports the number of times the LOC_RCVR_ STATUS was NOT_OK since the last time the register was read. The counter pegs at 0xFF and does not roll over

Table 102: Copper Specific Interrupt Enable Register
Device 3, Register 0x8012

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Auto-Negotiation Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
14:13	Reserved	RO	Always 0	Always 0	
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7:4	Reserved	R/W	0x0	Retain	
3	FLP Exchange Complete But No Link Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	Reserved	R/W	0x0	Retain	
1	Polarity Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Jabber Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 103: Copper Interrupt Status Register
Device 3, Register 0x8013

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Auto-Negotiation Error	RO,LH	0x0	0x0	An error is said to occur if MASTER/SLAVE does not resolve, or link does not come up after negotiation is completed. 1 = Auto-Negotiation error 0 = No Auto-Negotiation error
14:13	Reserved	RO	Always 0	Always 0	
12	Copper Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Copper Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Copper Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Copper Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	Copper False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7:4	Reserved	RO	Always 0	Always 0	
3	DME Exchange Complete But No Link	RO,LH	0x0	0x0	1 = DME exchange completed, but link not established 0 = No event detected
2	Reserved	RO	Always 0	Always 0	
1	Polarity Changed	RO,LH	0x0	0x0	1 = Polarity changed 0 = Polarity not changed
0	Jabber	RO,LH	0x0	0x0	1 = Jabber 0 = No jabber

Table 104: Interrupt Status Register
Device 3, Register 0x8017

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RO	0x0000	0x0000	
0	Port 0 Interrupt	RO	0x0	0x0	If there is at least 1 copper port, then this bit indicates port 0's interrupt status; otherwise, it is invalid. 1 = Interrupt active on port 0 0 = No interrupt active on port 0

Table 105: Link Drop Counter
Device 3, Register 0x8020

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x0C	Retain	
7:0	Link Drop Counter	RO, ROC	0x00	Retain	This counter increments every time the link transitions from up to down. The counter saturates at 8'hFF (max value) and is cleared when read.

Table 106: MAC Specific Control Register
Device 3, Register 0x8210

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Copper Transmit FIFO Depth	R/W	0x1	Retain	00 = 2KB packet @ ±100ppm 01 = 10KB packet @ ±100ppm 10 = 18KB packet @ ±100ppm 11 = 27KB packet @ ±100ppm
13	Enable TCLK During Power Down	R/W	0x0	Retain	1 = TCLK toggles during power down 0 = TCLK is off during power down
12:10	Reserved	R/W	0x0	Retain	Reserved
9	Power Down APLL's 125MHz Clock Output	R/W	0x0	Retain	1 = APLL's 125MHz Clock is Powered Down 0 = Power
8	Power Down APLL's 500MHz Clock Output	R/W	0x0	Retain	1 = APLL's 500MHz Clock is Powered Down 0 = Power
7:3	Reserved	R/W	0x00	Retain	
2	Power Down APLL's 400MHz Clock Output	R/W	0x0	Retain	1 = APLL's 400MHz Clock is Powered Down 0 = Power
1	Reserved	R/W	0x0	Retain	Reserved
0	Reserved	R/W	0x0	Retain	Reserved

Table 107: MAC Specific Interrupt Enable Register
Device 3, Register 0x8212

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	
7	FIFO Over/Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6:4	Reserved	R/W	0x0	Retain	
3	FIFO Idle Inserted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	FIFO Idle Deleted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1:0	Reserved	R/W	0x0	Retain	

Table 108: MAC Specific Status Register
Device 3, Register 0x8213

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	Always 00	Always 00	
7	FIFO Over/Underflow	RO,LH	0x0	0x0	1 = Over/underflow error 0 = No FIFO error
6:4	Reserved	RO	Always 0	Always 0	
3	FIFO Idle Inserted	RO,LH	0x0	0x0	1 = Idle inserted 0 = No idle inserted
2	FIFO Idle Deleted	RO,LH	0x0	0x0	1 = Idle deleted 0 = Idle not deleted
1:0	Reserved	RO	Always 0	Always 0	

Table 109: Tx FIFO Overflow/Underflow Counter
Device 3, Register 0x8214

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Tx FIFO Over-flow/Underflow Counter	RO, ROC	0x0000	Retain	16-bit counter for TxFIFO overflow/underflow error. The counter saturates at 16'hFFFF (max value) and will clear on read.

Table 110: Counter Control Register
Device 3, Register 0x8220

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0000	Retain	
1	Bad Link/SDD/ESD Counter Control	R/W	0x0	Retain	Controls the counters in registers 3.8221 to 3.8223. 1 = The counters count how many cycles. 0 = The counters count how many events.
0	Rx Error Counter Control	R/W	0x0	Retain	Controls the counters in register 3.8224. 1 = The counters count how many cycles. 0 = The counters count how many events.

Table 111: Bad Link Counter
Device 3, Register 0x8221

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Bad Link Counter	RO, ROC	0x0000	Retain	If register 3.8220.1 = 1, it counts each cycles of RX_ER assertion in the LINK FAILED state. If register 3.8220.1 = 0, it counts each events of RX_ER assertion in the LINK FAILED state. The counter saturates at 16'hFFFF (max value) and will clear on read.

Table 112: Bad SSD Counter
Device 3, Register 0x8222

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Bad SSD Counter	RO, ROC	0x0000	Retain	If register 3.8220.1 = 1, it counts each cycles of RX_ER assertion in the BAD SSD state. If register 3.8220.1 = 0, it counts each events of RX_ER assertion in the BAD SSD state. The counter saturates at 16'hFFFF (max value) and will clear on read.

Table 113: Bad ESD Counter
Device 3, Register 0x8223

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Bad ESD Counter	RO, ROC	0x0000	Retain	If register 3.8220.1 = 1, it counts each cycles of RX_ER assertion in the BAD ESD2, BAD END, and Rx ERROR states. If register 3.8220.1 = 0, it counts each events of RX_ER assertion in the BAD ESD2, BAD END, and Rx ERROR states. The counter saturates at 16'hFFFF (max value) and will clear on read.

Table 114: Rx Error Counter
Device 3, Register 0x8224

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Rx Error Counter	RO, ROC	0x0000	Retain	If register 3.8220.0 = 1, it counts each cycles of RX_ER assertion in the 25 MHz domain. If register 3.8220.0 = 0, it counts each event of RX_ER assertion in the 25 MHz domain. The counter saturates at 16'hFFFF (max value) and will clear on read.

Table 115: Receiver Status
Device 3, Register 0x8230

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Current SQI Level	RO	0x0	0x0	This register records the current Signal Quality Index SQI level is listed from 0 to 15 in accordance with the ascending signal quality. SQI is only valid to be read after linkup. SQI is not a good index during the linkup process or no link.
11:8	Lowest SQI Level	RO	0x0	0x0	This register records the lowest SQI value recorded since the last read of this register.
7:6	Reserved	RO	0x0	0x0	
5	Link Status	RO	0x0	0x0	1 = Link OK
4	Remote Receiver Status	RO	0x0	0x0	1 = Remote receiver status OK
3	Local Receiver Status	RO	0x0	0x0	1 = Local receiver status OK
2	Polarity Done Status	RO	0x0	0x0	1 = Polarity done
1	Alignment Done Status	RO	0x0	0x0	1 = Alignment done
0	Descrambler Lock Status	RO	0x0	0x0	1 = Descrambler locked

Table 116: Link Training Time
Device 3, Register 0x8231

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	
7:0	Link Training Time	RO	0x00	Retain	Information about the Link Training time of the last link training (loc_rcvr_status AND rem_rcvr_status) 0x00 = 0ms 0x01 = 1ms .. 0x64 = 100ms .. 0xFA = 250ms 0xFB = more than 250ms .. = n/a 0xFF = measurement not possible

Table 117: Local Receiver Time
Device 3, Register 0x8232

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	
7:0	Local Receiver Time	RO	0x00	Retain	Time until loc_receiver = OK 0x00 = 0ms 0x01 = 1ms .. 0x64 = 100ms .. 0xFA = 250ms 0xFB = more than 250ms .. = n/a 0xFF = measurement not possible

Table 118: Remote Receiver Time
Device 3, Register 0x8233

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	
7:0	Remote Receiver Time	RO	0x00	Retain	Time until remote_receiver = OK 0x00 = 0ms 0x01 = 1ms .. 0x64 = 100ms .. 0xFA = 250ms 0xFB = more than 250ms .. = n/a 0xFF = measurement not possible

Table 119: Link Failures and Losses
Device 3, Register 0x8234

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Link Losses	RO	0x00	Retain	Number of Link Losses occurred since last power cycle (0...63)
9:0	Link Failures	RO	0x000	Retain	Number of Link Failures NOT causing a link loss (SSD failure, ESD failure, etc.) since last power cycle (0...1023) 0x000 = 0 failure 0x001 = 1 failure ... 0x3FE = 1022 failures 0x3FF = 1023 or more failures occurred

Table 120: Communication Ready Status
Device 3, Register 0x8235

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RO	0x0000	Retain	
0	Communication Ready Status	RO	0x0	Retain	Information on communication_ready 0 = communication_ready is NOT_OK/FALSE 1 = communication_ready is OK_TRUE

Table 121: Mean Square Error (DCQ.MSE)
Device 3, Register 0x8236

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	Retain	
9	Mean Square Error Value Valid	RO	0x0	Retain	1 = Invalid 0 = Valid
8:0	Mean Square Error Value	RO	0x000	Retain	0x000 : MSE = 0 0x001 : MSE = 1 ... 0x1FE : MSE = 510 0x1FF : MSE = 511

Table 122: Worst Case Mean Square Error (WC_DCQ.MSE)
Device 3, Register 0x8237

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	Retain	
9	Worst Case Mean Square Error Value Valid	RO	0x0	Retain	1 = Invalid 0 = Valid
8:0	Worst Case Mean Square Error Value	RO	0x000	Retain	0x000 : MSE = 0 0x001 : MSE = 1 ... 0x1FE : MSE = 510 0x1FF : MSE = 511

Table 123: Peak Mean Square Error
Device 3, Register 0x8238

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Worst Case Peak Mean Square Error Value since last read	RO	0x00	Retain	0x00 : peakMSE = 0 0x01 : peakMSE = 1 ... 0x3E : peakMSE = 62 0x3F : peakMSE = 63 0x4E - 0xFE : value invalid 0xFF : Measurement not possible
7:0	Current Peak Mean Square Error Value	RO	0x00	Retain	0x00 : peakMSE = 0 0x01 : peakMSE = 1 ... 0x3E : peakMSE = 62 0x3F : peakMSE = 63 0x4E - 0xFE : value invalid 0xFF : Measurement not possible

Table 124: DCQ MSE enable
Device 3, Register 0x8239

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0x0000	Retain	
0	DCQ MSE enable	R/W	0x0	Retain	1 = Enable DCQ MSE

Table 125: Interrupt Enable
Device 3, Register 0x8300

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0000	Retain	
1	LED Interrupt Enable	R/W	0x0	Retain	1 = Enable
0	GPIO Interrupt Enable	R/W	0x0	Retain	1 = Enable

Table 126: Interrupt Status
Device 3, Register 0x8301

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO, LH	0x0000	0x0000	
1	LED Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt occurred 1 = Interrupt occurred

Table 126: Interrupt Status
Device 3, Register 0x8301

Bits	Field	Mode	HW Rst	SW Rst	Description
0	GPIO Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt occurred 1 = Interrupt occurred

Table 127: GPIO/LED Control
Device 3, Register 0x8302

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0000	Retain	
1	LED Data	R/W	0x0	Retain	This bit has no effect unless register 3.8304.3 = 1. When register 3.8303.1 = 0, a read to this register will reflect the state of the LED pin, and a write will write the output register but have no effect on the LED pin. When register 3.8303.1 = 1, a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the LED pin.
0	GPIO Data	R/W	0x0	Retain	This bit has no effect unless register 3.8304.11 = 1 When register 3.8303.0 = 0, a read to this register will reflect the state of the GPIO pin, and a write will write the output register but have no effect on the GPIO pin. When register 3.8303.0 = 1, a read to this register will reflect the state of the output register, and a write will write the output register and drive the state of the GPIO pin.

Table 128: GPIO/LED Control
Device 3, Register 0x8303

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0000	Retain	
1	LED Output Enable	R/W	0x1	Retain	This bit has no effect unless register 3.8304.3 = 1. 0 = Input 1 = Output
0	GPIO Output Enable	R/W	0x1	Retain	This bit has no effect unless register 3.8304.11 = 1. 0 = Input 1 = Output

Table 129: GPIO/LED Control
Device 3, Register 0x8304

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	

Table 129: GPIO/LED Control
Device 3, Register 0x8304

Bits	Field	Mode	HW Rst	SW Rst	Description
11	GPIO Pin Function	R/W	0x0	Retain	GPIO Function 0 = GPIO is used for LED function. 1 = GPIO is used for GPIO function.
10:8	GPIO Interrupt Select	R/W	0x0	Retain	Interrupt is effective only when register 3.8303.0 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on Low level 011 = Interrupt on High level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on LtoH or HtoL
7:4	Reserved	R/W	0x0	Retain	
3	LED Pin Function	R/W	0x0	Retain	LED Function 0 = LED is used for LED function. 1 = LED is used for GPIO function.
2:0	LED Interrupt Select	R/W	0x0	Retain	Interrupt is effective only when register 3.8303.1 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on Low level 011 = Interrupt on High level 100 = Interrupt on High to Low 101 = Interrupt on Low to High 110 = Reserved 111 = Interrupt on LtoH or HtoL

Table 130: GPIO/LED Control
Device 3, Register 0x8305

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0x000	Retain	
4	Tristate Disable for INTn	R/W	0x0	Retain	0 = tristate enabled for INT I/O pin 1 = tristate disable on INT I/O pin
3	INT Open Source Control	R/W	0x0	Retain	INT Open Source Control 1 = Open source I/O, where the output is driven High for an active interrupt and tri-stated for an inactive one, and there would be an external pull-down to drive the line Low
2	INT Open Drain Control	R/W	0x0	Retain	INT Open Drain Control 1 = Open drain I/O, where the output is driven Low for an active interrupt and tri-stated for an inactive one, and there would be an external pull-up to drive the line High
1	LED Open Drain Control	R/W	0x0	Retain	LED Open Drain Control 1 = Open drain I/O

Table 130: GPIO/LED Control
Device 3, Register 0x8305

Bits	Field	Mode	HW Rst	SW Rst	Description
0	GPIO Open Drain Control	R/W	0x0	Retain	GPIO Open Drain Control 1 = Open drain I/O

Table 131: LED Function Control Register
Device 3, Register 0x8310

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	0x00	
7:4	GPIO Pin Control for LED Functionality	R/W	0x1	Retain	GPIO needs to be configured in LED function mode, otherwise register 3.8310.7:4 has no effect. 0000 = On - Receive, Off - No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = Traffic Ready 0110 = On - 100 Mbps Link, Off - Else 0111 = On - 100 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
3:0	LED Control	R/W	0x1	Retain	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 2 blinks - 100 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = Communication Ready 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

Table 132: LED Polarity Control Register
Device 3, Register 0x8311

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	GPIO Pin Mix Percentage for LED Functionality	R/W	0x8	Retain	This register is only used when GPIO is configured in LED function mode. When using 2 terminal bi-color LEDs, the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
11:8	LED Mix Percentage	R/W	0x8	Retain	When using 2 terminal bi-color LEDs, the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
7:4	Reserved	R/W	0x0	Retain	
3:2	GPIO Pin Polarity for LED Functionality	R/W	0x0	Retain	This register is only used when GPIO is configured in LED function mode. 00 = On - drive GPIO low, Off - drive GPIO High 01 = On - drive GPIO high, Off - drive GPIO Low 10 = On - drive GPIO low, Off - tri-state GPIO 11 = On - drive GPIO high, Off - tri-state GPIO
1:0	LED Polarity	R/W	0x0	Retain	00 = On - drive LED low, Off - drive LED High 01 = On - drive LED high, Off - drive LED Low 10 = On - drive LED low, Off - tri-state LED 11 = On - drive LED high, Off - tri-state LED

Table 133: LED Timer Control Register
Device 3, Register 0x8312

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force INTn	R/W	0x0	Retain	1 = INTn pin forced to be asserted 0 = Normal operation
14:12	Pulse Stretch Duration	R/W	0x4	Retain	000 = No pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
11	Interrupt Polarity	R/W	0x1	Retain	0 = Interrupt active high 1 = Interrupt active low
10:8	Blink Rate	R/W	0x1	Retain	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7:4	Reserved	R/W	0x0	Retain	
3:2	Speed Off Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
1:0	Speed On Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

Table 134: TDR Threshold of Negative Threshold
Device 3, Register 0x850B

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	
14:8	Negative Threshold 1	R/W	0x0F	Retain	Negative threshold for distance between window0 and window1
7	Reserved	R/W	0x0	Retain	
6:0	Negative Threshold 0	R/W	0x12	Retain	Negative threshold for distance < window0

Table 135: TDR Threshold of Negative Threshold
Device 3, Register 0x850C

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	
14:8	Negative Threshold 3	R/W	0x0A	Retain	Negative threshold for distance between window1 and window2
7	Reserved	R/W	0x0	Retain	
6:0	Negative Threshold 2	R/W	0x0C	Retain	Negative threshold for distance between window2 and window3

Table 136: TDR Result
Device 3, Register 0x8510

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Amplitude	RO	0x00	Retain	The amplitude of reflected pulse 8'b1111_1111 = Maximum positive reflection 8'b1000_0000 = No reflection 8'b0000_0000 = Maximum negative reflection
7:0	Distance	RO	0x00	Retain	The distance of reflection

Table 137: Advanced VCT Wait for Time Up for pwr_mgt
Device 3, Register 0x8511

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Wait for 200 ms to Start Test	R/W	xx	16'hffff	Lower 16 bit

Table 138: Advanced VCT Wait for 3 us Before Sending Out New Pulse
Device 3, Register 0x8512

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Wait for 200 ms to Start Test	R/W	xx	16'hcbd5	Lower 8 bit is for 3 us timer, upper 4 bit is for 200 ms timer

Table 139: 100BASE-T Pair Swap and Polarity
Device 3, Register 0x8515

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	

Table 139: 100BASE-T Pair Swap and Polarity
Device 3, Register 0x8515

Bits	Field	Mode	HW Rst	SW Rst	Description
6	Register 3.8515 Valid	RO	0x0	0x0	The contents of 3.8515.0 is valid only if register 3.8515.6 = 1. 1 = Valid 0 = Invalid
5:1	Reserved	RO	0x18	0x18	
0	Pair 1,2 (MDI[0]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive

Table 140: Advanced VCT Control
Device 3, Register 0x8517

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Enable Test	R/W, SC	0x0	0x0	1 = Enable test 0 = Disable test This bit will self-clear when the test is completed.
14	Test Status	RO	0x0	0x0	1 = Test completed 0 = Test not started/in progress
13:11	Reserved	R/W	0x0	0x0	
10:8	Number of Sample Averaged	R/W	6	Retain	0 = 2 samples 1 = 4 samples 2 = 8 samples 3 = 16 samples 4 = 32 samples 5 = 64 samples 6 = 128 samples 7 = 256 samples
7:6	Mode	R/W	0x0	Retain	00 = Maximum peak above threshold 01 = First or last peak above threshold. See register 3.851C.13. 10 = Offset 11 = Sample point at distance set by 3.8518.7:0
5:0	Peak Detection Hysteresis	R/W	0x03	Retain	0x00 = 0 mV 0x01 = 7.81 mV ... 0x3F = ± 492 mv

Table 141: Advanced VCT Sample Point Distance
Device 3, Register 0x8518

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	0x00	

Table 141: Advanced VCT Sample Point Distance
Device 3, Register 0x8518

Bits	Field	Mode	HW Rst	SW Rst	Description
9:0	Distance to Measure / Distance to Start	R/W	0x000	Retain	When register 3.8517.7:6 = 11, the measurement is taken at this distance. (00 to 3FF) When register 3.8517.7:6 = 0x, any distance below this distance is not considered (00 to FF). Bit 9:8 is ignored.

Table 142: Advanced VCT Cross Pair Positive Threshold
Device 3, Register 0x8519

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RO	0x0000	0x0000	

Table 143: Advanced VCT Same Pair Impedance Positive Threshold 0 and 1
Device 3, Register 0x851A

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	
14:8	Same-Pair Positive Threshold 10m - 50m	R/W	0x0F	Retain	0x00 = 0 mV 0x01 = 7.81 mV ... 0x7F = - 992 mV
7	Reserved	RO	0x0	0x0	
6:0	Same-Pair Positive Threshold < 10m	R/W	0x12	Retain	0x00 = 0 mV 0x01 = 7.81 mV ... 0x7F = - 992 mV

Table 144: Advanced VCT Same Pair Impedance Positive Threshold 2 and 3
Device 3, Register 0x851B

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	
14:8	Same-Pair Positive Threshold 110m - 140m	R/W	0x0A	Retain	0x00 = 0 mV 0x01 = 7.81 mV ... 0x7F = - 992 mV
7	Reserved	RO	0x0	0x0	

Table 144: Advanced VCT Same Pair Impedance Positive Threshold 2 and 3
Device 3, Register 0x851B

Bits	Field	Mode	HW Rst	SW Rst	Description
6:0	Same-Pair Positive Threshold 50m - 110m	R/W	0x0C	Retain	0x00 = 0 mV 0x01 = 7.81 mV ... 0x7F = - 992 mV

Table 145: Advanced VCT Same Pair Impedance Positive Threshold 4 and Transmit Pulse Control
Device 3, Register 0x851C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	0x0	0x0	
13	First Peak/Last Peak Select	R/W	0x0	Retain	This register takes effect only if register 3.8517.7:6 = 01. 0 = First peak 1 = Last peak
12	Break Link Prior to Measurement	R/W	0x0	Retain	1 = Do not wait 1.5s to break link before starting VCT 0 = Wait 1.5s to break link before starting VCT
11:10	Transmit Pulse Width	R/W	0x1	Retain	00 = Full pulse (128 ns) 01 = 3/4 pulse 10 = 1/2 pulse 11 = 1/4 pulse
9:8	Transmit Amplitude	R/W	0x0	Retain	00 = Full amplitude 01 = 3/4 amplitude 10 = 1/2 amplitude 11 = 1/4 amplitude

7	Distance Measurement Point	R/W	0x0	Retain	If register 3.8517.7:6 = 00, then
					0 = Measure distance when amplitude drops to 50% of peak amplitude
					1 = Measure distance at actual maximum amplitude
					If register 3.8517.7:6 = 01, then
					0 = Measure distance when amplitude drops below hysteresis
					1 = Measure distance at actual maximum amplitude
					If 3.8517.7:6 = 1X, then this bit is ignored.

6:0	Same-Pair Positive Threshold For Cable Length Longer Than 15 m	R/W	0x06	Retain	0x00 = 0 mV 0x01 = 7.81 mV ... 0x7F = 992 mV

Table 146: TDR Threshold of Negative Threshold
Device 3, Register 0x851D

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Ignore Activity	R/W	0x0	Retain	1 = Block checking of wire activity

Table 146: TDR Threshold of Negative Threshold
Device 3, Register 0x851D

Bits	Field	Mode	HW Rst	SW Rst	Description
14:8	Negative Threshold 4	R/W	0x06	Retain	Negative threshold for distance > window3
7:0	Reserved	R/W	0xFF	Retain	

Table 147: DSP VCT
Device 3, Register 0x8580

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0x0000	Retain	
0	DSP VCT Mode	R/W	0x0	Retain	1 = Enable DSP VCT mode

Table 148: Copper Port Packet Generation
Device 3, Register 0x8610

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	
7	Packet Generator Transmit Trigger	R/W	0x0	Retain	This bit is only valid when all of the following are true: - bit 6 =1 - bit 3 =1 - bit 3.8611.15:0 is not equal to all 0s A read of this bit gives the following: 1 = Packet generator transmit done 0 = Packet generator is transmitting data When this bit is 1, a write of 0 will trigger the packet generator to transmit again. When this bit is 0, a write of 0 or 1 will have no effect.
6	Packet Generator Enable Self-Clear Control	R/W	0x0	Retain	0 = Bit 3 will self-clear after all packets are sent 1 = Bit 3 will stay High after all packets are sent
5	Reserved	R/W	0x0	Retain	
4	Enable CRC Checker	R/W	0x0	Retain	1 = Enable 0 = Disable
3	Enable Packet Generator	R/W	0x0	Retain	1 = Enable 0 = Disable
2	Payload of Packet to Transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = A5, 5A, A5, 5A
1	Length of Packet to Transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes

Table 148: Copper Port Packet Generation
Device 3, Register 0x8610

Bits	Field	Mode	HW Rst	SW Rst	Description
0	Transmit an Errored Packet	R/W	0x0	Retain	1 = Tx packets with CRC errors and Symbol error 0 = No error

Table 149: Copper Port Packet Size
Device 3, Register 0x8611

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Burst	R/W	0x0000	Retain	0x0000 = Continuous 0x01 to 0xFFFF = Burst 1 to 65535 packets

Table 150: Checker Control
Device 3, Register 0x8612

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x000	Retain	
4	CRC Counter Reset	R/W, SC	0x0	0x0	1 = Reset This bit will self-clear after write to 1.
3:0	Reserved	R/W	0x0	Retain	

Table 151: Pktgen Control
Device 3, Register 0x8613

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Packet Generator Constant Payload Enable	R/W	0x0	Retain	1 = Payload of packet is controlled by register 3.8613.14 when packet generator is enabled 0 = Payload of packet is controlled by register 3.8610.2 when packet generator is enabled
14	Packet Generator Constant Payload Value	R/W	0x0	Retain	1 = All 1's in the payload when register 3.8613.15 = 1 0 = All 0's in the payload when register 3.8613.15 = 1
13:8	Reserved	R/W	0x00	Retain	
7:0	Packet Generator Inter-Packet Gap	R/W	0x0B	Retain	This value plus 1 is Inter-Packet Gap in bytes

Table 152: Copper Port Packet Counters
Device 3, Register 0x8614

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Count	RO	0x0000	Retain	0x0000 = No packets received 0xFFFF = 65535 packets received (max count) Bit 3.8610.4 must be set to 1 in order for the register to be valid.

Table 153: Copper Port CRC Counters
Device 3, Register 0x8615

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	CRC Error Count	RO	0x0000	Retain	0x0000=NoCRCerrorsdetectedinthepacketsreceived 0xFFFF = 65535 CRC errors detected in the packets received (max count) Bit 3.8610.4 must be set to 1 in order for the register to be valid.

Table 154: BIST Control
Device 3, Register 0x8617

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W, SC	0x0000	Retain	
0	BIST Enable	R/W, SC	0x0	Retain	1 = BIST enable 0 = BIST disable

Table 155: BIST Status
Device 3, Register 0x8618

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	R/W	0x0000	Retain	
2:0	BIST Status	RO	0x0	Retain	0 = Not started 1 = In progress 4 = Aborted 6 = No error 7 = Error

Table 156: BIST Counters
Device 3, Register 0x8619

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	BIST Packet Count	RO, ROC	0x00	Retain	0x00 = No packets received 0xFF = 256 packets received (max count) Bit 3.8617.0 must be set to 1 in order for register to be valid.
7:0	BIST Error Count	RO, ROC	0x00	Retain	0x00 = No CRC errors detected in the packets received 0xFF = 256 CRC errors detected in the packets received (max count) Bit 3.8617.0 must be set to 1 in order for register to be valid.

Table 157: Misc Test
Device 3, Register 0x861A

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TX_TCLK Enable	R/W	0x0	Retain	The transmit clock can be driven to the HSDACP/N pin. 1 = Enable 0 = Disable
14	Average Test Mode	R/W	0x0	Retain	1 = Average over 16 samples 0 = Normal, number of samples to average over is determined by 3.861B.12:11
13:8	Reserved	R/W	0x00	Retain	
7	Temperature Sensor Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6	Temperature Sensor Interrupt	RO, LH	0x0	0x0	1 = Temperature reached threshold 0 = Temperature below threshold
5	One Shot Temperature Sample	R/W	0x0	Retain	This bit is valid only when register 3.861B.15:14 = 2'b10. 1 = Temperature sense 0 = Idle
4:0	Reserved	R/W	0x00	0x00	

Table 158: Temperature Sensor 1
Device 3, Register 0x861B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Temperature Sensor Enable	R/W	0x3	Retain	00 = Sample every 1 second (sensor output read time is around 10.36 ms) 01 = Sense rate decided by register 3.861B.10:8 10 = Use 3.861A.5 to enable 11 = Disable

Table 158: Temperature Sensor 1
Device 3, Register 0x861B

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Reserved	R/W	0x0	Retain	
12:11	Temperature Sensor Number of Samples to Average	R/W	0x1	Retain	00 = Average over 2^6 samples 01 = Average over 2^8 samples 10 = Average over 2^10 samples 11 = Average over 2^12 samples This register is ignored when 3.861A.14 = 1
10:8	Temperature Sensor Sampling Rate	R/W	0x5	Retain	Sampling Rate 000 = Reserved 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = 2.3 ms 110 = 6.4 ms 111 = 11.9 ms
7:0	Temperature Sensor Alternative Reading (8-bit)	RO	x	x	Average temperature reading based on sample size specified in register 3.861B.12:11 & 3.861A.14 Temperature in ×C = 3.861B.7:0 - 75 that is, for 100×C, the value of this register field is 8'b1010_1111.

Table 159: Temperature Sensor 2
Device 3, Register 0x861C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Temperature Interrupt Threshold	R/W	0x96	Retain	Temperature Sensor Interrupt Threshold Temperature in ×C = 3.861C.15:8 - 75 that is., for 100×C, this register field should be 8'b1010_1111. If the temperature in register 3.861C.7:0 is equal or greater than this field, the Temperature Sensor Interrupt register (3.861A.6) will be set when the interrupt is enabled (3.861A.7 = 1'b1).
7:0	Temperature Sensor Instantaneous Reading	RO	xxxxx	xxxxx	Instantaneous temperature reading based on sample rate specified in register 3.861B.10:8. Temperature in ×C = 3.861C.7:0 - 75 that is, for 100×C, the value of this register field is 8'b1010_1111. If it is equal or greater than register 3.861C.15:8, the Temperature Sensor Interrupt register (3.861A.6) will be set when the interrupt is enabled (3.861A.7 = 1'b1).

Table 160: PTP Control Register
Device 3, Register 0x8630

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Tx Side PTP's SFD Selection	R/W	0x0	Retain	Tx side PTP's SFD selection 1 = From tx_en 0 = From SFD
14	Tx Side PTP's Preamble Selection	R/W	0x1	Retain	Tx side PTP's preamble selection 1 = Enable detection of preemptable packets delimiter 0 = Disable detection of preemptable packets delimiter
13	Rx Side PTP's SFD Selection	R/W	0x0	Retain	Rx side PTP's SFD selection 1 = From rx_dv 0 = From SFD
12	Rx Side PTP's Preamble Selection	R/W	0x1	Retain	Rx Side PTP's Preamble Selection 1 = Enable detection of preemptable packets delimiter 0 = Disable detection of preemptable packets delimiter
11	Reserved		0x0	0x0	
10	PTP software reset	R/W, SC	0x0	Retain	1= software reset
9	PTP Power Down	R/W	0x1	Retain	1 = Power down 0 = Power up
8	Reserved	R/W	0x0	Retain	
7:6	PTP Event Request/Trigger Select For LED Pin	R/W	0x0	Retain	01 = Use LED pin for PTP output trigger pulse 10 = Use LED pin for PTP One Pulse Per Second (1PPS) output 11 = Use LED pin for PTP input trigger pulse
5:4	PTP Event Request/Trigger Select For GPIO Pin	R/W	0x0	Retain	01 = Use GPIO pin for PTP output trigger pulse 10 = Use GPIO pin for PTP for other functions 11 = Use GPIO pin for PTP input trigger pulse
3:1	Reserved	R/W	0x0	Retain	
0	Enable LED/GPIO for PTP Status	R/W	0x0	Retain	Used to bring PTP status to the LED pin.

Table 161: PTP Control Register2 mac_address[15:0]
Device 3, Register 0x8631

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTP mac address[15:0]	R/W	0x0000	Retain	User-programmed port MAC address for use by PTP if PTP frames are modified and keep_sa register is disabled

Table 162: PTP Control Register3 mac_address [31:16]
Device 3, Register 0x8632

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTP mac address[31:16]	R/W	0x0000	Retain	User-programmed port MAC address for use by PTP if PTP frames are modified and keep_sa register is disabled

Table 163: PTP Control Register 4 mac_address [47:32]
Device 3, Register 0x8633

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTP mac address[47:32]	R/W	0x0000	Retain	User-programmed port MAC address for use by PTP if PTP frames are modified and keep_sa register is disabled

Table 164: PTP Control Register 5 other fields
Device 3, Register 0x8634

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0x00	Retain	
8:3	Reserved	R/W	0x01	Retain	
2	PTP one step_ enable	R/W	0x1	Retain	This signal is used to control the enable/disable of one step feature. This bit overrides the internal 'OneStep' register 0= PTP does not support one step feature 1= The value in OneStep register takes effect.
1	PTP Keep Start of Frame	R/W	0x1	Retain	Preempt drop start after discard. Define macro PTP_PREM_EN to use this pin 0 = Keep start of new frame even if previous frame is not complete 1 = Discard any new frame starts if previous frame is not complete
0	PTP rg_igr_preempt_en	R/W	0x0	Retain	Enable ingress preemption. Define macro PTP_PREM_EN to use this pin 0 = Preemption disabled 1 = Preemption enabled

Table 165: DISABLE_IN Control Register
Device 3, Register 0x8640

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO	0x0000	Retain	
1	Status of Tx DISABLE_IN	RO	0x0	Retain	1 = Tx is disabled 0 = Tx is not disabled

Table 165: DISABLE_IN Control Register
Device 3, Register 0x8640

Bits	Field	Mode	HW Rst	SW Rst	Description
0	Tx DISABLE_IN Function Enable	R/W	0x1	Retain	1 = Enable Tx disable in function 0 = Disable Tx disable in function

Table 166: LPSD Control Register
Device 3, Register 0x8700

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0x0000	Retain	
4	Local Wake Status after T1 Port Sleep	RO, LH	0x0	Retain	This status is valid only after T1 Port Sleep Mode 1 = The device came out of T1 Port Sleep Mode because a pulse was received at the WAKE_IN pin
3	Remote Wake Status after T1 Port Sleep	RO, LH	0x0	Retain	This status is valid only after T1 Port Sleep Mode 1 = The device powered up due to energy received on the MDIN/P pins 0 = No energy has been detected on the MDIN/P pins
2	LPSD Local Wake Status	RO, LH	0x0	Retain	This status is valid only after an LPSD power up. 1 = The device powered up because a pulse was received at the WAKE_IN pin 0 = The device did not power up due to a pulse received at the WAKE_IN pin
1	LPSD Remote Wake Status	RO, LH	0x0	Retain	This status is valid only after an LPSD power up. 1 = The device powered up because of energy received at the MDIP/N pins 0 = The device did not power up due to energy received at the MDIP/N pins
0	LPSD Power Down Enable	R/W	0x0	Retain	1 = Enable an LPSD power down 0 = Do not enable an LPSD power down

Table 167: LPSD Control Register 2
Device 3, Register 0x8701

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Enable LPSD Circuit Programming	R/W, SC	0x0	Retain	1 = Write digital register values to the LPSD circuit
14:13	Set WAKE_IN Pulse Width	R/W	0x0	Retain	Allows for setting the pulse width needed at the WAKE_IN pin to power up the device after an LPSD power down. 00 = 30us 01 = 1.0ms 10 = 8.0ms 11 = 32.0ms

Table 167: LPSD Control Register 2
Device 3, Register 0x8701

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Disable LPSD Local Wake Up	R/W	0x0	Retain	Disable LPSD Local Wake Up after an LPSD power down 1 = The device will not wake up if a pulse is received at the WAKE_IN pin 0 = The device will wake up if a pulse is received at the WAKE_IN pin
11	Disable LPSD Remote Wake Up	R/W	0x0	Retain	Disable LPSD Remote Wake Up after an LPSD power down 1 = The device will not wake up if energy is received at the MDIP/N pins 0 = The device will wake up if energy is received at the MDIP/N pins
10:0	Reserved	R/W	0x000	Retain	

Table 168: Sleep/Wake Request
Device 3, Register 0x8702

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	R/W	0x000	Retain	
5	Enable Passive Mode	R/W	0x0	Retain	1 = Enable. This will put the Port in T1 Port Sleep Mode by powering down the port without completing a Sleep handshake
4	Local Wake Request	R/W	0x0	Retain	1 = Trigger wake request to the LP. If the device is in sleep, WUP is generated to wake up the LP. If the device is powered up, WUR is generated to the LP after link up.
3:2	Reserved	R/W	0x0	Retain	
1	Sleep Abort	R/W	0x0	Retain	1 = Abort the Sleep Request Received from the link partner.
0	Local Sleep Request	R/W	0x0	Retain	1 = Sleep Request. Device will initiate sleep handshake with link partner. This register does not do anything if 3.8707.0 is 0

Table 169: Sleep Status
Device 3, Register 0x8703

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	R/W	0x0000	Retain	

Table 169: Sleep Status
Device 3, Register 0x8703

Bits	Field	Mode	HW Rst	SW Rst	Description
2:0	Sleep Status	RO	0x0	Retain	3'b000 = Normal 3'b001 = Sleep 3'b010 = Sleep Failed 3'b100 = Sleep Request has been aborted

Table 170: Wakeup Status
Device 3, Register 0x8704

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0x0000	Retain	
0	Wakeup Status	RO	0x0	Retain	1 = Wakeup received

Table 171: Sleep/Wakeup Interrupt Status
Device 3, Register 0x8705

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0x000	Retain	
8	Pulse Received on WAKE_IN pin (Digital or Analog Pulse)	RO, LH	0x0	Retain	1 = Pulse Received on WAKE_IN pin (Digital or Analog pulse)
7	Pulse Received on WAKE_IN pin (Analog Pulse)	RO, LH	0x0	Retain	1 = Pulse Received on WAKE_IN pin (only in Deep Sleep Mode)
6	WUR Received	RO, LH	0x0	Retain	1 = WUR Received
5	WUP Received when device in Deep Sleep Mode	RO, LH	0x0	Retain	1 = WUP Received when device in Deep Sleep Mode
4	WUP Received when device in T1 Port Sleep Mode	RO, LH	0x0	Retain	1 = WUP Received when device in T1 Port Sleep Mode
3	Sleep Request Aborted	RO, LH	0x0	Retain	1 = Sleep Request has been aborted
2	Sleep Fail Status	RO, LH	0x0	Retain	1 = Sleep Failed since last read
1	Sleep Status	RO, LH	0x0	Retain	1 = Sleep completed since last read
0	Wakeup Status	RO, LH	0x0	Retain	1 = Wakeup received since last read

Table 172: Sleep/Wakeup Interrupt Enable
Device 3, Register 0x8706

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0x000	Retain	
8	Pulse Received on WAKE_IN pin (Digital or Analog Pulse) Interrupt Enable	R/W	0x0	Retain	1 = Enable
7	Pulse Received on WAKE_IN pin (Analog Pulse) Interrupt Enable	R/W	0x0	Retain	1 = Enable
6	WUR Received Interrupt Enable	R/W	0x0	Retain	1 = Enable
5	WUP Received when device in Deep Sleep Mode Interrupt Enable	R/W	0x0	Retain	1 = Enable
4	WUP Received when device in T1 Port Sleep Mode Interrupt Enable	R/W	0x0	Retain	1 = Enable
3	Sleep Request Aborted Interrupt Enable	R/W	0x0	Retain	1 = Enable
2	Sleep Fail Status Interrupt Enable	R/W	0x0	Retain	1 = Enable
1	Sleep Status Interrupt Enable	R/W	0x0	Retain	1 = Enable
0	Wakeup Status Interrupt Enable	R/W	0x0	Retain	1 = Enable

Table 173: Sleep/Wakeup Configuration
Device 3, Register 0x8707

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0x0000	Retain	
2	CIC Enable Default	R/W	See Descr.	Retain	At HW Reset, this register field gets the default from the value written before an LPSD sleep is enabled, which is saved and restored after power up 1 = 1'b0 will be shifted into LPSD SR before sleep as default of 3.8707.1 0 = value of 3.8707.1 will be shifted into LPSD SR before sleep as default of 3.8707.1

Table 173: Sleep/Wakeup Configuration
Device 3, Register 0x8707

Bits	Field	Mode	HW Rst	SW Rst	Description
1	CIC command enable	R/W	See Descr.	Retain	At HW Reset, this register field gets the default from the value written before an LPSD sleep is enabled, which is saved and restored at power up. 1 = TC10 Sleep/WakeUp Command to RGMII/SGMII is supported
0	TC10 Sleep/WakeUp Capability Supported	RO	See Descr.	Retain	At HW Reset, this register field gets the default from the configuration pin 1 = TC10 Sleep/WakeUp Capability is supported The value of this bit must be maintained when this register is written to.

Table 174: Sleep/Wakeup Interrupt Status 2
Device 3, Register 0x870A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO, LH	0x0	Retain	
4	LPS Received from LP	RO, LH	0x0	Retain	1 = LPS Received from Link Partner
0	Reserved	RO, LH	0x0	Retain	

Table 175: Sleep/Wakeup Interrupt Enable 2
Device 3, Register 0x870B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0x0	Retain	
4	LPS Received from LP Interrupt Enable	R/W	0x0	Retain	1 = Enable
3:0	Reserved	R/W	0x0	Retain	

3.4 Com and MAC Registers

Table 176: Com and MAC Registers – Register Map

Register Name	Register Address	Table and Page
Com Port Control Register	Device 4, Register 0x8000	Table 177, p. 158
RGMII Output Impedance Control	Device 4, Register 0x8001	Table 178, p. 159
MAC Specific Control Register	Device 4, Register 0x8210	Table 179, p. 159
Interrupt Enable Register	Device 4, Register 0x8212	Table 180, p. 160
Interrupt Status Register	Device 4, Register 0x8213	Table 181, p. 160
MAC Specific Status Register	Device 4, Register 0x8214	Table 182, p. 161
WOL Control Register	Device 4, Register 0x8215	Table 183, p. 161
WOL Status Register	Device 4, Register 0x8216	Table 184, p. 162
WOL Magic Packet Destination Address Word 2	Device 4, Register 0x8217	Table 185, p. 162
WOL Magic Packet Destination Address Word 1	Device 4, Register 0x8218	Table 186, p. 162
WOL Magic Packet Destination Address Word 0	Device 4, Register 0x8219	Table 187, p. 162
IO Pad Control	Device 4, Register 0x821A	Table 188, p. 163
GPIO Control Register	Device 4, Register 0x821B	Table 189, p. 163
Undervoltage Control	Device 4, Register 0x8700	Table 190, p. 164
Undervoltage Interrupt Enable	Device 4, Register 0x8703	Table 191, p. 165
Undervoltage Status	Device 4, Register 0x8704	Table 192, p. 166
APHY Register ID	Device 4, Register 0x8EFF	Table 193, p. 167
Wake Source Sent out the GPIO Pin	Device 4, Register 0xFD20	Table 194, p. 167

Table 177: Com Port Control Register
Device 4, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x0	SC	Common Software Reset Writing a 1 to this bit resets the RGMII/RMII modules (outside the copper PCS). When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = Reset 0 = Normal operation
14:12	Reserved	R/W	0x0	0x0	
11	Common Power Down	R/W	0x0	0x0	Writing a 1 to this bit causes the chip to power down. 1 = Power down 0 = Normal operation
10	Isolate	R/W	0x0	0x0	1 = Tri-state the output pins of RXC, RXCLK, and RXD 0 = Normal operation
9	Tri-state TCLK	R/W	0x0	0x0	1 = Tri-state the output TCLK in MII mode
8:4	Reserved	R/W	0x0	0x0	
3	RGMII Receive Timing Control	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to this register must be followed by software reset (4.8000.15) to take effect. 1 = Receive clock transitions when data stable 0 = Receive clock transitions when data transitions
2	RGMII Transmit Timing Control	R/W	See Descr.	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset (4.8000.15) to take effect. 1 = Transmit clock internally delayed 0 = Transmit clock not internally delayed If the device is configured to RGMII Mode 2, then the default is 0; otherwise, it is 1.
1:0	MAC Interface	RO	See Descr.	Retain	These bits reflect the configured MAC interface mode. 00 = MII (TCLK output) 01 = RGMII mode 1 10 = RMII 11 = RGMII mode 2

Table 178: RGMII Output Impedance Control
Device 4, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	
14	Reserved	RO	0x0	0x0	
13:12	Reserved	R/W	0x0	Retain	
11:8	PMOS Value	R/W	0010, if configured to RGMII mode 0001, all other modes	Retain	Programmable value of PMOS transistors to control the drive strength and slew rate value of all Host mode pads.
7:4	NMOS Value	R/W	0010, if configured to RGMII mode 0001, all other modes	Retain	Programmable value of NMOS transistors to control drive strength and slew rate value of all Host mode pads.
3:0	Reserved	RW	0xB	Retain	

Table 179: MAC Specific Control Register
Device 4, Register 0x8210

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	RMII Rx FIFO Depth	R/W	0x0	Retain	00 = supports max 2KB packet at +/-100ppm 01 = supports max 10KB packet at +/-100ppm 10 = supports max 18KB packet at +/-100ppm 11 = supports max 27KB packet at +/-100ppm
13:12	Reserved		0x0	0x0	
11:8	RMII Rx FIFO Idle Delete Limit	R/W	0x3	Retain	Minimum nimble of idles to be kept between packets before FIFO deletes idles
7	RMII Rx FIFO Enable	R/W	0x1	Retain	Write to 0 only to bypass RMII FIFO
6:0	Reserved	R/W	0x0000	Retain	

Table 180: Interrupt Enable Register
Device 4, Register 0x8212

Bits	Field	Mode	HW Rst	SW Rst	Description
15	WOL Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
14:7	Reserved	R/W	0x00	Retain	
6	RMII FIFO Over/Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
5:2	Reserved	R/W	0x0	Retain	
1	RMII FIFO Idle Inserted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Rx FIFO Idle Deleted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 181: Interrupt Status Register
Device 4, Register 0x8213

Bits	Field	Mode	HW Rst	SW Rst	Description
15	WOL Interrupt Status	RO,LH	0x0	0x0	1 = WOL event triggered 0 = No WOL event
14:7	Reserved	RO	Always 00	Always 00	
6	RMII FIFO Over/Underflow	RO,LH	0x0	0x0	1 = Over/underflow error 0 = No error
5:2	Reserved	RO	Always 0	Always 0	
1	RMII FIFO Idle Inserted	RO,LH	0x0	0x0	1 = Idle inserted 0 = Idle not inserted
0	RMII FIFO Idle Deleted	RO,LH	0x0	0x0	1 = idle deleted 0 = Idle not deleted

Table 182: MAC Specific Status Register
Device 4, Register 0x8214

Bits	Field	Mode	HW Rst	SW Rst	Description
15	VDDO Level	R/W	0x0	Retain	The VDDO supply voltage used when 1.8V is not used. The bit mapping is: 0 = 3.3V 1 = 2.5V This register defaults to 0 (VDDO = 3.3V). If VDDO = 2.5V then this bit must be programmed to 1.
14	RGMII in-band enable	R/W	0x0	Retain	1 = RGMII will send in-band status during idle 0 = RGMII will not send in-band status during idle
13	Enable RCLK During Power Down	R/W	0x0	Retain	1 = RCLK toggles during power down 0 = RCLK is off during power down
12	RGMII receive ready	RO	0x0	0x0	1= RGMII has received ready signal from MAC
11:5	Reserved	R/W	0x00	Retain	
4	Device select	RO	0x0	0x0	1 = 88Q1111 device 0 = 88Q1110 device
3:2	Reserved	R/W	0	Retain	Reserved
1:0	Reserved	R/W	0	Retain	Reserved

Table 183: WOL Control Register
Device 4, Register 0x8215

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	
14	Magic Packet Match Enable	R/W	0x0	Retain	Allows matching received packets with a Magic Packet (packet containing 6 bytes of FF followed by 16 instances of the destination address) to assert the WOL detection logic 1 = Enable Magic Packet matching for WOL detection 0 = Disable Magic Packet matching for WOL detection
13	Link Up Enable		0x0	0x0	Allows link up event to assert the WOL detection logic 1 = Enable link up event for WOL detection 0 = Disable link up event for WOL detection
12	Clear WOL Sta-tus	R/W	0x0	Retain	1 = Clear status in 4.8216.14 0 = Retain status in 4.8216.14
11:0	Reserved	R/W	0x000	Retain	

Table 184: WOL Status Register
Device 4, Register 0x8216

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	
14	Magic Packet Match Detected	RO, LH	0x0	0x0	1 = At least 1 Received Packet Contained the Magic Packet Data 0 = No Received Packets Contained the Magic Packet Data
13	Link Change Detected	RO, LH	0x0	0x0	1 = Link status changed from down to up 0 = Link status did not change from down to up
12:0	Reserved	R/W	0x0000	Retain	

Table 185: WOL Magic Packet Destination Address Word 2
Device 4, Register 0x8217

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Magic Packet Destination Address {7:0,15:8}	R/W	0x0000	Retain	This data is the upper 47:32 bits of the destination address that must be seen repeated 16 times in a received packet in order for it to be a Magic Packet. This must be programmed since the PHY has no other way of knowing what the Destination Address is.

Table 186: WOL Magic Packet Destination Address Word 1
Device 4, Register 0x8218

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Magic Destination Address {23:16,31:24}	R/W	0x0000	Retain	This data is the middle 31:16 bits of the destination address that must be seen repeated 16 times in a received packet in order for it to be a Magic Packet. This must be programmed since the PHY has no other way of knowing what the Destination Address is.

Table 187: WOL Magic Packet Destination Address Word 0
Device 4, Register 0x8219

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Magic Destination Address {39:32,47:40}	R/W	0x0000	Retain	This data is the lower 15:0 bits of the destination address that must be seen repeated 16 times in a received packet in order for it to be a Magic Packet. This must be programmed since the PHY has no other way of knowing what the Destination Address is.

Table 188: IO Pad Control
Device 4, Register 0x821A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Slew Rate Control for MDIO pad	R/W	2'b01	Retain	00 = Slowest Edge Rate 11 = Fastest Edge Rate
13:12	Slew Rate Control for INTn Pad	R/W	2'b01	Retain	00 = Slowest Edge Rate 11 = Fastest Edge Rate
11:6	Reserved	R/W	0x00	Retain	
5	Pull-Down Enable for INTn Pad	R/W	0x0	Retain	1 = Enable Pull-Down for Pad
4	Pull-Up Enable for INTn Pad	R/W	0x0	Retain	1 = Enable Pull-Up for Pad
3	Pull-Down Enable for TXC/TXD/TCLK pads	R/W	0x1	Retain	1 = Enable Pull-Down for Pad
2	Pull-Up Enable for GPIO pad	R/W	0x1	Retain	1 = Enable Pull-Up for Pad
1	Pull-Up Enable for TX_ENABLE pad	R/W	0x1	Retain	1 = Enable Pull-Up for Pad
0	Pull-Up Enable for MDIO pad	R/W	0x0	Retain	1 = Enable Pull-Up for Pad

Table 189: GPIO Control Register
Device 4, Register 0x821B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0x0000	Retain	
0	Enable the selected wake source to the GPIO Pin	R/W	0x0	Retain	1 = Bring out the selected wake source to the GPIO pin

Table 190: Undervoltage Control
Device 4, Register 0x8700

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W, SC	0x0	Retain	
14:4	Reserved	R/W	0x000	Retain	
3	DVDD Undervoltage Enable	R/W	0x0	Retain	1 = Enable Undervoltage Circuit for DVDD Undervoltage Detection 0 = Disable Undervoltage Circuit for DVDD Undervoltage Detection
2	AVDD33 Undervoltage Enable	R/W	0x0	Retain	1 = Enable Undervoltage Circuit for AVDD33 Undervoltage Detection 0 = Disable Undervoltage Circuit for AVDD33 Undervoltage Detection
1	AVDD15 Undervoltage Enable	R/W	0x0	Retain	1 = Enable Undervoltage Circuit for AVDD15 Undervoltage Detection 0 = Disable Undervoltage Circuit for AVDD15 Undervoltage Detection
0	VDDO Undervoltage Enable	R/W	0x0	Retain	1 = Enable Undervoltage Circuit for VDDO Undervoltage Detection 0 = Disable Undervoltage Circuit for VDDO Undervoltage Detection

Table 191: Undervoltage Interrupt Enable
Device 4, Register 0x8703

Bits	Field	Mode	HW Rst	SW Rst	Description
15	DVDD Up Enable	R/W	0x0	Retain	1 = Enable Interrupt when DVDD is above the required voltage threshold for Normal Operation
14	AVDD33 Up Enable	R/W	0x0	Retain	1 = Enable Interrupt when AVDD33 is above the required voltage threshold for Normal Operation
13	AVDD15 Up Enable	R/W	0x0	Retain	1 = Enable Interrupt when AVDD15 is above the required voltage threshold for Normal Operation
12	VDDO Up Enable	R/W	0x0	Retain	1 = Enable Interrupt when VDDO is above the required voltage threshold for Normal Operation
11	VLPR Up Enable	R/W	0x0	Retain	1 = Enable Interrupt when VLPR is above the required voltage threshold for Normal Operation
10:6	Reserved	R/W	0x00	Retain	
5	FIRSTBOOT Enable	R/W	0x0	Retain	1 = Enable Interrupt for FIRSTBOOT event
4	VLPR Down Enable	R/W	0x0	Retain	1 = Enable Interrupt when VLPR is below the required voltage threshold for Normal Operation
3	DVDD Down Enable	R/W	0x0	Retain	1 = Enable Interrupt when DVDD is below the required voltage threshold for Normal Operation
2	AVDD33 Down Enable	R/W	0x0	Retain	1 = Enable Interrupt when AVDD33 is below the required voltage threshold for Normal Operation
1	AVDD15 Down Enable	R/W	0x0	Retain	1 = Enable Interrupt when AVDD15 is below the required voltage threshold for Normal Operation
0	VDDO Down Enable	R/W	0x0	Retain	1 = Enable Interrupt when VDDO is below the required voltage threshold for Normal Operation

Table 192: Undervoltage Status
Device 4, Register 0x8704

Bits	Field	Mode	HW Rst	SW Rst	Description
15	DVDD Up	RO, LH	0x0	Retain	1 = DVDD is above the required voltage threshold for Normal Operation
14	AVDD33 Up	RO, LH	0x0	Retain	1 = AVDD33 is above the required voltage threshold for Normal Operation
13	AVDD15 Up	RO, LH	0x0	Retain	1 = AVDD15 is above the required voltage threshold for Normal Operation
12	VDDO Up	RO, LH	0x0	Retain	1 = VDDO is above the required voltage threshold for Normal Operation
11	VLPR Up	RO, LH	0x0	Retain	1 = VLPR is above the required voltage threshold for Normal Operation
10:6	Reserved	RO, LH	0x00	Retain	
5	FIRSTBOOT Event	RO, LH	0x0	Retain	1 = FIRSTBOOT event happened
4	VLPR Down	RO, LH	0x0	Retain	1 = VLPR is below the required voltage threshold for Normal Operation
3	DVDD Down	RO, LH	0x0	Retain	1 = DVDD is below the required voltage threshold for Normal Operation
2	AVDD33 Down	RO, LH	0x0	Retain	1 = AVDD33 is below the required voltage threshold for Normal Operation
1	AVDD15 Down	RO, LH	0x0	Retain	1 = AVDD15 is below the required voltage threshold for Normal Operation
0	VDDO Down	RO, LH	0x0	Retain	1 = VDDO is below the required voltage threshold for Normal Operation

Table 193: APHY Register ID
Device 4, Register 0x8EFF

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	APHY Model Number	RO	0000_0000_001	0000_0000_001	Automotive PHY Model Number
4:0	SKU Number	RO	See Descr.	See Descr.	88Q1110 device = 00000 88Q1111 device = 00001

Table 194: Wake Source Sent out the GPIO Pin
Device 4, Register 0xFD20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0x0	0x0	
8	Register WAKE Request Enable	R/W	See Descr.	Retain	1 = The GPIO output pin will be asserted when the Wake Request register bit is asserted 0 = The GPIO output pin will not be asserted when the Wake Request register bit is asserted Note that the default of this bit is 0 unless programmed to 1 by the user.
7	Host Side Wake Request Enable	R/W	See Descr.	Retain	1 = The GPIO output pin will be asserted when q Wake Request is sent out of the Host side is asserted 0 = The GPIO output pin will not be asserted when a Wake Request is sent out of the Host side is asserted Note that the default of this bit is 0 unless programmed to 1 by the user.
6	Local Wake Enable	R/W	See Descr.	Retain	1 = The GPIO output pin will be asserted when a valid pulse is presented at the WAKE_IN pin (a local wake request) waking the device out of Deep Sleep 0 = The GPIO output pin will not be asserted when a valid pulse is presented at the WAKE_IN pin (a local wake request) waking the device out of Deep Sleep Note that the default of this bit is 0 unless programmed to 1 by the user.
5	Remote Wake Enable	R/W	See Descr.	Retain	1 = The GPIO output pin will be asserted a valid signal is presented at the MDIP/N pins (a remote wake request). 0 = The GPIO output pin will not be asserted when a valid signal is presented at the MDIP/N pins (a remote wake request) Note that the default of this bit is 0 unless programmed to 1 by the user.

Table 194: Wake Source Sent out the GPIO Pin
Device 4, Register 0xFD20

Bits	Field	Mode	HW Rst	SW Rst	Description
4	Powered Local Wake Enable	R/W	See Descr.	Retain	1 = The GPIO output pin will be asserted when a valid pulse is presented at the WAKE_IN pin (a local wake request) waking the device out of T1 Port Sleep Mode. 0 = The GPIO output pin will not be asserted when a valid pulse is presented at the WAKE_IN pin (a local wake request) waking the device out of T1 Port Sleep Mode. Note that the default of this bit is 0 unless programmed to 1 by the user.
3	Link Up Wake Request Enable	R/W	See Descr.	Retain	1 = The GPIO output pin will be asserted when a Wake request is received from the line when link is up (a WUR) 0 = The GPIO output pin will not be asserted when a Wake request is received from the line when link is up (a WUR) Note that the default of this bit is 0 unless programmed to 1 by the user.
2:0	Reserved	R/W	0x0	0x0	These bits are Read Only and should not be written to.

3.5 Auto-Negotiation Registers

Table 195: Auto-Negotiation Registers – Register Map

Register Name	Register Address	Table and Page
Auto-Negotiation Device Identifier 1 (0002)	Device 7, Register 0x0002	Table 196, p. 170
Auto-Negotiation Device Identifier 2 (0003)	Device 7, Register 0x0003	Table 197, p. 170
Auto-Negotiation Devices in Package 1 (0005)	Device 7, Register 0x0005	Table 198, p. 170
Auto-Negotiation Devices in Package 2 (0006)	Device 7, Register 0x0006	Table 199, p. 171
Auto-Negotiation Package Identifier 1 (000E)	Device 7, Register 0x000E	Table 200, p. 171
Auto-Negotiation Device Identifier 2 (000F)	Device 7, Register 0x000F	Table 201, p. 172
BASE T1 Auto-Negotiation Control (Hex 0200 Decimal 512)	Device 7, Register 0x0200	Table 202, p. 172
BASE T1 Auto-Negotiation Status (Hex 0201 Decimal 513)	Device 7, Register 0x0201	Table 203, p. 172
Auto-Negotiation Advertisement Register 1 (Hex 0202 Decimal 514)	Device 7, Register 0x0202	Table 204, p. 173
Auto-Negotiation Advertisement Register 2 (Hex 0203 Decimal 515)	Device 7, Register 0x0203	Table 205, p. 174
Auto-Negotiation Advertisement Register 3 (Hex 0204 Decimal 516)	Device 7, Register 0x0204	Table 206, p. 174
Link Partner Base Page Ability Register 1 (Hex 0205 Decimal 517)	Device 7, Register 0x0205	Table 207, p. 174
Link Partner Base Page Ability Register 2 (Hex 0206 Decimal 518)	Device 7, Register 0x0206	Table 208, p. 175
Link Partner Base Page Ability Register 3 (Hex 0207 Decimal 519)	Device 7, Register 0x0207	Table 209, p. 175
Next Page Transmit Register / Extended Next Page Transmit Register (Hex 0208 Decimal 520)	Device 7, Register 0x0208	Table 210, p. 175
Extended Next Page Transmit Register Unformatted Code Field U0 to U15 (Hex 0209 Decimal 521)	Device 7, Register 0x0209	Table 211, p. 175
Extended Next Page Transmit Register Unformatted Code Field U16 to U31 (Hex 020A Decimal 522)	Device 7, Register 0x020A	Table 212, p. 176
Link Partner Next Page Register / Link Partner Extended Next Page Ability Register (Hex 021B Decimal 539)	Device 7, Register 0x021B	Table 213, p. 176
Link Partner Extended Next Page Ability Register Unformatted Code Field U0 to U15 (Hex 021C Decimal 540)	Device 7, Register 0x021C	Table 214, p. 176
Link Partner Extended Next Page Ability Register Unformatted Code Field U16 to U31 (Hex 021D Decimal 541)	Device 7, Register 0x021D	Table 215, p. 177

Table 196: Auto-Negotiation Device Identifier 1 (0002)
Device 7, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	Marvell OUI is 00:0A:C2 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit18

Table 197: Auto-Negotiation Device Identifier 2 (0003)
Device 7, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x02	0x02	Organizationally Unique Identifier bits 19:24 00 0010 ^.....^ bit 19...bit24
9:4	Model Number	RO	110010	110010	Represents Automotive PHY products.
3:0	Revision Number	RO	0001	0001	Identifies the revision of the Device.

Table 198: Auto-Negotiation Devices in Package 1 (0005)
Device 7, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	Set to 0000000000
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-Negotiation present in package
6	Reserved	RO	0x0	0x0	Set to 0
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS present in package 0 = DTE XS not present in package
4	PHY XS Present	RO	0x0	0x0	1 = PHY XS present in package 0 = PHY XS not present in package
3	PCS Present	RO	0x1	0x1	1 = PCS present in package 0 = PCS not present in package
2	WIS Present	RO	0x0	0x0	1 = WIS present in package 0 = WIS not present in package

Table 198: Auto-Negotiation Devices in Package 1 (0005)
Device 7, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD present in package 0 = PMA/PMD not present in package
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package

Table 199: Auto-Negotiation Devices in Package 2 (0006)
Device 7, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Vendor Specific Device 2 Present	RO	0	0	1 = Vendor-specific device 2 present 0 = Vendor-specific device 2 not present
14	Vendor Specific Device 1 Present	RO	0	0	1 = Vendor-specific device 1 present 0 = Vendor-specific device 1 not present
13:0	Reserved	RO	0x0000	0x0000	Set to 00000000000000

Table 200: Auto-Negotiation Package Identifier 1 (000E)
Device 7, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	Marvell OUI is 00:0A:C2 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit18

Table 201: Auto-Negotiation Device Identifier 2 (000F)
Device 7, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x02	0x02	Organizationally Unique Identifier bits 19:24 00 0010 ^.....^ bit 19...bit24
9:4	Model Number	RO	110010	110010	Represents Automotive PHY products.
3:0	Revision Number	RO	0001	0001	Identifies the revision of the Device.

Table 202: BASE T1 Auto-Negotiation Control (Hex 0200 Decimal 512)
Device 7, Register 0x0200

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x1	0x1	This register will perform a software reset of the t-unit. 1 = Reset 0 = Normal
14:13	Reserved	RO	0x0	Retain	Set to 0
12	Auto-Negotiation Enable	R/W	0x0	Retain	A change in this bit will cause Auto-Negotiation to restart. 1 = Enable Auto-Negotiation process 0 = Disable Auto-Negotiation process
11:10	Reserved	RO	0x0	Retain	Set to 00
9	Restart Auto-Negotiation	R/W, SC	0x0	0x0	Setting this bit will cause Auto-Negotiation to restart. 1 = Restart Auto-Negotiation process 0 = Normal operation
8:0	Reserved	RO	0x000	0x000	Set to 00000000

Table 203: BASE T1 Auto-Negotiation Status (Hex 0201 Decimal 513)
Device 7, Register 0x0201

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	Set to 00000000
6	Page Received	RO, LH	0x0	0x0	This bit is set when a new link code word has been received and is stored in registers 7.0205, 7.0206, and 7.0207 if extended next pages are used, and in registers 7.021B, 7.021C, and 7.021D if regular next pages are used. 1 = A new page has been received 0 = A new page has not been received
5	Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete

Table 203: BASE T1 Auto-Negotiation Status (Hex 0201 Decimal 513)
Device 7, Register 0x0201

Bits	Field	Mode	HW Rst	SW Rst	Description
4	Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected
3	Auto-Negotiation Ability	RO	0x1	0x1	1 = PHY able to perform Auto-Negotiation
2	Link Status	RO,LL	0x0	0x0	This register bit indicates whether link status was down since the last read. For the current link status, read this register back-to-back. 1 = Link is up 0 = Link is down
1	Reserved	RO	0x0	0x0	
0	LP Autoneg Ability	RO	0x0	0x0	1 = LP is able to perform Auto-Negotiation 0 = LP is not able to perform Auto-Negotiation

Table 204: Auto-Negotiation Advertisement Register 1 (Hex 0202 Decimal 514)
Device 7, Register 0x0202

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	If 100BASE-T is advertised or extended next page is advertised and enabled, the required next pages are automatically transmitted. If no additional next pages are needed, register 7.0202.15 should be set to 0. 1 = Advertise 0 = Not advertised
14	Ack	RO	0x0	0x0	Value always 0, writes ignored
13	Remote Fault	R/W	0x0	Retain	1 = Set remote fault bit 0 = Do not set remote fault bit
12	Enable Device in Force Mode During Autoneg	R/W	0x0	Retain	1 = Force mode, force it to be Master/Slave 0 = Prefer mode
11:10	Pause	R/W	0x0	Retain	Used to advertise Pause capability; capability not related to the PHY
9:5	Echoed Nonce Field	R/W	0x00	Retain	
4:0	Selector Field	R/W	0x01	Retain	Selector field mode 00001 = 802.3

Note: A write to register 7.0202.15:0 does not take effect until any one of the following occur:
A) Soft reset (register 1.0000.15, 3.0000.15, 7.0200.15, or any other soft reset)
B) Low Power (register 1.0000.11, 3.0000.11, or any other low power) transitions from low power down to normal operation
C) Restart Auto-Negotiation is asserted (register 7.0200.9)
D) Auto-Negotiation Enable toggles (register 7.0200.12)

Table 205: Auto-Negotiation Advertisement Register 2 (Hex 0203 Decimal 515)
Device 7, Register 0x0203

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Technology Ability Field	R/W	0x001	Retain	Set to 0x001
4	Master/Slave	R/W	strap	Retain	1 = Master 0 = Slave
3:0	Transmitted Nonce Field	R/W	0x0	Retain	Set to 0s

Note: Same as register 7.0202

Table 206: Auto-Negotiation Advertisement Register 3 (Hex 0204 Decimal 516)
Device 7, Register 0x0204

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Technology Ability Field	R/W	0x0000	Retain	Set to 0s

Note: Same as register 7.0202

Table 207: Link Partner Base Page Ability Register 1 (Hex 0205 Decimal 517)
Device 7, Register 0x0205

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Ack	RO	0x0	0x0	Received Code Word Bit 14 1 = Link partner received link code word
13	Remote Fault	RO	0x0	0x0	Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
12	Force Master/Slave	RO	0x0	0x0	Received Code Word Bit 12 1 = Link Partner will force master
11:10	Pause	RO	0x0	0x0	Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
9:5	Echoed Nonce Field	RO	0x00	0x00	Link partner Echoed Nonce field
4:0	Selector Field	RO	0x00	0x00	Link partner Selector field

Table 208: Link Partner Base Page Ability Register 2 (Hex 0206 Decimal 518)
Device 7, Register 0x0206

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Technology Ability Field	RO	0x000	Retain	Link partner Technology field
4:0	Transmitted Nonce Field	RO	0x00	Retain	Link partner Echoed Nonce field

Table 209: Link Partner Base Page Ability Register 3 (Hex 0207 Decimal 519)
Device 7, Register 0x0207

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Technology Ability Field	RO	0x0000	Retain	Link partner Technology Ability field

Table 210: Next Page Transmit Register / Extended Next Page Transmit Register (Hex 0208 Decimal 520)
Device 7, Register 0x0208

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Note: A write to register 7.0208 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded.
This register is used for regular next page exchange and extended next page exchange.
Link fail will clear Reg 7.0208.

Table 211: Extended Next Page Transmit Register Unformatted Code Field U0 to U15 (Hex 0209 Decimal 521)
Device 7, Register 0x0209

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	R/W	0x0000	0x0000	U15 to U0

Note: A write to register 7.0208 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded, hence register 7.0209 should be written before register 7.0208 is written.
This register is used for extended next page exchange and is not used for regular next page exchange.
Link fail will clear register 7.0209.

Table 212: Extended Next Page Transmit Register Unformatted Code Field U16 to U31 (Hex 020A Decimal 522)
Device 7, Register 0x020A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	R/W	0x0000	0x0000	U31 to U16

Note: A write to register 7.0208 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded, hence register 7.020A should be written before register 7.0208 is written.
This register is used for extended next page exchange and is not used for regular next page exchange.
Link fail will clear register 7.020A.

Table 213: Link Partner Next Page Register / Link Partner Extended Next Page Ability Register (Hex 021B Decimal 539)
Device 7, Register 0x021B

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Receive Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Receive Code Word Bit 14
13	Message Page	RO	0x0	0x0	Receive Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Receive Code Word Bit 12
11	Toggle	RO	0x0	0x0	Receive Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Receive Code Word Bit 10:0

Note: This register is used for regular next page exchange and extended next page exchange.
Link fail will clear register 7.021B.

Table 214: Link Partner Extended Next Page Ability Register Unformatted Code Field U0 to U15 (Hex 021C Decimal 540)
Device 7, Register 0x021C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	RO	0x0000	0x0000	U15 to U0

Note: This register is used for extended next page exchange and is not used for regular next page exchange.
Link fail will clear register 7.021C.

Table 215: Link Partner Extended Next Page Ability Register Unformatted Code Field U16 to U31 (Hex 021D Decimal 541)
Device 7, Register 0x021D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	RO	0x0000	0x0000	U31 to U16

Note: This register is used for extended next page exchange and is not used for regular next page exchange.
Link fail will clear register 7.021D.

3.6 SGMII Registers

Note Only SGMII mode (31.8010.1:0 = 10) using 100 Mbps speed is supported. Any references to other modes should be disregarded.

Table 216: SGMII – Register Map

Register Name	Register Address	Table and Page
Fiber Control Register	Device 31, Register 0x8000	Table 217, p. 179
Fiber Status Register	Device 31, Register 0x8001	Table 218, p. 180
PHY Identifier	Device 31, Register 0x8002	Table 219, p. 181
PHY Identifier	Device 31, Register 0x8003	Table 220, p. 181
Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 31.8010.1:0 = 01)	Device 31, Register 0x8004	Table 221, p. 182
Fiber Auto-Negotiation Advertisement Register - SGMII (Register 31.8010.1:0 = 10)	Device 31, Register 0x8004	Table 222, p. 183
Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 31.8010.1:0 = 01)	Device 31, Register 0x8005	Table 223, p. 184
Fiber Link Partner Ability Register - SGMII (Register 31.8010.1:0 = 10)	Device 31, Register 0x8005	Table 224, p. 185
Fiber Auto-Negotiation Expansion Register	Device 31, Register 0x8006	Table 225, p. 185
Fiber Next Page Transmit Register	Device 31, Register 0x8007	Table 226, p. 186
Fiber Link Partner Next Page Register	Device 31, Register 0x8008	Table 227, p. 186
Extended Status Register	Device 31, Register 0x800F	Table 228, p. 187
Fiber Specific Control Register 1	Device 31, Register 0x8010	Table 229, p. 187
Fiber Specific Status Register	Device 31, Register 0x8011	Table 230, p. 188
Fiber Interrupt Enable Register	Device 31, Register 0x8012	Table 231, p. 189
Fiber Interrupt Status Register	Device 31, Register 0x8013	Table 232, p. 190
Fiber Receive Error Counter Register	Device 31, Register 0x8015	Table 233, p. 191
PRBS Control	Device 31, Register 0x8017	Table 234, p. 191
PRBS Error Counter LSB	Device 31, Register 0x8018	Table 235, p. 192
PRBS Error Counter MSB	Device 31, Register 0x8019	Table 236, p. 192
Fiber Specific Control Register 2	Device 31, Register 0x801A	Table 237, p. 192
Packet Generation	Device 31, Register 0x801C	Table 238, p. 193
CRC Counters	Device 31, Register 0x801D	Table 239, p. 193
Checker Control	Device 31, Register 0x801E	Table 240, p. 194
Packet Generation	Device 31, Register 0x801F	Table 241, p. 194

Table 217: Fiber Control Register
Device 31, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Fiber Reset	R/W	0x0	SC	Fiber Software Reset. Affects 31.80xx registers. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD of the internal bus is looped back to RXD of the internal bus. Link is broken when loopback is enabled. Loopback speed is determined by the mode the device is in. 1000BASE-X - loopback is always in 1000Mbps. SGMII - loopback follows the current speed specified. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	RO, R/W	0x0	Retain	If register 31.8010.1:0 (MODE[1:0]) = 01 (1000BASE-X mode) then this bit is always 0. If register 31.8010.1:0 (MODE[1:0]) = 10 (SGMII mode) then this bit is 1 when the PHY is at 100Mb/s, else it is 0. This bit is undefined if register 31.8010.1:0 (MODE[1:0]) = 00 or 11.
12	Auto-Negotiation Enable	R/W	0x1	Retain	If the value of this bit is changed, the link will be broken and Auto-Negotiation restarted For SGMII, Auto-Negotiation is enabled by default. For 1000BASE-X, Auto-Negotiation is off by default. When this bit gets set/reset, Auto-negotiation is restarted (bit 31.8000.9 is set to 1). 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	Power Down	R/W	See Descr.	0x0	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (31.8000.15) and Restart Auto-Negotiation (31.8000.9) are not set by the user. The Fiber logic will be powered down and this bit is set to 1 when the device is in RGMII mode 1 = Power down 0 = Normal operation
10	Isolate	RO	0x0	0x0	This function is not supported
9	Restart Fiber Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware, software reset (31.8000.15) or change in Auto-Negotiation enable (31.8000.12) regardless of whether or not the restart bit (31.8000.9) is set. The bit is set when Auto-negotiation is Enabled or Disabled in 31.8000.12 1 = Restart Auto-Negotiation Process 0 = Normal operation

Table 217: Fiber Control Register
Device 31, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Duplex Mode	R/W	0x1	Retain	Writing this bit has no effect unless one of the following events occur: Software reset is asserted (Register 31.8000.15) Restart Auto-Negotiation is asserted (Register 31.8000.9) Auto-Negotiation Enable changes (Register 31.8000.12) Power down (Register 31.8000.11) transitions from power down to normal operation 1 = Full-duplex 0 = Half-Duplex
7	Collision Test	RO	0x0	0x0	This bit has no effect.
6	Speed Selection (MSB)	RO, R/W	0x1	Retain	If register 31.8010.1:0 (MODE[1:0]) = 01 (1000BASE-X mode) then this bit is always 1. If register 31.8010.1:0 (MODE[1:0]) = 10 (SGMII mode) then this bit is 1 when the PHY is at 1000Mb/s, else it is 0. This bit is undefined if register 31.8010.1:0 (MODE[1:0]) = 00 or 11.
5:0	Reserved	RO	Always 000000	Always 000000	Always 0.

Table 218: Fiber Status Register
Device 31, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0	Always 0	0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	Always 0	Always 0	0 = PHY not able to perform full duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	Always 0	Always 0	0 = PHY not able to perform half-duplex 100BASE-X
12	10 Mb/s Full Duplex	RO	Always 0	Always 0	0 = PHY not able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	Always 0	Always 0	0 = PHY not able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	Always 0	Always 0	0 = PHY not able to perform full-duplex 100BASE-T2
9	100BASE-T2 Half-Duplex	RO	Always 0	Always 0	0 = PHY not able to perform half-duplex 100BASE-T2
8	Extended Status	RO	Always 1	Always 1	1 = Extended status information in Register 31.800F
7	Reserved	RO	Always 0	Always 0	Always 0.
6	MF Preamble Suppression	RO	Always 1	Always 1	1 = PHY accepts management frames with preamble suppressed

Table 218: Fiber Status Register (Continued)
Device 31, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
5	Fiber Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete Bit is not set when link is up due of Fiber Auto-Negotiation Bypass or if Auto-Negotiation is disabled.
4	Fiber Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected This bit is always 0 in SGMII mode.
3	Auto-Negotiation Ability	RO	See Descr.	See Descr.	1 = PHY able to perform Auto-Negotiation
2	Fiber Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 31.8011.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Reserved	RO,LH	Always 0	Always 0	Always 0
0	Extended Capa-bility	RO	Always 1	Always 1	1 = Extended register capabilities

Table 219: PHY Identifier
Device 31, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	Marvell OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 31.8002.15:0 show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18

Table 220: PHY Identifier
Device 31, Register 0x8003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 6'b000010	Always 6'b000010	Organizationally Unique Identifier bits 19:24 000011 ^.....^ bit 19...bit24
9:0	Reserved	RO	6'b000000	6'b000000	

Table 221: Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 31.8010.1:0 = 01)
Device 31, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 31.8000.15) Restart Auto-Negotiation is asserted (Register 31.8000.9) Power down (Register 31.8000.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
14	Reserved	RO	Always 0	Always 0	Always 0.
13:12	Remote Fault 2/ Remote Fault 1	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 31.8000.15) Re-start Auto-Negotiation is asserted (Register 31.8000.9) Power down (Register 31.8000.11) transitions from power down to normal operation Link goes down Device has no ability to detect remote fault. 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	Always 000	Always 000	Always set to 000
8:7	Pause	R/W	See Descr.	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 31.8000.15) Re-start Auto-Negotiation is asserted (Register 31.8000.9) Power down (Register 31.8000.11) transitions from power down to normal operation Link goes down 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.

Table 221: Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 31.8010.1:0 = 01)
Device 31, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
6	1000BASE-X Half-Duplex	R/W	See Descr.	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 31.8000.15) Re-start Auto-Negotiation is asserted (Register 31.8000.9) Power down (Register 31.8000.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
5	1000BASE-X Full-Duplex	R/W	0x1	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 31.8000.15) Re-start Auto-Negotiation is asserted (Register 31.8000.9) Power down (Register 31.8000.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
4:0	Reserved	R/W	0x00	0x00	Reserved bit is R/W to allow for forward compatibility with future IEEE standards.

Table 222: Fiber Auto-Negotiation Advertisement Register - SGMII (Register 31.8010.1:0 = 10)
Device 31, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link Status	RO	0x0	0x0	0 = Link is Not up on the Copper Interface 1 = Link is up on the Copper Interface
14	Reserved	RO	Always 0	Always 0	Must be 0.
13	Reserved	RO	Always 0	Always 0	Must be 0.
12	Duplex Status	RO	0x0	0x0	0 = Interface Resolved to Half Duplex 1 = Interface Resolved to Full Duplex
11:10	Speed[1:0]	RO	0x0	0x0	00 = Reserved 01 = Interface speed is 100 Mbps 10 = Interface speed is 1000 Mbps 11 = Reserved
9	Transmit Pause	RO	0x0	0x0	Note that if register 31.8010.7 is set to 0 then this bit is always forced to 0. 0 = Disabled 1 = Enabled

Table 222: Fiber Auto-Negotiation Advertisement Register - SGMII (Register 31.8010.1:0 = 10)
Device 31, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Receive Pause	RO	0x0	0x0	Note that if register 31.8010.7 is set to 0 then this bit is always forced to 0. 0 = Disabled 1 = Enabled
7	Fiber/Copper	RO	0x0	0x0	Note that if register 31.8010.7 is set to 0 then this bit is always forced to 0. 0 = Copper media, 1 = Fiber media
6:0	Reserved	RO	Always 0000001	Always 0000001	Always set to 0000001 as per the SGMII Specification

Table 223: Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 31.8010.1:0 = 01)
Device 31, Register 0x8005

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:12	Remote Fault 2/ Remote Fault 1	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13:12 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:9
8:7	Asymmetric Pause	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.

Table 223: Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 31.8010.1:0 = 01)
Device 31, Register 0x8005

Bits	Field	Mode	HW Rst	SW Rst	Description
6	1000BASE-X Half-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 6 1 = Link partner capable of 1000BASE-X half-duplex. 0 = Link partner not capable of 1000BASE-X half-duplex.
5	1000BASE-X Full-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 5 1 = Link partner capable of 1000BASE-X full-duplex. 0 = Link partner not capable of 1000BASE-X full-duplex.
4:0	Reserved	RO	0x00	0x00	Received Code Word Bits 4:0 are always 0

Table 224: Fiber Link Partner Ability Register - SGMII (Register 31.8010.1:0 = 10)
Device 31, Register 0x8005

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Must be 0
14	Acknowledge	RO	0x0	0x0	Acknowledge Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:0	Reserved	RO	0x0000	0x0000	Received Code Word Bits 13:0 Must receive 00_0000_0000_0001 per SGMII spec

Table 225: Fiber Auto-Negotiation Expansion Register
Device 31, Register 0x8006

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	Reserved. Always 00000000000.
3	Link Partner Next page Able	RO	0x0	0x0	For SGMII mode this bit is always 0. For 1000BASE-X mode register 31.8006.3 is set when a base page is received and the received link control word has bit 15 set to 1. The bit is cleared when link goes down. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	Always 1	Always 1	1 = Local Device is Next Page able

Table 225: Fiber Auto-Negotiation Expansion Register
Device 31, Register 0x8006

Bits	Field	Mode	HW Rst	SW Rst	Description
1	Page Received	RO, LH	0x0	0x0	Register 31.8006.1 is set when a valid page is received. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when there is sync status, the fiber receiver has received 3 non-zero matching valid configuration code groups and Auto-negotiation is enabled in register 31.8000.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 226: Fiber Next Page Transmit Register
Device 31, Register 0x8007

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to this register implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. This register only has effect in 1000BASE-X mode. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11. This bit is internally set to the opposite value each time a page is received
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 227: Fiber Link Partner Next Page Register
Device 31, Register 0x8008

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	This register only has effect in 1000BASE-X mode. The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12

Table 227: Fiber Link Partner Next Page Register
Device 31, Register 0x8008

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 228: Extended Status Register
Device 31, Register 0x800F

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	See Descr.	See Descr.	1 = 1000BASE-X full duplex capable 0 = not 1000BASE-X full duplex capable
14	1000BASE-X Half-Duplex	RO	See Descr.	See Descr.	1 = 1000BASE-X half duplex capable 0 = not 1000BASE-X half duplex capable
13	1000BASE-T Full-Duplex	RO	0x0	0x0	0 = not 1000BASE-T full duplex capable
12	1000BASE-T Half-Duplex	RO	0x0	0x0	0 = not 1000BASE-T half duplex capable
11:0	Reserved	RO	0x000	0x000	000000000000

Table 229: Fiber Specific Control Register 1
Device 31, Register 0x8010

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Fiber Transmit FIFO Depth	R/W	0x1	Retain	00 = 2KB packet @ ±100ppm 01 = 10KB packet @ ±100ppm 10 = 18KB packet @ ±100ppm 11 = 27KB packet @ ±100ppm
13	Block Carrier Extension Bit	R/W	0x0	Retain	Carrier extension and carrier extension with error are converted to idle symbols on the RXD only during full duplex mode. 1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension
12	SERDES Loopback	R/W	0x0	0x0	Register 31.8010.8 selects the line loopback path. 1 = Enable loopback from SERDES input to SERDES output 0 = Normal Operation
11	Assert CRS on Transmit	R/W	0x0	Retain	This bit has no effect in full-duplex. 1 = Assert on transmit 0 = Never assert on transmit

Table 229: Fiber Specific Control Register 1
Device 31, Register 0x8010

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Force Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. 1 = Force link good 0 = Normal operation
9	Reserved	R/W	0x0	Retain	Set to 0.
8	SERDES Loop-back Type	R/W	0x0	Retain	0 = Loopback Through PCS (Tx and Rx can be asynchro-nous) 1 = Loopback raw 10 bit data (Tx and Rx must be synchro-nous)
7:6	Reserved	R/W	0x0	Update	
5	Marvell Remote Fault Indication Enable	R/W	0x0	Retain	0 = Disable 1 = Enable, Remote Fault is indicated to link partner in less than 2 ms, only one bit of bit 5:4 can be set to 1
4	IEEE Remote Fault Indication Enable	R/W	0x0	Retain	0 = Disable 1 = Enable, Remote Fault is indicated to link partner after 20ms according to IEEE standard, only one bit of bit 5:4 can be set to 1
3	Reserved	R/W	0x1	Update	Must be set to 1
2	Reserved	R/W	0x1	Retain	Must be set to 1
1:0	Mode	R/W	0x2	See Descr.	The following modes of operation are supported: 00 = Reserved 01 = 1000BASE-X mode 10 = SGMII System mode 11 = Reserved

Table 230: Fiber Specific Status Register
Device 31, Register 0x8011

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO Always 100	2'b00	Retain	These status bits are valid only after resolved bit 31.8011.11 = 1. The resolved bit is set when Auto-Negotia-tion is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 31.8011.11 = 1. The resolved bit is set when Auto-Negotiation is com-pleted or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received

Table 230: Fiber Specific Status Register
Device 31, Register 0x8011

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled this bit is always 1. 1 = Resolved 0 = Not resolved
10	Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9:8	Reserved	RO	Always 0x0	Always 0x0	Always 0x0
7:6	Remote Fault Received	RO, LH	0x0	0x0	The mapping for this status is as follows: 00 = No Fault 01 = Link Failure detected at link partner 10 = Offline 11 = Auto-neg Error
5	Sync status	RO	0x0	0x0	1 = Sync status 0 = No Sync status
4	Fiber Energy Detect Status	RO	0x1	0x1	1 = No energy detected 0 = Energy Detected
3	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 31.8011.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
2	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 31.8011.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
1:0	Reserved	RO	Always 0x0	Always 0x0	Always 0x0

Table 231: Fiber Interrupt Enable Register
Device 31, Register 0x8012

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Always 0
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 231: Fiber Interrupt Enable Register
Device 31, Register 0x8012

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	FIFO Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6	Reserved	RO	Always 0	Always 0	0
5	Remote Fault Received Changed Enable	R/W	0x0	0x0	1 = Interrupt enable 0 = Interrupt disable
4	Fiber Energy Detect Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
3:0	Reserved	RO	Always 0000	Always 0000	0000

Table 232: Fiber Interrupt Status Register
Device 31, Register 0x8013

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	Always 0	Always 0	Always 0
12	Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier

Table 232: Fiber Interrupt Status Register
Device 31, Register 0x8013

Bits	Field	Mode	HW Rst	SW Rst	Description
7	FIFO Error	RO,LH	0x0	0x0	1 = FIFO Error 0 = No FIFO Error
6	Reserved	RO	0x0	0x0	0
5	Remote Fault Received Changed Enable	RO, LH	0x0	0x0	1 = Remote Fault received changed, read 31.8011.7:6 for detail 0 = No change on remote fault received
4	Fiber Energy Detect Changed	RO,LH	0x0	0x0	1 = Energy Detect state changed 0 = No Energy Detect state change detected
3:0	Reserved	RO	Always 00000	Always 00000	00000

Table 233: Fiber Receive Error Counter Register
Device 31, Register 0x8015

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported.

Table 234: PRBS Control
Device 31, Register 0x8017

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Set to 0s
7	Invert Checker Polarity	R/W	0x0	Retain	0 = Normal 1 = Invert
6	Invert Generator Polarity	R/W	0x0	Retain	0 = Normal 1 = Invert
5	PRBS Lock	R/W	0x0	Retain	0 = Counter Free Runs 1 = Do not start counting until PRBS locks first
4	Clear Counter	R/W, SC	0x0	0x0	0 = Normal 1 = Clear Counter
3:2	Pattern Select	R/W	0x0	Retain	00 = PRBS 7 01 = PRBS 23 10 = PRBS 31 11 = Generate 1010101010... pattern
1	PRBS Checker Enable	R/W	0x0	0x0	0 = Disable 1 = Enable
0	PRBS Generator Enable	R/W	0x0	0x0	0 = Disable 1 = Enable

Table 235: PRBS Error Counter LSB
Device 31, Register 0x8018

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count LSB	RO	0x0000	Retain	A read to this register freezes register 31.8019. Cleared only when register 31.8017.4 is set to 1.

Table 236: PRBS Error Counter MSB
Device 31, Register 0x8019

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count MSB	RO	0x0000	Retain	This register does not update unless register 31.8018 is read first. Cleared only when register 31.8017.4 is set to 1.

Table 237: Fiber Specific Control Register 2
Device 31, Register 0x801A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	R/W	0x0	0x0	Set to 0s
6	Serial Interface Auto-Negotiation bypass enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. 1 = Bypass Allowed 0 = No Bypass Allowed
5	Serial Interface Auto-Negotiation bypass status	RO	0x0	0x0	1 = Serial interface link came up because bypass mode timer timed out and fiber Auto-Negotiation was bypassed. 0 = Serial interface link came up because regular fiber Auto-Negotiation completed. If this bit is 1, then bit 31.8011.11 will be 0.
4	Reserved	R/W	0x0	0x0	Set to 0s
3	Fiber Transmitter Disable	R/W	0x0	Retain	1 = Transmitter Disable 0 = Transmitter Enable
2:0	SGMII Output Amplitude	R/W	3'b010	Retain	Differential voltage peak measured. See AC/DC section for valid VOD values. 000 = 14mV 001 = 112mV 010 = 210 mV 011 = 308mV 100 = 406mV 101 = 504mV 110 = 602mV 111 = 700mV

Table 238: Packet Generation
Device 31, Register 0x801C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Burst	R/W	0x00	Retain	0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets
7	Packet Generator Transmit Trigger	R/W	0x0	Retain	This bit is only valid when all of the following are true: bit 6 =1 bit3 =1 bit15:8 is not equal to all 0s A read of this bit gives the following: 1: Packet generator transmit done 0: Packet generator is transmitting data When this bit is 1 a write of 0 will trigger the packet generator to transmit again. When this bit is 0 a write of 0 or 1 will have no effect.
6	Packet Generator Enable Self Clear Control	R/W	0x0	Retain	0 = Bit 3 will self clear after all packets are sent 1 = Bit 3 will stay high after all packets are sent
5	Reserved	R/W	0x0	Retain	
4	Enable CRC Checker	R/W	0x0	Retain	1 = Enable 0 = Disable
3	Enable Packet Generator	R/W	0x0	Retain	1 = Enable 0 = Disable
2	Payload of Packet to Transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = 5A,A5,5A,A5,...
1	Length of Packet to Transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored Packet	R/W	0x0	Retain	1 = Tx packets with CRC errors & Symbol Error 0 = No error

Table 239: CRC Counters
Device 31, Register 0x801D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Count	RO	0x00	Retain	0x00 = no packets received 0xFF = 256 packets received (max count). Bit 31.801C.4 must be set to 1 in order for register to be valid.
7:0	CRC Error Count	RO	0x00	Retain	0x00 = no CRC errors detected in the packets received. 0xFF = 256 CRC errors detected in the packets received (max count). Bit 31.801C.4 must be set to 1 in order for register to be valid.

Table 240: Checker Control
Device 31, Register 0x801E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0x000	Retain	
4	CRC Counter Reset	R/W, SC	0x0	Retain	1 = Reset This bit will self-clear after writing 1.
3:0	Reserved	R/W	0x0	Retain	

Table 241: Packet Generation
Device 31, Register 0x801F

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Constant Packet Payload Enable	R/W	0x0	Retain	Enables a constant payload for packets generated by the packet generator. 1 = Enable constant packet payload 0 = Use other payload options
14	Constant Packet Payload Type	R/W	0x0	Retain	This bit selects the type of constant payload to use and is valid only when 31.801F.15 = 1 1 = use all 1s packet payload 0 = use all 0s packet payload
13:8	Reserved	R/W	0x00	Retain	
7:0	IPG Length	R/W	0x0B	Retain	The number in bit [7:0]+1 is the number of bytes for IPG

4 PTP Registers

The device's PTP registers are accessible using the MDC and MDIO pins and support the IEEE Serial Management Interface (SMI – Clause 22) used for PHY devices.

The PTP registers in the device are made up of one or more fields. The way in which each of these fields operate is defined by the field's Type. The function of each Type is described below.

Table 242: Register Types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs.
RES	Reserved. All reserved bits are read as zero unless otherwise noted.
Retain	The register value is retained after software reset is executed.
RO	Read only.
ROC	Read only clear. After read, register field is cleared.
RW	Read and Write with initial value indicated.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, register field is cleared to zero.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete.
Update	Value written to the register field does not take effect until soft reset is executed.
WO	Write only. Reads from this type of register field return undefined data.
NR	Non-Rollover Register

Table 243: PTP Registers – Register Map (Sheet 1 of 2)

Register Name	Register Address	Table and Page
PTP Port Config Register	Register 4.8800 – PTP Port	Table 244, p. 198
PTP Port Config Register	Register 4.8801 – PTP Port	Table 245, p. 199
PTP Port Config Register	Register 4.8802 – PTP Port	Table 246, p. 200
PTP Port Config Register	Register 4.8803 – PTP Port	Table 247, p. 202
PTP Port Status Register	Register 4.8808 – PTP Port	Table 248, p. 203
PTP Port Status Register	Register 4.8809 – PTP Port	Table 249, p. 204
PTP Port Status Register	Register 4.880A – PTP Port	Table 250, p. 204
PTP Port Status Register	Register 4.880B – PTP Port	Table 251, p. 204
PTP Port Status Register	Register 4.880C – PTP Port	Table 252, p. 205
PTP Port Status Register	Register 4.881D – PTP Port	Table 253, p. 206
PTP Port Status Register	Register 4.881E – PTP Port	Table 254, p. 206
PTP Port Status Register	Register 4.880F – PTP Port	Table 255, p. 206
PTP Port Status Register	Register 4.8900 – PTP Port	Table 256, p. 207
PTP Port Status Register	Register 4.8901 – PTP Port	Table 257, p. 208
PTP Port Status Register	Register 4.8902 – PTP Port	Table 258, p. 208
PTP Port Status Register	Register 4.8903 – PTP Port	Table 259, p. 208
Ingress Mean Path Delay Register	Register 4.890C – PTP Port	Table 260, p. 208
Ingress Path Delay Asymmetry Register	Register 4.891D – PTP Port	Table 261, p. 209
Egress Path Delay Asymmetry Register	Register 4.891E – PTP Port	Table 262, p. 209
PTP Global Config Register	Register 4.8E00 – PTP Global	Table 263, p. 210
PTP Global Config Register	Register 4.8E01 – PTP Global	Table 264, p. 210
PTP Global Config Register	Register 4.8E02 – PTP Global	Table 265, p. 211
PTP Global Config Register	Register 4.8E07 – PTP Global	Table 266, p. 211
PTP Mode Register, Index: 0x00	N/A	Table 267, p. 211
PTP Status Register	Register 4.8E08 – PTP Global	Table 268, p. 212
ReadPlus Command Register	Register 4.8E1E – PTP Global	Table 269, p. 213
ReadPlus Data Register	Register 4.8E1F – PTP Global	Table 270, p. 214
PTP Global Time Array Register	Register 4.8F00 – PTP Global	Table 271, p. 214
TAI Global Time Array Register	Register 4.8F01 – PTP Global	Table 272, p. 214
PTP Global Time Array Register	Register 4.8F02 – PTP Global	Table 273, p. 214
PTP Global Time Array Register	Register 4.8F03 – PTP Global	Table 274, p. 216
PTP Global Time Array Register	Register 4.8F04 – PTP Global	Table 275, p. 216
PTP Global Time Array Register	Register 4.8F05 – PTP Global	Table 276, p. 216
PTP Global Time Array Register	Register 4.8F06 – PTP Global	Table 277, p. 216
PTP Global Time Array Register	Register 4.8F07 – PTP Global	Table 278, p. 216
PTP Global Time Array Register	Register 4.8F08 – PTP Global	Table 279, p. 217
PTP Global Time Array Register	Register 4.8F09 – PTP Global	Table 280, p. 217
PTP Global Time Array Register	Register 4.8F0A – PTP Global	Table 281, p. 217
PTP Global Time Array Register	Register 4.8F0B – PTP Global	Table 282, p. 217
PTP Global Time Array Register	Register 4.8F0C – PTP Global	Table 283, p. 218

Table 243: PTP Registers – Register Map (Sheet 2 of 2)

Register Name	Register Address	Table and Page
PTP Global Time Array Register	Register 4.8F1D – PTP Global	Table 284, p. 218
PTP Global Time Array Register	Register 4.8F1E – PTP Global	Table 285, p. 218
TAI Global Config Register	Register 4.8C00 – TAI	Table 286, p. 220
TAI Global Config Register	Register 4.8C01 – TAI	Table 287, p. 224
TAI Global Config Register	Register 4.8C02 – TAI	Table 288, p. 224
TAI Global Config Register	Register 4.8C03 – TAI	Table 289, p. 224
TAI Global Config Register	Register 4.8C04 – TAI	Table 290, p. 225
TAI Global Config Register	Register 4.8C05 – TAI	Table 291, p. 225
TAI Global Status Register	Register 4.8D00 – TAI	Table 292, p. 226
TAI Global Status Register	Register 4.8D01 – TAI	Table 293, p. 228
TAI Global Status Register	Register 4.8D02 – TAI	Table 294, p. 228
TAI Global Status Register	Register 4.8C1E – TAI	Table 295, p. 228
TAI Global Status Register	Register 4.8C0F – TAI	Table 296, p. 229
TAI Global Config Register	Register 4.8C09 – TAI	Table 297, p. 229
TAI Global Config Register	Register 4.8C0A – TAI	Table 298, p. 229
TAI Global Config Register	Register 4.8C0B – TAI	Table 299, p. 229

4.1 PTP Port Registers

Table 244: PTP Port Config Register (Sheet 1 of 2)
Register 4.8800 – PTP Port

Bits	Field	Type	Description
15:12	TransSpec	RWS 0x1	PTP Transport Specific value. The Transport Specific bits present in PTP Common header are used to differentiate between IEEE1588, IEEE802.1AS etc. frames. This is to differentiate between various timing protocols running on either Layer2 or higher protocol layers. In addition to comparing the EtherType to determine that the incoming frame is a PTP frame, the TransSpec bits are compared to the incoming PTP common headers' Transport Specific bits. If there is a match then hardware logic time stamps the frames indicated by MsgTypeEn and optionally interrupts the CPU. If there is no match, and Transport Spec checking is enabled (see DisTSpecCheck bit below) the hardware will not perform any operations in the PTP core. For IEEE 1588 networks this is expected to be configured to a 0x0 and for IEEE 802.1AS networks this is expected to be configured to 0x1. The only valid TransSpec values for PTP hardware acceleration (PTP Port Register 4.8802) are 0x0 and 0x1.
11	DisTSpec Check	RWR	Disable Transport Specific Check. 0 = Enable checking for Transport Spec 1 = Disable checking for Transport Spec When this bit is cleared to a zero the Transport Spec part of the PTP Common header of incoming frames must match the configured TransSpec (above) in order for time stamping to occur (PTP hardware accelerated or not). This setting limits PTP time stamping to frames containing a TransSpec value that matches the value in the TransSpec register above. This allows time stamping to be limited to only IEEE 1588 or to only IEEE 802.1AS per their frame's Transport Specs (assuming their value is contained in the TransSpec register above). When this bit is set to a one the Transport Spec checking of the PTP frames is not performed before time stamping occurs. This setting allows PTP time stamping for all TransSpec values (although PTP hardware acceleration, PTP Port Register 4.8802, only works on IEEE 1588 and IEEE 802.1AS TransSpec values).
10:2	Reserved	RES	
1	DisTS Overwrite	RWR	Disable Time Stamp Counter Overwriting. 0 = Overwrite unread Time Stamps in the registers with new data 1 = Keep unread Time Stamps in the registers until read When this bit is cleared to a zero, PTPArr0Time, PTPArr1Time and PTPDepTime values get overwritten even though their corresponding valid bits (defined in PTP Port Status Data Structure below), are not cleared. When this bit is set to one, PTPArr0Time, PTPArr1Time and PTPDepTime values do not get overwritten with new time stamps until their corresponding valid bits (defined in PTP Port Status Data Structure below), are cleared.

Table 244: PTP Port Config Register (Sheet 2 of 2)
Register 4.8800 – PTP Port

Bits	Field	Type	Description
0	DisPTP	RWS	Disable Precise Time Stamp logic. 0 = PTP logic on this port is enabled 1 = PTP logic on this port is disabled When PTP logic is disabled the hardware logic does not recognize or timestamp PTP frames. Even interrupt generation logic is disabled. This disable disables all modes of PTP on this port (including PTP hardware acceleration if enabled - PTP Port Register 4.8802). **NOTE:** PTP should not be enabled on half-duplex ports when ArrTSMode or HWAccel (PTP Port Register 4.8802) are non zero.

Table 245: PTP Port Config Register
Register 4.8801 – PTP Port

Bits	Field	Type	Description
15:14	Reserved	RES	
13:8	IPJump	RWR	Internet Protocol Jump added to ETJump below. Set this register to point to the start of the frame's IP Version byte (802.1Q tagged frames are automatically compensated by ETJump). This field specifies how many bytes to skip starting at the first byte of the frame's EtherType (that is, where ETJump, below, left off) in order to jump to the beginning of the IPv4 or IPv6 headers in the frame. If an IPv4 or IPv6 version is found at this location of the frame, Layer 4 PTP processing occurs from there. This allows flexibility in the hardware to skip past the protocol chains that are specific to customer networks including MPLS etc. For example if ETJump is programmed to 0xC and IPJump is programmed to 0x16, this indicates to hardware to skip 0x22 bytes in order to get to the IP header. It can either be IPv4 or IPv6 header. **NOTE:** A value of 0x0 (default) is a special case that prevents further frame searching if ETJump did not find a match (that is, a zero value in IPJump prevents the IPJump mechanism from searching further).
7:5	Reserved	RES	
4:0	ETJump	RWS 0xC	EtherType Jump points to the start of the frame's EtherType (assuming it is not 802.1Q tagged). This field specifies how many bytes to skip starting from the start of the MAC-DA of the frame in order to get to the first byte of the EtherType of the frame. Frames found with an 0x8100 EtherType (802.1Q tag) at this location are automatically searched 4 bytes further into the frame for the next EtherType to compare (this extension is done once). If the PTPEType value (PTP Global Register 4.8E00) is found as the Ether Type in the frame, Layer 2 PTP processing occurs. If 0x0800 or 0x86DD is found the Layer 4 PTP processing occurs. If none of these values is found, PTP frame decoding is passed to the IPJump field above. This allows flexibility in the hardware to skip past the protocol chains that are specific to customer networks including DSA-Tag, IEEE802.1Q tag, Provider tag etc.

Table 246: PTP Port Config Register (Sheet 1 of 2)
Register 4.8802 – PTP Port

Bits	Field	Type	Description
15:8	ArrTSMode	RWR	Arrival Time Stamp Mode. This field is used to configure the Arrival Time Stamp mode as follows: 0x00 = Arrival Time Stamp frame modification is disabled. 0x01 = Add the PTPArr[x]Time associated with enabled PTP Event frames at the end of the frame increasing the frame's size by four bytes. 0x02 to 0x0F = Reserved 0x10 to 0xEF = Overwrite the PTPArr[x]Time associated with enabled PTP Event frames into the frame without increasing the frame's size. The location in the frame where the PTPArr[x]Time is placed is controlled by this register. It is placed ArrTSMode bytes past the start of the PTP Common Header. **For example, to place the time stamp in the four Reserved bytes in the PTP Common Header, set this register to a value of 0x10.** If the end of the frame is reached prior to the completion of this overwrite, the PTPArr[x]Time is placed at the end of the frame increasing the frame's size by enough bytes for it to fit. 0xF0 to 0xFF = Reserved **NOTE:** All frames will be processed using the above settings unless the frame can be hardware accelerated via setting the HWAccel bit below to a one. **NOTE:** Changing this register's value can only occur when PTP is idle. **NOTE:** Added PTPArr[x]Time bytes that increase the frame's size are included in the MIB counters and policy is performed on the resulting frame (for example, TCAM matching and frame size checking). This register must be zero if ExtHWAccel (below) is set to a one.
7	FilterAct	RWR	Filter LED Activity. 0 = LED Activity is activated for all frames 1 = LED Activity is not activated for most IEEE 802.1 frames This bit can filter all or most of the 802.1 Protocol frames from the Port's Activity LEDs. When this bit is set to a one all 802.1 protocol frames (those with a DA = 01:C2:80:00:00:0x) will be potentially filtered from the port's Activity LED as determined by the ArrLEDCtrl and DepLEDCtrl registers (PTP Port Register 4.8803). When this bit is cleared to a zero only the 802.1 gPTP protocol frames will be potentially filtered from the port's Activity LED.

Table 246: PTP Port Config Register (Sheet 2 of 2)
Register 4.8802 – PTP Port

Bits	Field	Type	Description
6	HWAccel	RWR	Port PTP Hardware Acceleration enable. 0 = No, or only Ingress PTP hardware acceleration 1 = Ingress and Egress PTP hardware acceleration is enabled Setting this bit to a one enables PTP hardware acceleration on this port. PTP hardware acceleration will automatically occur in the selected PTPMode (PTP Global Register 4.8E07) for the enabled PTP Domains once a Time Array (PTP Global Registers 4.8F02 to 4.8F0C, and 4.8F1D to 4.8F1E) is configured and enabled. Even then PTP hardware acceleration will only occur for the Transport Specs enabled on this port (PTP Port Register 4.8800). In this mode, any frame that cannot be hardware accelerated will be processed using the settings defined by ArrTSMode above (a type of fallback mode). Clearing this bit to a zero causes all frames to be processed using the settings defined by ArrTSMode above. Do not set this bit to a one if ExtHWAccel (below) is set to a one. **NOTE:** PTP Hardware Acceleration requires that the Time Stamping Clock Period (TAI Register 4.8C01) be 8000 picoseconds (8 ns) ± 100 PPM. **NOTE:** Changing this register's value can only occur when PTP is idle.
5	KeepSA	RWR	Keep Frame's SA. 0 = Place Port's SA into modified egressing PTP frames 1 = Keep the frame's SA even for modified egressing PTP frames Normally when the Data portion of a frame (the part of the frame between the EtherType and the CRC) is modified the address of the modifying entity is placed into the Source Address (SA) field of egressing frames. When this bit is cleared to zero this is what is done for modified PTP frames. When this bit is set to a one the SA portion of PTP frames is not modified.
4:2	Reserved	RES	
1	PTPDepInt En	RWR	PTP Port Departure Interrupt enable. 0 = Disable PTP Departure capture interrupts 1 = Enable PTP Departure capture interrupts This field enables the per-port interrupt for outgoing PTP frame from this port. When this bit is set to a one and this ports' PTPDepTimeValid bit (PTP Port Register 4.8900) is set to a one a PTP interrupt for this port will be indicted in PTP Global Register (register 4.8E08). **NOTE:** Hardware logic only time stamps the PTP frames when configured to do so by MsgTypeEn field (see PTP Global Register 4.8E00).
0	PTPArrInt En	RWR	PTP Port Arrival Interrupt enable. 0 = Disable PTP Arrival capture interrupts 1 = Enable PTP Arrival capture interrupts This field enabled the per-port interrupt for incoming PTP frames from this port. When this bit is set to a one and this port's PTPArr0TimeValid bit (PTP Port Register 4.8808) or its PTPArr1TimeValid bit (PTP Port Register 4.880C) is set to a one a PTP interrupt for this port will be indicated in PTP Global Register (register 4.8E08). **NOTE:** Hardware logic only time stamps the PTP frames when configured to do so by MsgTypeEn field (see PTP Global Register 4.8E00).

Table 247: PTP Port Config Register
Register 4.8803 – PTP Port

Bits	Field	Type	Description
15:8	ArrLED Ctrl	RWR	LED control for packets entering the device. When 0x0, if a received frame is classified as a PTP frame or an 802.1 protocol frame, the LED does not blink. But it blinks for every non-PTP or non-802.1 protocol frame. When 0x1, the LED blinks for every received frame classified as a PTP frame or an 802.1 protocol frame. It also blinks for every non-PTP frame or non-802.1 protocol frame. When 0xn, the LED blinks once for every n received frames classified as PTP or 802.1 protocol. It also blinks for every non-PTP frame or non-802.1 protocol frame. **NOTE:** This tracks all received PTP frames (even though the PTP core time stamps only the PTP event messages) and not just PTP frames that need time stamping or it tracks all received 802.1 protocol frames (any frame with a DA = 01:C2:80:00:00:0x). The FilterAct bit in PTP Port (register 4.8802) controls which frames are tracked. This register affect the port's Activity LED only. It does not change how the frames progress through the switch.
7:0	DepLED Ctrl	RWS 0x80	LED control for packets departing the device. When 0x0, if a transmitting frame is classified as a PTP frame or an 802.1 protocol frame, the LED does not blink. But it blinks for every non-PTP frame or non-802.1 protocol. When 0x1, the LED blinks for every transmitting frame classified as a PTP frame or an 802.1 protocol frame. It also blinks for every non-PTP frame or non-802.1 protocol frame. When 0xn, the LED blinks once for every n transmitting frames classified as PTP or 802.1 protocol. It also blinks for every non-PTP frame or non-802.1 protocol frame. **NOTE:** This tracks all transmitting PTP frames (even though the PTP core time stamps only the PTP event messages) and not just PTP frames that need time stamping or it tracks all transmitted 802.1 protocol frames (any frame with a DA = 01:C2:80:00:00:0x). The FilterAct bit in PTP Port (register 4.8802) controls which frames are tracked. This register affect the port's Activity LED only. It does not change how the frames progress through the switch.

Table 248: PTP Port Status Register
Register 4.8808 – PTP Port

Bits	Field	Type	Description
15:3	Reserved	RES	
2:1	PTPArr0IntStatus	RWR	PTP Arrival Time 0 Interrupt Status. The PTP Arrival time 0 Interrupt bit gets set for a given port when an incoming PTP frame is time stamped in PTPArr0Time counter as long as that frame was not hardware accelerated (see HWAccel in PTP Port (register 4.8802)). 0x0 = Normal, that is, none of the error conditions stated below are valid for this packet. 0x1 = If the PTPArr0Time counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that needed to use arrival0 counters arrived into the switch through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = If the incoming frame could not be time stamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPArr0TimeValid was 0x1 when this PTPFrame was processed in hardware logic. This can happen when there is more than one PTP frame that needs time stamping into arrival 0 counters arrives into the switch core before CPU clears the valid bits for the previous frame. 0x3 = Reserved **NOTE:** If the PTP frame gets discarded inside the switch for policy, CRC, queue congestion or any other reasons then one of the PTP arrival discard counters get updated (PTPNonTSArrDisCtr or PTPTSArrDisCtr). See the discard counter descriptions (PTP Port Register 4.8905) for further details.
0	PTPArr0 TimeValid	RWR	PTP Arrival 0 Time Valid. When the PTPArr0Time value is updated by hardware (which it will not do as long as the frame is hardware accelerated – see HWAccel in PTP Port (register 4.8802)), this bit is set to a 0x1 validating the time counter. 0x0 = PTPArr0Time is not valid. 0x1 = PTPArr0Time is valid and PTPArr0IntStatus represents the status information for the PTPArr0Time counter. Note that this is set by hardware for the frames which are assured to reach the CPU. For frames with CRC error etc., this bit will not be set but either PTPNonTSArrCtr or PTPTSArrCtr is updated. **NOTE:** This valid bit needs to be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware has no way to figure out if software is done reading all the relevant registers for a particular Time counter before clearing the valid bit.

Table 249: PTP Port Status Register
Register 4.8809 – PTP Port

Bits	Field	Type	Description
15:0	PTPArr0 Time [15:0]	RWR	PTP Arrival 0 Time counter bits [15:0] of a 32-bit register. This indicates the PTP Arrival 0 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPArr0TimeValid bit and PTPArr0IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one TSClkPer amount. The upper 16 bits of this register are contained in the register below.

Table 250: PTP Port Status Register
Register 4.880A – PTP Port

Bits	Field	Type	Description
15:0	PTPArr0 Time [31:16]	RWR	PTP Arrival 0 Time counter bits [31:16] of a 32-bit register. This indicates the PTP Arrival 0 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPArr0TimeValid bit and PTPArr0IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one TSClkPer amount. The lower 16 bits of this register are contained in the register above.

Table 251: PTP Port Status Register
Register 4.880B – PTP Port

Bits	Field	Type	Description
15:0	PTPArr0 SeqId	RWR	PTP Arrival 0 Sequence Identifier. This indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose time stamp information has been captured by hardware logic in PTPArr0Time register.

Table 252: PTP Port Status Register
Register 4.880C – PTP Port

Bits	Field	Type	Description
15:3	Reserved	RES	
2:1	PTPArr1IntStatus	RWR	PTP Arrival Time 1 Interrupt Status. The PTP Arrival time 1 Interrupt bit gets set for a given port when an incoming PTP frame is time stamped in PTPArr1Time counter as long as that frame was not hardware accelerated (see HWAccel in PTP Port (register 4.8802)). 0x0 = Normal, that is, none of the error conditions stated below are valid for this packet. 0x1 = If the PTPArr1Time counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that needed to use arrival1 counters arrived into the switch through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s).0x2 = If the incoming frame could n0t be time stamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPArr1TimeValid was 0x1 when this PTPFrame was processed in hardware logic. This can happen when there is more than one PTP frame that needs time stamping into arrival 1 counters arrives into the switch core before CPU clears the valid bits for the previous frame. 0x3 = Reserved **NOTE:** If the PTP frame gets discarded inside the switch for policy, CRC, queue congestion or any other reasons then one of the PTP arrival discard counters get updated (PTPNonTSArrDisCtr or PTPTSArrDisCtr). See the discard counter description (PTP Port Register 4.8905) for further details.
0	PTPArr1 TimeValid	RWR	PTP Arrival 1 Time Valid. When the PTPArr1Time value is updated by hardware (which it will not do as long as the frame is hardware accelerated – see HWAccel in PTP Port (register 4.8802)), this bit is set to a 0x1 validating the time counter. 0x0 = PTPArr1Time is not valid. 0x1 = PTPArr1Time is valid and PTPArr1IntStatus represents the status information for the PTPArr1Time counter. Note that this is set by hardware for the frames which are assured to reach the CPU. For frames with CRC error etc., this bit will not be set but either PTPNonTSArrCtr or PTPTSArrCtr is updated. **NOTE:** This valid bit needs to be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware has no way to figure out if software is done reading all the relevant registers for a particular Time counter before clearing the valid bit.

Table 253: PTP Port Status Register
Register 4.881D – PTP Port

Bits	Field	Type	Description
15:0	PTPArr1 Time [15:0]	RWR	PTP Arrival 1 Time counter bits [15:0] of a 32-bit register. This indicates the PTP Arrival 1 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPArr1TimeValid bit and PTPArr1IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one TSClkPer amount. The upper 16 bits of this register are contained in the register below.

Table 254: PTP Port Status Register
Register 4.881E – PTP Port

Bits	Field	Type	Description
15:0	PTPArr1 Time [31:16]	RWR	PTP Arrival 1 Time counter bits [31:16] of a 32-bit register. This indicates the PTP Arrival 1 time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPArr1TimeValid bit and PTPArr1IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one TSClkPer amount. The lower 16 bits of this register are contained in the register above.

Table 255: PTP Port Status Register
Register 4.880F – PTP Port

Bits	Field	Type	Description
15:0	PTPArr1 SeqId	RWR	PTP Arrival 1 Sequence Identifier. This indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose time stamp information has been captured by hardware logic in PTPArr1Time register.

Table 256: PTP Port Status Register
Register 4.8900 – PTP Port

Bits	Field	Type	Description
15:3	Reserved	RES	
2:1	PTPDepIntStatus	RWR	PTP Departure Time Interrupt Status. The PTP Departure time Interrupt bit gets set for a given port when an incoming PTP frame is time stamped in PTPDepTime counter as long as that frame was not hardware accelerated (see HWAccel in PTP Port (register 4.8802)). 0x0 = Normal, that is, none of the error conditions stated below are valid for this packet. 0x1 = If the PTPDepTime counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that needed to use departure counter departed out of the switch through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = If the outgoing frame could not be time stamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPDepTimeValid was 0x1 when this PTPFrame was processed in hardware logic. This can happen when there is more than one PTP frame that needs time stamping into departure counter leaves the switch core before CPU clears the valid bits for the previous frame. 0x3 = Reserved **NOTE:** If the PTP frame gets discarded inside the switch for CRC reasons then the PTP departure discard counter gets updated (PTPNonTSDepDisCtr or PTPTSDepDisCtr). See the discard counter description (PTP Port Register 4.8905) for further details.
0	PTPDep TimeValid	RWR	PTP Departure Time Valid. When the PTPDepTime value is updated by hardware (which it will not do as long as the frame is hardware accelerated – see HWAccel in PTP Port (register 4.8802)), this bit is set to a 0x1 validating the time counter. 0x0 = PTPDepTime is not valid. 0x1 = PTPDepTime is valid and PTPDepIntStatus represents the status information for the PTPDepTime counter. Note that this is set by hardware for the frames which are assured to depart the port. For frames with CRC error etc., this bit will not be set but either PTPNonTSDepCtr or PTPTSDepCtr is updated. **NOTE:** This valid bit needs to be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware has no way to figure out if software is done reading all the relevant registers for a particular Time counter before clearing the valid bit.

Table 257: PTP Port Status Register
Register 4.8901 – PTP Port

Bits	Field	Type	Description
15:0	PTPDep Time [15:0]	RWR	PTP Departure Time counter bits [15:0] of a 32-bit register. This indicates the PTP Departure time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPDepTimeValid bit and PTPDepIntStatus indicates the status of the PTP frame through the device described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one TSClkPer amount. The upper 16 bits of this register are contained in the register below.

Table 258: PTP Port Status Register
Register 4.8902 – PTP Port

Bits	Field	Type	Description
15:0	PTPDep Time [31:16]	RWR	PTP Departure Time counter bits [31:16] of a 32-bit register. This indicates the PTP Departure time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPDepTimeValid bit and PTPDepIntStatus indicates the status of the PTP frame through the device described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one TSClkPer amount. The lower 16 bits of this register are contained in the register above.

Table 259: PTP Port Status Register
Register 4.8903 – PTP Port

Bits	Field	Type	Description
15:0	PTPDep SeqId	RWR	PTP Departure Sequence Identifier. This indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose time stamp information has been captured by hardware logic in PTPDepTime register.

Table 260: Ingress Mean Path Delay Register
Register 4.890C – PTP Port

Bits	Field	Type	Description
15:0	Mean PathDelay	RWR	Ingress Mean Path Delay register. This indicates the cable delay between this port and its link partner in unsigned nanoseconds. This is used in HWAccel PTP mode (PTP Port (register 4.8802)).

Table 261: Ingress Path Delay Asymmetry Register
Register 4.891D – PTP Port

Bits	Field	Type	Description
15	IPDA Sign	RWR	Ingress Path Delay Asymmetry Sign. 0 = The Ingress Path Delay Asymmetry number is added 1 = The Ingress Path Delay Asymmetry number is subtracted This indicates the sign of the asymmetry value (below) beyond the Mean Path Delay (PTP Port Register 4.890C) that needs to be adjusted for more accurate cable measurements.
14:0	Ingress PathDelay Asymmetry	RWR	Ingress Path Delay Asymmetry register. This indicates the asymmetry value beyond the Mean Path Delay (PTP Port Register 4.890C) that needs to be added for more accurate cable measurements. This register is in unsigned nanoseconds.

Table 262: Egress Path Delay Asymmetry Register
Register 4.891E – PTP Port

Bits	Field	Type	Description
15	EPDA Sign	RWR	Egress Path Delay Asymmetry Sign. 0 = The Egress Path Delay Asymmetry number is added 1 = The Egress Path Delay Asymmetry number is subtracted This indicates the sign of the asymmetry value (below) beyond the Mean Path Delay (PTP Port Register 4.890C) that needs to be adjusted for more accurate cable measurements.
14:0	Egress PathDelay Asymmetry	RWR	Egress Path Delay Asymmetry register. This indicates the asymmetry value beyond the Mean Path Delay (PTP Port Register 4.890C) needs to be subtracted for more accurate cable measurements. This register is in unsigned nanoseconds.

4.2 PTP Global Registers

Table 263: PTP Global Config Register
Register 4.8E00 – PTP Global

Bits	Field	Type	Description
15:0	PTPEType	RWS to 0x88F7	PTP EtherType. All layer 2 PTP frames are recognized using a combination of a specific EtherType and MessageType values (part of the PTP Common Header). This field is used to identify the EtherType on these frames. The MsgTypeEn (specified below in register 4.8E01) qualifies the types of frames that the hardware needs to time stamp. For IEEE 802.1AS and IEEE1588 over Layer 2 Ethernet, the EtherType is expected to be programmed to 0x88F7.

Table 264: PTP Global Config Register
Register 4.8E01 – PTP Global

Bits	Field	Type	Description
15:0	MsgType En	RWR	Message Type Time Stamp Enable. MessageType is part of the PTP common header. There are PTP frames which need to be time stamped and some that do not need to be. This field identifies the PTP frame types that need to be time stamped for frames that are not hardware accelerated – see HWAccel in PTP Port Register 4.8802). The MessageType read from PTP frames is vectorized[1] and then used to access the appropriate bit in this register. If the selected bit is set to a one then that frame type will be time stamped both in ingress and egress. Else that frame type will not be time stamped. For example if MessageType field (in the PTP common header) with a value of 0x4 needs to be time stamped in hardware then MsgTypeEn[4] should be set to a one. Then the incoming PTP frames with a MessageTypefield of 0x4 will get time stamped into one of the Port's two available arrival capture registers (either PTPArr0Time or PTPArr1Time as identified by TSArrPtr[4] bit below). All outgoing PTP frames with the MessageType field of 0x4 will be timestamped into the Port's PTPDepTime capture register.

1. Vectorized term here refers to converting the hexadecimal MessageType field into a sixteen bit binary number.

Table 265: PTP Global Config Register
Register 4.8E02 – PTP Global

Bits	Field	Type	Description
15:0	TSArrPtr	RWR	Time Stamp Arrival Time Capture Pointer. If the incoming PTP frame needs to be time stamped (based on MsgTypeEn), this field determines whether the hardware logic should use PTPArr0Time or PTPArr1Time for storing the arriving frames' time stamp information. This field corresponds to the sixteen combinations of the vectorized MessageType. For example if TSArrPtr[2] is set to a one it indicates to the hardware that if MsgTypeEn [2] is set to a one then PTP frames with MessageType = 0x2 will use PTPArr1Time counter for storing the incoming PTP frames' time stamp. On the contrary if TSArrPtr[2] is cleared to a zero that indicates to the hardware that if MsgTypeEn[2] is set to a one then PTP frames with MessageType = 0x2 will use PTPArr0Time counter for storing the incoming PTP frames' time stamp.

Table 266: PTP Global Config Register
Register 4.8E07 – PTP Global

Bits	Field	Type	Description
15	Update	SC	Update Data. When this bit is set to a one the data written to bits [7:0] will be loaded into the PTP Global Config register referenced by the Pointer bits below. After the write has taken place this bit self clears to zero.
14:8	Pointer	RWR	Pointer to the desired octet of PTP Global Config. These bits select one of the possible PTP Global Config registers for both read and write operations. A write operation occurs if the Update bit is a one (the registers can be written to by writing this register in a single operation). Otherwise a read of the current Pointer occurs and the data found there is placed in the Data bits below (the desired register can be read by first writing to this register, with Update = 0, and then reading this register). The Pointer bits are used to access the Index registers as follows: 0x00 = PTP Mode Register 0x01 to 0x7F = Reserved
7:0	Data	RWR	Octet Data of the PTP Global Config register referenced by the Pointer bits above.

The index register accessed by the PTP Global Config register is described below.

Table 267: PTP Mode Register, Index: 0x00 (Sheet 1 of 2)

Bits	Field	Type	Description
7:5	Reserved	RES	

Table 267: PTP Mode Register, Index: 0x00 (Sheet 2 of 2)

Bits	Field	Type	Description
4	AltScheme	RWR	Alternate Scheme. This bit is used to define the values that are returned in the requestReceiptTimestamp field in IEEE 1588 pDelay Response messages and the correctionField and responseOriginTimestamp in pDelay Response Follow Up messages as follows: 0 = RequestReceiptTimestamp = t2, responseOriginTimestamp = t3 and the correctionField = 0 (fractional ns) 1 = RequestReceiptTimestamp = 0, responseOriginTimestamp = 0 and the correctionField = turn around time **NOTE:** This bit has no effect if the PTP frame is an IEEE 802.1AS frame (as indicated by the frame's TransSpec field).
3	GrandMstr	RWR	Grand Master Enable. This bit is used to enable hardware support for the ports on this device to act as if they are the PTP Grand Master as follows: 0 = Hardware accelerate with this device NOT being the Grand Master 1 = Hardware accelerate with this device being the Grand Master
2	OneStep	RWR	OneStep Enable. This bit is used to enable hardware One Step support for PTP frames in the mode selected by the PTPMode bits below as follows: 0 = Hardware accelerate using AutoFollowUp Two Step frame formats 1 = Hardware accelerate using One Step frame formats **NOTE:** This device does not support the receiving of One Step frames and the hardware conversion of these frames into Two Step when the PTPMode is End to End Transparent Clock.
1:0	PTPMode	RWR	PTP Mode. This register selects the PTP Mode of the device (for all ports) as follows: 0x0 = Boundary Clock 0x1 = Peer to Peer Transparent Clock 0x2 = End to End Transparent Clock 0x3 = Reserved For these settings to have an effect, at least one Time Array (PTP Global Registers 4.8F00 to 4.8F0C and 4.8F1D to 4.8F1E) must be configured for the Domain that will be used. This mode will then take effect on the ports whose Hardware Acceleration is enabled (HWAccel is set to a one in PTP Port Register 4.8802).

Table 268: PTP Status Register (Sheet 1 of 2)
Register 4.8E08 – PTP Global

Bits	Field	Type	Description
15	TrigGen Int	ROC	Trigger generate mode Interrupt. The TrigGenInt bit gets set by the TAI block when the TrigGenIntEn is set to a one (TAI Register 4.8C00) and when the one shot pulse is generated (TrigMode is set to one in TAI Register 4.8C00). It gets cleared by the reading of this register.
14	Event Int	RO	Event Capture Interrupt. This bit gets set by the TAI block when the EventIntEn is set to a one (TAI Register 4.8C00) and when an EventReq is captured in the EventCap Register. It gets cleared by writing a zero to the EventCapValid register (TAI Register 4.8C09). **NOTE:** This interrupt bit will also be set to a one, if enabled, whenever the EventCapValid bit (TAI Register 4.8D00) is set to a one. This allows software to test its interrupt routine.

Table 268: PTP Status Register (Sheet 2 of 2)
Register 4.8E08 – PTP Global

Bits	Field	Type	Description
13:11	Reserved	RES	
10:0	PTPInt [10:0]	RO	These PTP Interrupt bits gets set for a given port when an incoming PTP frame is time stamped and PTPArrIntEn for that port is set to a one. Similarly the PTP Interrupt bits get set for a given port when an outgoing PTP frame is time stamped and PTPDepIntEn for that port is set to a one. The hardware logic sets this per port bit based on above criteria and gets cleared upon software reading and clearing the corresponding time counter valid bits that are valid for that port.

Table 269: ReadPlus Command Register
Register 4.8E1E – PTP Global

Bits	Field	Type	Description
15	Read Plus Enable	R/W	Read Plus Enable 1 = Enable 0 = Disable
14:12	Reserved	Res	Reserved
11:8	PTPReg	R/W	PTP Registers 0x0 for 4.88xx – 4.89xx 0xE for 4.8Cxx – 4.8Dxx 0xF for 4.8Exx – 4.8Fxx **NOTE:** These registers need to use ReadPlus command otherwise readback value is not correct Register 4.8F00 to 4.8F1F, PTP Global Time Array Registers Registers 4.8C1E and 4.8C0F, PTP Global Time[31:0] Registers 4.8D01 and 4.8D02, Event Capture Time[31:0] Registers 4.8808 to 4.880B, PTP Arrival 0 Registers 4.880C, 4.881D, 4.881E and 4.880F, PTP Arrival 1 Registers 4.8900 to 4.8903, PTP Departure
7:5	Reserved	RES	
4:0	PTPAddr	R/W	PTP Address PTPAddr[3:0] = Lower four bits of the address of the PTP registers to be read. For 4.88xx, PTPAddr[4] = '0' For 4.89xx, PTPAddr[4] = '1' For 4.8Cxx, PTPAddr[4] = '0' For 4.8Dxx, PTPAddr[4] = '1' For 4.8Exx, PTPAddr[4] = '0' For 4.8Fxx, PTPAddr[4] = '1'

Table 270: ReadPlus Data Register
Register 4.8E1F – PTP Global

Bits	Field	Type	Description
15:0	Read Plus Data	R/W	Read Plus Data This register is used to read out the ReadPlus Data. To read 32-bit wide PTP registers, read from this register back-to-back.

Table 271: PTP Global Time Array Register
Register 4.8F00 – PTP Global

Bits	Field	Type	Description
15:0	ToDLoadPt [15:0]	RWR	Time of Day Load Point Register bits [15:0] of a 32-bit register. The ToDLoadPt register is used in multiple ways, but its contents are always relative to the PTP Global Time (aka, H/W Time) found in TAI Global Registers 4.8C1E and 4.8C0F. This register is used as follows in the various ToD Operations: ToD Store All Registers – it is used to determine the instant in time that the selected Time Array is loaded. The load occurs at the instant the PTP Global Time (TAI Global Registers 4.8C1E and 4.8C0F) matches the contents of this register. ToD Capture – it is used to capture the instant in time that the Capture occurred. On each ToD Capture, the contents of this register will be loaded with the current value contained in the PTP Global Time (TAI Global Registers 4.8C1E and 4.8C0F). The upper 16 bits of this register are contained in the register below.

Table 272: TAI Global Time Array Register
Register 4.8F01 – PTP Global

Bits	Field	Type	Description
15:0	ToDLoadPt [31:16]	RWR	Time of Day Load Point Register bits [31:16] of a 32-bit register. Value to be matched with global timer value – used to either load or capture the TOD. See the description above. The lower 16 bits of this register are contained in the register above.

Table 273: PTP Global Time Array Register (Sheet 1 of 2)
Register 4.8F02 – PTP Global

Bits	Field	Type	Description
15	ToDBusy	SC	Time of Day Busy. This bit must be set to a one to start a ToD operation (see ToD Op below). Only one ToD operation can be executing at one time so this bit must be zero before setting it to a one. When the requested ToD operation completes this bit will automatically be cleared to a zero.

Table 273: PTP Global Time Array Register (Sheet 2 of 2)
Register 4.8F02 – PTP Global

Bits	Field	Type	Description
14:12	ToDOp	RWR	Time of Day Opcode. The following ToD Opcodes are supported and are applied to the selected Time Array as indicated below: 0x0, 0x1 = Reserved 0x2 = Store Comp register only to selected TimeArray[1] 0x3 = Store All Registers to selected TimeArray @ ToDLoadPt[2] 0x4 = Capture selected TimeArray, Comp=Comp and ToDLoadPt=PTPGT[3] 0x5 to 0x7 = Reserved **NOTE:** A Store ToDOp will start the timer if ClkValid below is set to a one.
11	Reserved	RES	
10:9	TimeArray [1:0]	RWR	Time Array. The above ToD operation is performed to/from the physical Time Array specified by this register. The device contains multiple independent Time Arrays where each Time Array consists of: • 10-byte ToD time (PTP Global Registers 4.8F03 to 4.8F07), • 8-byte 1722 time (PTP Global Registers 4.8F08 to 4.8F0B), • 4-byte Compensation (PTP Global Registers 4.8F0C to 4.8F0D), • 1-byte Domain Number (bits [7:0] below), and a 1 bit Clock Valid (bit 8 below).
8	ClkValid	RWR	Clock Valid. When this bit is set to a one and then stored to a Time Array (by using ToDOp Store All Registers) the selected Time Array will start keeping time using the parameters loaded and that Time Array will be considered active. When this bit is cleared to a zero and then stored to a Time Array the selected Time Array will stop keeping time and it will be considered inactive.
7:0	Domain Number	RWR	Domain Number. This is the IEEE 1588 or IEEE 802.1ASbt frame Domain Number that is to be associated with the selected Time Array. It is used to select which Time Array is to be used when processing PTP frames in hardware. This Domain number will only be used on active Time Arrays (that is, Time Arrays whose ClkValid bit above is set to a one).

1. Updating only the Comp (Compensation) register is needed when a Time Array is active but the PPM difference between the local crystal and the associated Time Array's Grand Master clock has changed and needs to be adjusted
2. Loading all the parameters to a Time Array at a specific ToD Load Pt time is the way to start a Time Array clock with the predetermined relationship between its associated Grand Master clock and the PTP Global Time (TAI Global Registers 4.8C1E and 4.8C0F).
3. OpCode 0x4 reads the selected Time Array's current clock values. The Tod Load Pt register is set to the current PTP Global Time value so the relationship between the two clock can be compared.

Table 274: PTP Global Time Array Register
Register 4.8F03 – PTP Global

Bits	Field	Type	Description
15:0	ToD Nano [15:0]	RWR	Time Array Time of Day, Nanosecond portion, bits [15:0] of a 32-bit register. The five ToD registers (at PTP Global Registers 4.8F03 to 4.8F07) contain the 10 byte representation of time used in IEEE 1588 and IEEE 802.1AS frames. These registers are used to load this representation of time into the selected Time Array on ToD Store All Registers operations. They contain the selected Time Array's representation of this time after ToD Capture operations complete. The upper 16 bits of this register are contained in the register below.

Table 275: PTP Global Time Array Register
Register 4.8F04 – PTP Global

Bits	Field	Type	Description
15:0	ToD Nano [31:16]	RWR	Time Array Time of Day, Nanosecond portion, bits [31:16] of a 32-bit register. See the description above. The lower 16 bits of this register are contained in the register above.

Table 276: PTP Global Time Array Register
Register 4.8F05 – PTP Global

Bits	Field	Type	Description
15:0	ToD Sec [15:0]	RWR	Time Array Time of Day, Seconds portion, bits [15:0] of a 48-bit register. See the description above. The upper 32 bits of this register are contained in the registers below.

Table 277: PTP Global Time Array Register
Register 4.8F06 – PTP Global

Bits	Field	Type	Description
15:0	ToD Sec [31:16]	RWR	Time Array Time of Day, Seconds portion, bits [31:16] of a 48-bit register. See the description above. The lower 16 bits of this register are contained in the register above. The upper 16 bits of this register are contained in the register below.

Table 278: PTP Global Time Array Register
Register 4.8F07 – PTP Global

Bits	Field	Type	Description
15:0	ToD Sec [47:32]	RWR	Time Array Time of Day, Seconds portion, bits [47:32] of a 48-bit register. See the description above. The lower 32 bits of this register are contained in the registers above.

Table 279: PTP Global Time Array Register
Register 4.8F08 – PTP Global

Bits	Field	Type	Description
15:0	1722 Nano [15:0]	RWR	Time Array 1722 Time of Day in Nanoseconds, bits [15:0] of a 64-bit register. The four 1722 ToD registers (at PTP Global Registers 4.8F08 to 4.8F0B) contain an 8 byte representation of time used in IEEE 1722 frames (IEEE1722 uses only the lower 32 bits of this time. The 64-bit representation is used in PCI-e and it is a simple extension of the IEEE 1722 representation of time that wraps). These registers are used to load this representation of time into the selected Time Array on ToD Store All Registers operations. They contain the selected Time Array's representation of this time after ToD Capture operations complete. The upper 48 bits of this register are contained in the registers below.

Table 280: PTP Global Time Array Register
Register 4.8F09 – PTP Global

Bits	Field	Type	Description
15:0	1722 Nano [31:16]	RWR	Time Array 1722 Time of Day in Nanoseconds, bits [31:16] of a 64-bit register. See the description above. The lower 16 bits of this register are contained in the register above. The upper 32 bits of this register are contained in the registers below.

Table 281: PTP Global Time Array Register
Register 4.8F0A – PTP Global

Bits	Field	Type	Description
15:0	1722 Nano [47:32]	RWR	Time Array 1722 Time of Day in Nanoseconds, bits [47:32] of a 64-bit register. See the description above. The lower 32 bits of this register are contained in the registers above. The upper 16 bits of this register are contained in the register below.

Table 282: PTP Global Time Array Register
Register 4.8F0B – PTP Global

Bits	Field	Type	Description
15:0	1722 Nano [63:48]	RWR	Time Array 1722 Time of Day in Nanoseconds, bits [63:48] of a 64-bit register. See the description above. The lower 48 bits of this register are contained in the registers above.

Table 283: PTP Global Time Array Register
Register 4.8F0C – PTP Global

Bits	Field	Type	Description
15:0	ToD Comp [15:0]	RWR	Time Array Time of Day Compensation bits [15:0] of a 32-bit register. The two Time of Day Compensation registers (at PTP Global Registers 4.8F0C and 4.8F1D) are used to define the PPM difference between the local crystal clocking this PTP block and the PTP Grand Master device that this Time Array is tracking. Bits [30:0] of this register are used to define the difference between these two clocks in increments of 465.661 zeptoseconds (or 4.65661E-19 seconds, which is less than a single attosecond. For reference, picoseconds is 10^{-12}, femptoseconds is 10^{-15}, attoseconds is 10^{-18} and zeptoseconds is 10^{-21}). Set this register to the amount of time needed to be added or subtracted to each local 125 MHz PTP clock period in order to make it match its associated Grand Master's rate (that is, the PPM difference between the two). A difference of 1 PPM for a 125 MHz local PTP clock is 8 femtoseconds (8.0E-15 seconds) or a setting of 17,182 decimal (0x431E) in this register. The full range of this register (0x7FFF FFFF) results in 1.0 ns of compensation per local PTP Clock. Bit 31 of this register is used to indicate the direction of the difference: 0 = Local clock is slow (need to add the Comp to each cycle) 1 = Local clock is fast (need to subtract the Comp from each cycle) These registers are used to load the needed Compensation to the selected Time Array on ToD Store All Registers and on ToD Store only the Comp registers operations. They contain the selected Time Array's Compensation after a ToD Capture operation completes. Once a Time Array is set active, use the ToD Store only the Comp register operation to update any detected changes in the PPM difference between the local crystal and its associated Grand Master. The upper 16 bits of this register are contained in the register below.

Table 284: PTP Global Time Array Register
Register 4.8F1D – PTP Global

Bits	Field	Type	Description
15:0	ToD Comp [31:16]	RWR	Time Array Time of Day Compensation bits [31:16] of a 32-bit register. See the description above. The lower 16 bits of this register are contained in the register above.

Table 285: PTP Global Time Array Register (Sheet 1 of 2)
Register 4.8F1E – PTP Global

Bits	Field	Type	Description
15:12	1PPS Width	RWR	Pulse Width for the 1 Pulse Per Second on the Second signal. This register defines the pulse width of the selected 1 PPS signal (see 1 PPS Select bits below) in the units defined by the 1 PPS Width Range bits below. A value of 0x1 in this register selects 1 unit. A value of 0x0 selects 0 units (that is, stops the clock).
11	Reserved	RES	

Table 285: PTP Global Time Array Register (Sheet 2 of 2)
Register 4.8F1E – PTP Global

Bits	Field	Type	Description
10:8	1PPS Width Range	RWR	Pulse Width Range for the 1 Pulse Per Second on the Second signal. This register selects the units of time used to define the 1PPS Width (above) as follows (each higher numbered selection generates units that are 8x larger than the previous lower numbered selection): 0x0 = 8 ns units for a 125 MHz PTP clock 0x1 = 64 ns units for a 125 MHz PTP clock 0x2 = 512 ns units for a 125 MHz PTP clock 0x3 = 4,096 ns units for a 125 MHz PTP clock 0x4 = 32.768 µs units for a 125 MHz PTP clock 0x5 = 262.144 µs units for a 125 MHz PTP clock 0x6 = 2.097 ms units for a 125 MHz PTP clock 0x7 = 16.777 ms units for a 125 MHz PTP clock The narrowest width is 8 ns (by setting this register to 0x0 and the 1 PPS Width register to 0x1). The widest width is 251 ms or just a bit over ¼ second (by setting this register to 0x7 and the 1 PPS Width register to 0xF).
7:4	Reserved	RES	
3	1PPS Phase	RWR	Phase of the 1 Pulse Per Second on the Second signal. When this bit is set to a one the leading edge of the 1 PPS signal (the edge that occurs at the exact start of each second) is the falling edge of the signal. When this bit is cleared to a zero the leading edge of the 1 PPS signal is the rising edge of the signal.
2	Reserved	RES	
1:0	1PPS Select	RWR	Select for the 1 Pulse Per Second on the Second signal. This register selects the Time Array that is used to generate the 1 PPS signal. Any of the Time Arrays can be selected, but only one at a time can be selected. The selected Time Array will output the leading edge of the 1 PPS signal when its ToD Seconds (PTP Global Registers 4.8F05 to 4.8F07) gets incremented. This increment occurs whenever the Time Array's ToD Nanoseconds (PTP Global Registers 4.8F08 to 4.8F0B) reaches 1,000,000 ns such that this 1 PPS signal occurs at the exact start of each second. The selected 1 PPS signal is available on LED[0] pins.

4.3 PTP TAI Registers

Table 286: TAI Global Config Register (Sheet 1 of 4)
Register 4.8C00 – TAI

Bits	Field	Type	Description
15	Event CapOv	RWR	Event Capture Overwrite. 0 = Capture and Hold first PTP Event 1 = Capture all PTP Events and Retain the last PTP Event When this bit is cleared to a zero it configures the hardware to capture a single event, that is, take a snapshot of PTP Global Timer value at the first EventReq (see EventPhase below) and wait for software to read the EventCapRegister before capturing another event. This mode returns the data from the first EventReq. When this bit is set to a one it enables overwriting the EventCap registers (TAI Registers 4.8C09 to 4.8C0B) whenever an EventReq occurs (see EventPhase below). In this mode the hardware will overwrite the EventCapRegister even if the previously captured event register data has not been read by the software. This mode returns the data from the last EventReq.
14	EventCtr Start	RWR	Event Counter Start. 0 = Do not increment the Event Capture Counter 1 = Increment the Event Capture Counter on EventReq's When this bit is cleared to zero the EventCapCtr is not modified even when EventReq occurs (see EventPhase below). When this bit is set to a one it enables incrementing the EventCapCtr register (TAI Register 4.8C09) whenever an EventReq occurs (see EventPhase below).
13	Event Phase	RWR	Event Phase. 0 = Event Requests occur on the rising edge of the PTP_EVREQ LED[1] pin 1 = Event Requests occur on the falling edge of the PTP_EVREQ LED[1] pin When this bit is cleared to a zero an EventReq occurs on the rising edge of the PTP_EVREQ input or on the leading edge of PTP_TRIG when internally sampled (see the CaptureTrig bit in TAI Register 4.8C09). When this bit is set to a one an EventReq occurs on the falling edge of the PTP_EVREQ input or on the trailing edge of PTP_TRIG when internally sampled. When PTP_TRIG is selected to be internally captured (instead of using the PTP_EVREQ LED[1] pin – see Capture Trig in TAI Register 4.8C09) this Event Phase is used to invert the value of the normal internal PTP_TRIG that is captured. When Event Phase = 0 the leading edge (or normal rising edge) of the internal PTP_TRIG is captured. When Event Phase = 1 the trailing edge (or normal falling edge) of the internal PTP_TRIG is captured.

Table 286: TAI Global Config Register (Sheet 2 of 4)
Register 4.8C00 – TAI

Bits	Field	Type	Description
12	TrigPhase	RWR	Trigger Phase. 0 = The PTP Trigger output is active high on the PTP_TRIG LED[1] pin 1 = The PTP Trigger output is active low on the PTP_TRIG LED[1] pin When this bit is cleared to a zero the active phase of the PTP_TRIG output to the LED[1] is normal active high. For example, the pulse mode of PTP_TRIG will be normally low with a high pulse and the 50% duty cycle's leading edge is the rising edge. When this bit is set to a one the active phase of the PTP_TRIG output to the LED[1] is inverted to be active low. For example, the pulse mode of PTP_TRIG will be normally high with a low pulse and the 50% duty cycle's leading edge is the falling edge. **NOTE:** This bit has no effect on the internal phase of PTP_TRIG or any other signal used in the internal blocks of the device.
11	Reserved	RES	
10	IRLClk Gen Req	RWS	Ingress Rate Limiter's Clock Generation Request/Enable. When this bit is set to a one, it enables a 50% duty cycle clock generation for the Ingress Rate Limiter's logic (IRL Clk) as configured by the IRLClkGenAmt, IRLClkComp (both ps and sub-ps) and IRLGenTime fields. On Reset, this IRL Clock defaults to a 3.125 µs rate. This rate can be changed at any time by updating the IRLClkGenAmt and/or IRLClkComp (ps and Sub ps) registers.
9	TrigGen IntEn	RWR	Trigger Generator Interrupt Enable. 0 = Mask interrupts generated by the PTP Trigger logic 1 = Enable interrupts generated by the PTP Trigger logic When this bit is cleared to zero no interrupts are generated by the TrigGen logic. When this bit is set to a one the TAI block will generate an interrupt whenever a TrigGen pulse event has occurred. This interrupt will appear in the Trigger Mode Interrupt in PTP Global Register 4.8E08.
8	EventCap IntEn	RWR	Event Capture Interrupt Enable. 0 = Mask interrupts generated by the PTP Event Capture logic 1 = Enable interrupts generated by the PTP Event Capture logic When this bit is cleared to zero no interrupts are generated by the EventCap logic. When this bit is set to a one the TAI block will generate an interrupt whenever an EventReq occurs. This interrupt will appear in the Event Capture Interrupt in PTP Global Register 4.8E08.

Table 286: TAI Global Config Register (Sheet 3 of 4)
Register 4.8C00 – TAI

Bits	Field	Type	Description
7	TrigLock	SC	Trigger Lock. When this bit is set to a one the leading edge of PTP_TRIG (see TrigPhase above) will be adjusted to the value contained in the TrigGenTime register (TAI Register 4.8D00 and 4.8D01) if and only if the leading edge of PTP_TRIG occurs ± the number of PTP Clocks as defined in the TrigLockRange register below and PTP_TRIG is enabled (TrigGenReq, below, is set to a one) and the TrigGenTime register is non-zero. **NOTE:** The TrigLockRange, the TrigGenTime registers must be configured before this bit is set to a one. Once the TrigGenTime past in time, this bit will self clear (that is, it will be active for only one possible correction per wrap around of the 32-bit Global Timer). This bit will clear if the Global time has passed even if a correction was not needed or done. When this bit clears the Lock correction amount, if any, will be registered in the Lock Correction fields for PTP_TRIG (TAI Register 4.8D02).
6:4	TrigLock Range	RWR	Trigger Locking Range. These bits are used along with the TrigLock bit above. They determine the +/- error limit to adjust and re-center the leading edge of PTP_TRIG in PTP_CLK increments (8ns if using the internal clock)
3	Block Update	RWR	Block Update. 0 = Update the 50% duty cycle clock mode registers as written 1 = Update the 50% duty cycle clock mode registers as a block When the 50% duty cycle clock mode is enabled (see TrigMode below), the following registers are used to configure that mode: TrigGenAmt (TAI Register 4.8C02 and Register 4.8C03), TrigClkComp (TAI Register 4.8C04) and TrigClkCompSubPs (TAI Register 4.8C05). To compensate for PPM drift between this node's crystal and the Grand Master's crystal, these registers may need to be updated periodically. The same is true for the IRL clock which is configured using IRLClkGenAmt (TAI Register 4.8C06), IRLClkComp (TAI Register 4.8C07) and IRLClkCompSupPs (TAI Register 4.8C08). Setting this register bit to a one allows the updated values in these register groups (TAI Registers 4.8C02 to 4.8C05 and TAI Registers 4.8C06 to 4.8C08) to be presented to the hardware together at the same time and at a time when the hardware is not using these register values. This mode ensures smooth, glitch free, updates when the contents of more than one register needs to change during an update. The contents of the TRIG registers (TAI Registers 4.8C02 to 4.8C05) are presented to the hardware as a block whenever the TrigClkCompSubPs register is written to (at TAI Register 4.8C05). The contents of the IRL_Clk registers (TAI Registers 4.8C06 to 4.8C08) are presented to the hardware as a block whenever the IRLClkCompSubPs register is written to (at TAI Register 4.8C08). This means that the software does not need to write all of these registers during an update. Only the registers that are changing need to be written to (it is assumed that the sub-picosecond register will need to be adjusted for each update, so writing to this register triggers the update).

Table 286: TAI Global Config Register (Sheet 4 of 4)
Register 4.8C00 – TAI

Bits	Field	Type	Description
2	MultiPTP Sync	RWR	Multiple PTP device sync mode. Used in systems where multiple PTP enabled devices' need to synchronize their PTP Global Time counters (TAI Registers 4.8C1E to 4.8C0F). 0 = Normal Event Request mode 1 = Enable Multiple PTP device sync mode When this bit is cleared to zero, the EventRequest interface operates normally (that is, an EventReq transfers the value of the PTP Global Time[31:0] register to the EventCapTime[31:0] register based on the setting of the EventCapOv register above). When this bit is set to a one an EventReq (see EventPhase above) transfers the value in TrigGenAmt[31:0] (TAI Registers 4.8C02 to 4.8C03) into the PTP Global Time[31:0] register (TAI Registers 4.8C1E and 4.8C0F). The EventCapTime[31:0] (TAI Registers 4.8D01 and 4.8D02) is also updated at the same time with the previous value that the PTP Global Time[31:0] register contained prior to be updated.
1	TrigMode	RWR	Trigger Mode. 0 = 50% duty cycle clock mode 1 = Pulse (one-shot) mode When this bit is cleared to zero the 50% duty cycle clock mode is enabled. In this mode the value specified in the TrigGenAmt is used as the period for generating a 50% duty cycle clock on the PTP_TRIG signal. Note that the minimum clock period that can be generated on the PTP_TRIG signal is 4 times the TSClkPer amount. The frequency of this clock can be adjusted in ps increments (see TrigClkComp, TAI Register 4.8C04) and it can be realigned to a specific time (see TrigLock bit above). The first leading edge of the 50% duty cycle clock will occur the first time the PTP Global Time (PTP TAI Registers 4.8C1E and 4.8C0F) equals the value in the non-zero TrigGenTime register (PTP TAI Registers 4.8D00 and 4.8D01) after TrigGenReq, below, is set to a one. This leading edge control occurs as long as the TrigGenTime register is non-zero. If it is zero the leading edge will occur when the TrigGenReq bit below is set to a one without regard to the PTP Global Time. The phase of the leading edge is controlled by the TrigPhase bit above. When this bit is set to a one, Pulse mode is enabled. This mode matches the PTP Global Timer (TAI Registers 4.8C1E and 4.8C0F) and the TrigGenAmt register (TAI Registers 4.8C02 and 4.8C03) to generate a pulse at that time on the PTP_TRIG signal. The width of the pulse is specified by PulseWidth and PulseWitdhRange (TAI Register 4.8C05). **NOTE:** The minimum pulse width that can be generated is one TSClkPer amount (TAI Register 4.8C01) and the maximum pulse width is more than 30 million times the TSClkPer. The phase of the pulse is controlled by TrigPhase bit above.
0	TrigGen Req	RWR or SC	Trigger Generation Request/Enable. When this bit is set to a one, it enables a one-shot pulse or the 50% duty cycle clock generation on PTP_TRIG as previously configured by the TrigGenAmt, TrigMode, TrigClkComp (ps and Sub ps), PulseWidth, and TrigGenTime fields. If TrigMode (above) is set to a one (pulse mode) this bit will self clear after the pulse occurs (that is, the trailing edge of the pulse as defined by the Pulse Width and Pulse Width Range registers (TAI Register 4.8C05). If TrigMode is cleared to a zero the 50% duty cycle clock will continue running as long as this bit is set to a one.

Table 287: TAI Global Config Register Register 4.8C01 – TAI

Bits	Field	Type	Description
15:0	TSClkPer	RWS 0x1F40	Time Stamping Clock Period in picoseconds. This field specifies the clock period for the time stamping clock supplied to the PTP hardware. When this device is using the 125 MHz internally generated clock for the PTP hardware, the value of this register must be 0x1F40, or 8000 decimal which indicates a clock period of 8000 ps or 8 ns (or 125 MHz).

Table 288: TAI Global Config Register Register 4.8C02 – TAI

Bits	Field	Type	Description
15:0	TrigGen Amt [15:0]	RWR	Trigger Generation Amount bits [15:0] of a 32-bit register. This field specifies the PTP Time Application Interface trigger generation time amount. When TrigMode is set to one, the value specified in this field is compared with the PTP Global Timer (TAI Registers 4.8C1E and 4.8C0F) and when it matches the first time, a pulse is generated on PTP_TRIG whose width is controlled by PulseWidth (TAI Register 4.8C05). In this mode there is an internal delay of three TSClkPer before the leading edge of the pulse will be seen on the PTP_TRIG output pin. When TrigMode is cleared to zero, the value in this field is used as a clock period in TSClkPer increments (TAI Register 4.8C01) to generate an output clock on the PTP_TRIG signal (see TrigPhase in TAI Register 4.8C00). In this mode the TrigClkComp amount (TAI Register 4.8C04) and TrigClkCompSubPs (TAI Register 4.8C05) gets accumulated once per TrigGenAmt cycle and when this accumulated value exceeds the value specified in TSClkPer, one TSClkPer amount gets added to or subtracted from the next trailing edge of PTP_TRIG clock output. **NOTE:** In 50% duty cycle clock mode the contents of this register can be presented to the hardware at the same time all the other 50% duty cycle registers are. See BlockUpdate in TAI Register 4.8C00. The upper 16 bits of this register are contained in the register below.

Table 289: TAI Global Config Register Register 4.8C03 – TAI

Bits	Field	Type	Description
15:0	TrigGen Amt [31:16]	RWR	Trigger Generation Amount bits [31:16] of a 32-bit register. This field specifies the PTP Time Application Interface trigger generation time amount. See the description above. The lower 16 bits of this register are contained in the register above.

Table 290: TAI Global Config Register
Register 4.8C04 – TAI

Bits	Field	Type	Description
15	TrigComp Dir	RWR	Trig Clock Compensation Direction. When the accumulated TrigClkComp amount (below) exceeds the value in TSClkPer (TAI Register 4.8C01), one TSClkPer amount gets added to or subtracted from the next PTP_TRIG clock output. This bit determines which as follows: 0 = Add one TSClkPer to the next PTP_TRIG cycle 1 = Subtract one TSClkPer from the next PTP_TRIG cycle
14:0	TrigClk Comp	RWR	Trigger mode Clock Compensation Amount. This value is in picoseconds as an unsigned number. This field is used in 50% duty cycle clock mode only (when TrigMode is cleared to zero and TrigGenReq is set to one). This field specifies the remainder amount in ps for the clock that is being generated with a period specified by the TrigGenAmt (TAI Registers 4.8C02 and 4.8C03). This field must be set as an absolute error number in ps (in other words it is a magnitude difference) regardless if the local clock is too fast or too slow compared to the reference clock. The direction of the clock compensation is configured in the CompDir bit above. In the 50% duty cycle clock mode this register gets accumulated once per TrigGenAmt cycle and when this accumulated value exceeds the value specified in TSClkPer (TAI Register 4.8C01), one TSClkPer amount gets added to or subtracted from the next PTP_TRIG clock output. This requires that the absolute value of TrigClkComp must not exceed the size of the TSClkPer. If it does, the TSClkPer needs to be adjusted in size (either up or down) until the remainder that remains is less that the TSClkPer and that value gets put into this register. **NOTE:** In 50% duty cycle clock mode the contents of this register can be presented to the hardware at the same time all the other 50% duty cycle registers are. See BlockUpdate in TAI Register 4.8C00.

Table 291: TAI Global Config Register (Sheet 1 of 2)
Register 4.8C05 – TAI

Bits	Field	Type	Description
15:12	Pulse Width	RWS 0xF	Pulse width for PTP_TRIG. This pulse width is in units of TSClkPer (TAI Register 4.8C01). This specifies the width of the pulse that gets generated on PTP_TRIG (see TrigPhase in TAI Register 4.8C00) when the one shot pulse mode is selected (TrigMode is set to one and TrigGenReq is set to one). The default TSClkPer, or Pulse Width unit is 8 ns (assuming the Pulse Width Range, below, is 0x0). **NOTE:** Setting this register to 0x0 will cause unpredictable results.
11	Reserved	RES	

Table 291: TAI Global Config Register (Sheet 2 of 2)
Register 4.8C05 – TAI

Bits	Field	Type	Description
10:8	Pulse Width Range	RWR	Pulse Width Range for the PTP_TRIG signal. This register selects the units of time used to define the Pulse Width (above) as follows (each higher numbered selection generates units that are 8x larger than the previous lower numbered selection): 0x0 = 8 ns units for a 125 MHz PTP clock or 1 x TSClkPer 0x1 = 64 ns units for a 125 MHz PTP clock or 8 x TSClkPer 0x2 = 512 ns units for a 125 MHz PTP clock or 64 x TSClkPer 0x3 = 4,096 ns units for a 125 MHz PTP clock or 512 x TSClkPer 0x4 = 32.768 µs units for a 125 MHz PTP clock or 4,096 x TSClkPer 0x5 = 262.144 µs units for a 125 MHz PTP clock or 32,768 x TSClkPer 0x6 = 2.097 ms units for a 125 MHz PTP clock or 262,144 x TSClkPer 0x7 = 16.777 ms units for a 125 MHz PTP clock or 2,097,152 x TSClkPer The narrowest width is 8 ns (assuming a 125 MHz PTP clock) or one TSClkPer (by setting this register to 0x0 and the Pulse Width register, above, to 0x1). The widest width is 251 ms (assuming a 125 MHz PTP clock) or just a bit over ¼ second (by setting this register to 0x7 and the Pulse Width register to 0xF). The maximum number is 31,457,280 TSClkPer.
7:0	TrigClk Comp SubPs	RWR	Trigger mode Clock Compensation Amount. This value is in sub-picoseconds as an unsigned number. This field is used in 50% duty cycle clock mode only (when TrigMode is cleared to zero and TrigGenReq is set to one). This field specifies the remainder amount in sub ps increments for the clock that is being generated with a period specified by the TrigGenAmt (TAI Registers 4.8C02 and 4.8C03). This field must be set as an absolute error number in Sub ps (in other words it is a magnitude difference) regardless if the local clock is too fast or too slow compared to the reference clock. The direction of the clock compensation is configured in the CompDir bit above. Each unit in this register is 1/256th of a ps or approximately 4 femtoseconds (actual number is 3.90625 femtoseconds per unit). In the 50% duty cycle clock mode this register gets accumulated once per TrigGenAmt cycle and when this accumulated value exceeds on ps, one ps gets added to the accumulated Trig Clock Compensation (TAI Register 4.8C04). **NOTE:** In 50% duty cycle clock mode the contents of this register can be presented to the hardware at the same time all the other 50% duty cycle registers are. The writing to this register is used to transfer this data as a block. See BlockUpdate in TAI Register 4.8C00.

Table 292: TAI Global Status Register (Sheet 1 of 2)
Register 4.8D00 – TAI

Bits	Field	Type	Description
15	Reserved	RES	

Table 292: TAI Global Status Register (Sheet 2 of 2)
Register 4.8D00 – TAI

Bits	Field	Type	Description
14	Capture Trig	RWR	Capture Trig. 0 = Capture PTP_EVREQ pin events 1 = Capture PTP_TRIG internal events When this bit is cleared to a zero the Event Capture register looks at events on the PTP_EVREQ pin. When this bit is set to a one the Event Capture register looks at events from the waveform generated by PTP_TRIG. This allows observing the rising or falling edge of the PTP_TRIG (the EventPhase register is still active, PTP TAI Register 4.8C00) without the need of using pins. This is used to ensure the edges have not drifted over time so they can be re-aligned if needed.
13:10	Reserved	RES	
9	EventCap Err	RWR	Event Capture Error. This bit gets set by the hardware logic when an EventReq has occurred (see EventPhase in TAI Register 4.8C00) where the EventCapValid bit, below, is already set to a one and the EventCapOv bit (TAI Register 4.8C00) is cleared to a zero. This condition could happen if the EventReqs are occurring faster than the local CPU can process them (and clear the EventCapValid bit before the next EventReq). Some number of missed EventReq can be seen in the EventCapCtr, below, if its enabled.
8	EventCap Valid	RWR	Event Capture Valid. This bit is set to a one whenever the EventCap (Event Capture – TAI Registers 4.8D01 and 4.8D02) register contains the time of a captured event. Software needs to clear this bit to a zero to enable the EventCap Register to be able to acquire a subsequent event if the EventCapOv (Event Capture Override – TAI Register 4.8C00) is not enabled. Clearing this bit to a zero also clears the EventInt (Event Capture Interrupt – PTP Global Register 4.8E08).
7:0	EventCap Ctr	RWR	Event Capture Counter. This field is incremented once by each EventReq (see EventPhase in PTP TAI Register 4.8C00) as long as EventCtrStart (PTP TAI Register 4.8C00) is set to one. This counter wraps around and can be cleared by writing zeros to it.

Table 293: TAI Global Status Register
Register 4.8D01 – TAI

Bits	Field	Type	Description
15:0	EventCap Register [15:0]	RWR	Event Capture Register bits [15:0] of a 32-bit register. This register captures the value of the PTP Global Timer (TAI Registers 4.8C1E and 4.8C0F) when an EventReq (see EventPhase in TAI Register 4.8C00) has occurred. If the EventCapOv (TAI Register 4.8C00) is set to a one, then this register indicates the time captured for the last event. When EventCapErr is set to a one, the contents in this register no longer represent the time of the first event. **NOTE:** The maximum jitter for the EventCapRegister time amount with respect to the EventReq on the LED/GPIO pin is one TSClkPer amount. **NOTE:** The minimum EventReq input signal high or low width must be equal to or greater than 1.5 times the TSClkPer amount. **NOTE:** For the hardware to capture the EventReq on the LED/GPIO input signal, the minimum gap between two consecutive events must be 150 plus 5 times the TSClkPer amount. The upper 16 bits of this register are contained in the register below.

Table 294: TAI Global Status Register
Register 4.8D02 – TAI

Bits	Field	Type	Description
15:0	EventCap Register [31:16]	RWR	Event Capture Register bits [31:16] of a 32-bit register. This register captures the value of the PTP Global Timer (TAI Registers 4.8C1Eand 4.8C0F) when an EventReq (see EventPhase in TAI Register 4.8C00) has occurred. See the description above. The lower 16 bits of this register are contained in the register above.

Table 295: TAI Global Status Register
Register 4.8C1E – TAI

Bits	Field	Type	Description
15:0	PTPGlobalTime [15:0]	RO	PTP Global Timer bits [15:0] of a 32-bit register. This indicates the global timer value that is running off of the free running switch core clock. This counter wraps around in hardware. To support synchronization of PTP Global Time between multiple devices in a system, this register gets updated with the value specified in TrigGenAmt when MultiPTPSync is set to a one (TAI Register 4.8C00) and an EventReq occurs (see EventPhase in TAI Register 4.8C00). The upper 16 bits of this register are contained in the register below.

Table 296: TAI Global Status Register
Register 4.8C0F – TAI

Bits	Field	Type	Description
15:0	PTPGlobalTime [31:16]	RO	PTP Global Timer bits [31:16] of a 32-bit register. This indicates the global timer value that is running off of the free running switch core clock. This counter wraps around in hardware. See the description above. The lower 16 bits of this register are contained in the register above.

Table 297: TAI Global Config Register
Register 4.8C09 – TAI

Bits	Field	Type	Description
15:0	TrigGen Time [15:0]	RWR	Trigger Generation Time bits [15:0] of a 32-bit register. This field specifies the PTP Global Time (TAI Registers 4.8C1E and 4.8C0F) where the 1st leading edge of PTP_TRIG will occur (with a three TSClkPer latency) when PTP Trig is in the continuous square wave mode (i.e, when TrigMode is 0x0, offset 0x00 above) as long as this register's value is non-zero. If its value is zero, the 1st leading edge of PTP_TRIG will occur when TrigGenReg is set to a one (TAI Register 4.8C00). This register is also used to for re-locking the leading edge of the square wave (see TrigLock in TAI Register 4.8C00). The upper 16 bits of this register are contained in the register below.

Table 298: TAI Global Config Register
Register 4.8C0A – TAI

Bits	Field	Type	Description
15:0	TrigGen Time [31:16]	RWR	Trigger Generation Time bits [31:16] of a 32-bit register. See the description above. The lower 16 bits of this register are contained in the register above.

Table 299: TAI Global Config Register (Sheet 1 of 2)
Register 4.8C0B – TAI

Bits	Field	Type	Description
15:5	Reserved	RES	
4	LockCorr Valid	RO	Trig Lock Correction Valid. 0 = Trig Lock Correction is not valid or did not occur 1 = Trig Lock Correction is valid and did occur When a Trigger Lock is enabled (TAI Register 4.8C00) this bit is cleared to zero. When the Trigger Lock completes this bit will be set to a one if and only if a Trigger Lock occurred for PTP_TRIG. In this case the Lock Correction value below will show the amount of adjustment that was made (if any).

Table 299: TAI Global Config Register (Sheet 2 of 2)
Register 4.8C0B – TAI

Bits	Field	Type	Description
3:0	Lock Correction	RO	Trig Lock Correction amount. When the TrigLock bit is set to a one (TAI Register 4.8C00) enabling a potential clock adjustment, these bits are cleared to zero. When the TrigLock bit is cleared to zero (indicating that the requested clock adjustment is now past in time) these bits will reflect the magnitude and direction that was applied to the PTP_TRIG leading edge of the generated clock. A value of zero means no adjustment was necessary. If bit 3 is a one then the leading edge of the clock was moved n number of clocks earlier in time where n is shown in bits [2:0]. If bit 3 is a zero then the leading edge of the clock was moved n number of clocks later in time where n is shown in bits [2:0].

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Table 300: Absolute Maximum Ratings

Stresses above values listed in Table 300 and Max T_J listed in Table 301 may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to these limits for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDA}	Power Supply Voltage on AVDD15 with respect to VSS	–	–	1.65	V
V_{DDAR}	Power Supply Voltage on AVDD33 with respect to VSS	–	–	3.63	V
V_{REG_IN}	Power Supply Voltage on REG_IN (VDD33) with respect to VSS	–	–	3.63	V
V_{DD}	Power Supply Voltage on DVDD with respect to VSS	–	–	1.16	V
V_{DDO}	Power Supply Voltage on VDDO with respect to VSS	–	–	3.63	V
V_{PIN}	Voltage applied to any digital input pin	–	–	3.63 or VDDO + 0.4 whichever is less	V

5.2 Recommended Operating Conditions

Table 301: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}[1]	AVDD15 Supply	For AVDD15	1.39	1.5	1.61	V
V_{DDAR}[1]	AVDD33 Supply	For AVDD33	3.07	3.3	3.53	V
V_{DD}[1]	DVDD Supply	For DVDD	0.98	1.05	1.12	V
V_{DDO}[1]	VDDO Supply	For VDDO at 1.8V	1.67	1.8	1.93	V
		For VDDO at 2.5V	2.33	2.5	2.68	V
		For VDDO at 3.3V	3.07	3.3	3.53	V
RSET	Internal bias reference	Resistor connected to V_{SS}	–	4990 ± 1% Tolerance	–	
T_A	Ambient operating temperature	Automotive Grade 1	-40	–	+125	°C
T_J	Maximum junction temperature	–	–	–	135	°C

1. Maximum noise allowed on supplies is 50 mV peak-peak.

5.3 Package Thermal Information

Table 302: Thermal Conditions for 88Q1110/88Q1111 40-Pin QFN Package

Symbol	Parameter[1]	Condition	Min	Typ	Max	Unit
θ_{JA}	Junction-to-ambient thermal resistance $\theta_{JA} = (T_J - T_A) / P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	47.98	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	43.60	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	42.71	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	42.08	–	°C/W
θ_{JB}	Junction-to-board thermal resistance $\theta_{JB} = (T_J - T_B) / P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface	JEDEC with no air flow	–	31.44	–	°C/W
θ_{JC}	Junction-to-case thermal resistance $\theta_{JC} = (T_J - T_C) / P_{top}$ P_{top} = Power dissipation from the top of the package	JEDEC with no air flow	–	23.15	–	°C/W
ψ_{JT}	Junction-to-top-center thermal characterization parameter $\psi_{JT} = (T_J - T_{top}) / P$ P = Total power dissipation T_{top} = Temperature on the top center of the package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	2.21	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	2.50	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	2.72	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	2.90	–	°C/W

1. For more information, see θJC, θJA & Temperature Calculations, MV-S700019-00.

5.4 Current Consumption

5.4.1 Current Consumption when Using External Regulators

5.4.1.1 Current Consumption AVDD15

Table 303: Current Consumption AVDD15
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Unit
I_{AVDD}	1.5V Power to analog core	AVDD15	RGMII over 100BASE-T1 with traffic	–	13	15	mA
			IEEE Power Down (88Q1110)	–	9	11	mA
			IEEE Power Down (88Q1111)	–	30	32	mA
			MII over 100BASE-T1 with traffic	–	13	15	mA
			RMII over 100BASE-T1 with traffic	–	13	15	mA
			SGMII over 100BASE-T1 with traffic	–	33	36	mA

5.4.1.2 Current Consumption AVDD33

Table 304: Current Consumption AVDD33
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Unit
I_{AVDDR}	Analog 3.3V supply	AVDD33	RGMII over 100BASE-T1 with traffic	–	11	11	mA
			IEEE Power Down (88Q1110, 88Q1111)	–	0	2	mA
			MII over 100BASE-T1 with traffic	–	11	11	mA
			RMII over 100BASE-T1 with traffic	–	11	11	mA
			SGMII over 100BASE-T1 with traffic	–	11	12	mA

5.4.1.3 Current Consumption DVDD

Table 305: Current Consumption DVDD
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Unit
I_{VDD}	1.05V Power to digital core	DVDD	RGMII over 100BASE-T1 with traffic	–	9	22	mA
			IEEE Power Down (88Q1110)	–	2	14	mA
			IEEE Power Down (88Q1111)	–	4	16	mA
			MII over 100BASE-T1 with traffic	–	9	22	mA
			RMII over 100BASE-T1 with traffic	–	9	22	mA
			SGMII over 100BASE-T1 with traffic	–	11	24	mA

5.4.1.4 Current Consumption VDDO

Table 306: Current Consumption VDDO
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Min	Typ	Max	Unit
I_{VDDO}	Power to the digital I/Os	VDDO	RGMII over 100BASE-T1 with traffic	VDDO = 3.3V	–	7	9	mA
				VDDO = 2.5V	–	6	8	mA
				VDDO = 1.8V	–	2	6	mA
			SGMII over 100BASE-T1 with traffic	VDDO = 3.3V	–	2	2	mA
				VDDO = 2.5V	–	2	2	mA
				VDDO = 1.8V	–	1	2	mA
			IEEE Power Down (88Q1110)	VDDO = 3.3V	–	2	9	mA
				VDDO = 2.5V	–	2	8	mA
				VDDO = 1.8V	–	1	6	mA
			IEEE Power Down (88Q1111)	VDDO = 3.3V	–	2	2	mA
				VDDO = 2.5V	–	2	2	mA
				VDDO = 1.8V	–	1	2	mA
			MII over 100BASE-T1 with traffic	VDDO = 3.3V	–	9	11	mA
				VDDO = 2.5V	–	7	9	mA
				VDDO = 1.8V	–	4	6	mA
			RMII over 100BASE-T1 with traffic	VDDO = 3.3V	–	10	12	mA
				VDDO = 2.5V	–	8	10	mA
				VDDO = 1.8V	–	5	7	mA

5.4.2 Current Consumption when Using Internal Regulators

5.4.2.1 Current Consumption REG_IN

Table 307: Current Consumption REG_IN
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Unit
I_{REG_IN}	3.3V Internal Regulator Supply	REG_IN	RGMII over 100BASE-T1 with traffic	–	27	36	mA
			IEEE Power Down (88Q1110)	–	15	23	mA
			IEEE Power Down (88Q1111)	–	36	44	mA
			MII over 100BASE-T1 with traffic	–	27	35	mA
			RMII over 100BASE-T1 with traffic	–	27	36	mA
			SGMII over 100BASE-T1 with traffic	–	45	58	mA

Note When using internal regulators, AVDD15 and DVDD are supplied internally using the 3.3V VDD33(REG_IN) regulator supply. VDDO and AVDD33 still need to be supplied externally.

5.4.3 Current Consumption at Reset

Table 308: Current Consumption at Reset - FF, 104°TJ, +5% V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	AVDD15 Supply	AVDD15 at 1.5735V	--	4.4	--	mA
V_{DDAR}[1]	AVDD33 Supply	AVDD33 at 3.4665V	--	0.5	--	mA
V_{DD}	DVDD Supply	DVDD at 1.1002V	--	15.5	--	mA
V_{DDO}	VDDO Supply	VDDO at 3.467V	--	2.3	--	mA

Table 309: Current Consumption at Reset - TT, NVNT

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	AVDD15 Supply	AVDD15 at 1.4985V	--	3.6	--	mA
V_{DDAR}[1]	AVDD33 Supply	AVDD33 at 3.3006V	--	0.2	--	mA
V_{DD}	DVDD Supply	DVDD at 1.10477V	--	5.5	--	mA
V_{DDO}	VDDO Supply	VDDO at 3.302V	--	2.3	--	mA

5.5 DC Operating Conditions

5.5.1 Digital Pins

Table 310: Digital Pins
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Unit
VIH	Input high voltage	All digital inputs	VDDO = 3.3V	VDDO*0.7	–	VDDO + 0.4V	V
			VDDO = 2.5V	VDDO*0.7	–	VDDO + 0.4V	V
			VDDO = 1.8V	VDDO*0.7	–	VDDO + 0.4V	V
VIL	Input low voltage	All digital inputs	VDDO = 3.3V	-0.4	–	VDDO*0.3	V
			VDDO = 2.5V	-0.4	–	VDDO*0.3	V
			VDDO = 1.8V	-0.4	–	VDDO*0.3	V
VOH	High level output voltage	All digital outputs	–	VDDO - 0.4V	–	–	V
VOL	Low level output voltage	All digital outputs	–	–	–	0.4	V
I_{ILK}	Input leakage current	–	–	–	–	10	µA
C_{IN}	Input capacitance	All pins	–	–	–	5	pF

5.5.2 TX_ENABLE, GPIO, RX, INTn, and MDIO Pins

Table 311: TX_ENABLE and GPIO Output Pins - VDDO = 3.3V/2.5V
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins		Condition	Host Mode	Register Settings	Min	Typ	Max	Unit
VOH	High level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 3.3V/2.5V	LEDB = 1	IOH = 2.2 mA	MII/RMII	4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001	VDDO - 0.4	–	–	V
			LEDB = 0	IOH = 2.2 mA		4.8001.11:8 =4'b0001 4.8001.7:4 = 4'b0001				
VOL	Low level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 3.3V/2.5V	LEDB = 1	IOL = 2.2 mA	MII/RMII	4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001	–	–	0.4	V
			LEDB = 0	IOL = 20 mA		4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001				
VOH	High level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 3.3V/2.5V	LEDB = 1	IOH = 2.6 mA	RGMII	4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010	VDDO - 0.4	–	–	V
			LEDB = 0	IOH = 2.6 mA		4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010				
VOL	Low level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 3.3V/2.5V	LEDB = 1	IOL = 2.6 mA	RGMII	4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010	–	–	0.4	V
			LEDB = 0	IOL = 20 mA		4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010				
VOH	High level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 3.3V/2.5V	LEDB = 1	IOH = 8 mA	RGMII/ MII/RMII	4.8001.11:8 = 4'b1111 4.8001.7:4 = 4'b1111	VDDO - 0.4	–	–	V
			LEDB = 0	IOH = 8 mA		4.8001.11:8 = 4'b1111 4.8001.7:4 = 4'b1111				
VOL	Low level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 3.3V/2.5V	LEDB = 1	IOL = 8 mA	RGMII/ MII/RMII	4.8001.11:8 = 4'b1111 4.8001.7:4 = 4'b1111	–	–	0.4	V
			LEDB = 0	IOL = 20 mA		4.8001.11:8 = 4'b1111 4.8001.7:4 = 4'b1111				

Table 312: TX_ENABLE and GPIO Output Pins - VDDO = 1.8V
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins		Condition	Host Mode	Register Settings	Min	Typ	Max	Unit
VOH	High level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 1.8V	LEDB = 1	IOH = 2 mA	MII/RMII	4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001	VDDO - 0.4	–	–	V
			LEDB = 0	N/A		4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001				
VOL	Low level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 1.8V	LEDB = 1	IOL = 2 mA	MII/RMII	4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001	–	–	0.4	V
			LEDB = 0	N/A		4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001				
VOH	High level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 1.8V	LEDB = 1	IOH = 2.4 mA	RGMII	4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010	VDDO - 0.4	–	–	V
			LEDB = 0	N/A		4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010				
VOL	Low level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 1.8V	LEDB = 1	IOL = 2.4 mA	RGMII	4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010	–	–	0.4	V
			LEDB = 0	N/A		4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010				
VOH	High level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 1.8V	LEDB = 1	IOH = 7.6 mA	RGMII/ MII/RMII	4.8001.11:8 = 4'b1111 4.8001.7:4 = 4'b1111	VDDO - 0.4	–	–	V
			LEDB = 0	N/A		4.8001.11:8 = 4'b1111 4.8001.7:4 = 4'b1111				
VOL	Low level output voltage	TX_ENABLE/ GPIO outputs at VDDO = 1.8V	LEDB = 1	IOL = 7.6 mA	RGMII/ MII/RMII	4.8001.11:8 = 4'b1111 4.8001.7:4 = 4'b1111	–	–	0.4	V
			LEDB = 0	N/A		4.8001.11:8 = 4'b1111 4.8001.7:4 = 4'b1111				

Table 313: RX[1] Output Pins - VDDO = 3.3V/2.5V

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Host Mode	Register Settings	Min	Typ	Max	Unit
VOH	High level output voltage	RX[1] outputs at VDDO = 3.3V/2.5V	IOH = 5 mA	MII/RMII	4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001	VDDO - 0.4	–	–	V
VOL	Low level output voltage	RX[1] outputs at VDDO = 3.3V/2.5V	IOL = 5 mA	MII/RMII	4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001	–	–	0.4	V
VOH	High level output voltage	RX[1] outputs at VDDO = 3.3V/2.5V	IOH = 5 mA	RGMII	4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010	VDDO - 0.4	–	–	V
VOL	Low level output voltage	RX[1] outputs at VDDO = 3.3V/2.5V	IOL = 5 mA	RGMII	4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010	–	–	0.4	V

1. TCLK for MII also has these parameters associated with it.

Table 314: RX[1] Output Pins - VDDO = 1.8V

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Host Mode	Register Settings	Min	Typ	Max	Unit
VOH	High level output voltage	RX[1] outputs at VDDO = 1.8V	IOH = 4.7 mA	MII/RMII	4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001	VDDO - 0.4	–	–	V
VOL	Low level output voltage	RX[1] outputs at VDDO = 1.8V	IOL = 4.7 mA	MII/RMII	4.8001.11:8 = 4'b0001 4.8001.7:4 = 4'b0001	–	–	0.4	V
VOH	High level output voltage	RX[1] outputs at VDDO = 1.8V	IOH = 4.7 mA	RGMII	4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010	VDDO - 0.4	–	–	V
VOL	Low level output voltage	RX[1] outputs at VDDO = 1.8V	IOL = 4.7 mA	RGMII	4.8001.11:8 = 4'b0010 4.8001.7:4 = 4'b0010	–	–	0.4	V

1. TCLK for MII also has these parameters associated with it.

Table 315: INTn and MDIO Output Pins - VDDO = 3.3V/2.5V

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Host Mode	Register Settings	Min	Typ	Max	Unit
VOH	High level output voltage	INTn output at VDDO = 3.3V/2.5V	IOH = 2 mA	RGMII/ MII/RMII	4.821A.13:12 = 2'b00	VDDO - 0.4	–	–	V
			IOH = 4 mA		4.821A.13:12 = 2'b01				
			IOH = 6 mA		4.821A.13:12 = 2'b10	–	–	0.4	
			IOH = 8 mA		4.821A.13:12 = 2'b11				
VOL	Low level output voltage	INTn output at VDDO = 3.3V/2.5V	IOL = 2 mA	RGMII/ MII/RMII	4.821A.13:12 = 2'b00	VDDO - 0.4	–	–	V
			IOL = 4 mA		4.821A.13:12 = 2'b01				
			IOL = 6 mA		4.821A.13:12 = 2'b10	–	–	0.4	
			IOL = 8 mA		4.821A.13:12 = 2'b11				
VOH	High level output voltage	MDIO output at VDDO = 3.3V/2.5V	IOH = 2 mA	RGMII/ MII/RMII	4.821A.15:14 = 2'b00	VDDO - 0.4	–	–	V
			IOH = 4 mA		4.821A.15:14 = 2'b01				
			IOH = 6 mA		4.821A.15:14 = 2'b10	–	–	0.4	
			IOH = 8 mA		4.821A.15:14 = 2'b11				
VOL	Low level output voltage	MDIO output at VDDO = 3.3V/2.5V	IOL = 2 mA	RGMII/ MII/RMII	4.821A.15:14 = 2'b00	VDDO - 0.4	–	–	V
			IOL = 4 mA		4.821A.15:14 = 2'b01				
			IOL = 6 mA		4.821A.15:14 = 2'b10	–	–	0.4	
			IOL = 8 mA		4.821A.15:14 = 2'b11				

Table 316: INTn and MDIO Output Pins - VDDO = 1.8V
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Host Mode	Register Settings	Min	Typ	Max	Unit
VOH	High level output voltage	INTn output at VDDO = 1.8V	IOH = 1.9 mA	RGMII/ MII/RMII	4.821A.13:12 = 2'b00	VDDO - 0.4	–	–	V
			IOH = 3.8 mA		4.821A.13:12 = 2'b01				
			IOH = 5.7 mA		4.821A.13:12 = 2'b10	–	–	0.4	
			IOH = 7.6 mA		4.821A.13:12 = 2'b11				
VOL	Low level output voltage	INTn output at VDDO = 1.8V	IOL = 1.9 mA	RGMII/ MII/RMII	4.821A.13:12 = 2'b00	VDDO - 0.4	–	–	V
			IOL = 3.8 mA		4.821A.13:12 = 2'b01				
			IOL = 5.7 mA		4.821A.13:12 = 2'b10	–	–	0.4	
			IOL = 7.6 mA		4.821A.13:12 = 2'b11				
VOH	High level output voltage	MDIO output at VDDO = 1.8V	IOH = 1.9 mA	RGMII/ MII/RMII	4.821A.15:14 = 2'b00	VDDO - 0.4	–	–	V
			IOH = 3.8 mA		4.821A.15:14 = 2'b01				
			IOH = 5.7 mA		4.821A.15:14 = 2'b10	–	–	0.4	
			IOH = 7.6 mA		4.821A.15:14 = 2'b11				
VOL	Low level output voltage	MDIO output at VDDO = 1.8V	IOL = 1.9 mA	RGMII/ MII/RMII	4.821A.15:14 = 2'b00	VDDO - 0.4	–	–	V
			IOL = 3.8 mA		4.821A.15:14 = 2'b01				
			IOL = 5.7 mA		4.821A.15:14 = 2'b10	–	–	0.4	
			IOL = 7.6 mA		4.821A.15:14 = 2'b11				

5.5.2.1 Internal Resistors

These values are based on pad specifications.

Table 317: Internal Resistors

Symbol	Parameter	Min	Typ	Max	Units
$R_{Pull-Up}$	Pull-Up Resistance	30	–	150	k
$R_{Pull-Down}$	Pull-Down Resistance	30	–	150	k

5.5.3 IEEE Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications:

- IEEE 802.3bw 100BASE-T1

Table 318: IEEE Transceiver Parameters

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Unit
V_{ODIFF}	Absolute Peak Differential Output Voltage[1]	MDIP/N	100BASE-T1 mode	–	–	2.2	V
V_{DIST}	Peak Distortion[2]	MDIP/N	IEEE Test Mode 4	–	–	15	mV
J_{TXOUT}	Transmit Jitter rms	MDIP/N	IEEE Test Mode 2	–	–	50	ps

1. Transmit power conforms to IEEE 802.3bw Transmit PSD mask.
2. Measured with procedure outlined in IEEE 802.3bw transmitter electrical specifications.

5.5.4 SGMII Interface Transmitter DC Characteristics

Table 319: SGMII Interface Transmitter DC Characteristics

Symbol	Parameter[1]	Min	Typ	Max	Units
V_{OH}	Output Voltage High	–	945[2]	1050	mV
V_{OL}	Output Voltage Low	700	735[2]	–	mV
V_{RING}	Output Ringing	–	–	10	mV
$\|V_{OD}\|$[3]	Output Voltage Swing (differential, peak)	Programmable - see Table 237 for details.			mV peak
V_{OS}	Output Offset Voltage (also called Common mode voltage)	Variable - see 5.5.4.1 for details.			mV
R_O	Output Impedance (single-ended) (50 ohm termination)	40	–	60	ohms
Delta R_O	Mismatch in a pair	–	–	10	%
Delta V_{OD}	Change in V_{OD} between 0 and 1	–	–	25	mV
Delta V_{OS}	Change in V_{OS} between 0 and 1	–	–	25	mV
I_{S+}, I_{S-}	Output current on short to VSS	–	–	40	mA
I_{S+-}	Output current when txp and txn are shorted	–	–	12	mA
I_{X+}, I_{X-}	Power off leakage current			10	mA

1. Parameters are measured with outputs AC connected with 100 ohm differential load.
2. Register 31.801A.2:0 = 3'b010
3. Output amplitude is programmable by writing to Register 31.801A.2:0.

Table 320: Programming Output Amplitude (Device 31, Register 0x801A)

Register Bits	Field	Description
2:0	SGMII Output Amplitude	Differential voltage peak measured. Note that V_{OL} must be greater than 700 mV. 000 = 14 mV 001 = 112 mV 010 = 210 mV 011 = 308 mV 100 = 406 mV 101 = 504 mV 110 = 602 mV 111 = 700 mV

5.5.4.1 Common Mode Voltage (Voffset) Calculations

There are four different main configurations for the SGMII interface connections. These are:

- DC connection to an LVDS receiver
- AC connection to an LVDS receiver
- DC connection to an CML receiver
- AC connection to an CML receiver

If AC coupling or DC coupling to an LVDS receiver is used, the DC output levels are determined by the following:

- Internal bias. See Figure 31 for details. (If AVDD15 is used to generate the internal bias, the internal bias value will typically be 1.5V.)
- The output voltage swing is programmed by Register 31.801A.2:0.

V_{offset}(i.e., common mode voltage) = (internal bias) - single-ended peak-peak voltage swing. See Figure 31 for details.

If DC coupling is used with a CML receiver, then the DC levels will be determined by a combination of the MACs output structure and the 88Q1110/88Q1111 input structure shown in the CML Inputs diagram in Figure 31. Assuming the same MAC CML voltage levels and structure, the common mode output levels will be determined by:

V_{offset} (i.e., common mode voltage) = (internal bias) - single-ended peak-peak voltage swing/2. See Figure 32 for details.

If DC coupling is used, the output voltage DC levels are determined by the AC coupling considerations above, plus the I/O buffer structure of the MAC.

Figure 31: AC connections (CML or LVDS receiver) or DC connection LVDS receiver

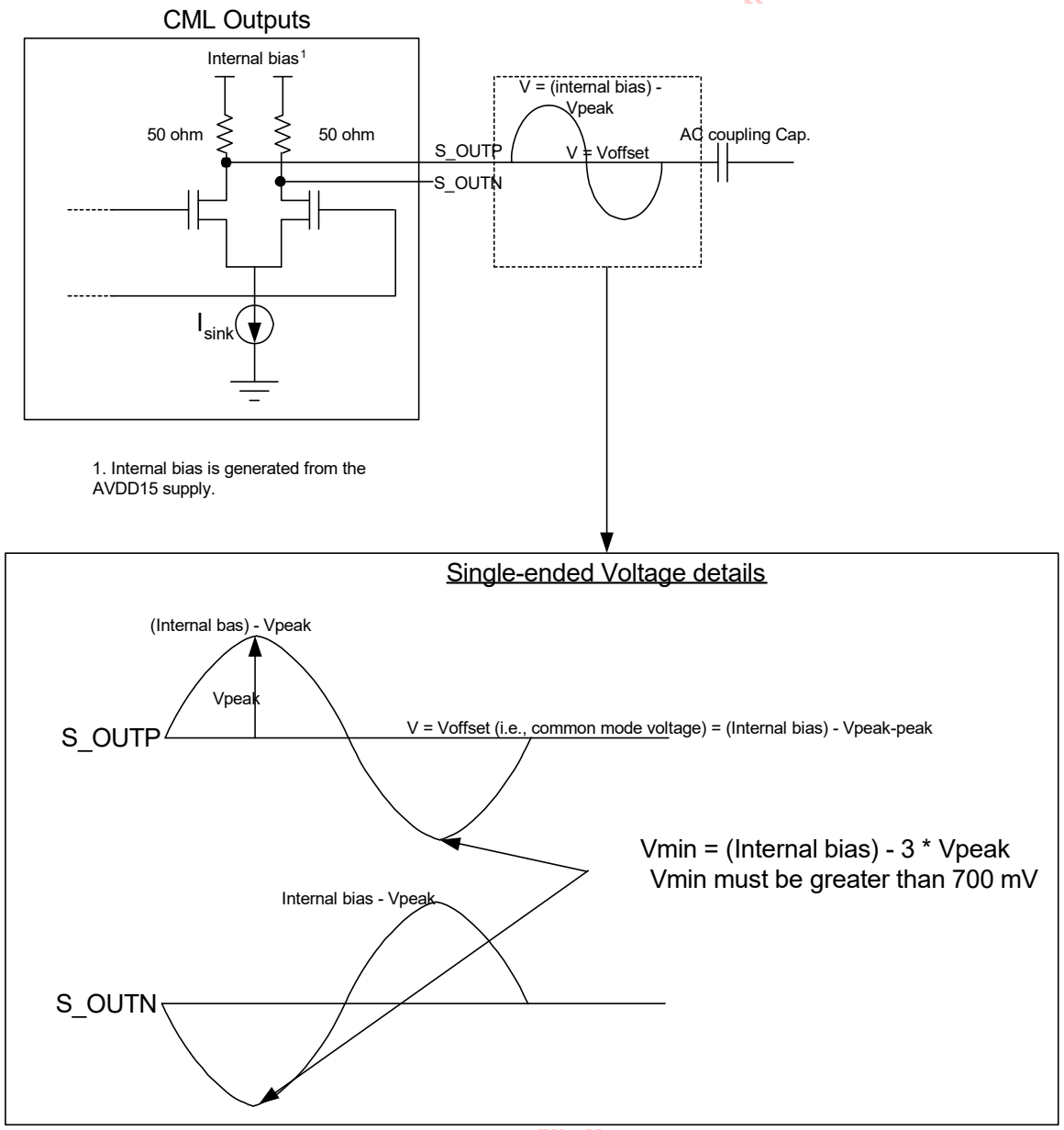
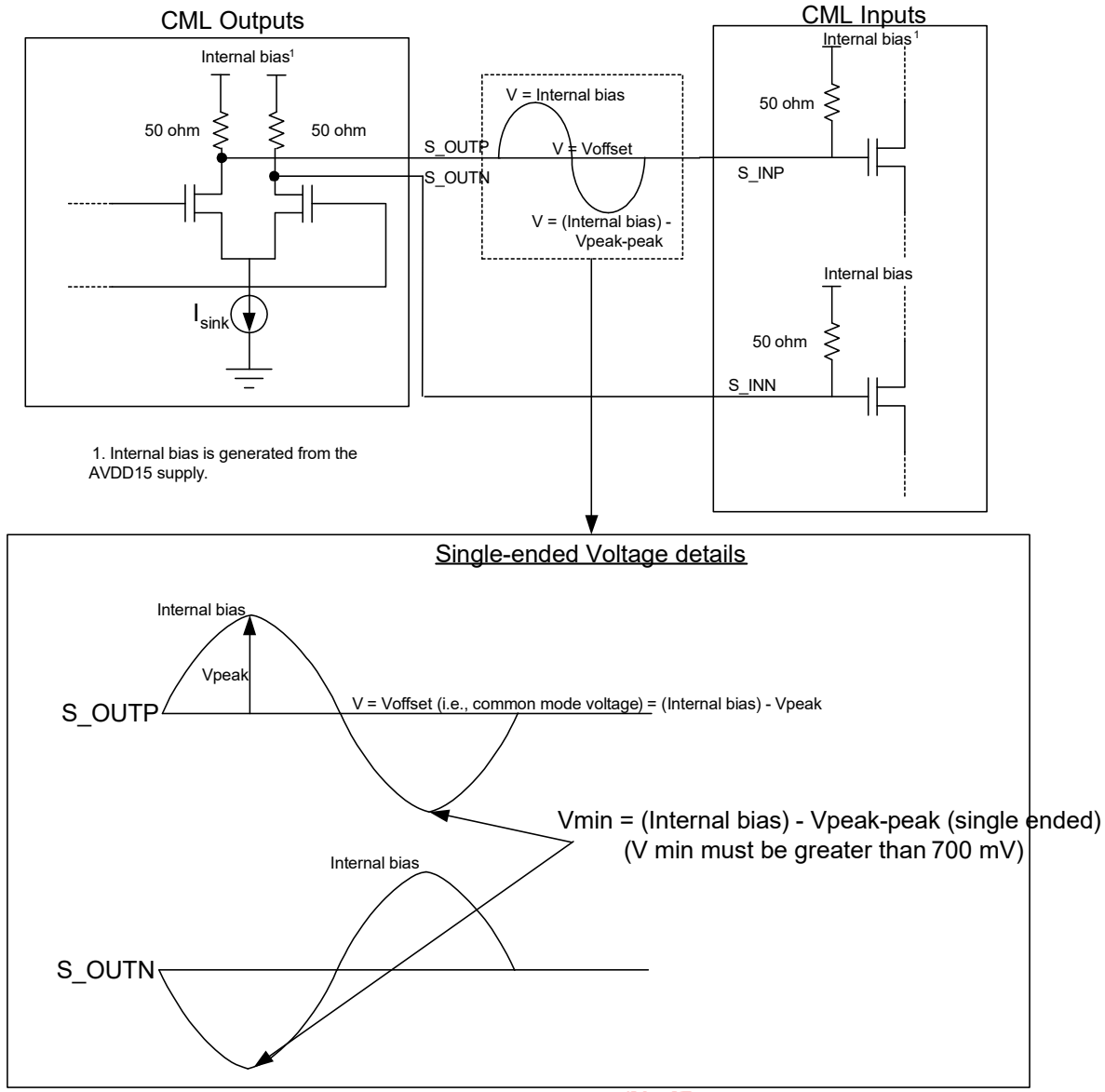


Figure 32: DC connection to a CML receiver



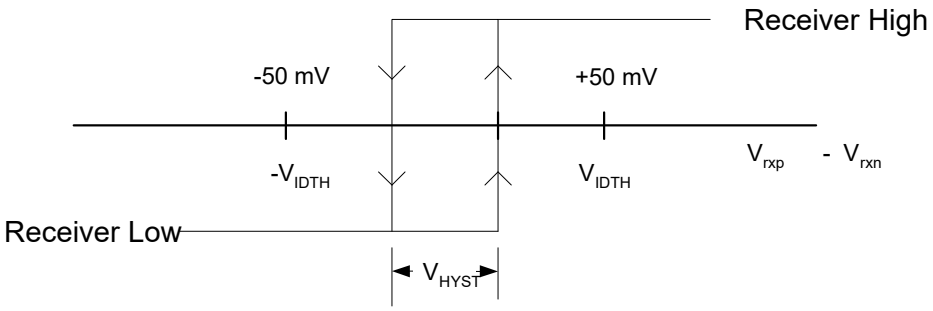
5.5.4.2 Receiver DC Characteristics

Table 321: Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_I	Input Voltage range a or b	675	–	1725	mV
V_{IDTH}[1]	Input Differential Threshold |S_INP - S_INN|	-50	–	+50	mV
V_{HYST}[1]	Input Differential Hysteresis	25	–	–	mV
R_{IN}	Receiver 100 ohm Differential Input Impedance	80	–	120	ohm

1. Receiver is at high level when Vrxp - Vrxn is greater than VIDTH(min) and is at low level when Vrxp - Vrxn is less than -VIDTH(min). A minimum hysterisis of VHYST is present between -VIDTH and +VIDTH as shown in the figure.

Figure 33: Input Differential Hysteresis



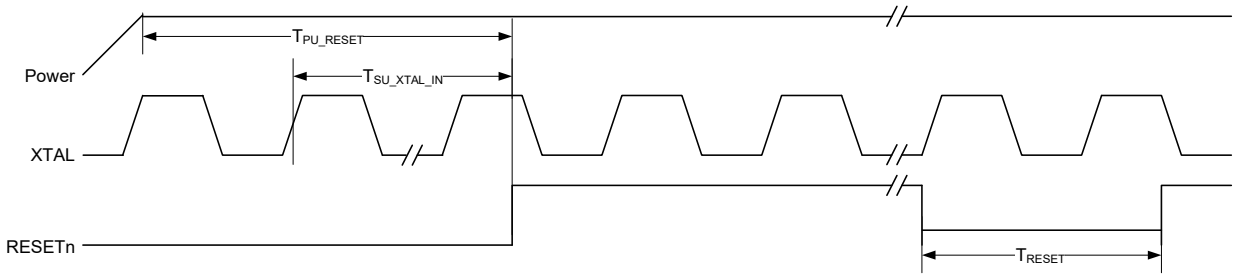
5.6 AC Electrical Specifications

5.6.1 Reset Timing

Table 322: Reset Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to RESETn de-asserted	1	–	–	ms
$T_{SU\_XTAL\_IN}$	Number of valid XTAL_IN cycles prior to RESETn de-asserted	10	–	–	clocks
T_{RESET}	Minimum reset pulse width during normal operation	1	–	–	ms
T_{RESET_MDIO}	Minimum wait time from RESET de-assertion to first MDIO access	1	–	–	ms

Figure 34: Reset Timing



5.6.2 XTAL_IN/XTAL_OUT Timing

Table 323: 25 MHz Crystal Requirements
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_T	Target Frequency	–	–	25.0	–	MHz
	Frequency Tolerance	–	-100	–	100	ppm
C_L	Load Capacitance	User Specified	–	6	12	pF
C_S	Shunt Capacitance	–	–	–	CL/6	pF
RL or ESR	Equivalent Series Resistance	–	–	100	150	ohms
D_L	Drive Level	–	100	–	–	µW

Figure 35: Crystal Reference Schematic

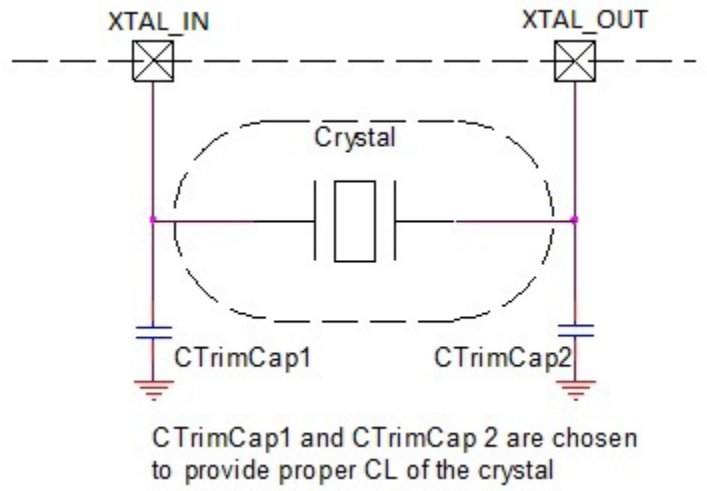
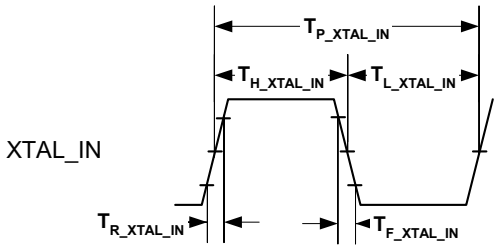


Table 324: 25 MHz Oscillator Requirements

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_T	Target Frequency	–	–	25.0	–	MHz
	Frequency Tolerance	–	-100		+100	ppm
$T_{P\_XTAL\_IN}$	XTAL_IN Period	–	–	40	–	ns
$V_{SWING\_XTAL\_IN}$	XTAL_IN Swing	See Application Note MV-S301630-00	0.8	–	1.5	Vpp
$T_{H\_XTAL\_IN}$	XTAL_IN High Time	–	13	20	27	ns
$T_{L\_XTAL\_IN}$	XTAL_IN Low Time	–	13	20	27	ns
$T_{R\_XTAL\_IN}$	XTAL_IN Rise Time	10 to 90%	–	3	–	ns
$T_{F\_XTAL\_IN}$	XTAL_IN Fall Time	10 to 90%	–	3	–	ns
$T_{J\_XTAL\_IN}$	XTAL_IN Total Jitter	12 KHz to 20 MHz	–	–	4.0	ps RMS
$C_{\_XTAL\_OUT}$	Capacitor value from XTAL_OUT to ground	Ceramic	–	0.1	–	µF

Figure 36: XTAL_IN Timing

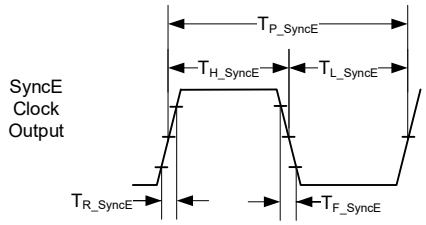


5.6.3 SyncE Recovered Clock Output Timing

Table 325: SyncE Recovered Clock Output Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_SyncE}	Period	25 MHz	–	39.999	–	ns
T_{H_SyncE}	High Time	25 MHz	–	19.035	–	ns
T_{L_SyncE}	Low Time	25 MHz	–	19.508	–	ns
T_{R_SyncE}	Rise Time	25 MHz	–	0.777	–	ns
T_{F_SyncE}	Fall Time	25 MHz	–	0.680	–	ns
T	Duty Cycle	25 MHz	48.972	49.394	49.854	%

Figure 37: SyncE Clock Output Timing



5.7 MAC Interface Timing

5.7.1 RGMII AC Characteristics

Table 326: General RGMII Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
T_{RISE}/T_{FALL}	Rise/Fall Time (20% – 80%)	–	–	0.75	ns

Note

- Rise and fall time depend on 50 trace impedance, capacitive load, and recommended trace length of <4 inches.
- Rise and fall time should be measured at the receiver.

5.7.2 RGMII 100 Mbps Input Timing

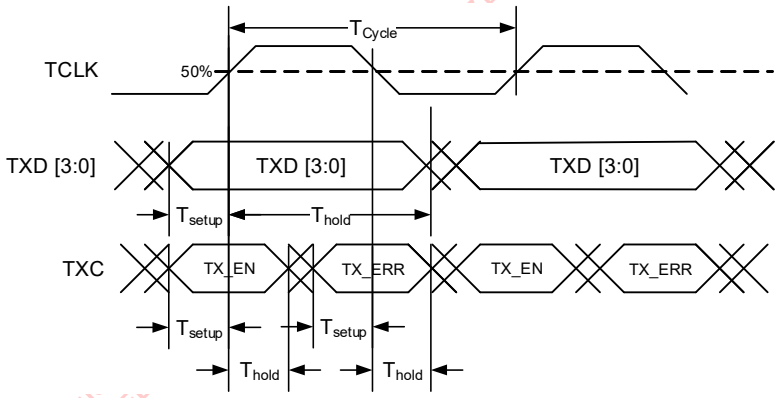
5.7.2.1 PHY Input TCLK with No Internal Delay

Table 327: PHY Input TCLK with No Internal Delay - Register 4.8000.2 = 0 (RGMII Mode 2)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{cycle}	Cycle Time	--	--	40	--	ns
T_{setup}	Setup Time	Register 4.8000.2 = 0	1.2	–	–	ns
T_{hold}	Hold Time		1.2	–	–	ns

Figure 38: PHY Input TCLK with No Internal Delay – Register 4.8000.2 = 0



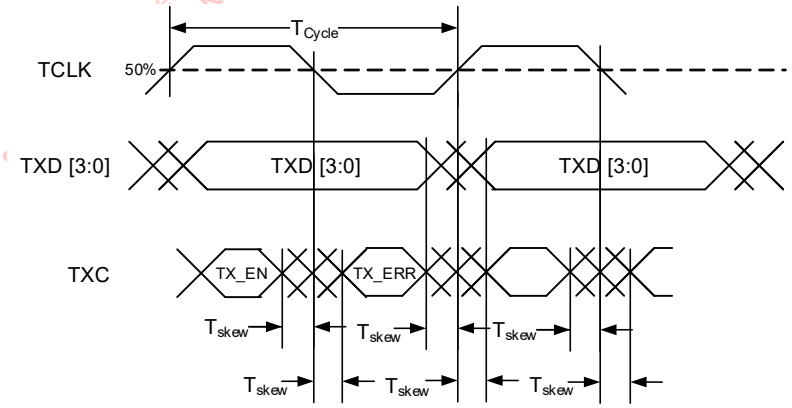
5.7.2.2 PHY Input TCLK with Internal Delay

Table 328: PHY Input TCLK with Internal Delay - Register 4.8000.2 = 1 (RGMII Mode 1)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{cycle}	Cycle Time	--	--	40	--	ns
T_{skew}	Skew Time	Register 4.8000.2 = 1	- .65	–	.65	ns

Figure 39: PHY Input TCLK with Internal Delay – Register 4.8000.2 = 1



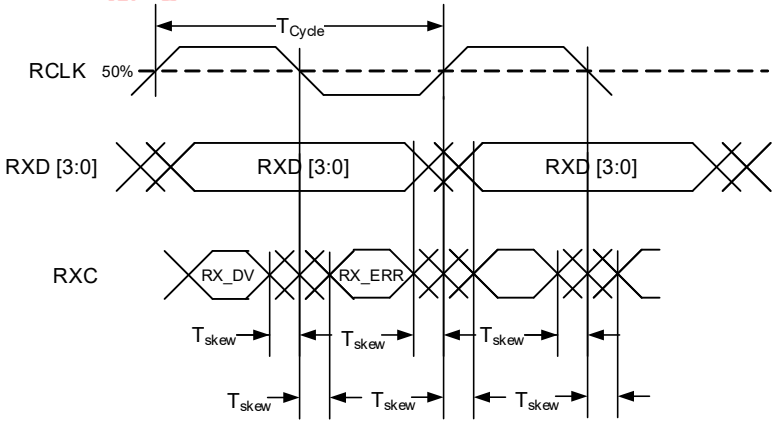
5.7.3 RGMII 100 Mbps Output Timing

5.7.3.1 PHY Output RCLK with No Internal Delay

Table 329: PHY Output RCLK with No Internal Delay - Register 4.8000.3 = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{cycle}	Cycle Time	--	--	40	--	ns
T_{skew}	Skew Time	Register 4.8000.3 = 0	- 0.5	–	0.5	ns

Figure 40: PHY Output RCLK with No Internal Delay - Register 4.8000.3 = 0

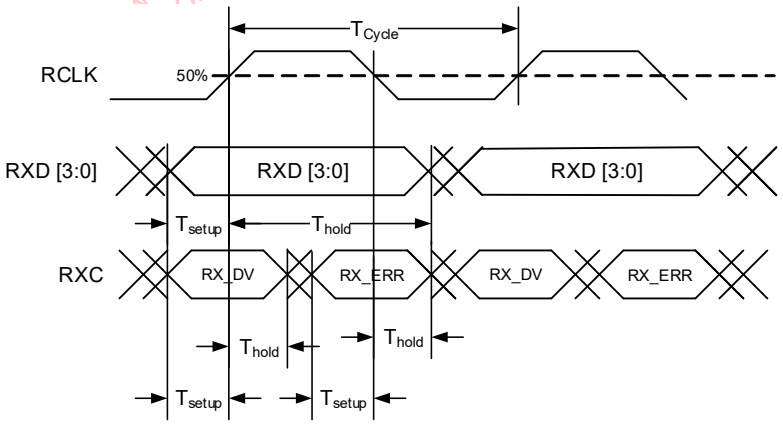


5.7.3.2 PHY Output RCLK with Internal Delay

Table 330: PHY Output RCLK with Internal Delay - Register 4.8000.3 = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{cycle}	Cycle Time	--	--	40	–	ns
T_{setup}	Setup Time	Register 4.8000.3 = 1	1.2	–	–	ns
T_{hold}	Hold Time		1.2	–	–	ns

Figure 41: PHY Output RCLK with Internal Delay - Register 4.8000.3 = 1



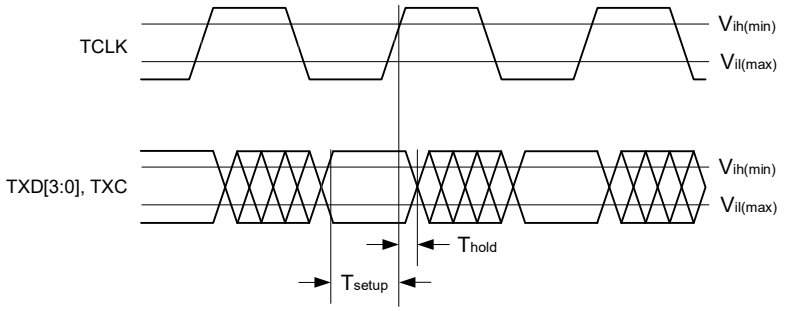
5.7.4 MII Interface Timing

5.7.4.1 MII PHY Input Timing

Table 331: MII PHY Input Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
T_{setup}	Setup Time	15	–	–	ns
T_{hold}	Hold Time	0	–	–	ns

Figure 42: MII PHY Input Timing

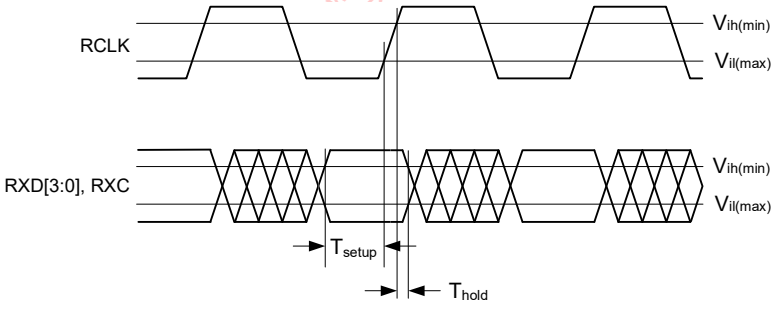


5.7.4.2 MII PHY Output Timing

Table 332: MII PHY Output Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
T_{setup}	Setup Time	10	–	–	ns
T_{hold}	Hold Time	10	–	–	ns

Figure 43: MII PHY Output Timing

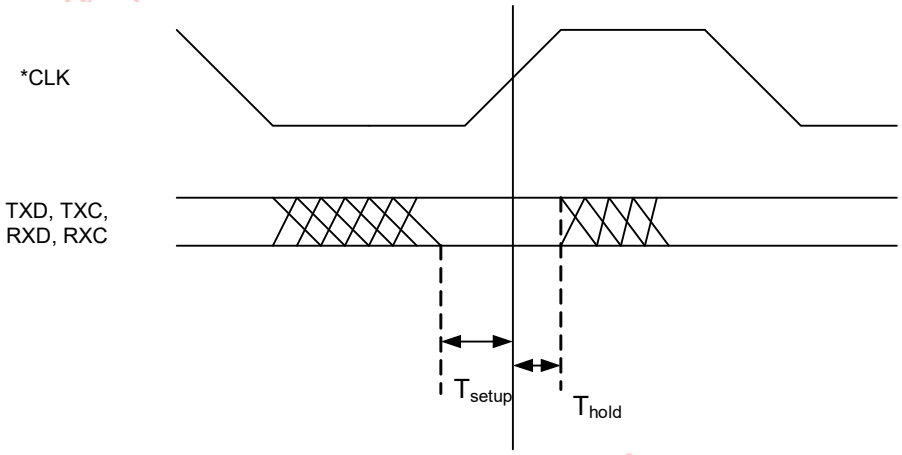


5.7.5 RMII Interface Timing

Table 333: RMII Interface Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
	RCLK Frequency	–	50	–	MHz
	RCLK Duty Cycle	35	–	65	%
T_{setup}	TXD[1:0], RXD[1:0], RXC Data setup to RCLK rising edge	4	–	–	ns
T_{hold}	TXD[1:0], TXC, RXD[1:0], RXC data hold from RCLK rising edge	2	–	–	ns

Figure 44: RMII Timing

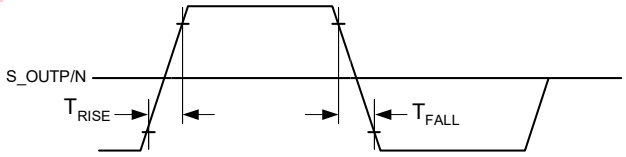


5.7.6 Output AC Characteristics

Table 334: Output AC Characteristics
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
T_{FALL}	VOD Fall Time (20 to 80%)	100	–	200	ps
T_{RISE}	VOD Rise Time (20 to 80%)	100	–	200	ps
T_{SKEW1}	Skew between Two Members of a Differential Pair	–	–	20	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14 × rms Random)	–	127	–	ps

Figure 45: Serial Interface Rise and Fall Time



5.7.7 Input AC Characteristics

Table 335: Input AC Characteristics
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14 × rms Random)	–	–	599	ps

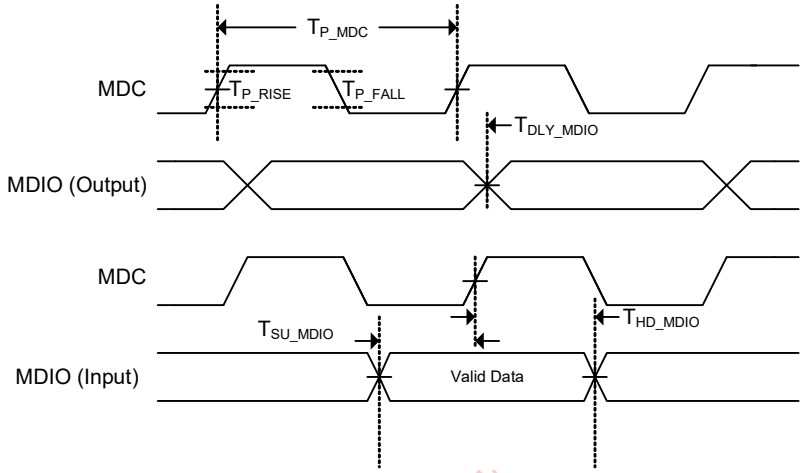
5.8 MDC/MDIO Timing

Table 336: MDC/MDIO Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time	0	–	20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time	10	–	–	ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time	10	–	–	ns
T_{P_MDC}	MDC Period	80	–	–	ns[1]
T_{P_RISE}	MDC Rise Time	--	--	10	ns
T_{P_FALL}	MDC Fall Time	--	--	10	ns

1. Maximum frequency = 12.5 MHz.

Figure 46: MDC/MDIO Timing



5.9 Latency Timing

5.9.1 Transmit Latency Timing

Table 337: Transmit Latency Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Parameter	Condition	Min	Typ	Max	Unit
MAC Interface	RGMII[1]	748	–	877	ns
	MII[1]	243	–	291	ns
	RMII[1]	603	–	753	ns
	SGMII[1]	742	–	878	ns

1. Assumes default FIFO settings with 64-byte to 1518-byte packets, at ±100 PPM

Figure 47: RGMII/MII/RMII Transmit Latency Timing

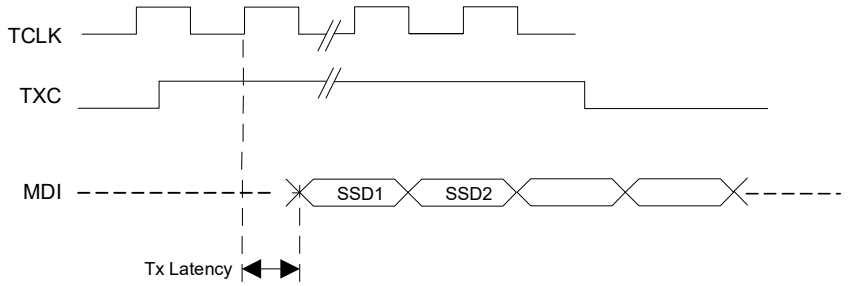
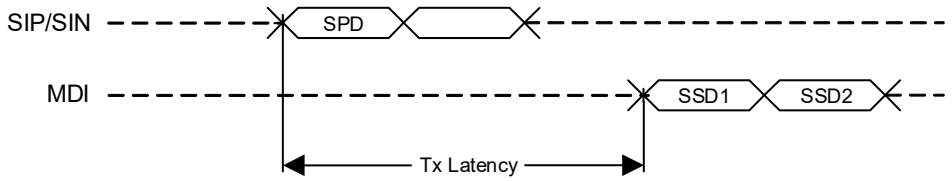


Figure 48: SGMII Transmit Latency Timing



5.9.2 Receive Latency Timing

Table 338: Receive Latency Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Parameter	Condition	Min	Typ	Max	Unit
MAC Interface	RGMII	747	–	861	ns
	MII	786	–	901	ns
	RMII[1]	913	–	1086	ns
	SGMII[1]	1196	–	1358	ns

1. Assumes default FIFO settings with 64-byte to 1518-byte packets, at ±100 PPM

Figure 49: RGMII/MII/RMII Receive Latency Timing

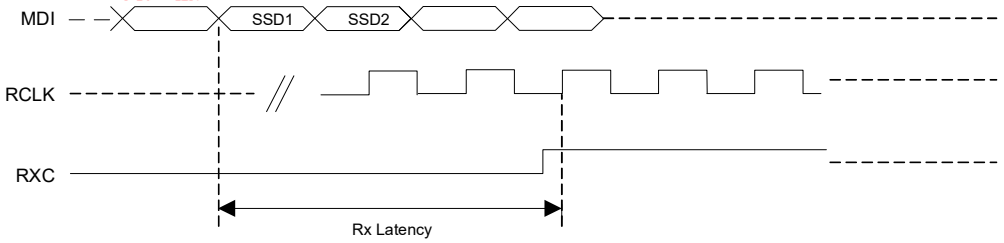
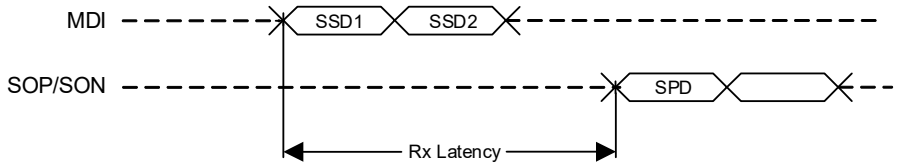


Figure 50: SGMII Receive Latency Timing



6 Package Mechanical Dimensions

6.1 40-Pin QFN Package Dimensions

Figure 51: 88Q1110/88Q1111 40-Pin QFN Package Mechanical Drawing

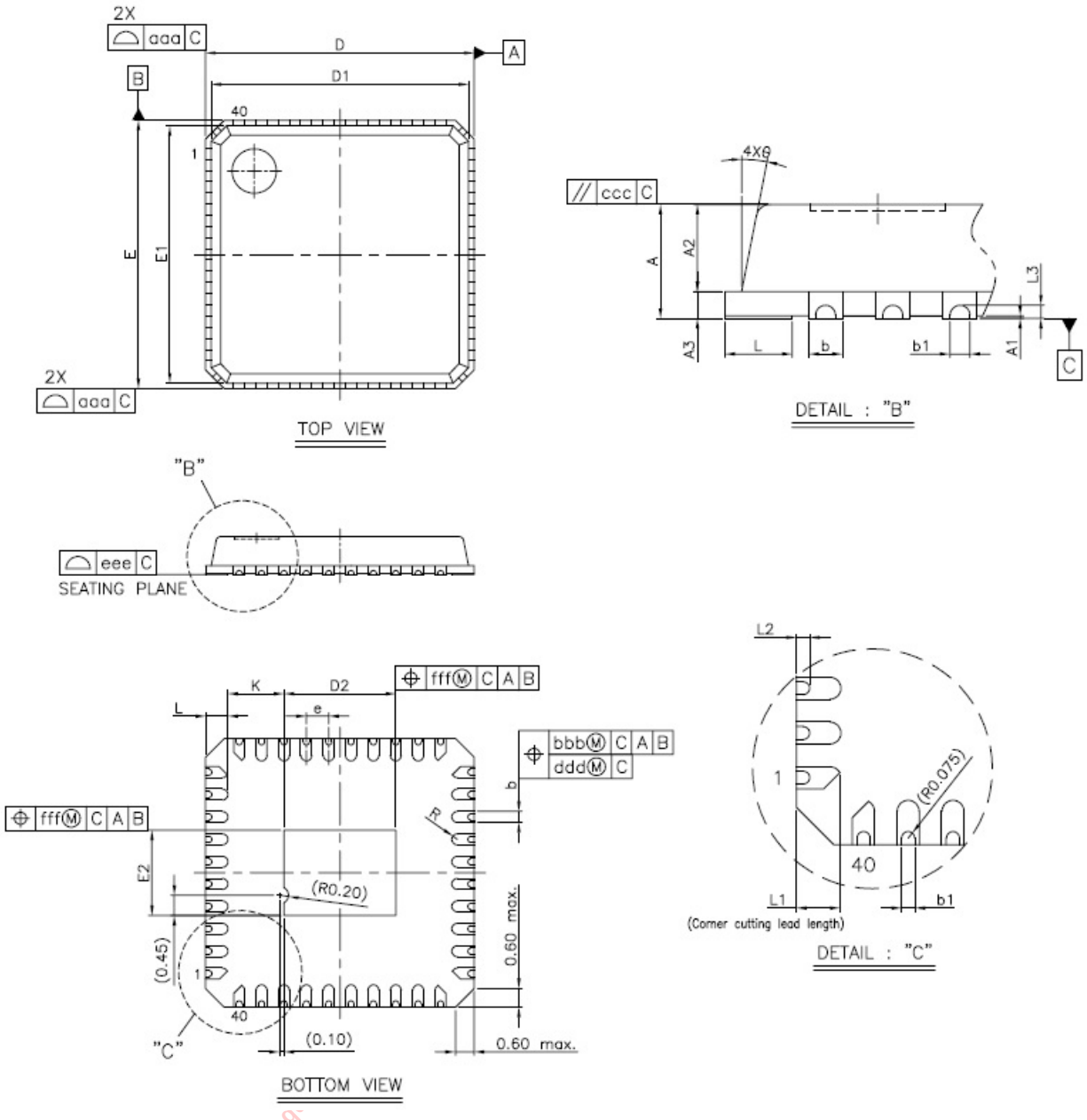


Table 339: Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	0.800	0.850	0.900
A1	0.000	0.020	0.050
A2	0.600	0.650	0.700
A3		0.203 REF.	
b	0.180	0.250	0.300
b1	0.100	0.150	0.200
D	5.92	6.00	6.08
D1		5.750 BSC	
D2	2.400	2.500	2.600
E	5.92	6.00	6.08
E1		5.750 BSC	
E2	1.800	1.900	2.000
L	0.400	0.500	0.600
L1	0.387	0.487	0.587
L2	0.100	0.150	0.200
L3	0.050	0.100	0.150
e		0.500 BSC	
Θ	0°	--	14°
R	0.100	--	0.150
K	1.05	1.25	1.45
Tolerances of Form and Position			
aaa		0.150	
bbb		0.100	
ccc		0.100	
ddd		0.050	
eee		0.080	
fff		0.100	

6.2 Package Maximum Pressure and Storage Temperature

Table 340: Package Maximum Pressure and Storage Temperature

Symbol	Parameter	Min	Typ	Max	Unit
$P_{PRESSURE}$	Maximum pressure on the 40-pin QFN (6 mm x 6 mm) package	–	–	20	N
$T_{STORAGE}$[1]	Storage temperature	-55	–	+125[2]	°C

1. The conditions for storing unpowered and unmounted devices are as follows:
   - Packed inside a vacuum-sealed moisture barrier bag with desiccant and humidity indicator card (HIC)
   - Stored at <40°C and <90% relative humidity (RH)
2. 125°C is only used as bake temperature for not more than 24 hours. Long-term storage (for example, weeks or longer) should be kept at 85°C or lower.

7 Ordering Part Number/Package Marking

7.1 Ordering Part Number

Figure 52 shows the ordering part numbering scheme for the 88Q1110/88Q1111 devices. Refer to the relevant release notes on the Marvell® extranet for the latest revision and complete part ordering information.

Figure 52: Ordering Part Number

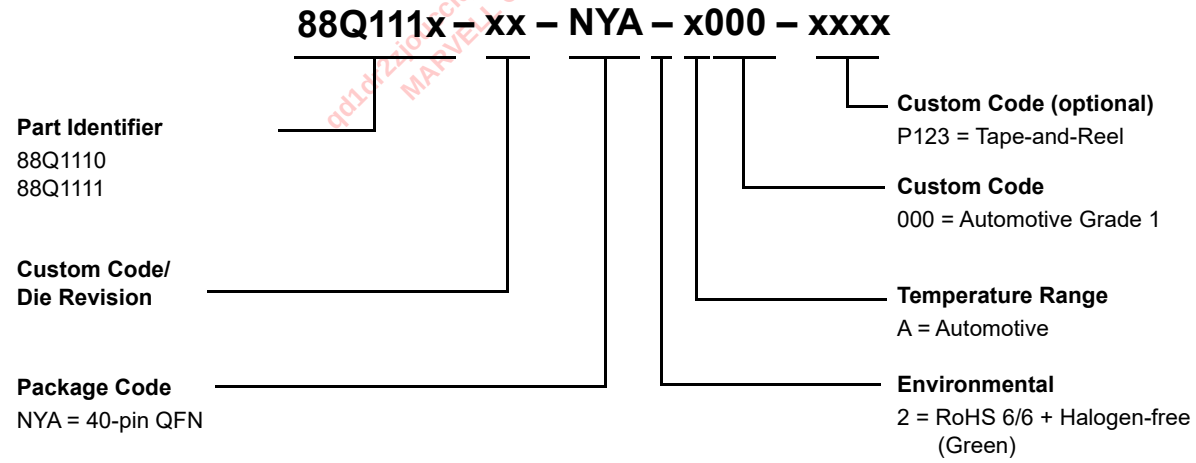


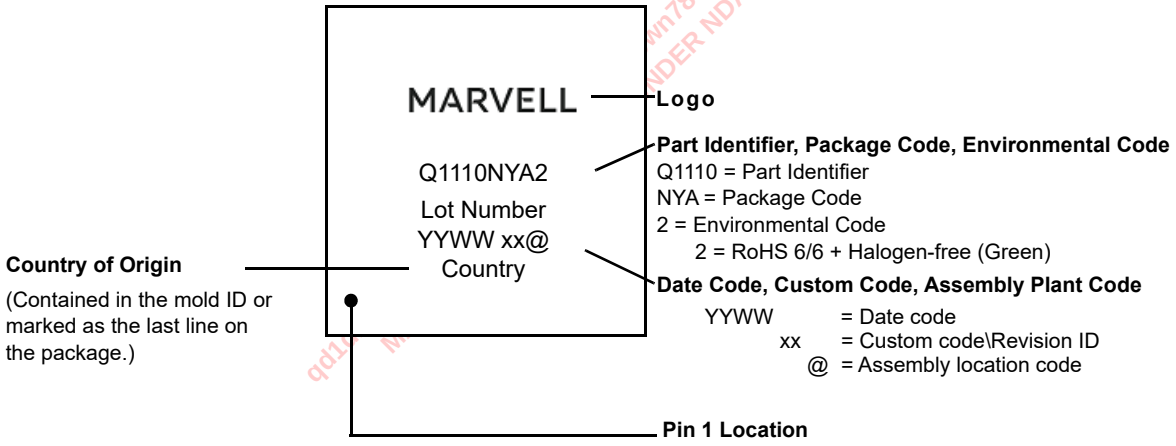
Table 341: 88Q1110/88Q1111 Part Ordering Options

Package Type	Features	Part Order Number
40-pin QFN	100BASE-T1 Operation-Grade 1	88Q1110-xx-NYA2A000 (Green, RoHS 6/6 and Halogen-free package, Automotive Grade 1)
		88Q1110-xx-NYA2A000-P123 (Green, RoHS 6/6 and Halogen-free package, Automotive Grade 1, Tape-and-Reel)
		88Q1111-xx-NYA2A000 (Green, RoHS 6/6 and Halogen-free package, Automotive Grade 1)
		88Q1111-xx-NYA2A000-P123 (Green, RoHS 6/6 and Halogen-free package, Automotive Grade 1, Tape-and-Reel)

7.2 Package Marking

Figure 54 shows a sample package marking and pin 1 location for the 88Q1110 40-pin QFN package (Automotive, Green).

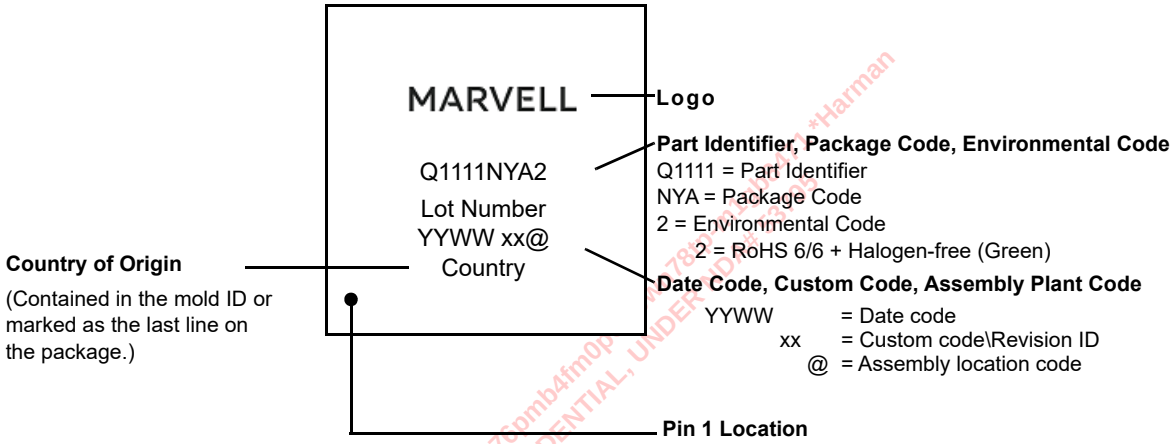
Figure 53: 88Q1110 Sample Package Marking and Pin 1 Location – Automotive Grade 1



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 54 shows a sample package marking and pin 1 location for the 88Q1111 40-pin QFN package (Automotive, Green).

Figure 54: 88Q1111 Sample Package Marking and Pin 1 Location – Automotive Grade 1



Note: The above example is not drawn to scale. Location of markings is approximate.

A Revision History

Table 342: Revision History (Sheet 1 of 4)

Revision	Date	Description
Rev. G	May 26, 2023	Datasheet release.
	April 20, 2023	Table 336, MDC/MDIO Timing, T_{P_RISE} and T_{P_FALL} Min 10 ns values corrected to Max 10 ns
Rev. F	April 19, 2023	Datasheet release.
	April 12, 2023	Section 2.4.1, Hardware Reset, on page 47. corrected 10 ms reference to 1 ms to match T_{RESET} Min value listed in Section 5.6.1, Reset Timing, on page 247.
Rev. E	January 12, 2023	Datasheet release.
	December 12, 2022	Table 341, 88Q1110/88Q1111 Part Ordering Options, on page 264, added Tape-and-Reel Part Order Numbers
	November 28, 2022	Added Table 174, Sleep/Wakeup Interrupt Status 2, on page 156 Added Table 175, Sleep/Wakeup Interrupt Enable 2, on page 156
	November 9, 2022	Figure 17, LPSD Block Diagram - VBAT Option 1, updated Q1 to Darlington bipolar Figure 18, LPSD Block Diagram - VBAT Option 2, added Buffer
	September 16, 2022	Table 339, Package Dimensions - clarified Symbol K, Dimension in mm, from Min .200 to Min 1.05, Nom 1.25 and Max 1.45
	April 14, 2022	Cover and Product Overview - added “Brightlane™”, and grammatical updates Section 1, Signal Description - Table 3, Table 4, Table 5, Table 6, Table 15, and Table 16 grammatical updates to clarify pin usage Table 39, LPSD Electrical Characteristics, on page 59, $I_{STANDBY}$ Current Max value changed from 45 to 35, added footnote regarding higher current for voltages above 12V, and changed V_{INH} Min from 1.5V to 2.0V Figure 19, INH Output Example Configurations, on page 60, changed ‘Output high level at 1.5V - 3.63V’ to ‘Output high level at 2.0V - 3.63V’ Table 98, 100BASE-T1 Status Register, on page 123 bits 7:0 removed “MSB of” from definition Table 100, PHY Status, on page 124, bits 15:8 added “Same as 3.8008.7:0” to definition Table 168, Sleep/Wake Request, on page 153. updated bit 4 Field name and Definition Added Section Section 5.4.3, Current Consumption at Reset, on page 235 Added Section 5.5.2.1, Internal Resistors, on page 241 Updated Section 5.7.1, RGMII AC Characteristics, on page 251, Section 5.7.2, RGMII 100 Mbps Input Timing, on page 251, and Section 5.7.3, RGMII 100 Mbps Output Timing, on page 253 Section 5.8, MDC/MDIO Timing, on page 258, added MDC Rise and Fall details

Table 342: Revision History (Sheet 2 of 4)

Revision	Date	Description
Rev. D	May 11, 2021	Datasheet release.
	May 10, 2021	Features, on page 3, removed Compliance bullet, added AEC-Q100 automotive standard compliant, and changed 'Automotive-grade temperature range from -40 °C to +125 °C' to 'Supports Automotive Grade 1 (-40 °C to +125 °C)' Section 2.23.1.1, Emission, second bullet, changed Meet to Meets Section 2.23.1.2, Immunity, second bullet, changed Tolerate to Tolerates and filed to field, last bullet, changed Meet to Meets Section 2.23.1.3, Electrostatic Discharge, first bullet corrected (HMB) to (HBM) and added ±6kV (MDI pins). second bullet, changed Mode to Model, last bullet changed Meet to Meets
Rev. C	January 28, 2021	Datasheet release.
	January 27, 2021	Updated Figure 17, LPSD Block Diagram - VBAT Option 1 Section 2.21.3.3, Trigger Pulse Generate Function, Register 4.C08 to 4.8E08 Table 131, LED Function Control Register bits 7:4, Mode 0101 exposed to Traffic Ready, bits 3:0 Mode 0111 exposed to Communication Ready Table 148, Copper Port Packet Generation bit 7 3.9611.15:0 changed to 3.8611.15:0
	January 27, 2021	Table 171, Sleep/Wakeup Interrupt Status, bits 8:7 exposed Table 172, Sleep/Wakeup Interrupt Enable, bits 8:7 exposed Table 173, Sleep/Wakeup Configuration, exposed bit 2 CIC Enable Default, bit 0 Mode changed from R/W to RO, and updated description. Added Note to Section 3.6, SGMII Registers regarding 100 Mbps speed only for SGMII mode Table 188, IO Pad Control Added TCLK and HW Rst to 0x1 Table 189, GPIO Control Register bit 0 updated description Table 217, Fiber Control Register bit 15 description 4.80xx reference changed to 31.80xx Table 246, PTP Port Config Register, bit 6 Note - removed “If the PTP_EXTCLK...” Table 286, TAI Global Config Register - bits 6:4 removed “...or PTP_EXTCLK...” Table 287, TAI Global Config Register - removed “When this device’s PTP...” Table 291, TAI Global Config Register - bits 15:12 - replaced “If the PTP_ EXTCLK...” with The default Table 298, TAI Global Config Register - Reserved. Table 301, Recommended Operating Conditions added T_J Max value and removed footnote 2. Section 5.4, Current Consumption - updated all values Section 5.5.4, SGMII Interface Transmitter DC Characteristics changed occurrences of Fiber to SGMII, added Power off leakage current values, and Table 320 removed Register 26 reference. Section 5.5.4.1, Common Mode Voltage (Voffset) Calculations changed the word Fiber to SGMII Added SGMII Transmit and Receive Latency Timing details to Section 5.9, Latency Timing
	January 11, 2021	Added Section , Enabling Wake Sources out the GPIO Pin Updated Section 2.18.2.3, New Clause 22 MDIO Register Access Method Added Table 194, Wake Source Sent out the GPIO Pin

Table 342: Revision History (Sheet 3 of 4)

Revision	Date	Description
Rev. C (cont.)	December 2, 2020	Updated Section 2.4.3, Undervoltage Protection to include VLPR description details. Table 191, Undervoltage Interrupt Enable exposed bit 5 FIRSTBOOT Enable Table 192, Undervoltage Status exposed bit 5 FIRSTBOOT Event
	November 25, 2020	Removed Table 189, Undervoltage Hysteresis Control, register bits 3:0 definitions. Removed Table 190, Undervoltage Threshold Control, register bits 3:0 definitions. Updated Section 5.5.2, TX_ENABLE, GPIO, RX, INTn, and MDIO Pins.
	October 27, 2020	Datasheet to Final status Updates per Characterization data throughout.
	September 1, 2020	Corporate rebranding and template update
		New Marvell logos added to all figures with Marvell logo marking
Rev. B	April 17, 2020	Datasheet release.
	April 9, 2020	Updated Table 328, PHY Input TCLK with Internal Delay - Register 4.8000.2 = 1 (RGMII Mode 1), Thold Min removed, Tskew added, and updated Figure 39.
	March 24, 2020	Updated Disclaimer Added Table 5, 88Q1111 Device Functional Block Diagram Updated Table 2.5, Power Management, on page 49 Updated Application Notes bullet items on page 60 Updated Figure 19, INH Output Example Configurations, on page 60 Updated Figure 20, TDR Trend Line, on page 63 Updated Table 69 - Table 74 formatting Updated Section 5.5, DC Operating Conditions, on page 236 Added Section 5.5.4, SGMII Interface Transmitter DC Characteristics, on page 242 Updated heading titles in Section 5.7.6 and Section 5.7.6 Updated Figure 51 to better reflect actual Epad shape and dimensions.
	December 10, 2019	Updated Figure 4, 88Q1110 Device Functional Block Diagram Updated Section 2.4, Resets Updated Figure 17 LPSD Block Diagram, added Figure 18
	November 22, 2019	Updated Table 10, 88Q1110 Low Power Signal Detect, on page 26, pin 38 INH definition Updated Table 21, 88Q1111 Low Power Signal Detect, on page 33, pin 38 INH definition Added Typ values - Section 5.4, Current Consumption, on page 233.
	November 5, 2019	Added Section 2.3.3, Synchronous SERDES Loopback, on page 46 Added Section 2.5.1.3, Wake from Sleep, on page 56 Added Section 2.9, Packet Generator and Packet Checker, on page 65 Added Section 2.21.1, PTP Control, on page 85 Added Section 2.21.2, Packet Time Stamping, on page 86 Added Section 2.21.3, Time Application Interface (TAI), on page 100 Added Section 2.21.4, ReadPlus Command, on page 104
		Updated title and section headings in Section 2.23, Electromagnetic Compatibility (EMC) Performance, on page 108 Added Section 3, General Registers, on page 109 Added Section 4, PTP Registers, on page 195

Table 342: Revision History (Sheet 4 of 4)

Revision	Date	Description
Rev. A	October 22, 2019	Datasheet release.
	October 18, 2019	Updated Disclaimer
		Table 39, LPSD Electrical Characteristics, on page 59 • ISTANDBY Max changed from 30 µA to 45 µA.
		Table 300, Absolute Maximum Ratings, on page 231 • VDD Max changed from 1.155 to 1.16 Table 302, Thermal Conditions for 88Q1110/88Q1111 40-Pin QFN Package, on page 232 • added Thermal data values Table 310, Digital Pins, on page 236 • VIH Max values changed from VDDO + 0.4 to VDDO + 0.7 • VIL Max values to VDDO*0.3 • IILK Max value from 2 to 10 Table 310, TX_ENABLE and GPIO Pins, on page 236 • VOH and VOL Condition, added footnote • VOL from 20 mA to -20 mA • IILK Max from 2 to 10
	October 10, 2019	Table 301, Recommended Operating Conditions, on page 231: • DVDD Supply updated Min and Max values from 0.97 and 1.182 to 0.98 and 1.12, respectively. • VDDO, For VDDO at 2.5V, Min from 2.32 to 2.33.
	October 2, 2019	Table 9, 88Q1110 Power, Ground, and Internal Regulators, on page 25 • VDDO pin definition changed to “VDDO must be supplied externally.” Table 20, 88Q1111 Power, Ground, and Internal Regulators, on page 32 • VDDO pin definition changed to “VDDO must be supplied externally.” Table 47, 88Q1110 Configuration Pin Mapping, on page 72 • added “88Q1110” to table title. Table 52, 88Q1111 Configuration Pin Mapping, on page 75 • added “88Q1111” to table title. • CONFIG2, CONFIG6 - Sampled Big Definition - added “The sampled value must be 10, so the CONFIG2 pin must be floating and the CONFIG6 pin must have a pull-down added.” Under Table 54 after the first sentence • added “, however; the CONFIG2 pin must be floating and the CONFIG6 pin must have a pull-down added.”
Rev. --	September 16, 2019	Initial version.

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