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1. Test setup:-

Hardware used: - B2-SP25-IDCEvo

Image flashed: ES2 Artifact-903, Minor change in Android code for few test cases

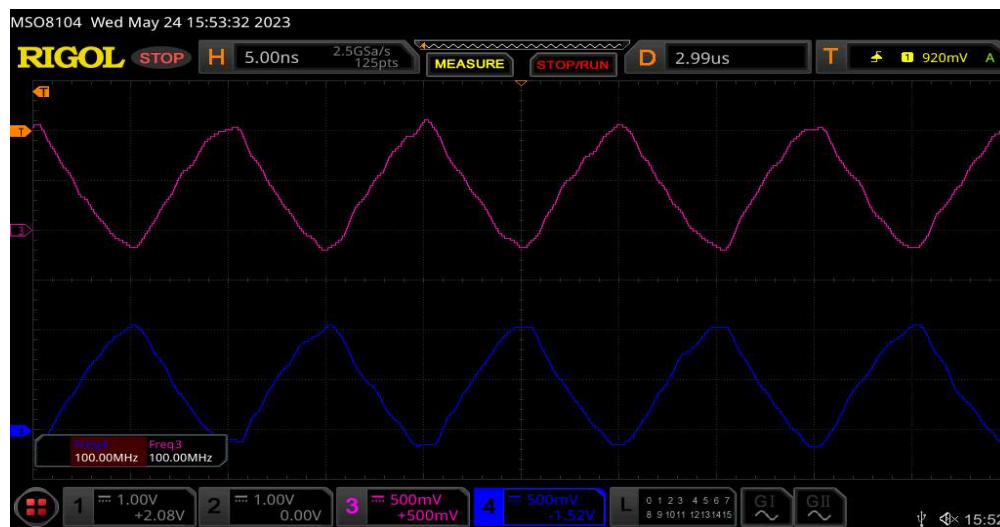
Signals probed:

- WLAN1_SOC_PCIE2L_L(0)_TX_N, WLAN1_SOC_PCIE2L_L(0)_TX_P
- WLAN1_SOC_PCIE2L_L(0)_RX_N, WLAN1_SOC_PCIE2L_L(0)_RX_P
- WLAN1_SOC_PCIE_PERST(2)_Q
- WLAN1_SOC_PCIE_CLKREQ(2)_Q
- WLAN1_SOC_PCIE2L_REFCLK0_N, WLAN1_SOC_PCIE2L_REFCLK0_P
- ONUG3V3_BT_Wifi

CRO used: - RIGOL MSO8104 (1GHz, 10 Gsa/s))

2. Waveforms and results:-

2.1. Frequency of PCIe_REFCLK_P, PCIe_REFCLK_N



Legend:

Violet: WLAN1_SOC_PCIE2L_REFCLK0_P

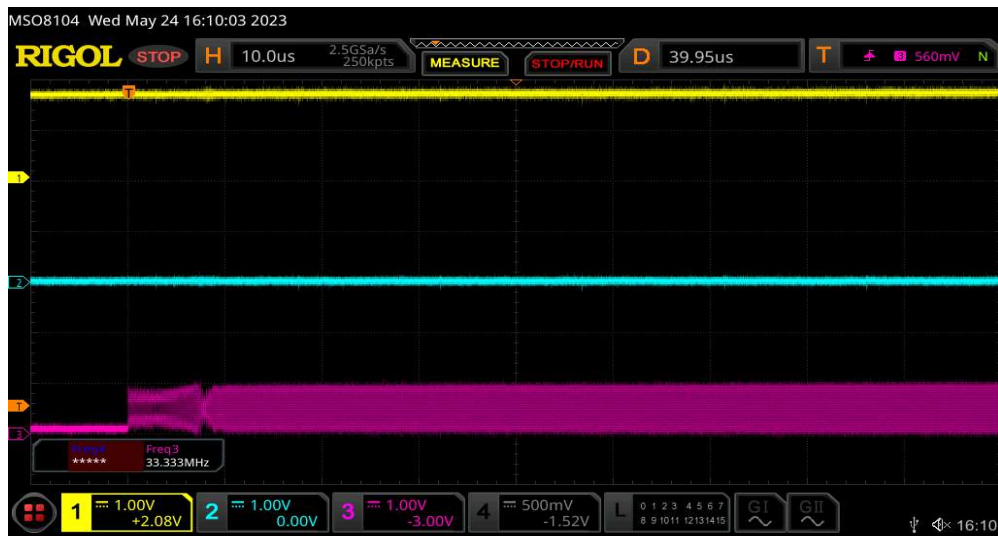
Blue: WLAN1_SOC_PCIE2L_REFCLK0_N

Result: - PCIe Clock frequency = 100MHz

Note: -

The PCIe standard specifies a 100 MHz clock (Refclk) with at least ± 300 ppm frequency stability for Gen 1, 2, 3 and 4, and at least ± 100 ppm frequency stability for Gen 5, at both the transmitting and receiving devices.

2.2. Rough estimation of PCIe_REFCLK stabilization:-

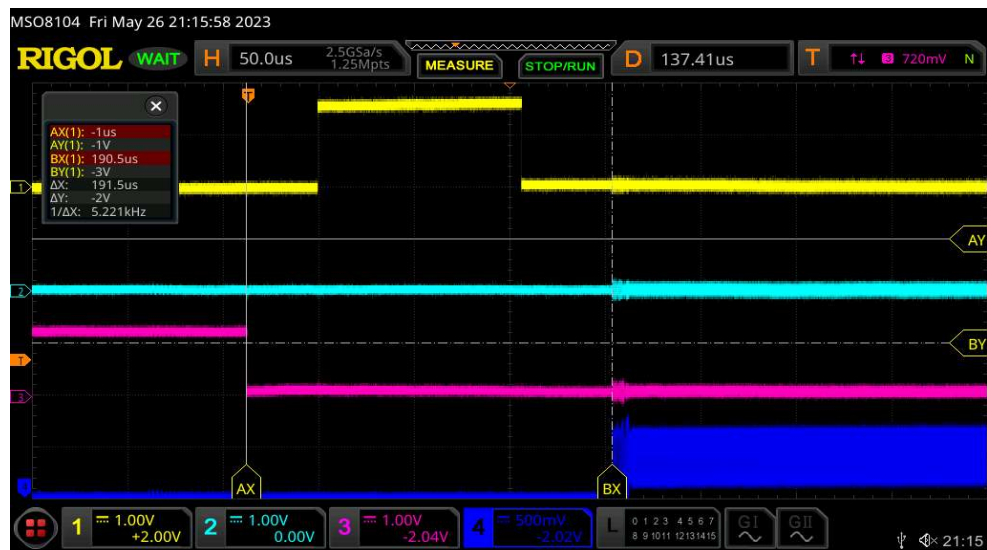


Legend:

Vioet: WLAN1_SOC_PCIE2L_REFCLK0_P

Result : - PCIe Clock stabilization takes around 20us.

2.3. PCIe clock gating using CLKREQ line:-



Legend:

Yellow: ONUG3V3_BT_Wifi

Cyan: WLAN1_SOC_PCIE_PERST(2)_Q

Violet: WLAN1_SOC_PCIE_CLKREQ(2)_Q

Blue: WLAN1_SOC_PCIE2L_REFCLK0_P

Result: - PCIe CLKREQ line is used to enable and gate the PCIe clock. When CLKREQ line is low, then PCIe clock is enabled and when it goes high then PCIe clock can be disabled.

Time to enable PCIe clock from falling edge of CLKREQ line is 191.5 us (approx.).

Note: -

As per IDCEvo wifi chip (CYW8x570) datasheet Page no - 50, CLKREQ pin is as below.

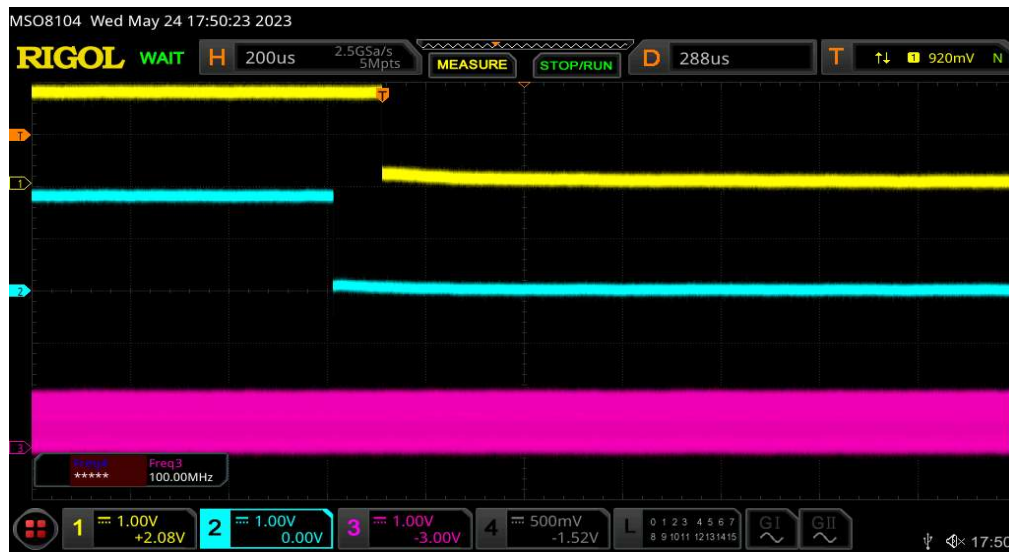
Output structure, as per the 1.0 of the Local Bus Specification, Revision 2.0			
N5	PCIE_CLKREQ_L	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.

When PCIE_CLKREQ_L pin of wifi chip is made High, then clock is gated or turned off.

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GPH0[4] port configuration			
GPH0[4]	[19:16]	RW	Sets the port configuration 0x0 = Input 0x1 = Output 0x2 = PCIEG5_CLKREQ2 0x3 ~ 0xE = Reserved 0xF = NWEINT_GPH0[4]
			0x0000_0000

2.4. PCIe Clock is maintained even after PCIe enumeration fails:-



Legend:

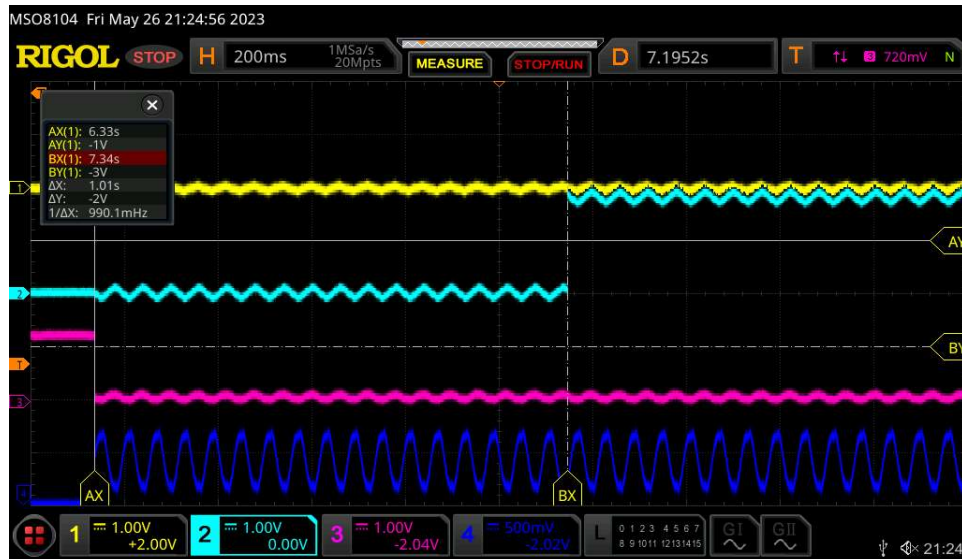
Yellow: ONUG3V3_BT_Wifi

Cyan: WLAN1_SOC_PCIE_PERST(2)_Q

Violet: WLAN1_SOC_PCIE2L_REFCLK0_P

Result: - PCIe clock is maintained, even after PCIe enumeration fails.

2.5. Time gap between PERST and CLKREQ



Legend:

Yellow: ONUG3V3_BT_Wifi
Cyan: WLAN1_SOC_PCIE_PERST(2)_Q
Violet: WLAN1_SOC_PCIE_CLKREQ(2)_Q
Blue: WLAN1_SOC_PCIE2L_REFCLK0_P

Result: - Time gap between falling edge of CLKREQ line and rising edge of PERST# line is 1.01 seconds.

Note: -

PERST# line is PCIe Reset line, which is made high in probe function of PCIe controller driver.

2.6. Time sequence of various signals on normal power up of target:-

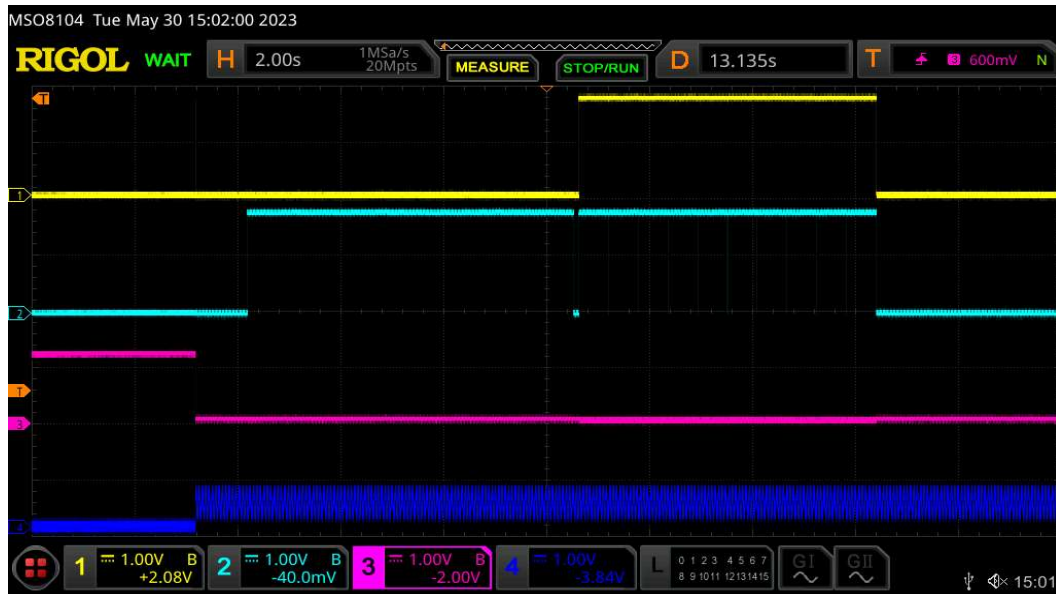


Legend:

Yellow: ONUG3V3_BT_Wifi
Cyan: WLAN1_SOC_PCIE_PERST(2)_Q
Violet: WLAN1_SOC_PCIE_CLKREQ(2)_Q
Blue: WLAN1_SOC_PCIE2L_REFCLK0_P

Result: - Time gap between rising edge of CLKREQ and rising edge of Power-On-GPIO be 13.16 seconds. In this case, Power-ON-GPIO is asserted due to "PCIe enumeration command" running in init.wifi.rc. Here, falling edge of CLKREQ line is taken as reference only.

2.7. PCIe enumeration fail waveform at Power ON:



Legend:

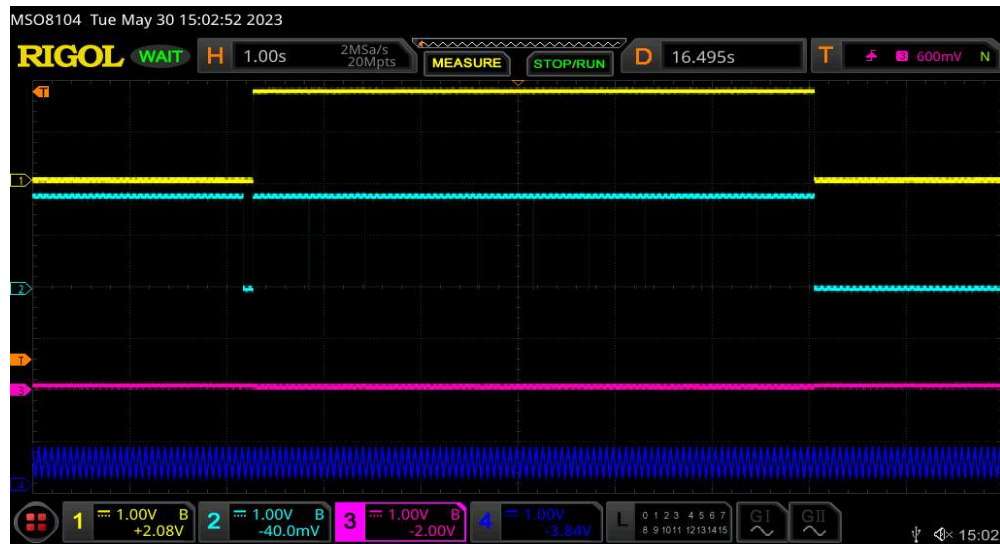
Yellow: ONUG3V3_BT_Wifi

Cyan: WLAN1_SOC_PCIE_PERST(2)_Q

Violet: WLAN1_SOC_PCIE_CLKREQ(2)_Q

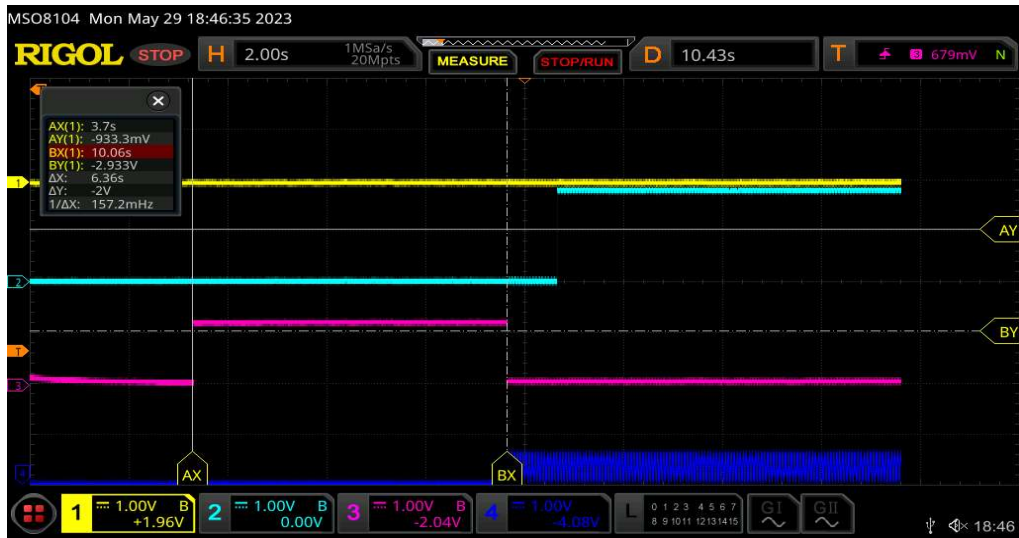
Blue: WLAN1_SOC_PCIE2L_REFCLK0_P

Result: - At Power On, PCI enumeration is triggered using a command in an init.rc script, if enumeration does not pass, then 10 times retries are done, which can be seen as PERST# line coming LOW 10 times in above waveform. The expanded view is shown below.



Note: - In above waveform with Cyan colour, we can see PERST# signal coming LOW for 10 times.

2.8. Time gap between CLK REQ rising and falling edge at Power-On:



Legend:

Yellow: ONUG3V3_BT_Wifi

Cyan: WLAN1_SOC_PCIE_PERST(2)_Q

Violet: WLAN1_SOC_PCIE_CLKREQ(2)_Q

Blue: WLAN1_SOC_PCIE2L_REFCLK0_P

Result: - CLKREQ line is high for 6.36 seconds at Power On.

2.9. Waveform for PCIe_TXD and PCIe_RXD line:-

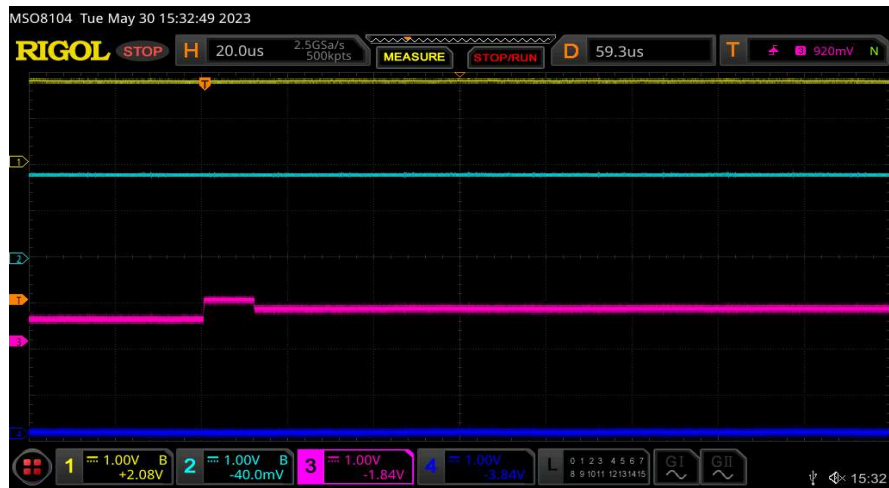
CRO probes were connected to below lines: -

ONUG3V3_BT_Wifi, WLAN1_SOC_PCIE_PERST(2)_Q, WLAN1_SOC_PCIE2L_L(0)_TX_P and WLAN1_SOC_PCIE2L_L(0)_RX_P signals.

When target was powered up to capture data lines, it generates panic. Panic log back trace is as below. Waveform is also shown below but it is of no use.

```
6 3 4:[ 16.680230][ C2] CPU: 2 PID: 188 Comm: kworker/u14:6 Tainted: G      E 5.15.41-android13-8-g539e26b439f0-ab903 #1
6 3 4:[ 16.680238][ C2] Hardware name: BMW IDCevo (v920-EVT0 SP21 B1) Android IVI VM (DT)
6 3 4:[ 16.680245][ C2] Workqueue: pcie_wq exynos_v920_pcie_dislink_work [pcie_exynos_v920_dw_rc]
6 3 4:[ 16.680268][ C2] pstate: 204000c5 (nzCv dalF +PAN -UAO -TCO -DIT -SSBS BTYPE=--)
6 3 4:[ 16.680275][ C2] pc : pci_generic_config_read+0x98/0xbc
1 3 0:[ 16.680288][ C2] lr : pci_generic_config_read+0x28/0xbc
6 3 4:[ 16.680295][ C2] sp : fffffffc00bf4b9e0
6 3 4:[ 16.680300][ C2] x29: fffffffc00bf4b9e0 x28: fffffffc00116a750 x27: 00000000000000c0
6 3 4:[ 16.680310][ C2] x26: fffffff89ece7d800 x25: 0000000000000000 x24: 0000000000000018
1 3 0:[ 16.680320][ C2] x23: 0000000000000004 x22: fffffffc00bf4ba74 x21: fffffff8801e164b0
6 3 4:[ 16.680332][ C2] x20: 0000000000000004 x19: fffffffc00bf4ba74 x18: fffffffc00be7d060
1 3 0:[ 16.680340][ C2] x17: 00000000000000c6 x16: 0000000000005853e x15: 000000000000001b
6 3 4:[ 16.680349][ C2] x14: 000000000000dd3e x13: 0000000000000096 x12: 0000000000000002
6 3 4:[ 16.680358][ C2] x11: 000000020000102e x10: 0000000000000002 x9 : 0000000000000000
1 3 0:[ 16.680366][ C2] x8 : 0000000000000000 x7 : 7f7f7f7f7f7f7f7f x6 : ff626871646d6466
6 3 4:[ 16.680375][ C2] x5 : 0000000000000010 x4 : fffffffc00bf4ba74 x3 : 0000000000000004
1 3 0:[ 16.680383][ C2] x2 : 0000000000000018 x1 : 0000000000000000 x0 : fffffffc00a9c8018
6 3 4:[ 16.680393][ C2] Kernel panic - not syncing: Asynchronous SError Interrupt
6 3 4:[ 16.680400][ C2] CPU: 2 PID: 188 Comm: kworker/u14:6 Tainted: G      E 5.15.41-android13-8-g539e26b439f0-ab903 #1
1 3 0:[ 16.680406][ C2] Hardware name: BMW IDCevo (v920-EVT0 SP21 B1) Android IVI VM (DT)
6 3 4:[ 16.680412][ C2] Workqueue: pcie_wq exynos_v920_pcie_dislink_work [pcie_exynos_v920_dw_rc]
1 3 0:[ 16.680425][ C2] Call trace:
6 3 4:[ 16.680429][ C2] dump_backtrace+0x0/0x1d4
6 3 4:[ 16.680440][ C2] show_stack+0x1c/0x2c
6 3 4:[ 16.680446][ C2] dump_stack_lvl+0x68/0x84
6 3 4:[ 16.680461][ C2] dump_stack+0x1c/0x40
1 3 0:[ 16.680469][ C2] panic+0x164/0x3a8
6 3 4:[ 16.680476][ C2] test_taint+0x0/0x24
6 3 4:[ 16.680485][ C2] arm64_serror_panic+0x70/0x98
6 3 4:[ 16.680492][ C2] do_serror+0x104/0x134
1 3 0:[ 16.680498][ C2] el1h_64_error_handler+0x38/0x54
6 3 4:[ 16.680507][ C2] el1h_64_error+0x7c/0x80
6 3 4:[ 16.680515][ C2] pci_generic_config_read+0x98/0xbc
6 3 4:[ 16.680522][ C2] exynos_v920_generic_own_config_read+0x110/0x16c [pcie_exynos_v920_dw_rc]
1 3 0:[ 16.680534][ C2] pci_bus_read_config_dword+0x84/0xd8
6 3 4:[ 16.680541][ C2] pci_read_config_dword+0x44/0x54
6 3 4:[ 16.680549][ C2] pci_scan_bridge_extend+0x74/0x61c
1 3 0:[ 16.680557][ C2] pci_scan_child_bus_extend+0x218/0x350
6 3 4:[ 16.680565][ C2] pci_rescan_bus+0x20/0x4c
6 3 4:[ 16.680574][ C2] exynos_v920_pcie_poweron+0x57c/0x918 [pcie_exynos_v920_dw_rc]
6 3 4:[ 16.680585][ C2] exynos_v920_pcie_dislink_work+0x198/0x1dc [pcie_exynos_v920_dw_rc]
1 3 0:[ 16.680595][ C2] process_one_work+0x1ac/0x394
```

When CRO probe was removed from TXD and RxD lines of PCIe, then it booted normally without any panic.



Legend:

Yellow: ONUG3V3_BT_Wifi

Cyan: WLAN1_SOC_PCIE_PERST(2)_Q

Violet: WLAN1_SOC_PCIE2L_L(0)_TX_P

Blue: WLAN1_SOC_PCIE2L_L(0)_RX_P

Result: When CRO probe was connected to PCIe TxD and RxD lines, then it is generating panic. When CRO probes are disconnected then it boots without panic.