Preliminary Specification

HD Radio™ Series

[PNP Baseband SOC]

PN3034HT

[Triple / MRC+1-channel Receiver with AAA]

DATA SHEET

PnpNetwork Technologies, Inc.

FEB 2020

(Version 0.93)

Note: This documentation is preliminary and subject to change. PnpNetwork Technologies, Inc. reserves the right to do any kind of modification in this datasheet regarding both hardware and software implementations without notice.

Revision History

Bars appearing in the left margin of the document as shown here indicate changes made to this document since the last revision issued.

Date	Revision	Description	Author
2020.02.11	**Version 0.93**	**Revised from PN3034HT data sheet**	**Jeremy**

Contents

1. Introduction

1.1 Overview

The PN3034HT is a superior system on chip for HD Radio™ applications. It fully supports IBOC (In-Band On-Channel) system consists of flexible software/hardware COFDM demodulator and Radio/Audio DSP. Several interfaces such as SPI, I2C and UART are implemented providing customers with more flexibility. And these interfaces fully support "RX_IDD_2206" HD Radio™ standard.

The PN3034HT integrates the DSP Core, offering the low-power, high-performance Radio/Audio processing, supports enhanced HD Radio™ audio applications. The DSP core eliminates the need for the audio companion processors normally required for audio-based applications. By removing the need for costly application coprocessors and external memory subsystems, the PN3034HT chipset solution reduces BOM costs.

1.2 Features

- Standards support: IBOC system for HD Radio™ application
- Digital I/Q Tuner interface for 3 external RF tuners
- Outstanding Mobility and 1st Adjacent Channel Rejection Performance
- Low power consumption: Max 730mW(TBD)
- 32-bits RISC architecture with integrated 24-bits audio processing instructions
- MRC Diversity support
- 16Mbyte Mobile SDRAM stacked for high technology audio codec process and data service
- 10 x 10 mm2, 0.65 mm pitch, 179-pin Fine pitch BGA technology.

1.3 Applications

- Automotive Digital Radio System for HD Radio™
- Aftermarket car radio and audio system
- Boom Box and Audio component system
- Smart Speaker system with HD Radio™
- Kitchen Radio application

1.4 Ordering Information

Part Number		PN3034HT
Package Information	Ball Pitch	0.65mm
	Body Size	10mm x 10mm x 1.2mm
	Ball Count (Type)	179 balls (FBGA)
Supply Voltage	Core	1.1V ~ 1.2V (TBD)
	I/O	3.0V
Operation Temperature		-40 ~ +85°C
Storage Temperature		-50 ~ +150°C

Table 1-1 Ordering Information

- Note: PN3034HT is pin to pin compatible with PAIOS^{2}-AD, PN3034Mx series and PAIOS^{X}-VD series.

1.4.1 Order type overview

Number	Target Application	Internal tuner	Digital I/Q tuner Interface
PN3034HT	[MRC / Phase Diversity Antenna] HD Radio™ 3-ch Receiver Baseband SOC for MRC Audio & Data(*1) mode with AAA(*2) + BGS/DATA(*3)	No	Up to 3
	[Single Antenna] HD Radio™ 3-ch Receiver Baseband SOC for the applications in below. - Audio & Data mode with AAA + BGS(*4) + Data(*5) - 1st Audio & Data mode with AAA +2nd Audio & Data mode with AAA+ BGS/DATA		

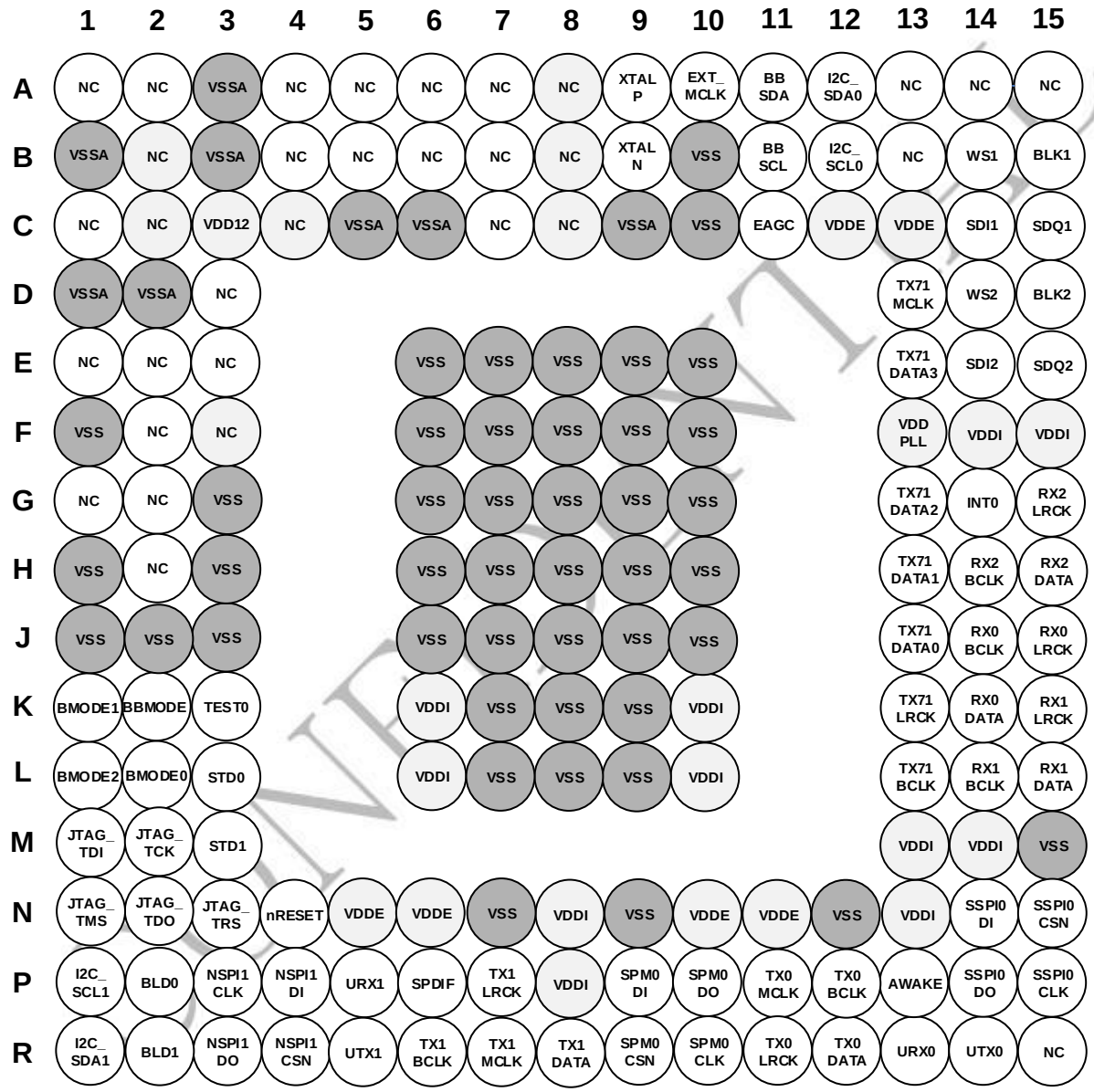
Table 1-2 Order type overview

* Note 1: “Audio & Data” means audio and data service are received simultaneous on the same frequency station.
* Note 2: “AAA” means Automatic level and time Alignment Audio for seamless blending between Analog and Digital Radio.
* Note 3: “BGS/Data” means the separated tuner can be used for back ground scanning or data service on the other frequency stations time-dependently.
* Note 4: “+ BGS” means the separated tuner can be always used for back ground scanning on the other frequency stations.
* Note 5: “+ DATA” means the separated tuner can be always used for DATA service on the other frequency stations.

2. Pin Information

2.1 Pin Assignment

- Top View



PN3034HT Pin assignment

3. Pin Descriptions

TYPE Description

I : Input ,O : Output , IO : Bidirectional ,AP : Analog Power ,DP : Digital Power , DG : Digital Ground

- DSP and Interfaces Pins

Pin	Symbol	Type	Function	Description
A12	I2C_SDA0	IO	I2C	I^2C DATA (Master only)
B12	I2C_SCL0	O	I2C	I^2C CLK (Master only)
R1	I2C_SDA1	IO	I2C	I^2C DATA (Master/Slave)
P1	I2C_SCL1	IO	I2C	I^2C CLK (Master/Slave)
A11	BB_SDA	IO	I2C	I^2C DATA (Master only)
B11	BB_SCL	O	I2C	I^2C CLK (Master only)
R14	UART_TX0	O	UART	UART0 Transfer data
R13	UART_RX0	I	UART	UART0 Receive data
P10	SPM0_DO	O	SPI	SPI0 master / Data out / MOSI
P9	SPM0_DI	I	SPI	SPI0 master / Data in / MISO
R9	SPM0_CSN	O	SPI	SPI0 master / Chip select / SS
R10	SPM0_CLK	O	SPI	SPI0 master Clock/ CLK
G14	INT0	IO	GPIO	External Interrupt Input[0]
R5	UART_TX1	IO	GPIO	UART1 TX
P5	UART_RX1	IO	GPIO	UART1 RX
P2	BLD0	IO	GPIO	GPIO0 / Blending Out0
R2	BLD1	IO	GPIO	GPIO1 / Blending Out1
R3	NSPI1 DO	IO	GPIO	SPI1 DO (Master or Slave)
P4	NSPI1 DI	IO	GPIO	SPI1 DI (Master or Slave)
P3	NSPI1 CLK	IO	GPIO	SPI1 CLK (Master or Slave)
R4	NSPI1 CSN	IO	GPIO	SPI1 nCS (Master or Slave)
P14	NSPI0 DO	IO	GPIO	SPI0 Slave MISO
N15	NSPI0 CSN	IO	GPIO	SPI0 Slave nCS
N14	NSPI0 DI	IO	GPIO	SPI0 Slave MOSI
P15	NSPI0 CLK	IO	GPIO	SPI0 Slave CLK
P6	SPDIF	IO	GPIO	SPDIF/ GPIO3[6]
P11	TX0_MCLK	O	I2S	I^2S TX0 Main Clock
R11	TX0_LRCK	IO	I2S	I^2S TX0 Left / Right CLK

P12	TX0_BCLK	IO	I2S	I²S TX0 Bit Clock
R12	TX0_DATA	O	I2S	I²S TX0 Data
R7	TX1_MCLK	O	I2S	I²S TX1 Main Clock
P7	TX1_LRCK	IO	I2S	I²S TX1 Left / Right CLK
R6	TX1_BCLK	IO	I2S	I²S TX1 Bit Clock
R8	TX1_DATA	O	I2S	I²S TX1 Data
D13	TX71_MCLK	O	I2S	I²S TX71 Main Clock
E13	TX71_DATA3	O	I2S	I²S TX71 Data3
G13	TX71_ DATA2	O	I2S	I²S TX71 Data2
H13	TX71_ DATA1	O	I2S	I²S TX71 Data1
J13	TX71_ DATA0	O	I2S	I²S TX71 Data0
K13	TX71_LRCK	IO	I2S	I²S TX71 Left / Right CLK
L13	TX71_BCLK	IO	I2S	I²S TX71 Bit Clock
J14	RX0_BCLK	I	I2S	I²S RX0 Bit Clock
J15	RX0_LRCK	I	I2S	I²S RX0 Left-Right Clock
K14	RX0_DATA	I	I2S	I²S RX0 Data
L14	RX1_BCLK	I	I2S	I²S RX1 Bit Clock
K15	RX1_LRCK	I	I2S	I²S RX1 Left-Right Clock
L15	RX1_DATA	I	I2S	I²S RX1 Data
H14	RX2_BCLK	I	I2S / GPIO	I²S RX2 Bit Clock (Reserved for GPIO)
G15	RX2_LRCK	I	I2S / GPIO	I²S RX2 Left-Right Clock (Reserved for GPIO)
H15	RX2_DATA	I	I2S / GPIO	I²S RX2 Data (Reserved for GPIO)
C11	EAGC	O	Tuner IF	External AGC
A13	BLK0	I	Tuner IF	Digital I/Q Input BCLK0
B13	WS0	I	Tuner IF	Digital I/Q Input WS0
A14	SDI0	I	Tuner IF	Digital I/Q Input Serial Data-I 0
A15	SDQ0	I	Tuner IF	Digital I/Q Input Serial Data-Q 0
B15	BLK1	I	Tuner IF	Digital I/Q Input BCLK1
B14	WS1	I	Tuner IF	Digital I/Q Input WS1
C14	SDI1	I	Tuner IF	Digital I/Q Input Serial Data-I 1
C15	SDQ1	I	Tuner IF	Digital I/Q Input Serial Data-Q 1
D15	BLK2	I	Tuner IF	Digital I/Q Input BCLK2
D14	WS2	I	Tuner IF	Digital I/Q Input WS2
E14	SDI2	I	Tuner IF	Digital I/Q Input Serial Data-I 2
E15	SDQ2	I	Tuner IF	Digital I/Q Input Serial Data-Q 2

- MODE & SYSTEM Pins

Pin	Symbol	Type	Function	Description
L2	BMODE[0]	I	MODE	Configure Pin Boot MODE[0] 1)note
K1	BMODE[1]	I	MODE	Configure Pin Boot MODE[1] 2)note
L1	BMODE[2]	I	MODE	Configure Pin Boot MODE[2] 2)note
A10	EXT_MCLK	I	MODE	External Clock
K2	BBMODE	I	MODE	DSP or BASEBAND Mode Selection
K3	TEST0	I	MODE	Digital Part Test Mode Selection
N4	RESET_N	I	RESET	SYSTEM RESET IN
A9	XTAL P	I	CLOCK	Crystal Positive
B9	XTAL N	I	CLOCK	Crystal Negative
L3	STDO	I	MODE	Standard Mode0
M3	STD1	I	MODE	Standard Mode1
P13	AWAKE	I	MODE	AWAKE
R15	NC	-	-	Reserved for future use
N2	JTAG_TDO	IO	JTAG	DSP Debug Serial Instruction/Data Shift Output Port
N3	JTAG_TRS	IO	JTAG	DSP Debug Active Low Input Port
M1	JTAG_TDI	IO	JTAG	DSP Debug Serial Instruction/Data Shift Input Port
N1	JTAG_TMS	IO	JTAG	DSP Debug TAP Controller Port
M2	JTAG_TCK	IO	JTAG	DSP Debug Clock Port

Please refer to details for detail mode selection in section 6.2.

Note:

1) BMODE[0] = 1 → System clock Input = 24.576MHz or BMODE[0] = 0 → System clock Input = 23.52Mhz

2) BMODE[2:1] = [1][0] → Booting From Serial Flash Memory BMODE[2:1] = [1][1] → Waiting for UART Download

BMODE[2:1] = [0][1] --> SPI Bridge Enabled between SPIM0 and SPIS1. So, Host can access Serial flash directly.(TBD)

- Reserved Pins (TBD)

Pin	Symbol	Type	Function	Description
A1, A2, A4, A5 A6, A7, B4 B5, B6, B7, C1 C7, D3, E3, E1 E2, F2, G1 G2, H2	NC	-	-	Reserved for future use

- Analog Power Pins (TBD)

Pin	Symbol	Type	Function	Description
A8, B2, B8, C8, C2, C4, F3	NC	AP	POWER	Reserved for future use
C3	VDD12	AP	POWER	Analog Part Power Supply
A3, B1, B3, C5, C6, C9, D1, D2, F1, G3, H1, H3, J1, J2, J3	VSSA	AP	POWER	Analog Part Ground

- Digital Power Pins

Pin	Symbol	Type	Function	Description
F14, F15, K6, L6, K10, L10, N8, P8, M13, M14, N13	VDDI	DP	POWER	Digital Power supply voltage for Core
C12, C13, N5, N6, N10, N11	VDDE	DP	POWER	Digital Power supply voltage for I/O & SDRAM
F13	VDDPLL	DP	POWER	Digital Power supply voltage for PLL
B10, C10, E6, E7, E8, E9, E10, F6, F7, F8, F9, F10 ,G6, G7, G8, G9, G10, H6, H7, H8, H9, H10, J6, J7, J8, J9, J10, K7, K8, K9, L7, L8, L9, M15, N7, N9, N12	VSS	DG	POWER	Ground.

4. Functional Description

This chapter describes PN3034HT internal structure, components and interfaces as shown in figure 4-1. The algorithms and architectures used in the PN3034HT have been efficiently optimized in order to minimize hardware and chip area.

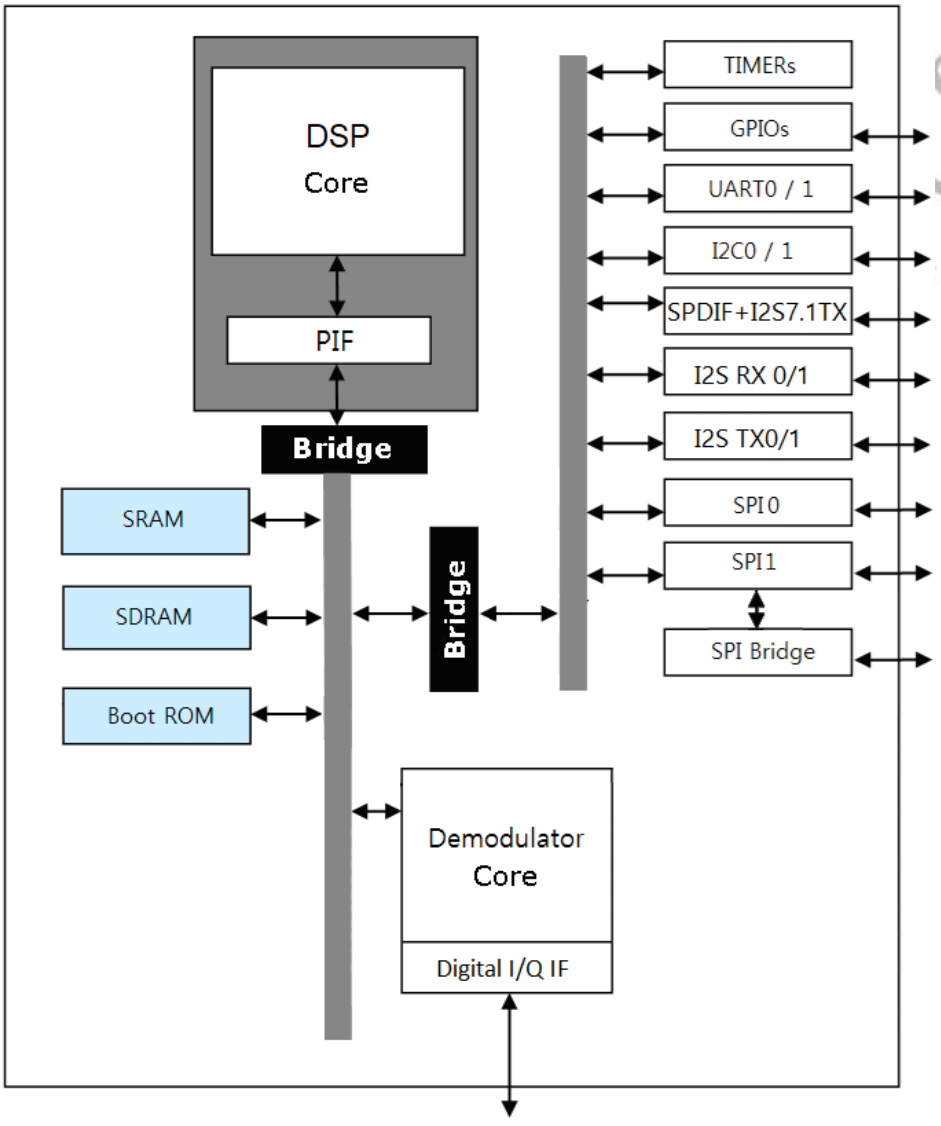


Figure 4-1 Functional Block Diagram

4.1 General Functions

The following is a total feature list and is spread over multiple commercial releases.
The initial releases will not include all of these simultaneously.

- ❑ Support for HD Radio™ IBOC system
- ❑ High-performance 32Bits DSP Core with 24-bits Audio processing
- ❑ Advanced 10 x 10 mm^2, 0.65 mm pitch, 179-pins Fine pitch BGA technology.

4.2 DSP Functions

- ❑ Based on standard 32-bits RISC architecture with integrated 24-bits audio processing instructions
- ❑ Industry-leading low-power consumption and Dual MACs
- ❑ Predictive pre-fetch cache memory subsystem for improvement of high density memory latency
- ❑ Ultra-low power consumption increases battery life in portable applications
- ❑ Full 24-bits internal audio resolution throughout delivers extremely high quality audio output

4.3 HD Radio™ Functions

- Standards support IBOC system for HD Radio™
- Up to 3 IBOC demodulator support
- Additional back ground scanning support for HD Radio™ signals
- Fully compatible with "RX_IDD_2206" HD Radio™ Commercial Receiver Baseband Processor Command and Data Interface Definition and CDM4
- Outstanding Mobility and 1st Adjacent Channel Rejection Performance
- IBOC FM mode supported: MP1, MP2, MP3, MP5, MP6, (optional) MP11
- Supplemental Program Services(SPS) in MP1, MP2, MP3, MP5, MP6 in FM mode
- IBOC AM mode supported: MA1, MA3
- Support AM reduced digital bandwidth broadcasting configuration with audio BW management.
- Automatic Audio (Time) Alignment of Analog and Digital signal on audio instance only (Requires analog audio as an input to the baseband)
- Automatic Audio (Level) Alignment of Analog and Digital signal on audio instance only (Requires analog audio as an input to the baseband)
- Fast SPS to MPS switching and Data Functionality
- Service support: SIS(+), AAS data, SIG, On-chip LOT, On-chip PSD decoding, On-chip Tagging

4.4 Tuner Interface Functions

- 3 x Digital I/Q interfaces support for External Tuner connection
- FM Sample Rate supported – 912KHz/882KHz/744KHz/675KHz/650KHz
- AM Sample Rate supported - 912KHz/882KHz/744KHz/675KHz/650KHz/55.1KHz, 46.5KHz
- Support Split mode, Multiplexed mode, Analog/Digital mode, MSB bit shift mode
- Software and hardware switching of sample rates supported

4.5 Diversity Functions

- MRC Diversity support for IBOC FM
- Better C/N performance and seamless switching between master and slave tuner

4.6 PLL Functions

- Input Frequency: 24.576MHz
- Output Frequency: 37.5MHz~600MHz

4.7 I^2S TX Functions

- 2 x Master or Slave I^2S interface.
- Programmable clock generation (I^2S master/slave mode, MCLK, BCLK, LRCK).
- Programmable data width (up to 32-bits).
- Sample rate converter supporting for externally provided clock in slave mode.

4.8 I^2S 7.1 Channel Functions

- 1 x Master or Slave I^2S 7.1ch interface.
- Programmable clock generation (I^2S master/slave mode, MCLK, BCLK, LRCK).
- Programmable data width (up to 32-bits).
- 1-pair I^2S with TDM mode (DSP MODE)

4.9 SPDIF Functions

- 1 x SPDIF interface for Stereo channel audio PCM.
- Fixed sample rate output for 44.1KHz sample rate audio

4.10 I^2S RX Functions

- 2 x Slave I^2S RX interface.
- Programmable clock generation (I2S master mode, BCLK, LRCK).
- Programmable data width (up to 32-bits).
- Sample rate converter supporting for externally provided clock in slave mode.

4.11 I^2C Functions

- Support 2 x channels I^2C
- Detect/generate Start and Stop events
- Identify its slave (ID) address (in Slave mode)
- Identify the transfer direction (receive/transmit)
- Transfer data byte-wise according to the SCL clock line
- Generate an ACK signal following a byte receive
- Inspect an ACK signal following a byte transmit
- Generate vectored interrupt for receive and transmit events and receive/transmit/bus error exceptions
- Generate the clock signal (in Master mode)

4.12 UART Functions

- Support 2 x UART interfaces and one of them supports HSUART mode
- Programmable Baud Rate Generator
- 5- to 8-bits full-duplex asynchronous serial communication.
- Parity generation and error detection
- HUART mode supports communication at up to 115,200 bps x2 and 115,200 bps x8 (TBD)
- UART mode supports communication at up to 115,200 bps

4.13 SPI Functions

- 2 x Master /Slave Serial Peripheral Bus Interface
- 8- or 16-bits Programmable Data Length Per Chip Select
- Programmable Phase and Polarity Per Chip Select (master mode)
- Communication at up to main (clock/2) bps (slave), main (clock/2) bps(master mode)

4.14 SPI Bridge Functions

- Host can program the serial flash directly through SPI interface by using SPI bridge feature. (TBD)

5. Peripheral Descriptions

5.1 I²C Interface

The I²C is a standard 2 wire serial interface used to connect the acacia with I²C device or host. I²C bus application includes EEPROM, LCD, host controllers. The I²C interface is able to:

- Detect/generate Start and Stop events
- Identify its slave (ID) address (in Slave mode)
- Identify the transfer direction (receive/transmit)
- Transfer data byte-wise according to the SCL clock line
- Generate an ACK signal following a byte receive
- Inspect an ACK signal following a byte transmit
- Generate vectored interrupt for receive and transmit events and receive/transmit/bus error exceptions
- Generate the clock signal (in Master mode)

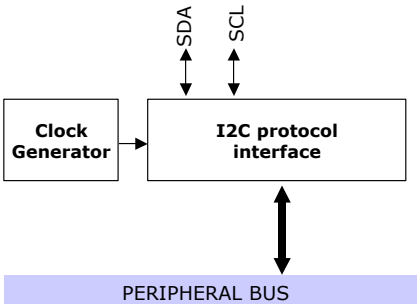


Figure 5-1 I²C Block Diagram

5.2 SPI Interface

The SPI makes a serial communication with external through SPM_CLK, SPM_CSN, SPM_DI, SPM_DO pin. The SPM_CLK is clock for the serial communication, SPM_CSN are chip enable signals, SPM_DI is serial data-in, and SPM_DO is serial data-out.

The SPM Master communicates in unit of 8-bits character. If CPU writes the contents to communicate to command register, SPI Master executes communication for command register and then clears the VALID bit in command register with 0 and stops operation. That is, always when CPU sends command through command register, SPI Master does its operations.

The SPI communicates in specified unit of character and the length of character, which is possible from 1-bit to 16-bits, is defined by setting of register.

The SPI operation modes are DMA mode and non-DMA mode. The DMA mode is used to transfer large data through SPI, it reduces interrupt's occurrence to CPU. In Non-DMA mode, each finish of 1-character transfer makes interrupt to CPU.

5.2.1 Characteristics SPI Bus

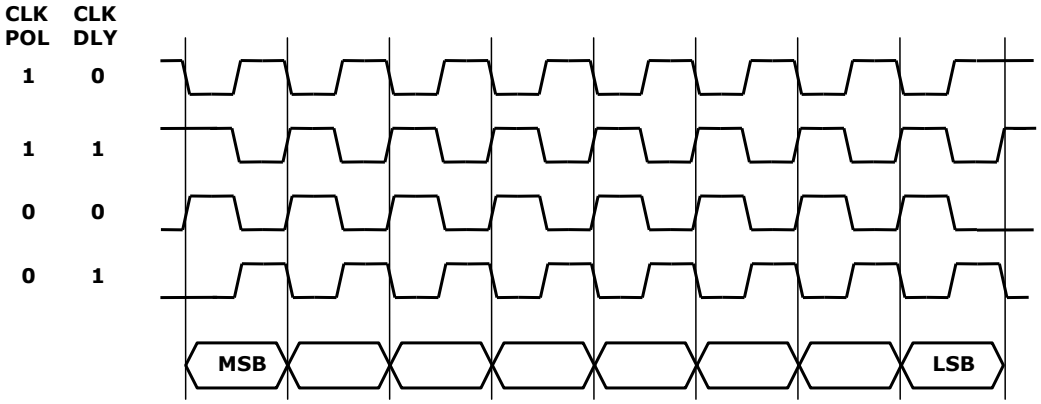


Figure 5-5 SPI Clock Polarity

5.2.2 SPI Timing Diagram

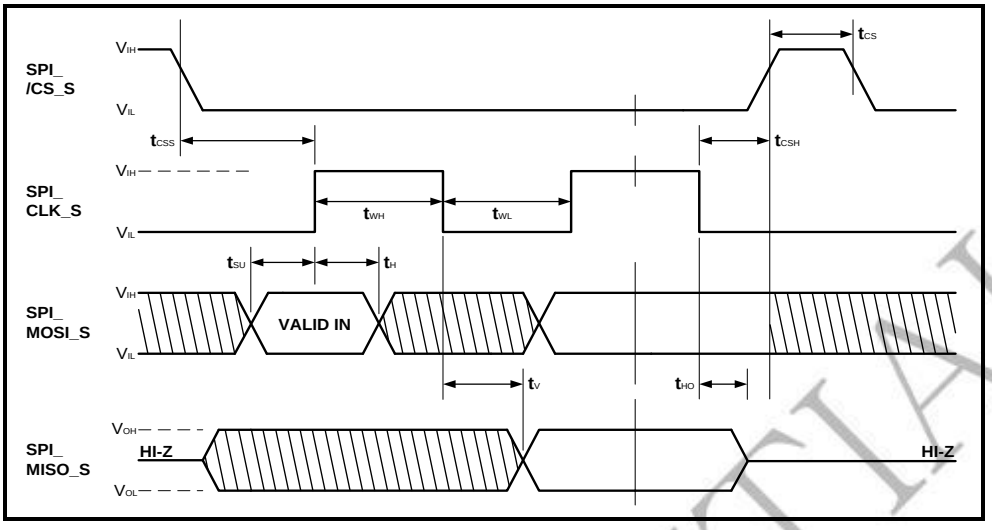


Figure 5-6 SPI Timing Diagram

5.2.3 SPI Timing Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{CLKF} f_{CLKN} f_{CLKS}	CLK Clock Frequency	Normal Mode Standby Mode	0 0	- -	Fbus/2 Fbus/2	MHz MHz
t_{CS}	Minimum CS High Time		CYC bus * 5	-	-	ns
t_{CSS}	CS Setup Time		CYC bus * 2	-	-	ns
t_{CSH}	CS Hold Time		CYC bus * 2	-	-	ns
t_{WH}	SCK High Time		CYC bus * 1	-	-	ns
t_{WL}	SCK Low Time		CYC bus * 1	-	-	ns
t_{SU}	Data In Setup Time		10	-	-	ns
t_{H}	Data In Hold Time		10	-	-	ns
t_{V}	Data Time		0		20	ns
t_{HD}	Hold Setup Time		0	0	0	ns

Table 5-1 SPI Timing

* Fbus = Bus Frequency, CYC bus = 1 clock cycle time of Bus Clock
* PN3034HT's Bus Frequency ≒ 190MHz(TBD) in Reference Firmware.

5.3 UART & HSUART Interface

The UART (Universal Asynchronous Receiver/Transmitter) core and HSUART (High Speed Universal Asynchronous Receiver/Transmitter) core provides serial communication capabilities, which allow communication with modem or other external devices, like another computer using a serial cable and RS232 protocol. This core is designed to be maximally compatible with the industry standard National Semiconductors' 16550A device. The UART core implements the AMBA bus interface for communication with the system. It has an 8-bits data bus for compatibility reason. The core requires one interrupt. It requires 2 pads in the chip (serial in and serial out) and, optionally, another six modem control signals, which can otherwise be implemented using general purpose I/Os on the chip.

5.4 *I²S TX Interface*

- I²S TX is peripheral which delivers audio data to DAC and it supports DMA mode. DMA reduces interrupt frequency to DSP core as a result DMA increases whole chip operation efficiency.

- In slave mode, I²S TX receives the signal BCLK, LRCK from outside device possibly codec/DAC.

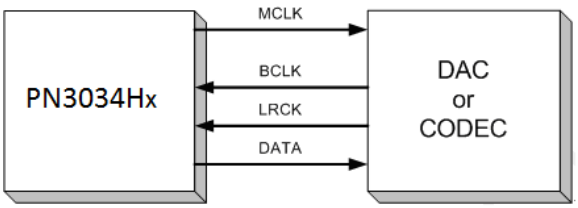


Figure 5-8 I²S Slave Mode = DAC Master Mode

- In master mode, divided DSP core clock signals are delivered to outside device as MCLK, BCLK, and LRCK.

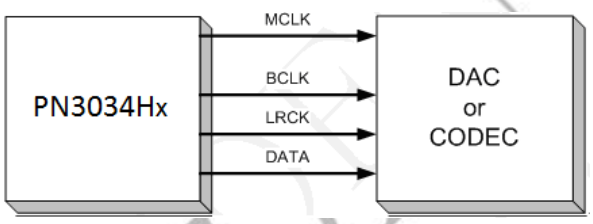


Figure 5-9 I²S Master Mode = DAC Slave Mode

In the block diagram below, signal name which is ended with "_S" are supplied by outside device in slave mode. Signal name which is ended with _M are drive outside device in master mode. MCLK does not exist in I²S specification but generally used by commercially available CODEC/DAC as main clock to support specific sampling frequency.

BCLK is serial clock and LRCK is word select signal.

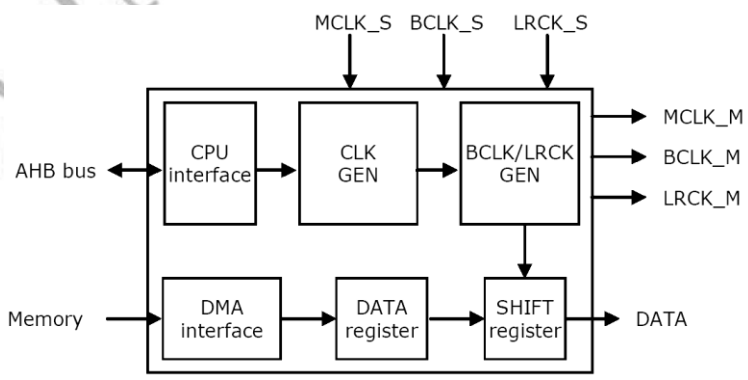


Figure 5-10 I²S Interface Block Diagram

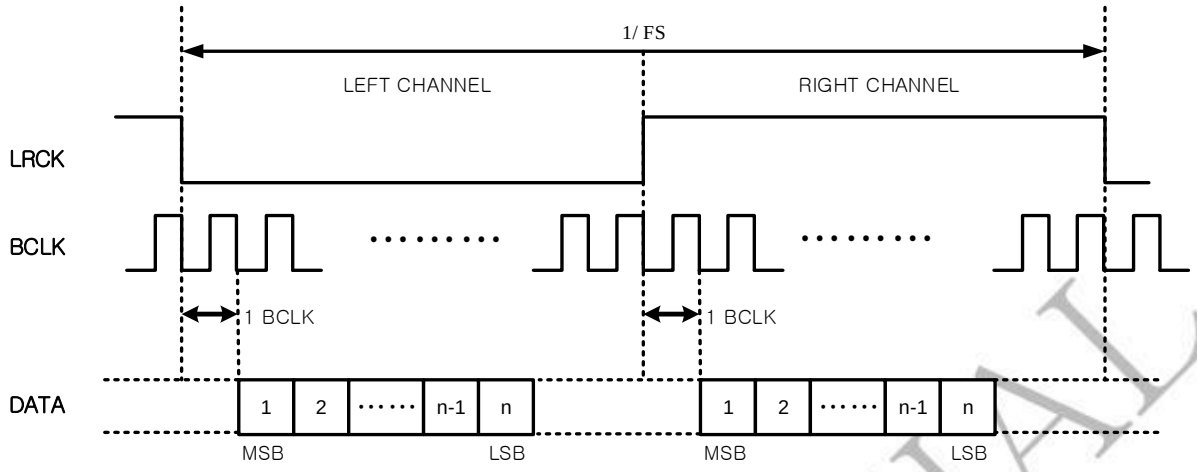


Figure 5-11 I²S Timing Diagram

- The MSB is available on the 2nd rising edge of BCLK following a DATA transition.

Sample Rate Frequency	LRCK	BCLK	Valid Data Bit Number (n) *1)	MCLK	MODE
44.1KHz	44.1KHz	1.4112MHz	16-bits	-	-

Table 5-2 Sample Rate Frequency Table

Note

1) The number of all data in each channel is 16-bits. (TBD)

5.5 I²S RX Interface

- I²S RX is peripheral which delivers audio data from outside of chip and it support DMA. DMA reduce interrupt frequency to DSP core as a result DMA increase whole chip operation efficiency.

- Clock signals and data are delivered to outside device as BCLK, LRCK and DATA.

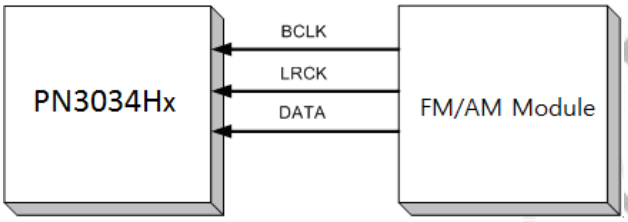


Figure 5-12 I²S RX Mode

Please refer to below block diagram.

In the block diagram below, signal name which is ended with "_S" are supplied by outside device

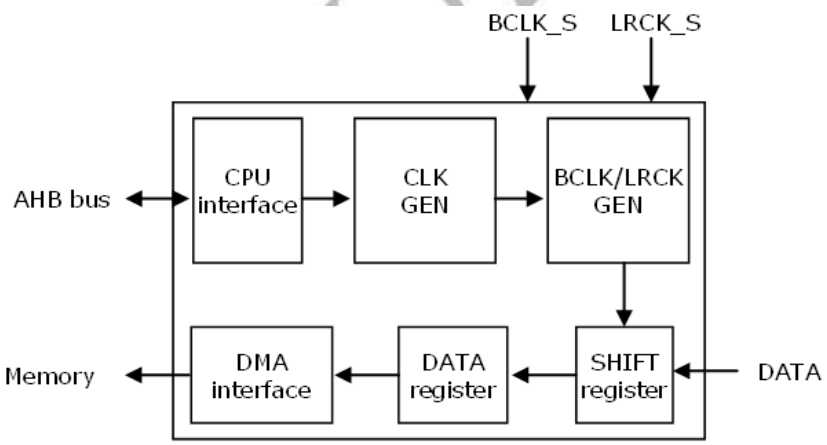


Figure 5-13 I²S RX Interface Block Diagram

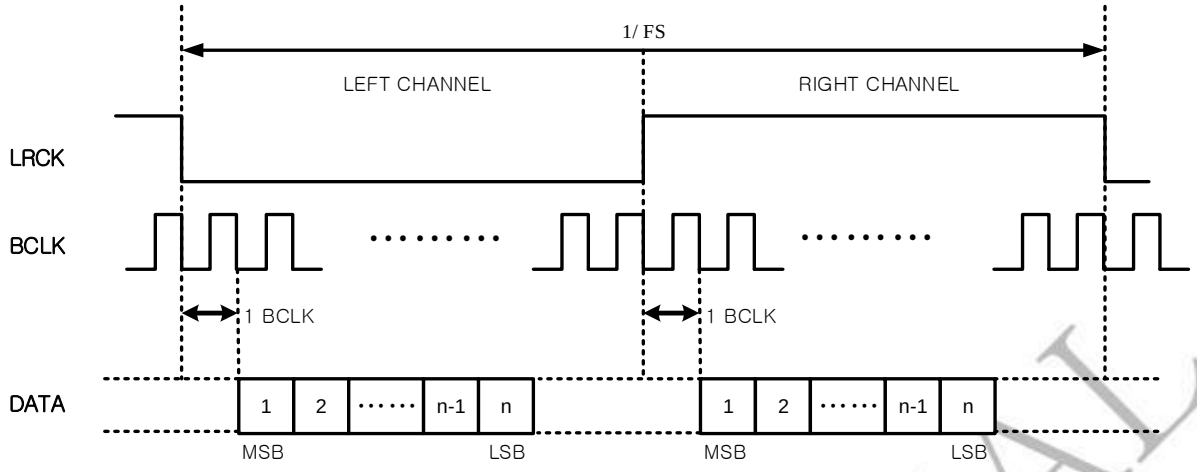


Figure 5-14 I²S RX Timing Diagram

- The MSB is available on the 2nd rising edge of BCLK following a DATA transition.

Sample Rate Frequency	LRCK	BCLK	Valid Data Bit Number (n) *2)	MODE
24KHz	24KHz	1.536MHz	16-bits	I²S RX mode1)
32KHz	32KHz	2.048MHz	16-bits	
44.1KHz	44.1KHz	2.8224MHz	16-bits	
48KHz	48KHz	3.072MHz	16-bits	

Table 5-3 Sample Rate Frequency Table

Note

1) PN3034HT has sample rate conversion function in I²S RX mode.

2) The number of all data is 32-bits and 16-bits will be valid in I²S RX's data.

5.6 Digital I/Q Interface

- Digital I/Q Interface is peripheral which delivers RF tuner's I & Q data from outside of chip and it support DMA. DMA reduces interrupt frequency to DSP core as a result DMA increases whole chip operation efficiency.

- Clock signals and data are delivered to outside device as BCLK, LRCK and Serial Data-I / Serial Data Data-Q

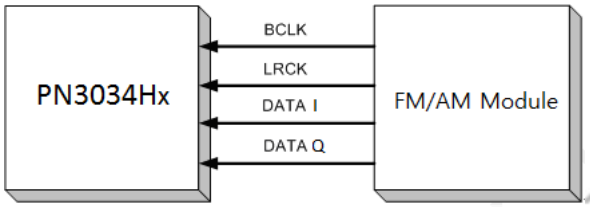


Figure 5-12 Digital I/Q Mode

- Support Split mode and Multiplexed mode in below.

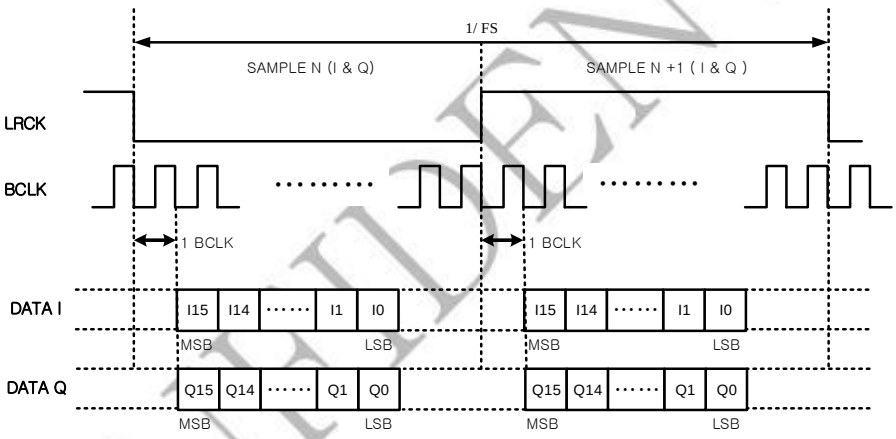


Figure 5-14 Digital I/Q Split mode Timing Diagram

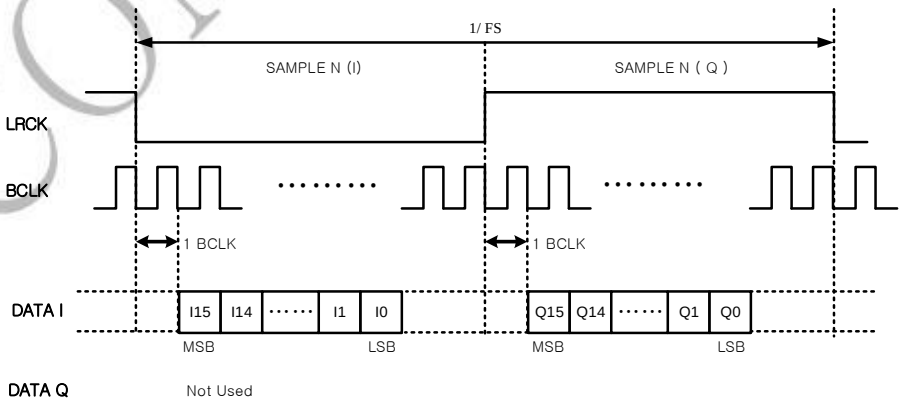


Figure 5-15 Digital I/Q Multiplexed mode Timing Diagram

6. Application

6.1 Clock application

– *Crystal Oscillator*

PN3034HT has an oscillation circuit and PLL. It can generate the Master clock by connecting to a crystal oscillator, a capacitor and a fixed resistor as shown in the circuit diagram below.

It is recommended to use a crystal oscillator with a maximum frequency tolerance of ±50ppm.

Please contact the manufacturer of the crystal oscillator for the appropriate values of the load capacitors and resistors. PN3034HT input clock support 24.576MHz or 23.52Mhz.

6.2 Operation Mode Selection

– BMODE[0] (Pin L2)

BMODE[0] = {1} : System clock input from Crystal Oscillator is 24.576Mhz

BMODE[0] = {0} : System clock input from Crystal Oscillator is 23.52Mhz

– BMODE[1:2] (Pin K1 & Pin L1)

BMODE [1][2] = {0 , 1} : Normal system booting mode with firmware in serial flash.

BMODE [1][2] = {1 , 1} : Firmware program mode into serial flash via UART downloading

BMODE [1][2] = {1 , 0} : SPI bridge mode between SPM0 and NSPI0. Host can directly access to serial flash

– AWAKE (R15) –TBD-

This pin should be controlled to Low during normal system operation

– BBMODE & TEST0 (Pin K2 & K3)

This pin should be connected to ground [Low state] for normal system booting mode with DSP.

– STD[0:1] (Pin L3 & Pin M3)

STD0, STD1 = {0 , 0} : Default setting

STD0, STD1 = {1 , 0} : Reserved for future use

STD0, STD1 = {0 , 1} : Reserved for future use

STD0, STD1 = {1 , 1} : Reserved for future use

7. Electrical Characteristics

7.1 Absolute Maximum Rating

Operating the PN3034HT under conditions that exceed those listed in Table 9-1 may result in damage to the device. Absolute maximum ratings are limiting values and are considered individually, while all other parameters are within their specified operating ranges. Functional operation of the PN3034HT device under any of the conditions listed in Table 9-1 is not implied. Exposure to absolute maximum ratings for extended periods of time may affect the device's reliability.

Symbol	Description	Value	Units
T_J	Junction temperature	-40 to +125	°C
V_{VDDI}	Core Supply Voltage	-0.5 to + 1.4	V
V_{VDDE}	I/O Supply Voltage	-0.5 to + 3.6	V
V_{VDDIO}	Analog Supply Voltage	-0.5 to + 3.6	V
V_{VDD12} V_{VDD12P}	Analog Core Supply Voltage	-0.5 to + 1.4	V

Table 9-1 Absolute Maximum Ratings (TBD)

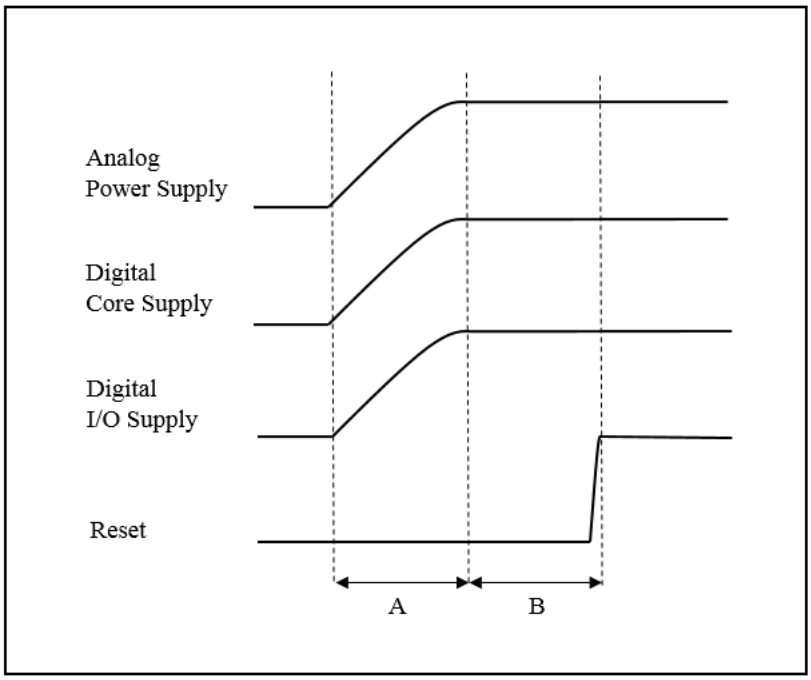
7.2 Recommended operating conditions

Symbol	Description	Min	Max	Units
T_{op}	Operation Temperature	-40	+85	°C
T_{STG}	Storage Temperature	-50	+150	°C
V_{VDDI}	Core Supply Voltage	0.99	1.21	V
V_{VDDE}	I/O Supply Voltage	2.7	3.3	V
V_{IH}	High Level Input voltage at I/O	0.7 * V_{VDDE}	V_{VDDE} +0.3	V
V_{IL}	Low Level Input voltage at I/O	V_{VDDE} -0.3	0.3 * V_{VDDE}	V
V_{HYS}	Input Hysteresis Voltage	0.4	-	V
V_{VDD12} V_{VDD12P}	Analog Core Supply Voltage (TBD)	-	-	V
V_{VDD}	Analog Supply Voltage	2.7	3.3	V

Table 9-2 Recommended Ratings (TBD)

7.3 Power-on and Reset Timing

Please refer to timing chart and table for proper power-on and IC reset.



Characteristic	Symbol	Min	Max	Unit
Power Supply Sequence	A	Don't Care	-	µs
Setup time for IC Reset	B	500		µs

Table 9-3 Power-On and Reset Timing (TBD)

7.4 Power Consumption

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{VDD12-ALL}$	Supply Current for Core	$V_{VDD12ALL}$ = 1.2V Triple HD Mode	-	420	-	mA
I_{VDDE}	Supply Current for IO	V_{VDDE} = 3.0V Triple HD Mode	-	37	-	mA
I_{VDD12_A}	Supply Current for Analog	V_{VDD12_A} =1.2V Triple HD Mode	-	5	-	mA
P_{TPOW}	Total Power Consumption	Triple HD Mode	-	630	-	mW

Table 9-4 Power Consumption (TBD)

8. *Package Dimension*

- The Package dimension of PN3034HT

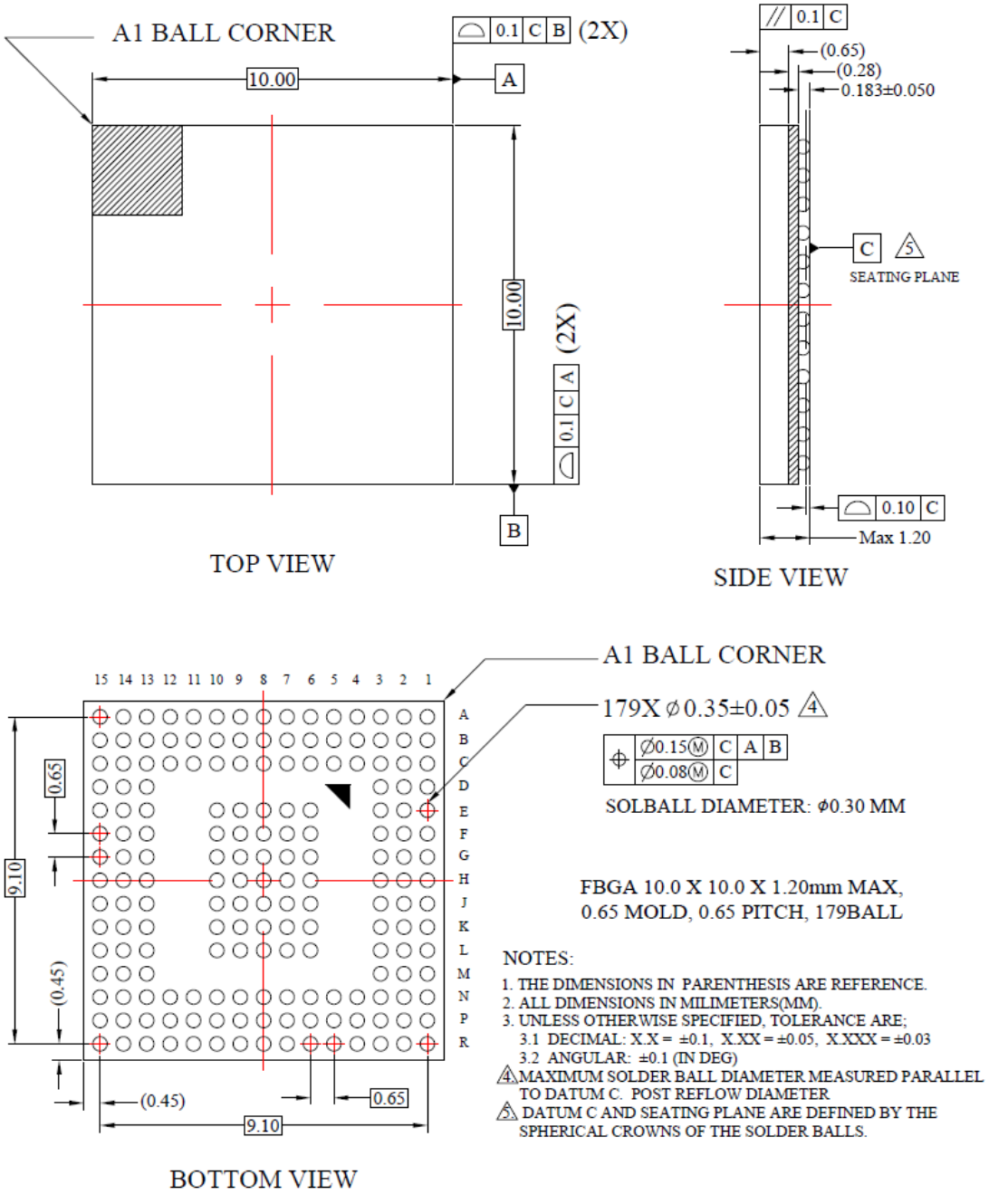


Figure 11.1 PN3034HT Package Dimension

9. PCB Mounting Guidelines

Guidelines for mounting the PN3034HT onto a printed circuit board (PCB) are presented in this part, including land pad and handling, SMT Process.

9.1 Handling

Floor life time will be modified by environmental conditions other than 30'C/60%RH. If partial lots are used, the remaining SMD packages must be resealed or placed in safe storage within one hour of bag opening.

Refer to JEDEC spec (J-STD-033B) for details

Level	Floor life (out of bag) at factory Ambient 30'C/60%RH or as started
2	1 year
2a	4 weeks
3	168 hours
4	72 hours

Table 12 -2 Moisture classification level and floor life

9.2 DRYING

Component drying options for various moisture sensitivity levels and ambient humidity exposures of £≤ 60% RH are given in the following tables. Drying per an allowable option resets the floor life clock. If dried and sealed in an MBB with fresh desiccant, the shelf life is reset. Table 12-3 gives conditions for re-bake of SMD packages at a user site after the floor life has expired or other conditions have occurred to indicate excess moisture exposure.

PN3034HT condition: **Leve3, 9 hours, Bake @125℃**

Package Body Thickness	**Level**	**Bake @ 125°C**		**Bake @ 90°C ≤ 5% RH**		**Bake @ 40° C ≤ 5% RH**	
		Exceeding Floor Life by >72 hours	Exceeding Floor Life by ≤ 72 hours	Exceeding Floor Life by >72 hours	Exceeding Floor Life by ≤ 72 hours	Exceeding Floor Life by >72 hours	Exceeding Floor Life by ≤ 72 hours
≤ 1.4mm	2						
	2a	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	3	**9 hours**	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days

Table 12 -3 Reference Conditions for Drying Mounted or Un-mounted SMD Packages

9.3 SMT Process

- Screen print process

1. Type3 or type4 is recommended for solder paste.
2. No clean flux is recommended for lead-free condition.

- Component placement

Standard pick-and-place machines can be used for placing a package. The following methods can be used for recognition and positioning

1. Use ball inspection and compliant tip nozzle
2. It is recommended that the side-lighting option on pick and place machine
3. It is preferable to use IC placement/ fine pitch placement machines over chip-shooters for better accuracy.
4. Solder ball self-align when placed at an offset due to self-centering nature of it.
5. Little or no force needs to be exerted during placement to prevent damage to a part.
   It is recommended that balls be dipped into solder paste on PCB to greater than 20% of paste block height.

- Reflow and cleaning

1. Compatible with industry standard reflow process for both lead-free process.
2. Qualified for up to three reflow operation (260˚C peak) per J-STD-020.
3. Nitrogen gas is recommended (oxygen level<75ppm) to avoid oxidation or void formation.
4. Reflow profile depends on whole parts and board density.
5. Follow recommended recipe from paste manufacturer for reflow profile.

- Rework

The key features for rework are listed below.

1. Rework procedure used is identical to the one used for most BGA packages.
2. Rework reflow process should duplicate original reflow profile used for assembly.
3. Rework system should include localized convection heating element with profiling capacity, a bottom side pre-heater and a part pick and placer with image overlay.

9.4 The temperature profile of a reflow process

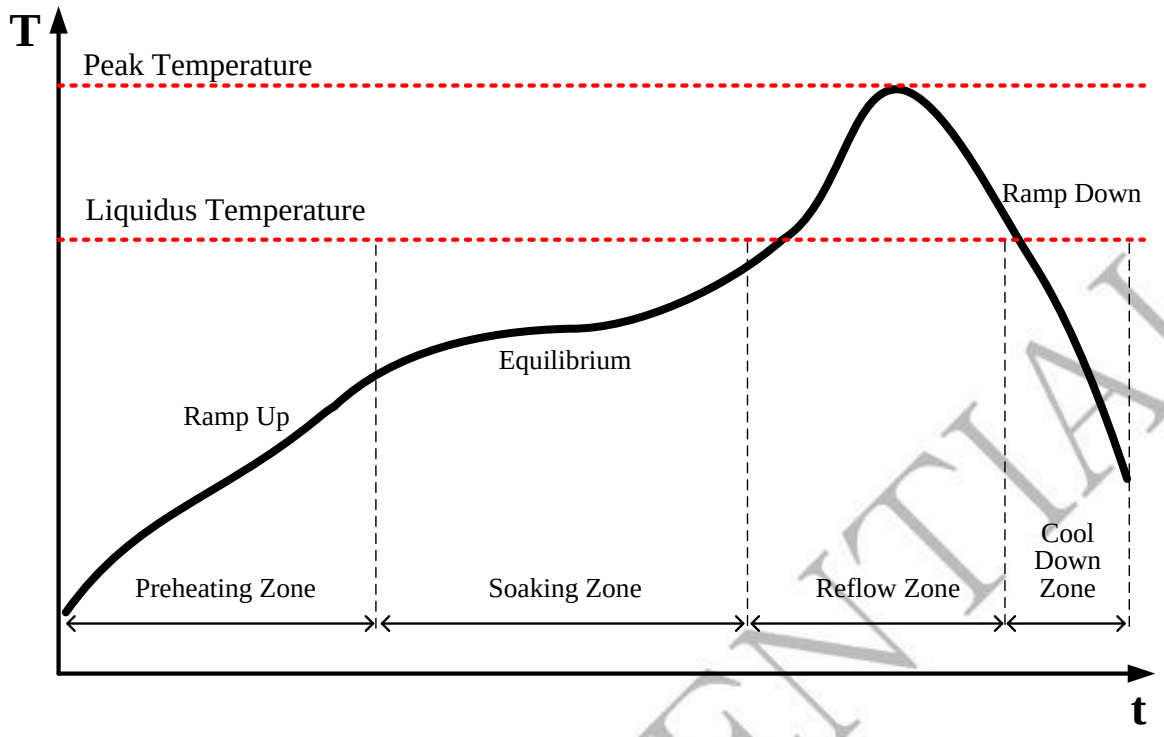


Figure 12-3 The temperature profile of a reflow process

Parameter	Tin-lead Alloy (SnPb or SnPbAg)	Lead-free Alloy (SnAgCu)	Main Requirements From
Preheating rate	2.5℃/sec	**2.5℃/sec**	Flux system(Solder paste)
Soaking temperature	140 ~ 170℃	**140 ~ 170℃**	Flux system(Solder paste)
Soaking time	80 second	**80 second**	Flux system(Solder paste)
Peak temperature	225℃	**245℃ ～ 260℃**	Alloy(Solder paste)
Reflow time over Liquidus	60 second	**60 or 90 second**	Alloy(Solder paste)
Liquidus temperature		**217℃or 219℃**	
Cool Down rate	2.5℃/sec	**2.5℃/sec**	

Table 12-4 The temperature profile of a reflow process

10. Part Materials

10.1 Package Materials

- The Package Materials of PN3034HT

Line	Description	Image
1st	Company logo	
2nd	Device name*1	
3rd	Application name*2	
4th	Chip revision	
5th	Manufacturing date (KYYWW)*3	
6th (vertical)	Assembly lot number(CYWWPPTTT)*4	

*1 Device name : PN3034HT

*2 Application name : HD Radio SoC

*3 Manufacturing date : KYYWW

- K : Site
- YYWW : Date code

*4 Assembly lot number : CYWWPPTTT

- C : Customer code
- Y : Years
- WW : Week
- PP : Package code
- TTT : Serial No.

Table 10-1 Marking Information: PN3034HT

PnpNetwork Technologies, Inc.
www.pnpnetworkwork.com
support@pnpnetwork.com
T : 82-2-2240-0800
3F, Fine Venture BLD, 41 , Seongnamdearo 925beon-gil, Bundang-gu, Seongnam-si, Gyeonggi-do, Korea 13496