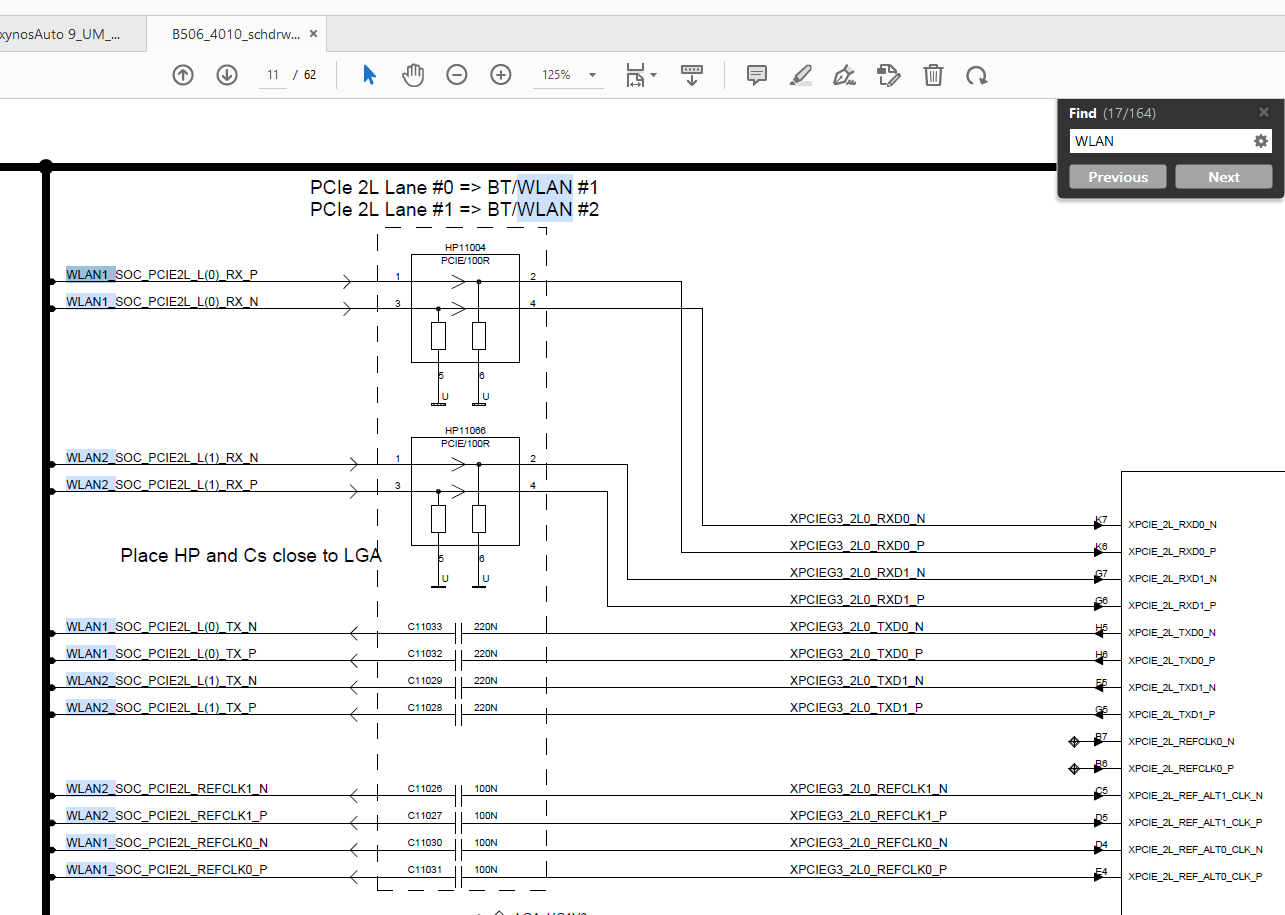
B2 hardware schematic screenshot: -



TRM of V920 SOC: -

Chart, treemap chart

Description automatically generated

Graphical user interface, text, application, email

Description automatically generated

Hi..I looked into V920 TRM document what we are having. We could see that PCIe pins of SOC with WLAN1 and WLAN2 chips are as below.

PCIe pins for WLAN1: -

XPCIE\_2L\_RXD0\_N

XPCIE\_2L\_RXD0\_P

XPCIE\_2L\_TXD0\_N

XPCIE\_2L\_TXD0\_P

XPCIE\_2L\_REF\_ALT0\_CLK\_N

XPCIE\_2L\_REF\_ALT0\_CLK\_P

XPCIE\_PERSTN2

XPCIE\_CLKREQ2

PCIe pins for WLAN2: -

XPCIE\_2L\_RXD1\_N

XPCIE\_2L\_RXD1\_P

XPCIE\_2L\_TXD1\_N

XPCIE\_2L\_TXD1\_P

XPCIE\_2L\_REF\_ALT1\_CLK\_N

XPCIE\_2L\_REF\_ALT1\_CLK\_P

XPCIE\_PERSTN3

XPCIE\_CLKREQ3

I could see Ball-Map description is there only in Page - 154 of TRM.

While looking into "PCI Express: Register Description" chapter of TRM, section : 28.5.3 PCIe\_GEN3 2 Lane Link.

I could see Base addresses as below -

PCIe\_GEN3\_2L0 Link Base address : 0x1300\_0000

PCIe\_GEN3\_2L1 Link Base address : 0x1500\_0000

But when I see target or .dtsi file then Base addresses observed is as below: -

For WALN1: PCIe port - pcie\_2: pcie@161C0000

For WALN2: PCIe port - pcie\_3: pcie@161C1000

So, with available information/document, we are unable to map PCIe pins with PCIe port and its base addresses.