# PCIe enumeration in-stability issue in IDCEvo: -

Contents

[PCIe enumeration in-stability issue in IDCEvo: - 1](#_Toc141699844)

[1. Block Diagram showing Power-On-GPIO and Reset signals : - 2](#_Toc141699845)

[2. Power-On-GPIO becoming high after PERST# is releasing, which is not correct: - 2](#_Toc141699846)

[3. Power sequence time diagram as per PCIe specification: - 3](#_Toc141699847)

[4. Correction in power-up sequence with our patch: - 4](#_Toc141699848)

[5. Result: - 4](#_Toc141699849)

## Block Diagram showing Power-On-GPIO and Reset signals : -

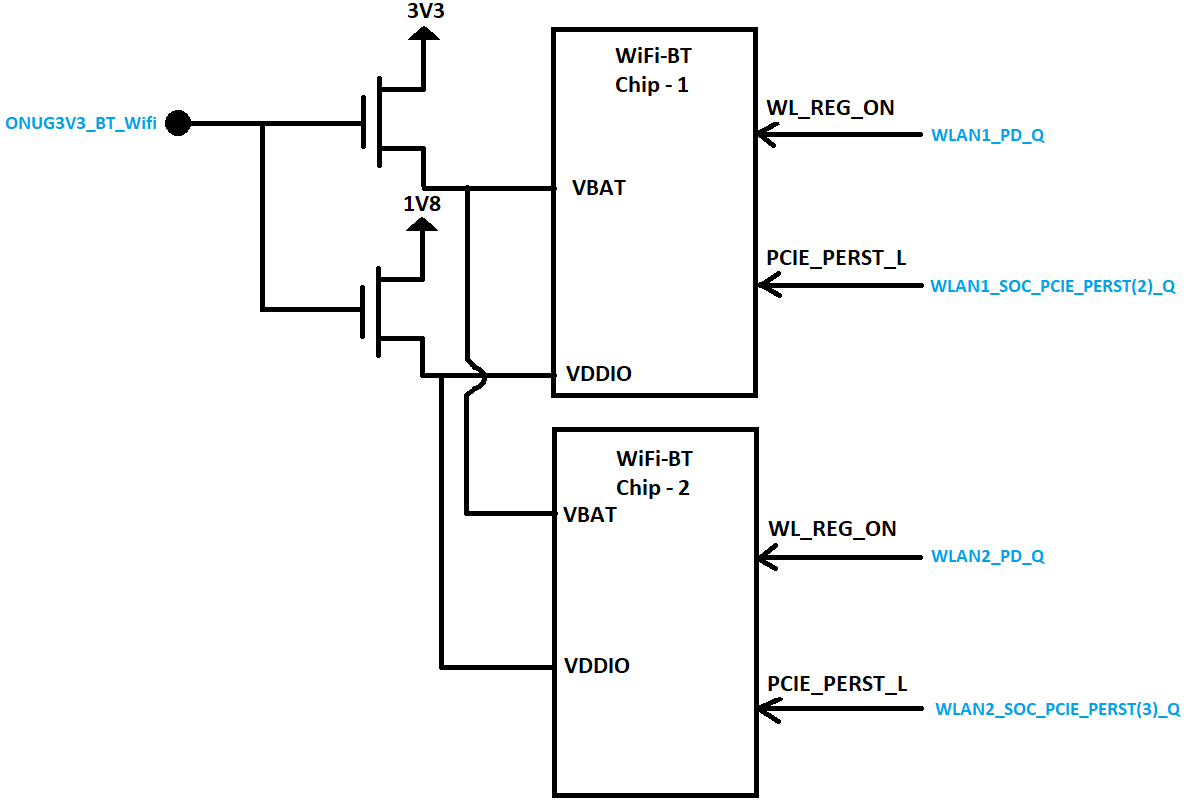


Figure – 1

## Power-On-GPIO becoming high after PERST# is releasing, which is not correct: -

A screen shot of a computer

Description automatically generated with low confidence

Figure – 2

Legend:

Yellow: ONUG3V3\_BT\_Wifi

Cyan: WLAN1\_SOC\_PCIE\_PERST(2)\_Q

Violet: WLAN1\_SOC\_PCIE\_CLKREQ(2)\_Q

Blue: WLAN1\_SOC\_PCIE2L\_REFCLK0\_P

The above waveform is not following PCIe compliance. Power to PCIe-Endpoint should become stable before release of PERST# signal.

Fix: - This we are correcting with a patch to Android-kernel repo, by asserting “ONUG3V3\_BT\_Wifi” signal in probe function of Exynos PCIe controller driver using “Pinctrl” select state.

## Power sequence time diagram as per PCIe specification: -

As per PCIe specification “PCI Express® Card Electromechanical Specification Revision 3.0 July 21, 2013”, page No – 30, the initial power up sequence should be as below.

Diagram of a diagram of a power stable

Description automatically generated

Figure - 3

Same we can see in WiFi chip (Cypress: CYW8x570 ) data sheet, page no - 86, Power to the chip should be stable before release of PERST# signal. It is shown below.

A diagram of a computer

Description automatically generated

Figure – 4

## Correction in power-up sequence with our patch: -

## 

A screen shot of a computer

Description automatically generated

Figure – 5

Legend:

Yellow: ONUG3V3\_BT\_Wifi

Green: WLAN1\_SOC\_PCIE\_PERST(2)\_Q

Blue: WLAN1\_SOC\_PCIE\_CLKREQ(2)\_Q

Violet: WLAN1\_SOC\_PCIE2L\_REFCLK0\_P

## Result: -

1. Power to Wifi chip is enabled about 11.54 seconds before release of PERST# signal.
2. PCIE\_CLKREQ signal goes to LOW about 6.26s after Power to WiFi chip is stable.

It follows PCIe Electromechanical specification and WiFi chip data sheet.