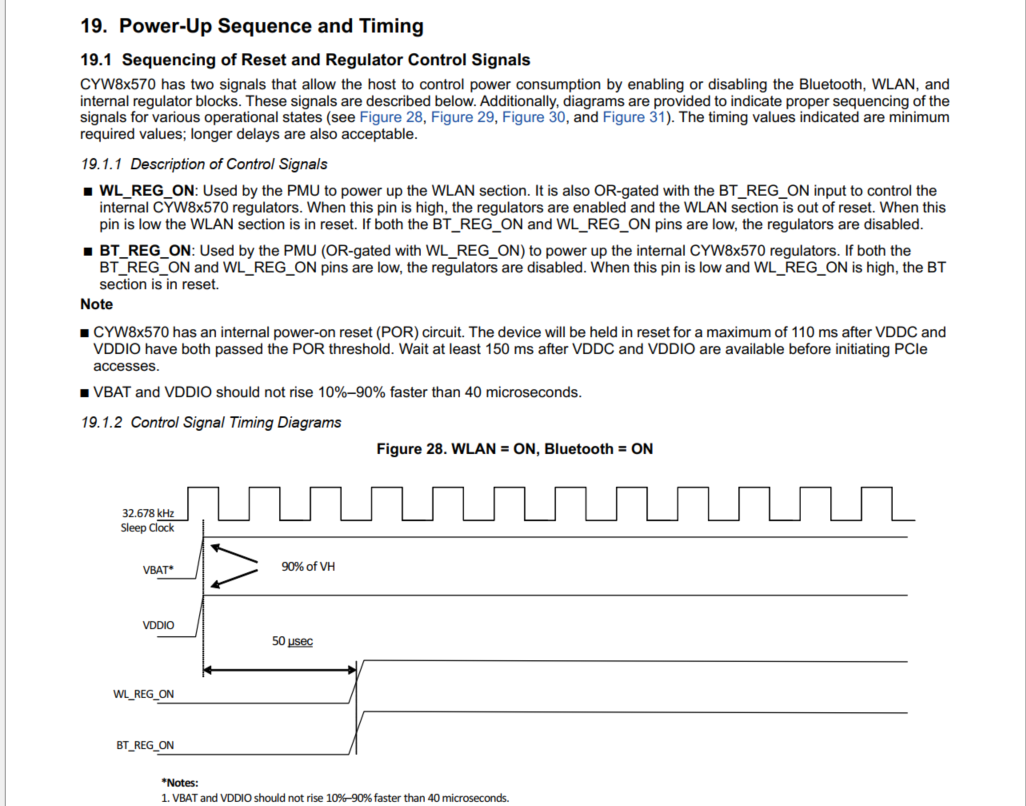
# WifI-BT chip Power sequencing: -

VBAT = 3.3V

VDDIO = 1.8V

Pg. 84 of datasheet: -



# PERST# signal: -

#PERST is a sideband signal used by the PCIe Host to indicate the PCIe devices, that the power and the reference-clock are stable.

**On RC side**

#PERST signal is generally asserted once the RC initialization (clocks init, phy init, controller init) is completed and is ready for link initialization.

**On EP Side**

Once the EP detects that the #PERST is asserted, it is an indication to EP that the RC provided power and clock are stable and EP side can start initialization on the device for PCIe linkup.

The below diagram clearly shows the usage of #PERST signal, where it is asserted once the power and reference clock are stable.

Diagram of a diagram of a power stable

Description automatically generated

Required waveform: -

# IDCEvo Waveform: -

