

The *device capabilities 2* register adds indication of completion timeout support and timeout ranges, with the *device control register 2* giving the ability to set the timeout or disable it. These ranges go from 50μs to 64s. The *device status register 2* is not used.

**Configuration space hex dump for WIFI chip: -**

00: be 12 31 bd 06 04 10 08 02 00 80 02 00 00 00 00

10: 04 00 80 60 00 00 00 00 04 00 00 60 00 00 00 00

20: 00 00 00 00 00 00 00 00 00 00 00 00 be 12 31 bd

30: 00 00 00 00 48 00 00 00 00 00 00 00 d7 01 00 00

40: 00 00 00 00 00 00 00 00 01 58 03 06 08 41 00 00

50: 00 00 00 00 00 00 00 00 05 68 8b 00 00 10 a0 b2

60: 00 00 00 00 01 00 00 00 09 a0 38 00 46 01 00 80

70: 00 30 10 18 00 00 00 00 00 00 00 00 00 00 00 00

80: 00 30 00 18 00 00 00 00 80 80 00 00 00 00 00 00

90: 04 00 00 00 00 01 00 00 00 00 00 00 00 00 00 00

a0: 11 ac 3f 00 00 80 00 00 00 88 00 00 10 00 02 00

b0: 82 8f 00 10 10 2c 11 00 12 dc 46 00 40 01 12 10

c0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

d0: 1f 08 08 00 00 04 00 00 06 00 00 00 01 00 00 00

e0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

f0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Capability Pointer : Offset – 34h

Capability pointer (offset 0x34) - 0x00000048

Next capability (offset 0x48) - 0x06035801 ( Capability ID - 0x01, Next Capability pointer - 0x58)

Next capability (offset 0x58) - 0x008b6805 ( Capability ID - 0x05, Next Capability pointer - 0x68)

Next capability (offset 0x68) - 0x0038a009 ( Capability ID - 0x09, Next Capability pointer - 0xa0)

Next capability (offset 0xa0) - 0x003fac11 ( Capability ID - 0x11, Next Capability pointer - 0xac)

Next capability (offset 0xac) - 0x00020010 (Capabilty ID – 0x10, Next Capability pointer – 0x00)

Now, we find the PCIe capability register (0x10), a next pointer (0x00, end of chain).

**Capabilty ID – 0x10 indicates PCI Express Capability ID: -**

A diagram of a device

Description automatically generated

Base address of “PCI Express Capability ID – 0x10) = 0xac

**“Device Capabilities 2” Register: -**

Offset of “Device Capabilities 2” Register = 0xac + 0x24 = 0xd0

Device Capabilities 2 Register = 0x0008081f

A diagram of a computer

Description automatically generated

Bit[0:3] = 1111b => Completion Timeout: Range ABCD

Bit[4] = 1 => **Completion Timeout Disable Supported**

**Completion Timeout Disable Supported** - A value of 1b indicates support for the Completion Timeout Disable mechanism.The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. This mechanism is optional for Root Ports.

**“Device Control 2” Register: -**

Offset of “Device Control 2” Register = 0xac + 0x28 = 0xd4

“Device Control 2” Register = 0x0400

A diagram of a device control system

Description automatically generated

Bit[0:3] = 0000b => Default range: 50 μs to 50 ms

Bit[4] = 0 => **Completion Timeout Disable** - When Set, this bit disables the Completion Timeout mechanism.

**Configuration space hex dump for Root port(0000:00:00.0): -**

00: 4d 14 ee ec 07 01 10 40 01 00 04 06 00 00 01 00

10: 00 00 00 00 00 00 00 00 00 01 ff 00 00 00 00 10

20: 00 00 00 00 01 00 01 00 00 00 00 00 00 00 00 00

30: 00 00 00 00 40 00 00 00 00 00 00 00 ff 01 00 00

40: 01 50 c3 db 00 00 00 00 00 00 00 00 00 00 00 00

50: 05 70 8a 01 00 00 00 00 00 00 00 00 00 00 00 00

60: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

70: 10 b0 42 00 23 80 00 00 10 21 1b 00 04 e8 73 00

80: 40 00 12 f0 00 00 00 00 c0 03 40 00 10 00 01 00

90: 00 00 00 00 1f 0c 01 00 00 00 00 00 1e 00 80 01

a0: 04 00 00 02 00 00 00 00 00 00 00 00 00 00 00 00

b0: 11 00 1f 00 05 00 00 00 05 00 01 00 00 00 00 00

c0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

d0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

e0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

f0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Capability Pointer : Offset – 34h

Capability pointer (offset 0x34) - 0x00000040

Next capability (offset 0x40) - 0xdbc35001 ( Capability ID - 0x01, Next Capability pointer - 0x50)

Next capability (offset 0x50) - 0x018a7005 ( Capability ID - 0x05, Next Capability pointer - 0x70)

Next capability (offset 0x70) - 0x0042b010 ( Capability ID - 0x10, Next Capability pointer - 0xb0)

Capability ID – 0x10 => PCIe Express Capability ID

Next capability (offset 0xb0) - 0x001f0011 ( Capability ID - 0x11, Next Capability pointer - 0x00)

Next pointer = 0x00 => end of chain

“**Device Capabilities 2” register: -**

Offset of “Device Capabilities 2” register = 0x70 + 0x24 = 0x94

Value at “Device Capabilities 2” register = 0x00010c1f

Bit[3:0] = 1111b => Completion Timeout: Range ABCD

Bit[4] = 1 => **Completion Timeout Disable Supported**

**“Device Control 2” Register: -**

Offset of “Device Control 2” Register = 0x70 + 0x28 = 0x98

“Device Control 2” Register = 0x0000

Bit[3:0] = 0000b => Default range: 50 μs to 50 ms

Bit[4] = 0b => Completion Timeout Not Disable

**Setpci: -**

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