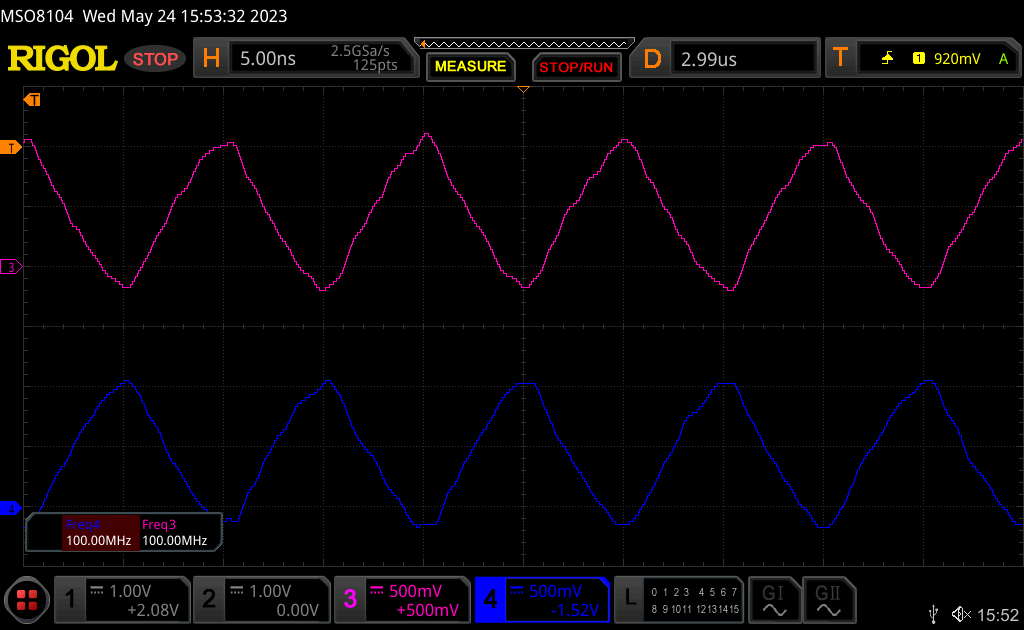
Target used for taking waveform: - B2-SP25-IDCEvo

Image flashed: - ES2 Artifact-903

# Waveforms: -

## Waveform for PCIe\_REFCLK\_P and PCIe\_REFCLK\_N: -



Result: 100MHz

## PCIe\_REFCLK stabilization: -

A screenshot of a computer

Description automatically generated with low confidence

Result : - Clock stabilization takes around 20us

## PCIe enumeration failed case

A screen shot of a computer

Description automatically generated with low confidence

Legend: - Yellow – Power-On-GPIO

Cyan – PERST# GPIO

Violet – PCIe\_REFCLK

A screen shot of a device

Description automatically generated with low confidence

Result: - CLK continues even after enumeration fails. PERST# line toggles 10 times due to retries.

**Waveform result date – 26-05-2023: -**

**Test setup: -** PCI enum. command commented in “init.wifi.rc”

Waveform 1: - Normal power On.

A screen shot of a computer

Description automatically generated with low confidence

Legend:

Yellow – Power On GPIO

Cyan – PERST,

Violet – CLKREQ,

Blue – Clock

Result: - Normal power On. CLKREQ is asserted in PCIe controller drivers probe function. Also, PERST gpio is set to high in PCIe controller drivers probe function.

Time gap between rising edge of CLKREQ and Power-On-Gpio(using BT initrc) = 15.6 sec (approx.)

Waveform 2: - Time difference between PERST and CLKREQ

A screen shot of a device

Description automatically generated with low confidence

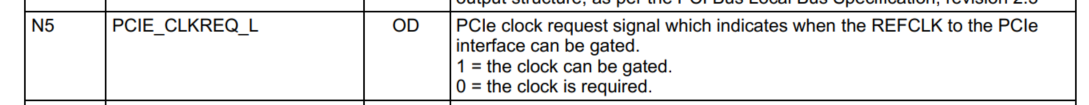
Waveform 3: - Time difference between CLKREQ and PCIe\_REFCLK

A screen shot of a computer

Description automatically generated with low confidence

**Date 27-05-2023: -**

As per IDCEvo wifi chip (CYW8x570) datasheet Page no - 50, CLKREQ pin is as below.



When PCIE\_CLKREQ\_L pin of wifi chip is made High, then clock is gated or turned off.

Exynos SOC TRM: - (Page 303)

A picture containing text, screenshot, line, font

Description automatically generated

**Waveform result date – 29-05-2023: -**

**Test 1: -**

**Test setup: -** Original Artifact 903 flashed

1. ) Power up of target

A screen shot of a computer

Description automatically generated with low confidence

Result: - Time gap between rising edge of CLKREQ and rising edge of Power-On-GPIO be 13.1 seconds. In this case, Power-ON-GPIO is asserted due to PCIe enumeration command running in init.wifi.rc.

**BT and Wifi init.rc conflict: -**

|  |  |  |
| --- | --- | --- |
|  | By init.wifi.rc | By BT init.rc |
| Assertion of Power-On-Gpio  (Taking PCIe\_CLKREQ rising as reference) | 13.16 s | 15.6 s |

Thus, BT team should avoid generating Power-On-GPIO in init.rc.

**Test 2: -**

Test setup: - In Android, assertion of Power-On-GPIO disabled from both init.wifi.rc and BT init.rc.

1. Normal power On

A screen shot of a computer

Description automatically generated with low confidence

Legend:

Yellow: Power-On-GPIO

Cyan: PERST#

Violet: CLK\_REQ

Blue: PCIe\_REFCLK

1. Time gap between CLK\_REQ falling edge and PERST rising edge at Power-On

A screen shot of a computer

Description automatically generated with low confidence

1. Time gap between CLK REQ rsing and falling edge at Power-On

A screen shot of a computer

Description automatically generated with low confidence