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# Test setup:-

Hardware used: - B2-SP25-IDCEvo

Image flashed: ES2 Artifact-903, Minor change in Android code for few test cases

Signals probed:

* WLAN1\_SOC\_PCIE2L\_L(0)\_TX\_N, WLAN1\_SOC\_PCIE2L\_L(0)\_TX\_P
* WLAN1\_SOC\_PCIE2L\_L(0)\_RX\_N, WLAN1\_SOC\_PCIE2L\_L(0)\_RX\_P
* WLAN1\_SOC\_PCIE\_PERST(2)\_Q
* WLAN1\_SOC\_PCIE\_CLKREQ(2)\_Q
* WLAN1\_SOC\_PCIE2L\_REFCLK0\_N, WLAN1\_SOC\_PCIE2L\_REFCLK0\_P
* ONUG3V3\_BT\_Wifi

CRO used: - RIGOL MSO8104 (1GHz, 10 Gsa/s))

# Waveforms and results: -

## Frequency of PCIe\_REFCLK\_P, PCIE\_REFCLK\_N

A screen shot of a graph

Description automatically generated with medium confidence

Legend:

Violet: WLAN1\_SOC\_PCIE2L\_REFCLK0\_P

Blue: WLAN1\_SOC\_PCIE2L\_REFCLK0\_N

**Result: -** PCIe Clock frequency = 100MHz

**Note: -**

The PCIe standard specifies a 100 MHz clock (Refclk) with at least±300 ppm frequency stabilityfor Gen 1, 2, 3 and 4, and at least ±100 ppmfrequency stabilityfor Gen 5,at both the transmitting and receiving devices.

## Rough estimation of PCIe\_REFCLK stabilization: -

A screenshot of a computer

Description automatically generated with low confidence

Legend:

Vioet: WLAN1\_SOC\_PCIE2L\_REFCLK0\_P

**Result** : - PCIe Clock stabilization takes around 20us.

## PCIe clock gating using CLKREQ line: -

A screen shot of a computer

Description automatically generated with low confidence

Legend:

Yellow: ONUG3V3\_BT\_Wifi

Cyan: WLAN1\_SOC\_PCIE\_PERST(2)\_Q

Violet: WLAN1\_SOC\_PCIE\_CLKREQ(2)\_Q

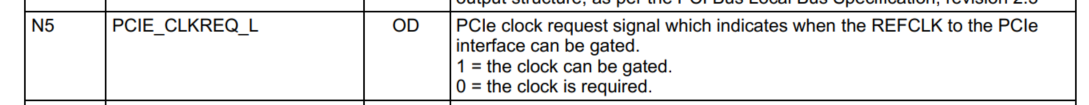
Blue: WLAN1\_SOC\_PCIE2L\_REFCLK0\_P

**Result: -**  PCIe CLKREQ line is used to enable and gate the PCIe clock. When CLKREQ line is low, then PCIe clock is enabled and when it goes high then PCIe clock can be disabled.

Time to enable PCIe clock from falling edge of CLKREQ line is 191.5 us (approx.).

Note: -

As per IDCEvo wifi chip (CYW8x570) datasheet Page no - 50, CLKREQ pin is as below.



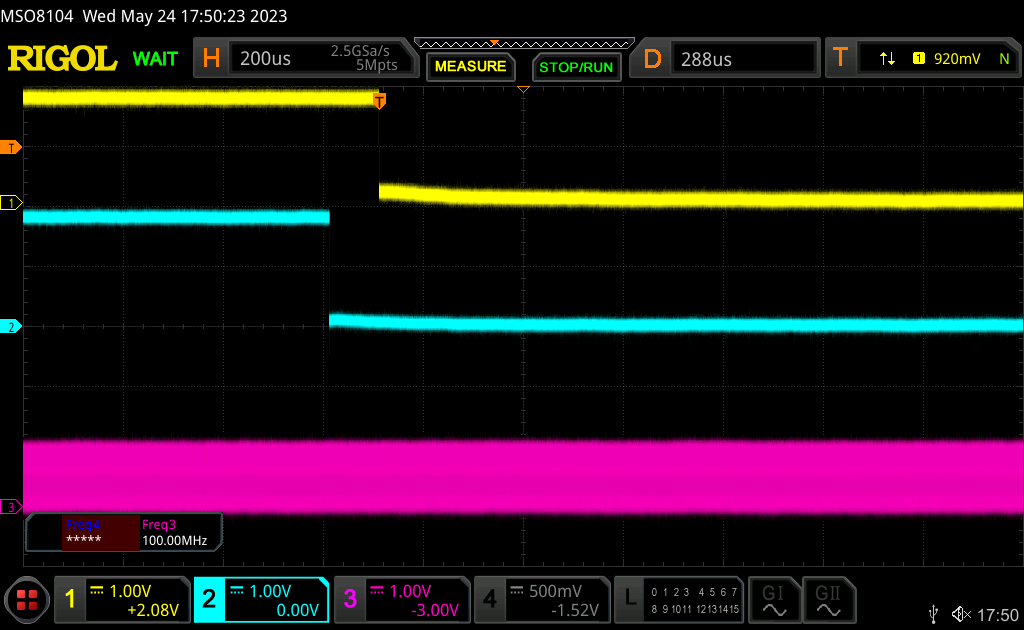
When PCIE\_CLKREQ\_L pin of wifi chip is made High, then clock is gated or turned off.

Exynos SOC TRM: Page 303

A picture containing text, screenshot, line, font

Description automatically generated

## PCIe Clock is maintained even after PCIe enumeration fails: -



Legend:

Yellow: ONUG3V3\_BT\_Wifi

Cyan: WLAN1\_SOC\_PCIE\_PERST(2)\_Q

Violet: WLAN1\_SOC\_PCIE2L\_REFCLK0\_P

**Result: -** PCIe clock is maintained, even after PCIe enumeration fails.

## Time gap between PERST and CLKREQ

A screen shot of a device

Description automatically generated with low confidence

Legend:

Yellow: ONUG3V3\_BT\_Wifi

Cyan: WLAN1\_SOC\_PCIE\_PERST(2)\_Q

Violet: WLAN1\_SOC\_PCIE\_CLKREQ(2)\_Q

Blue: WLAN1\_SOC\_PCIE2L\_REFCLK0\_P

**Result: -** Time gap betweenfalling edge of CLKREQ line and rising edge of PERST# line is 1.01 seconds.

Note: -

PERST# line is PCIe Reset line, which is made high in probe function of PCIe controller driver.

## Time sequence of various signals on normal power up of target:-

A screen shot of a computer

Description automatically generated with low confidence

Legend:

Yellow: ONUG3V3\_BT\_Wifi

Cyan: WLAN1\_SOC\_PCIE\_PERST(2)\_Q

Violet: WLAN1\_SOC\_PCIE\_CLKREQ(2)\_Q

Blue: WLAN1\_SOC\_PCIE2L\_REFCLK0\_P

**Result**: - Time gap between rising edge of CLKREQ and rising edge of Power-On-GPIO be 13.16 seconds. In this case, Power-ON-GPIO is asserted due to “PCIe enumeration command” running in init.wifi.rc.

Here, falling edge of CLKREQ line is taken as reference only.

## PCIe enumeration fail waveform at Power ON:

A screen shot of a computer

Description automatically generated with low confidence

Legend:

Yellow: ONUG3V3\_BT\_Wifi

Cyan: WLAN1\_SOC\_PCIE\_PERST(2)\_Q

Violet: WLAN1\_SOC\_PCIE\_CLKREQ(2)\_Q

Blue: WLAN1\_SOC\_PCIE2L\_REFCLK0\_P

**Result**: - At Power On, PCI enumeration is triggered using a command in an init.rc script, if enumeration does not pass, then 10 times retries are done, which can be seen as PERST# line coming LOW 10 times in above waveform. The expanded view is shown below.

A screen shot of a computer

Description automatically generated with low confidence

Note: - In above waveform with Cyan colour, we can see PERST# signal coming LOW for 10 times.

## Time gap between CLK REQ rising and falling edge at Power-On:

A screen shot of a computer

Description automatically generated with low confidence

Legend:

Yellow: ONUG3V3\_BT\_Wifi

Cyan: WLAN1\_SOC\_PCIE\_PERST(2)\_Q

Violet: WLAN1\_SOC\_PCIE\_CLKREQ(2)\_Q

Blue: WLAN1\_SOC\_PCIE2L\_REFCLK0\_P

Result: - CLKREQ line is high for 6.36 seconds at Power On.

## Waveform for PCIe\_TXD and PCIe\_RXD line: -

CRO probes were connected to below lines: -

ONUG3V3\_BT\_Wifi, WLAN1\_SOC\_PCIE\_PERST(2)\_Q, WLAN1\_SOC\_PCIE2L\_L(0)\_TX\_P and WLAN1\_SOC\_PCIE2L\_L(0)\_RX\_P signals.

When target was powered up to capture data lines, it generates panic. Panic log back trace is as below. Waveform is also shown below but it is of no use.

6 3 4:[ 16.680230][ C2] CPU: 2 PID: 188 Comm: kworker/u14:6 Tainted: G E 5.15.41-android13-8-g539e26b439f0-ab903 #1

6 3 4:[ 16.680238][ C2] Hardware name: BMW IDCEvo (v920-EVT0 SP21 B1) Android IVI VM (DT)

6 3 4:[ 16.680245][ C2] Workqueue: pcie\_wq exynos\_v920\_pcie\_dislink\_work [pcie\_exynos\_v920\_dw\_rc]

6 3 4:[ 16.680268][ C2] pstate: 204000c5 (nzCv daIF +PAN -UAO -TCO -DIT -SSBS BTYPE=--)

6 3 4:[ 16.680275][ C2] pc : pci\_generic\_config\_read+0x98/0xbc

1 3 0:[ 16.680288][ C2] lr : pci\_generic\_config\_read+0x28/0xbc

6 3 4:[ 16.680295][ C2] sp : ffffffc00bf4b9e0

6 3 4:[ 16.680300][ C2] x29: ffffffc00bf4b9e0 x28: ffffffc00116a750 x27: 00000000000000c0

6 3 4:[ 16.680310][ C2] x26: ffffff89ece7d800 x25: 0000000000000000 x24: 0000000000000018

1 3 0:[ 16.680320][ C2] x23: 0000000000000004 x22: ffffffc00bf4ba74 x21: ffffff8801e164b0

6 3 4:[ 16.680332][ C2] x20: 0000000000000004 x19: ffffffc00bf4ba74 x18: ffffffc00be7d060

1 3 0:[ 16.680340][ C2] x17: 00000000000002c6 x16: 000000000005853e x15: 000000000000001b

6 3 4:[ 16.680349][ C2] x14: 000000000005dd3e x13: 0000000000000096 x12: 0000000000000002

6 3 4:[ 16.680358][ C2] x11: 000000020000102e x10: 0000000000000002 x9 : 0000000000000000

1 3 0:[ 16.680366][ C2] x8 : 0000000000000000 x7 : 7f7f7f7f7f7f7f7f x6 : ff626871646d6466

6 3 4:[ 16.680375][ C2] x5 : 0000000000000010 x4 : ffffffc00bf4ba74 x3 : 0000000000000004

1 3 0:[ 16.680383][ C2] x2 : 0000000000000018 x1 : 0000000000000000 x0 : ffffffc00a9c8018

6 3 4:[ 16.680393][ C2] Kernel panic - not syncing: Asynchronous SError Interrupt

6 3 4:[ 16.680400][ C2] CPU: 2 PID: 188 Comm: kworker/u14:6 Tainted: G E 5.15.41-android13-8-g539e26b439f0-ab903 #1

1 3 0:[ 16.680406][ C2] Hardware name: BMW IDCEvo (v920-EVT0 SP21 B1) Android IVI VM (DT)

6 3 4:[ 16.680412][ C2] Workqueue: pcie\_wq exynos\_v920\_pcie\_dislink\_work [pcie\_exynos\_v920\_dw\_rc]

1 3 0:[ 16.680425][ C2] Call trace:

6 3 4:[ 16.680429][ C2] dump\_backtrace+0x0/0x1d4

6 3 4:[ 16.680440][ C2] show\_stack+0x1c/0x2c

6 3 4:[ 16.680446][ C2] dump\_stack\_lvl+0x68/0x84

6 3 4:[ 16.680461][ C2] dump\_stack+0x1c/0x40

1 3 0:[ 16.680469][ C2] panic+0x164/0x3a8

6 3 4:[ 16.680476][ C2] test\_taint+0x0/0x24

6 3 4:[ 16.680485][ C2] arm64\_serror\_panic+0x70/0x98

6 3 4:[ 16.680492][ C2] do\_serror+0x104/0x134

1 3 0:[ 16.680498][ C2] el1h\_64\_error\_handler+0x38/0x54

6 3 4:[ 16.680507][ C2] el1h\_64\_error+0x7c/0x80

6 3 4:[ 16.680515][ C2] pci\_generic\_config\_read+0x98/0xbc

6 3 4:[ 16.680522][ C2] exynos\_v920\_generic\_own\_config\_read+0x110/0x16c [pcie\_exynos\_v920\_dw\_rc]

1 3 0:[ 16.680534][ C2] pci\_bus\_read\_config\_dword+0x84/0xd8

6 3 4:[ 16.680541][ C2] pci\_read\_config\_dword+0x44/0x54

6 3 4:[ 16.680549][ C2] pci\_scan\_bridge\_extend+0x74/0x61c

1 3 0:[ 16.680557][ C2] pci\_scan\_child\_bus\_extend+0x218/0x350

6 3 4:[ 16.680565][ C2] pci\_rescan\_bus+0x20/0x4c

6 3 4:[ 16.680574][ C2] exynos\_v920\_pcie\_poweron+0x57c/0x918 [pcie\_exynos\_v920\_dw\_rc]

6 3 4:[ 16.680585][ C2] exynos\_v920\_pcie\_dislink\_work+0x198/0x1dc [pcie\_exynos\_v920\_dw\_rc]

1 3 0:[ 16.680595][ C2] process\_one\_work+0x1ac/0x394

When CRO probe was removed from TXD and RxD lines of PCIe, then it booted normally without any panic.

A screen shot of a graph

Description automatically generated with low confidence

Legend:

Yellow: ONUG3V3\_BT\_Wifi

Cyan: WLAN1\_SOC\_PCIE\_PERST(2)\_Q

Violet: WLAN1\_SOC\_PCIE2L\_L(0)\_TX\_P

Blue: WLAN1\_SOC\_PCIE2L\_L(0)\_RX\_P

**Result**: When CRO probe was connected to PCIe TxD and RxD lines, then it is generating panic. When CRO probes are disconnected then it boots without panic.