**SPI Native CS activation per word in TI-DRA604 SOC: -**

1. TI DRA604 SOC follows TRM same as that of AM335X SOC. As per TRM, following points were observed to enable SPI-CS per word: -
2. Each SPI controller module supports two Chip Select lines.

Diagram

Description automatically generated

1. Keeping SPIEN active between words i.e., for N words single CS: -

Text

Description automatically generated

1. MCSPI\_MODULCTRL[Single]: -

Calendar

Description automatically generated

**Software Design: -**

spi.c:

struct spi\_device{

u32 max\_speed\_hz;

u8 chip\_select;

u8 bits\_per\_word;

u16 mode;

void \*controller\_data;

…………………………….

}

dynamic\_spi\_node.c:

struct spi\_board\_info{

……..

void \*controller\_data;

u16 bus\_num;

u16 chip\_select;

………

}

struct spi\_contoller\_config\_data{

unsigned turbo\_mode:1;

/\* toggle chip select after every word \*/ unsigned cs\_per\_word:1;

};

Clears SINGLE bit

Of MODULCTRL

register

Spi-omap2-mcspi.c:

omap2\_mcspi\_work\_one () {

struct omap2\_mcspi\_device\_config \*cd;

cd = spi->controller\_data;

……………..

if (cd && cd->cs\_per\_word) {

/\*MIR\*/

pr\_info("MIR, Programmed CS Per Word\n");

chconf = mcspi->ctx.modulctrl;

chconf &= ~OMAP2\_MCSPI\_MODULCTRL\_SINGLE;

mcspi\_write\_reg(master, OMAP2\_MCSPI\_MODULCTRL, chconf);

mcspi->ctx.modulctrl = mcspi\_read\_cs\_reg(spi, OMAP2\_MCSPI\_MODULCTRL);

}

………………………..

}

Spi-omap2-mcspi.h:

struct omap2\_mcspi\_device\_config {

unsigned turbo\_mode:1;

/\* toggle chip select after every word \*/

unsigned cs\_per\_word:1;

};

**Code changes made:-**

Text

Description automatically generated