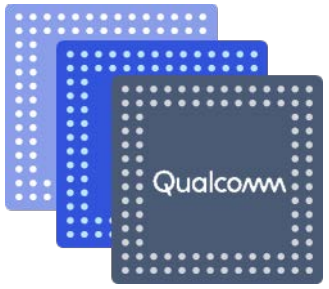
SA6155 Linux Android PCIe Overview

Qualcomm Technologies, Inc.

80-PK753-22 Rev. A



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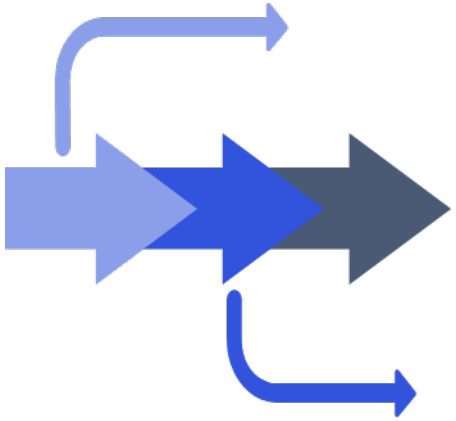
Revision History

Revision	Date	Description
A	January 2019	Initial release

Contents



Hardware Overview

Hardware Features

- This chipset has one peripheral component interconnect express (PCIe) root complex (RC): RC0 (Gen2 one lane)
- Conforms to *PCI Express Base 2.0 Specification*
- One lane to transmit and receive
- Maximum supported rates:
  - Gen2 – 5.0 GT/s
  - Gen1 – 2.5 GT/s
- Supports L0, L2/L3 ready, L3 modes
- Message signaled interrupt (MSI) and PCI legacy interrupt

Memory Resources

RC	Name	Base address	Size
RC0 (Gen2 one lane)	Configuration space	0x40100000	0x100000 (1 MB)
	I/O space	0x40200000	0x100000 (1 MB)
	Base address register (BAR) space	0x40300000	0x1fd00000 (512 MB)

Power Rails

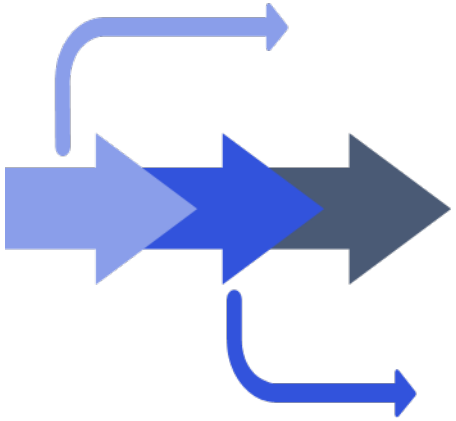
RC	Rail	Voltage
RC0 (Gen2 power rail)	VREG_L12A(PMIC) → VDDA_PCIE_1LANE_PLL_1P8	1.8 V
	VREG_L5A(PMIC) → VDDA_PCIE_1LANE_CORE (SDM)	0.928 V

Clocks

- External
  - PCIE_REFCLK: Provides a 100 MHz standard PCIe reference clock to the endpoint (EP)
- Internal
  - PCIe reference clock
    - From TCXO, 19.2 MHz
    - From GPLL0, 100 MHz
  - PCIe PIPE clock: Drives the internal logic for PCIe
  - PCIe AXI slave clock
  - PCIe AXI master clock
  - PCIe AXI slave Q2A clock
  - PCIe AHB clock
  - PCIe TBU clock
  - PCIe auxiliary clock
  - PCIe PHY auxiliary clock
  - PCIe LDO clock

Hardware Interrupts

- PCIe legacy interrupts
  - INTA#
  - INTB#
  - INTC#
  - INTD#
- MSI
- PCIe linkdown IRQ
  - Handler – `handle_linkdown_irq`
  - PCIe device drivers can register for linkdown notification
- AER interrupt
  - Handler – `handle_aer_irq`
- PCIe_WAKE_n
  - GPIO interrupt
  - Handler – `handle_wake_irq`



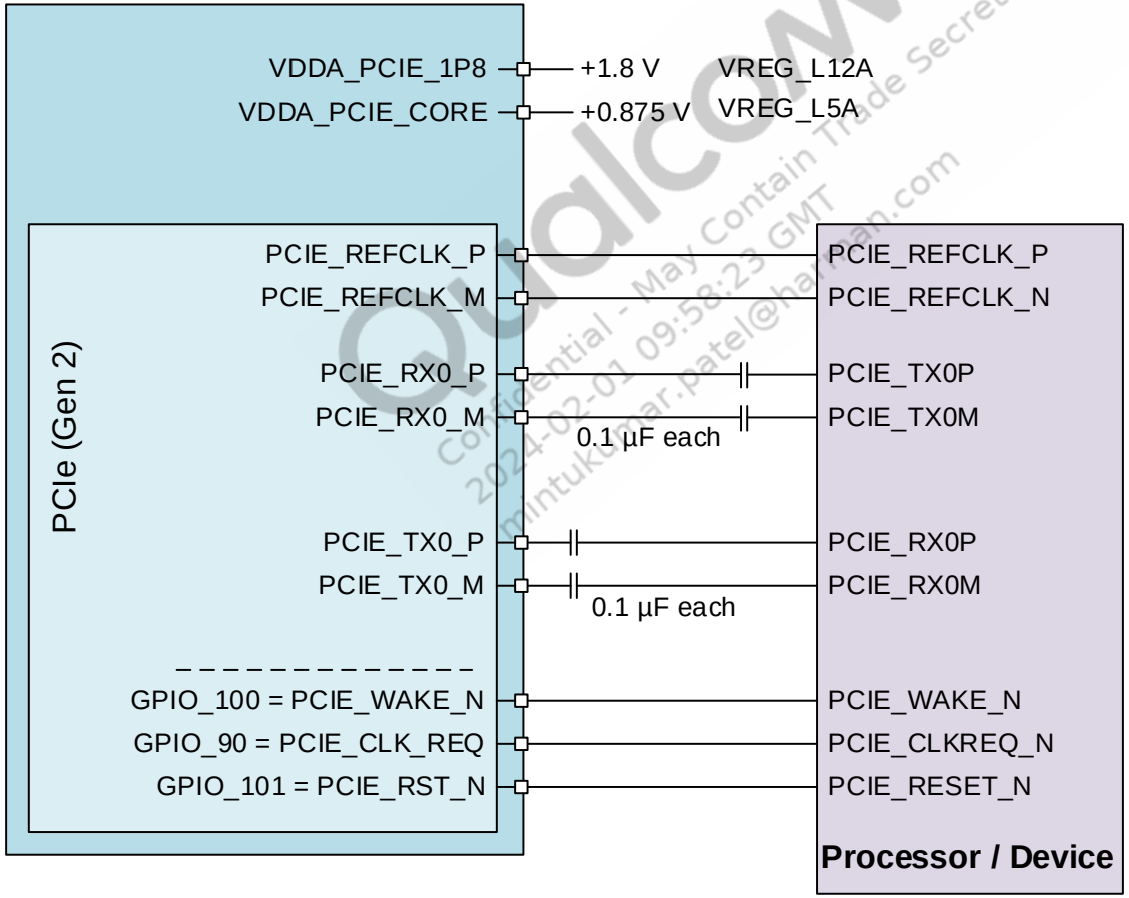
Software Overview

Software Drivers

Driver	Path
PCIe framework	`/kernel/drivers/pci/`
Host	`/kernel/drivers/pci/host/pci-msm.c`
Device tree configuration	`/kernel/arch/arm/boot/dts/qcom/(platform)-pcie.dtsi`

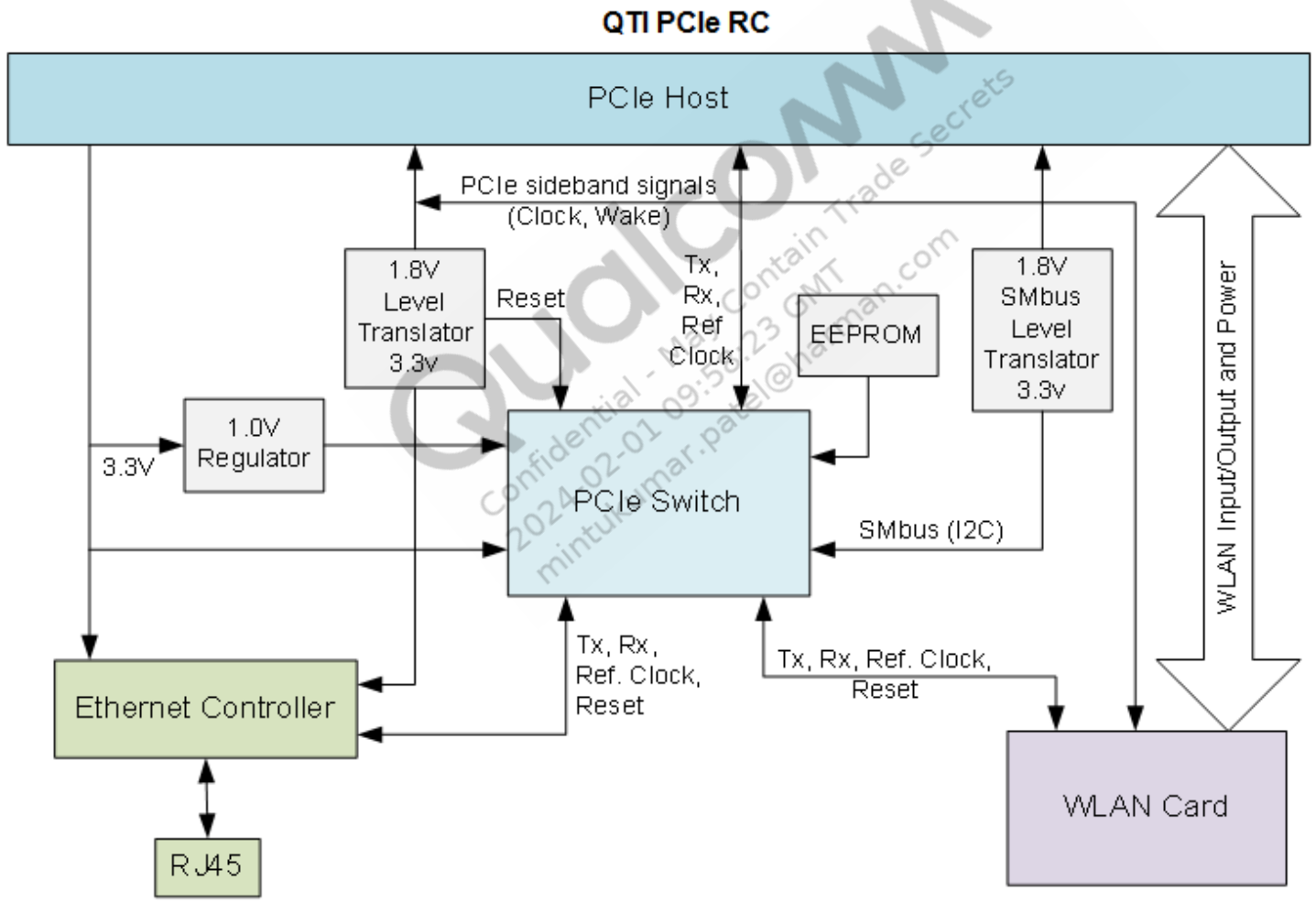
RC + Wi-Fi (External)

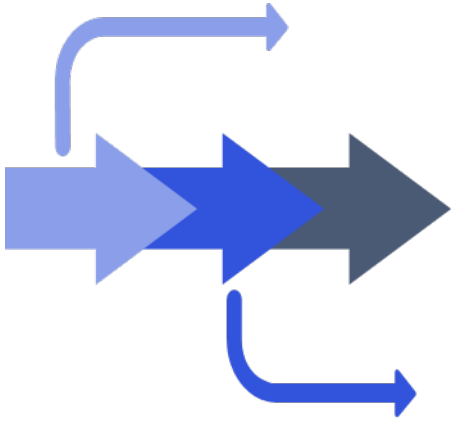
Provides Wi-Fi access point, hotspot, and so on.



RC + Switch + Wi-Fi and Ethernet

Provides Wi-Fi access point, hotspot, network connection, and so on.

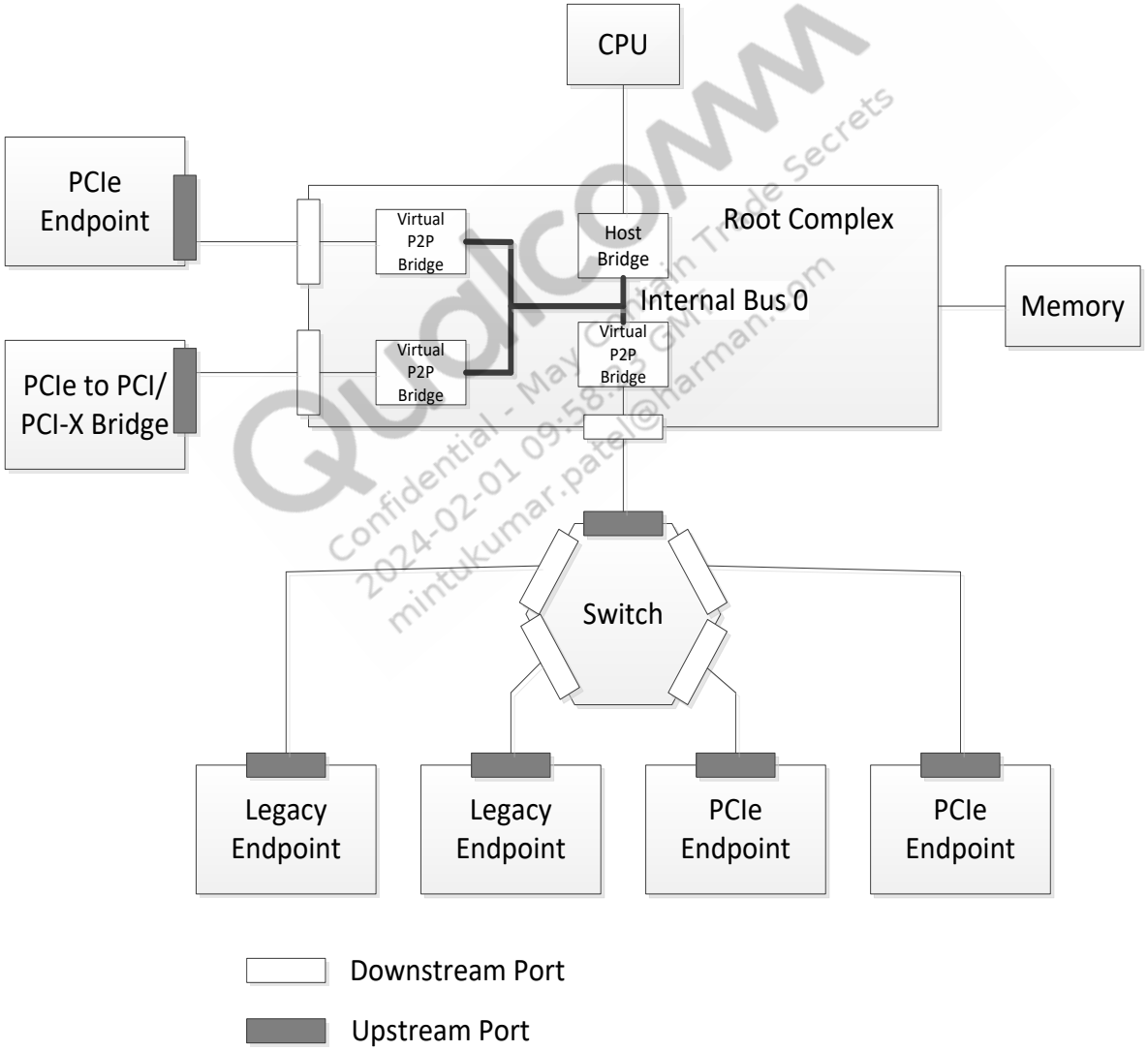




Technical Overview

PCIe Topology

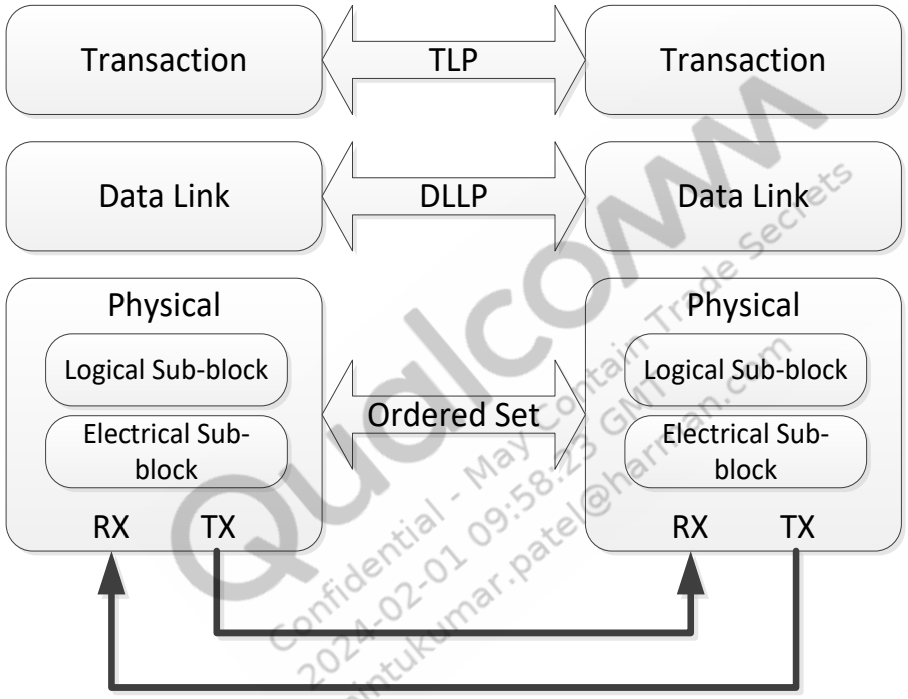
The following figure shows a sample PCIe topology.

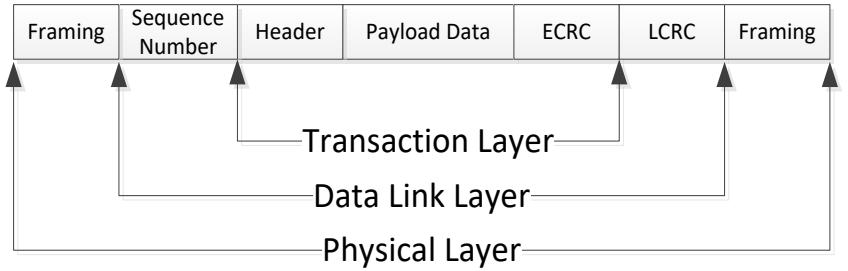


Common PCIe Terms

Term	Description
Domain	A single PCIe tree with one RC and one or more EPs
Bus	A point-to-point (external) or point-to-multipoints (internal) connection ▪ A PCIe domain can contain up to 256 buses ▪ The internal bus within the RC is always hardwired numbered as Bus 0 ▪ An external bus always connects to a downstream port and an upstream port
Device	▪ A component on either end of a PCIe link ▪ The addressing scheme limits up to 32 devices connected to a single PCIe bus
Function	▪ An addressable entity in the configuration space associated with a single function number ▪ Each device can contain up to eight functions

PCIe Layered Architecture





TLP Request Types

Request type	Description
Memory	▪ Transfers data to or from a location in the system memory map ▪ A locked memory read transaction is defined but not supported by QTI implementation
Input/output	▪ Transfers data to or from a location in the system input/output map ▪ Input/output addressing is only used to support legacy devices
Configuration	▪ Transfers data to or from a location in the configuration space of a PCIe device ▪ Used to discover device capabilities, program plug-and-play features, and check the status by the host
Message	Provides an in-band messaging and event reporting mechanism without consuming either memory or input/output address resources

Each request type has one of the following features:

Feature	Description
Posted	▪ Targeted device does not return a completion transaction layer packet (TLP) to the requester ▪ Improves performance but provides no feedback about whether the transaction has completed successfully or encountered an error
Nonposted	Requester sends a packet for which the targeted device should generate a response in the form of a completion TLP

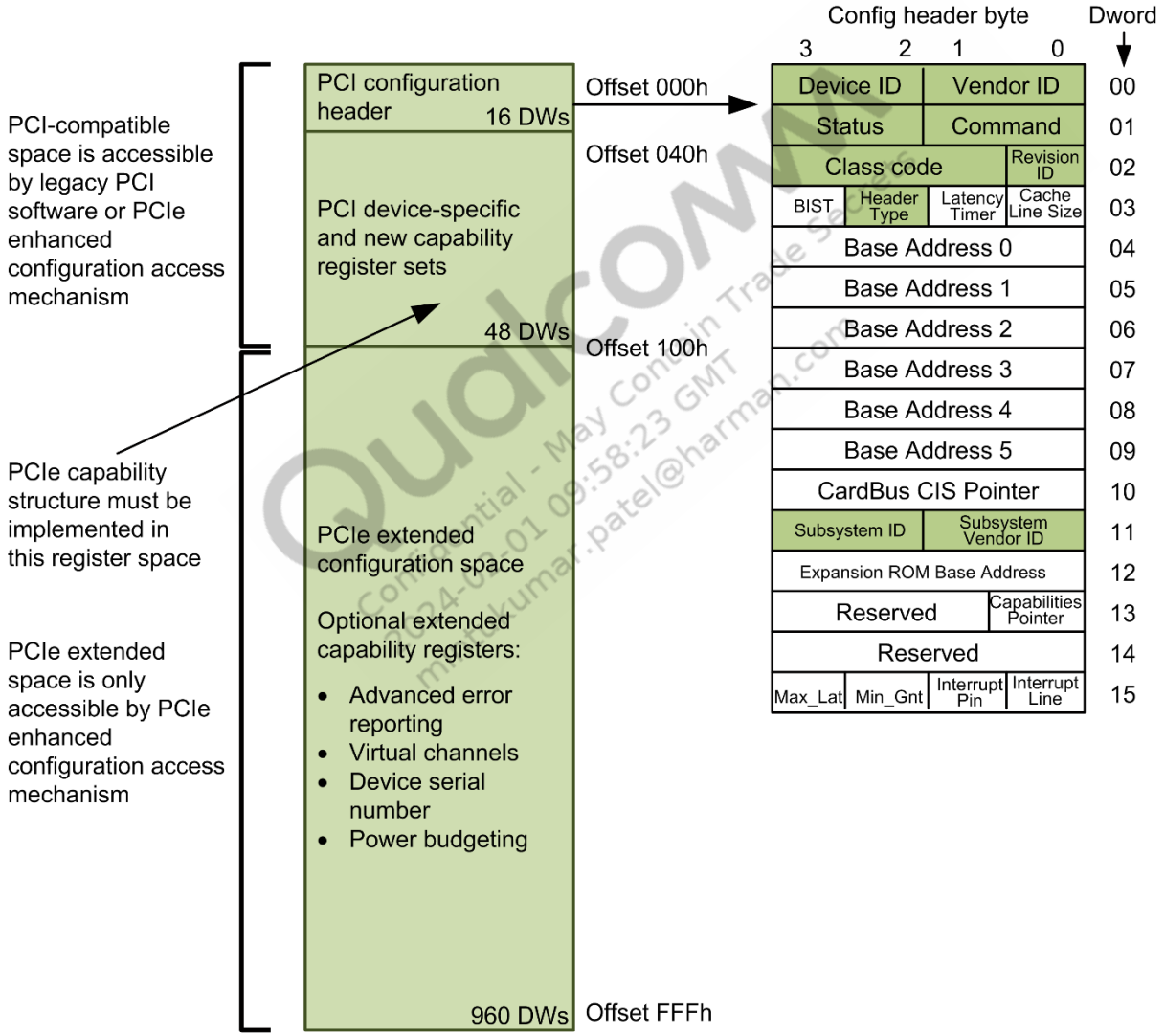
TLP Request Categories

Request type	Posted or Nonposted
Memory read	Nonposted
Memory write	Posted
Memory read lock	Nonposted
Input/output read	Nonposted
Input/output write	Nonposted
Configuration read (Type 0 and Type 1)	Nonposted
Configuration write (Type 0 and Type 1)	Nonposted
Message	Posted

TLP Routing and Addressing Rules

Rule	Description
Address	▪ Used with memory and input/output requests ▪ Two address formats are specified, a 64-bit format and a 32-bit format ▪ Input/output requests use only a 32-bit format
ID	▪ Used with configuration requests, ID routed messages, and completions ▪ Uses the bus, device, and function numbers to specify the destination for the TLP
Implicit	Special messages using implicit routing rule are defined to convey information related to power management, interrupt handling, error handling, and so on, between the RC and EPs

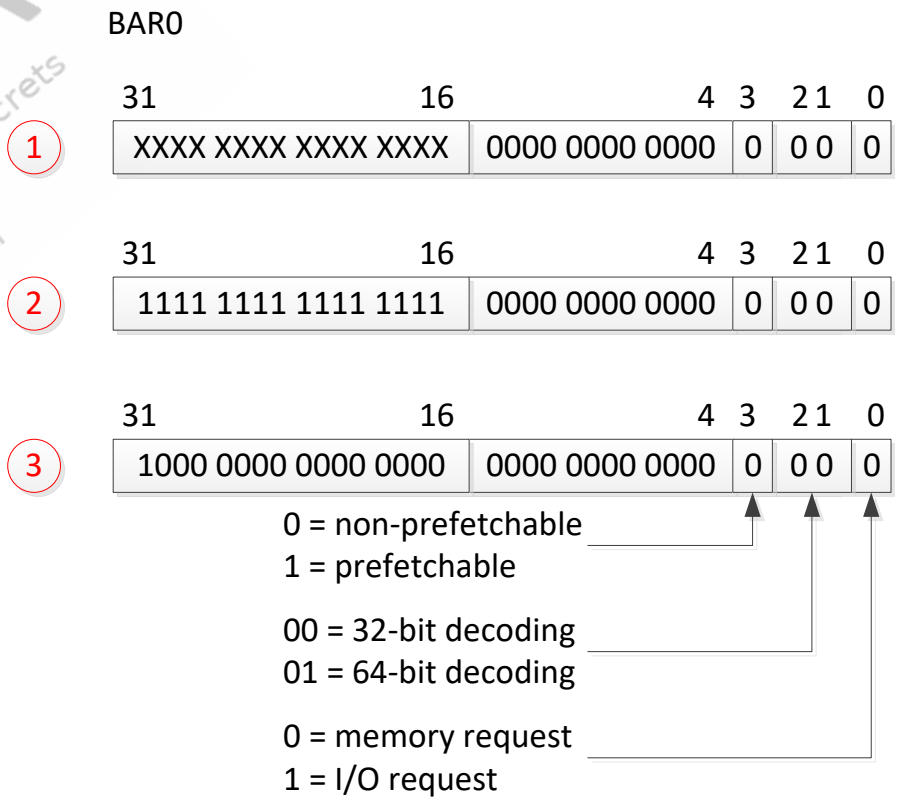
Configuration Space



BARs

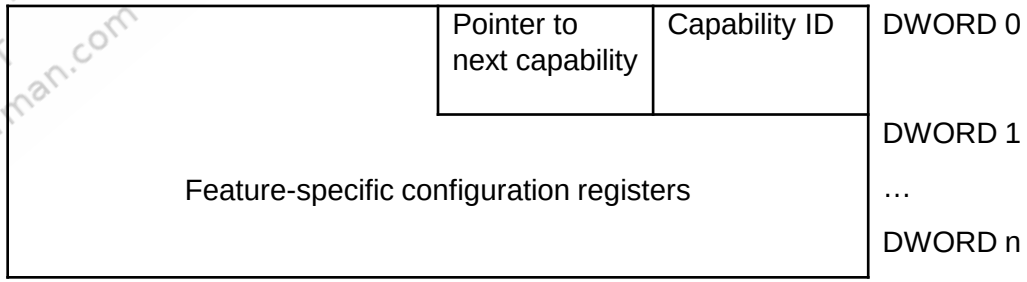
The following illustrates an usage example:

- Bits 0 to 3 indicate the type of memory (or registers) present on the device
  - BAR0 supports non-prefetchable, 32-bit decoding memory
- The software programs all 1s in BAR0 and reads it back
  - Writable bit positions change value from X to 1
  - From LSB to MSB, the software looks for the first writable bit position (bit 16) and determines that the memory (register) range covered by BAR0 is of size 2^{16} (64 KB)
- The software finds an available address space of 64 KB, starting from address 0x80000000, and programs 0x10000000 into BAR0
- Once the BARs are configured, the 64 KB memory (register) space on-device is mapped to 0x8000000000 to 0x8000FFFF in the system host processor PCIe address space



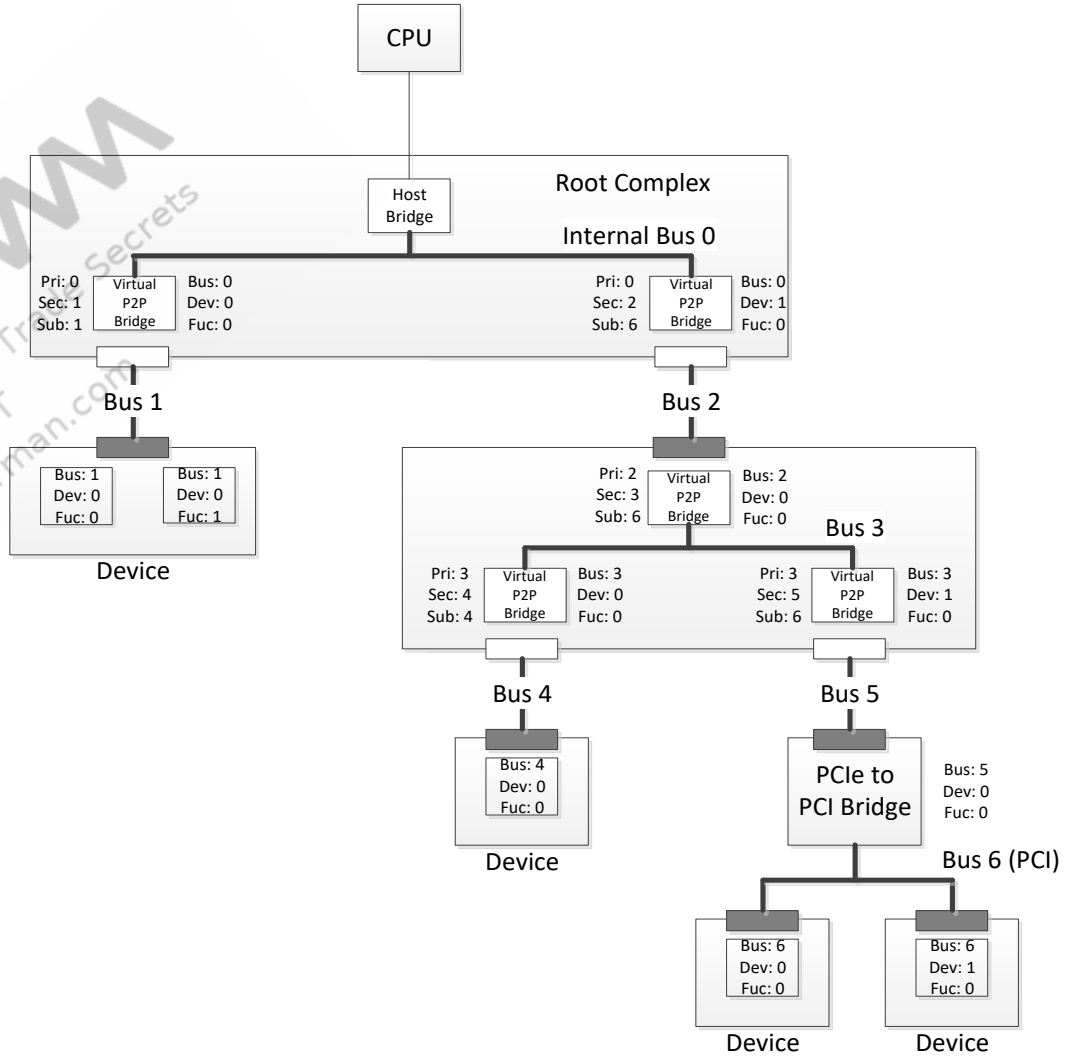
Capability List Entry

- Capability list bit (bit 4) in the configuration status register (byte offset 0x06) is set to 1 if the function implements the capability list
- Capability pointer register (byte offset 0x34) contains the address of the next entry of the capability list
- First byte of the next entry of the capability list is the capability ID
  - Identifies the supported capability, such as PCI express capability register set (0x10), PCI power management interface (0x01), and MSI (0x05)
- Second byte from the next entry of the capability list is the address of the next entry
  - If the value is 0, the list terminates



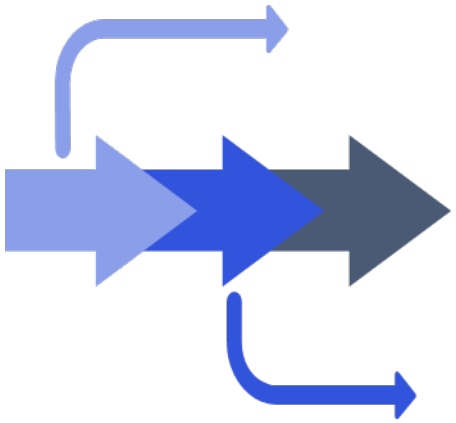
Enumeration

- The enumeration process:
  - Discovers if buses, devices, and functions exist in the system
  - Assigns a bus device function (BDF) number to each discovered function for ID-based routing
- Common terms for bus numbers:
  - Primary – Number of the bus towards the RC
  - Secondary – Number of the bus away from the RC
  - Subordinate – Highest bus number that exists on the downstream side



Software Interrupts

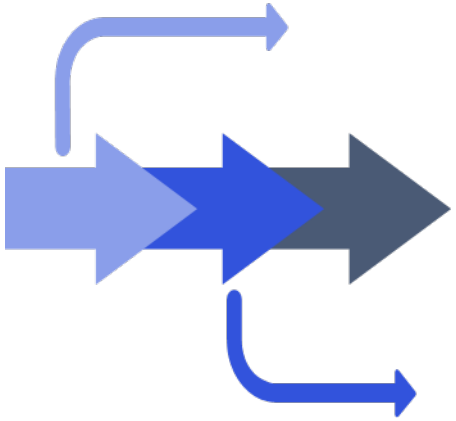
Interrupt	Description
Legacy PCI	▪ PCI bus defines four physical lines (INTA#, INTB#, INTC#, and INTD#) asserted by PCI devices to interrupt the system host processor ▪ PCIe defines in-band messages that act as virtual INTx# wires to support legacy PCI devices
MSI	▪ Eliminates the need for sideband signals ▪ Not based on message TLP, but on memory write TLP to a predetermined memory location



Debug Guidelines

Debugging

For debugging guidelines on QTI-specific implementation, see *PCIe Express Hardware and Software User Guide* (80-NH717-30).

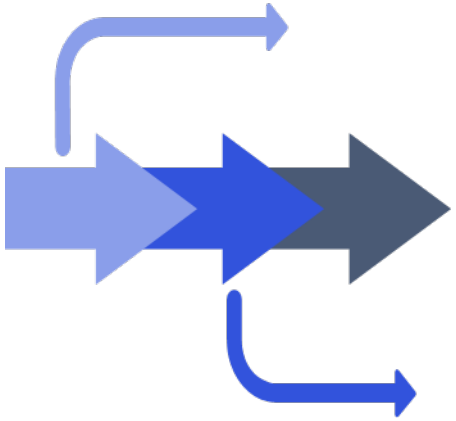


References

References

Documents	
Title	**Number**
Qualcomm Technologies, Inc.	
PCI Express Hardware and Software User Guide	80-NH717-30
Resources	
PCI Express Base 2.0 Specification	

Acronyms	
Acronym or term	**Definition**
BAR	Base address register
BDF	Bus device function
EP	Endpoint
MSI	Message signaled interrupt
PCIe	Peripheral component interconnect express
RC	Root complex
TLP	Transaction layer packet



Questions?

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