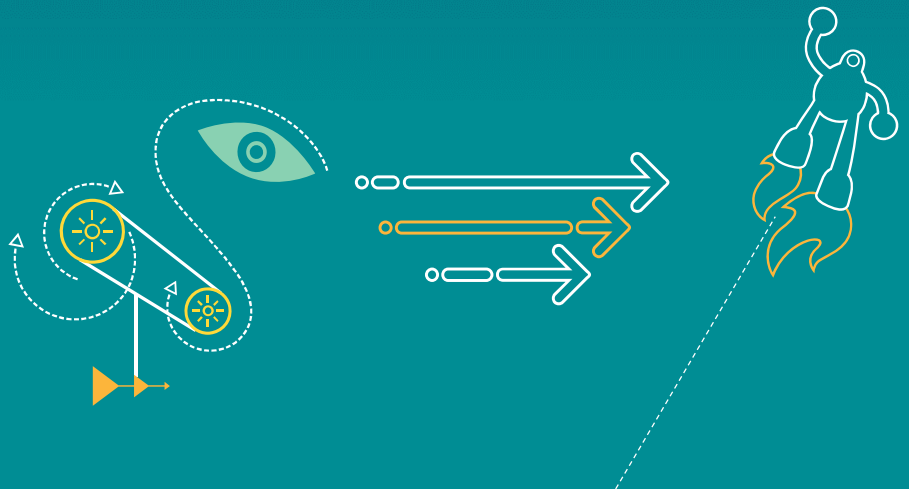
MSM8996 PCIe Software Overview

Qualcomm Technologies, Inc.



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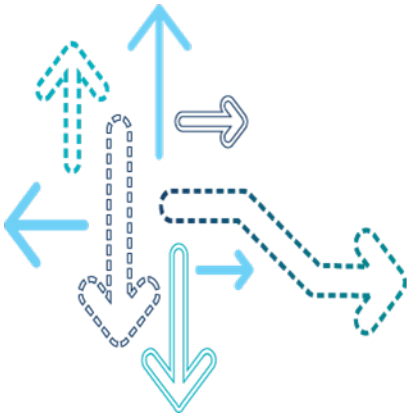
Revision History

Revision	Date	Description
A	August 2015	Initial release

Contents

- PCIe Hardware Overview
- PCIe Software Overview
- PCIe Debugging
- PCIe Technical Overview
- References
- Questions?

PCIe Hardware Overview

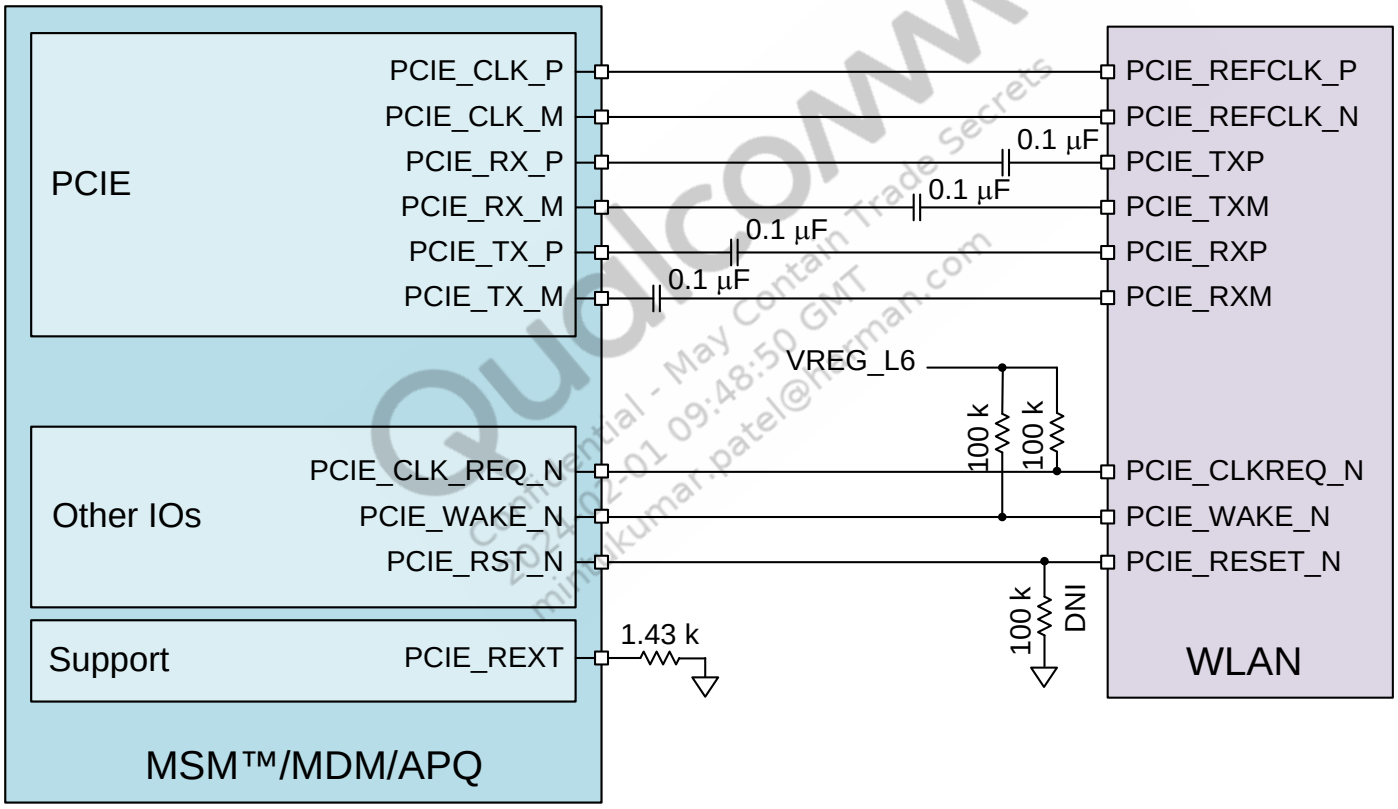


Hardware Features – MSM8996

- Gen1/2 one lane
- 3 Root complex
- Conforms to PCI Express Base 2.1 specification
  - One-lane transmit and receiver
  - Maximum supported clock rate of 5 GHz
  - ASPM support
    - L1
    - L1 substates
  - MSI and PCI legacy interrupts

Root Complex + Wi-Fi

- Provides Wi-Fi access point, hotspot, etc.



Note: The REFCLK driver does not require any external source terminations to meet PCIe clock requirements.

Host Controller Information – Memory Resources – MSM8996

Name	Base Address	Size
Configuration Space 0	0x0c100000	0x100000
IO Space 0	0x0c200000	0x100000
BAR Space 0	0x0c300000	0xd00000
Configuration Space 1	0x0d100000	0x100000
IO Space 1	0x0d200000	0x100000
BAR Space 1	0x0d300000	0xd00000
Configuration Space 2	0x0e100000	0x100000
IO Space 2	0x0e200000	0x100000
BAR Space 2	0x0e300000	0xd00000

Host Controller Information – Power Rails – MSM8996

Rail	Voltage
PM8996_L12	1.8V
PM8996_L28	.9V

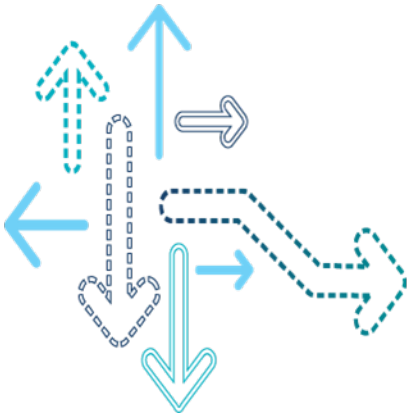
Host Controller Information – Clocks – MSM8996

- LN_BB_CLK
  - Reference source clock for PCIe
  - 19.2 MHz
- PCIe pipe clock
  - Drives internal logic for PCIe
- PCIe AXI slave clock
- PCIe AXI master clock
- PCIe AHB clock
- PCIe auxiliary clock
- PCIe PHY clocks
- SMMU AXI clock

Host Controller Information – Interrupts – MSM8996

- PCIe legacy interrupts
  - INTA#
  - INTB#
  - INTC#
  - INTD#
- MSI
- PCIe linkdown IRQ
  - Handler – `handle_linkdown_irq`
  - PCIe device drivers can register for linkdown notification
- AER interrupt
  - Handler – `handle_aer_irq`
- PCIe_WAKE_n
  - GPIO interrupt
  - Handler – `handle_wake_irq`

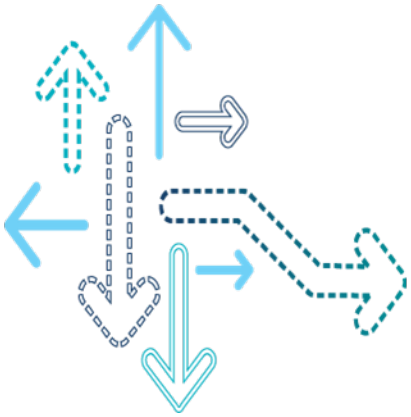
PCIe Software Overview



Software Driver

- PCIe framework
  - `/kernel/drivers/pci/`
- Host driver
  - `/kernel/drivers/pci/host/pci-msm.c`
- Device tree configuration
  - `/kernel/arch/arm/boot/dts/qcom/msm8996.dtsi`

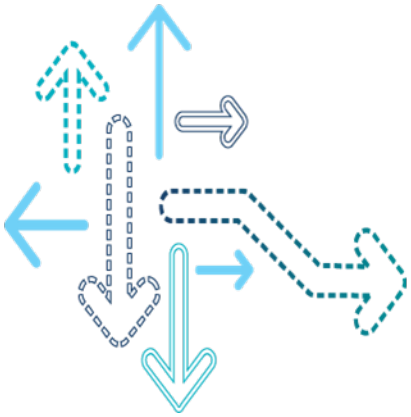
PCIe Debugging



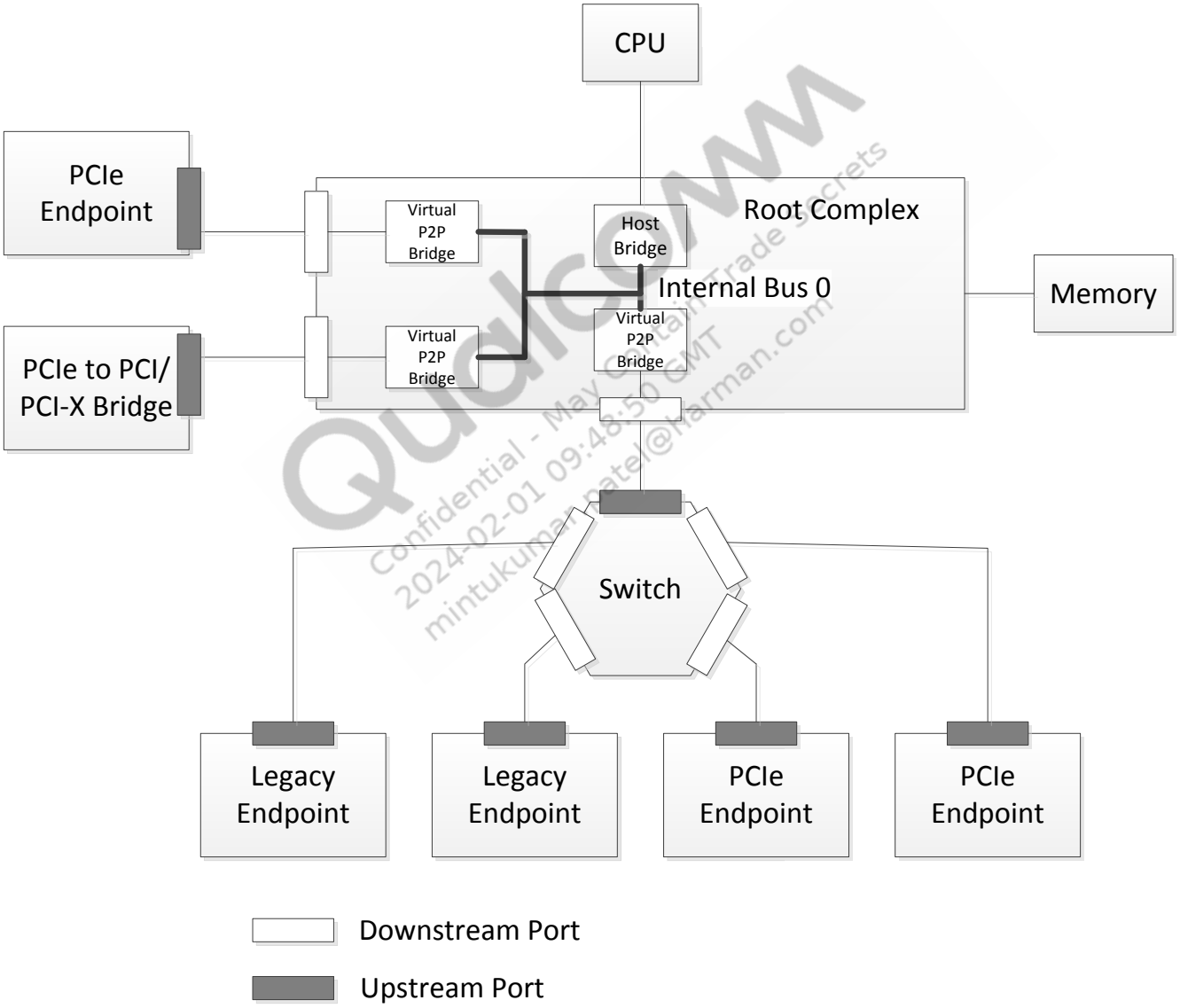
QTI-Specific Implementation Debugging

- Refer to the *PCIe Express Hardware and Software User Guide for APQ8084 and MSM8994 Linux* (80-NH717-30)

PCIe Technical Overview



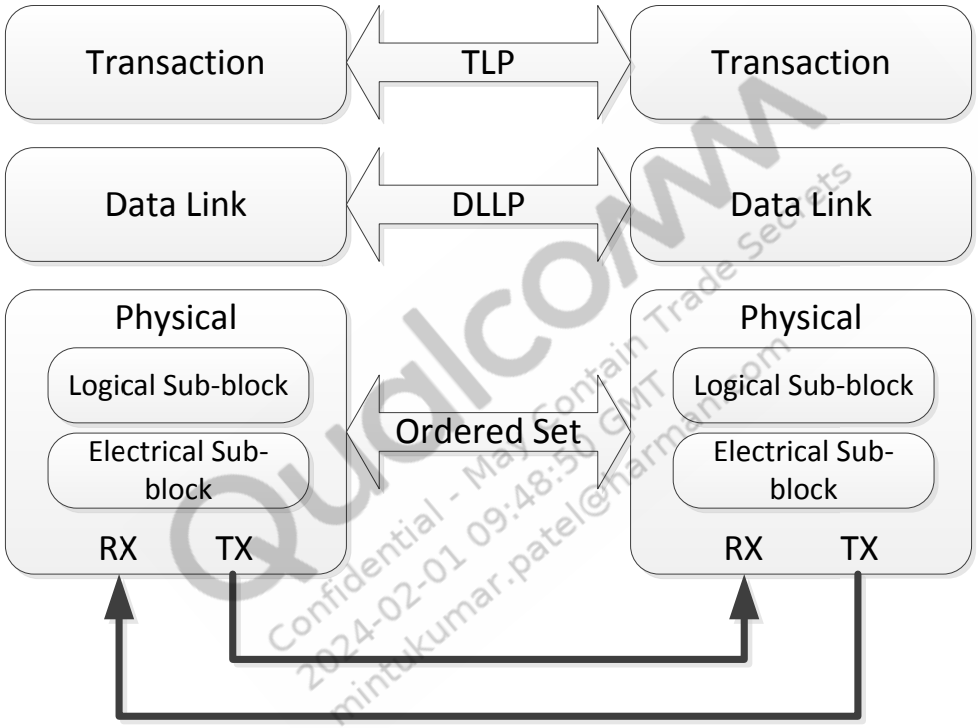
Sample PCIe Topology

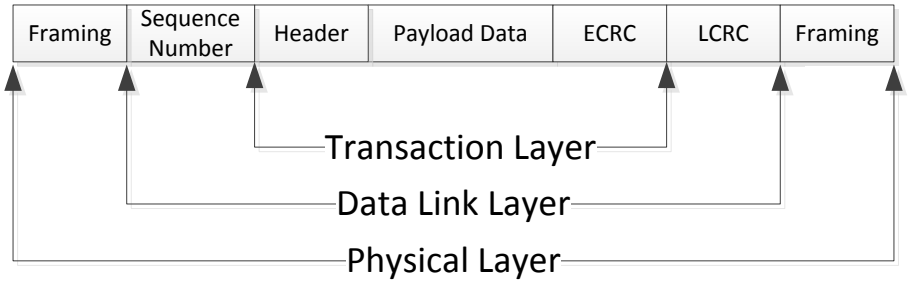


PCIe Terminology

- Domain
  - A single PCI Express (PCIe) tree with one Root Complex (RC) and one or more endpoints
- Bus
  - A point-to-point (external) or point-to-multipoints (internal) connection
  - A PCIe domain can contain up to 256 buses
  - The internal bus within the RC is always hardwired numbered as Bus 0
  - An external bus always connects to a downstream port and an upstream port
- Device
  - A component on either end of a PCIe link
  - The addressing scheme limits up to 32 devices connected to a single PCIe bus
- Function
  - An addressable entity in configuration space associated with a single function number
  - Each device can contain up to eight functions

Layered Architecture





Transaction Layer Packet (TLP) Request Categories

Request type	Nonposted or posted
Memory read	Nonposted
Memory write	Posted
Memory read lock	Nonposted
Input/output read	Nonposted
Input/output write	Nonposted
Configuration read (Type 0 and Type 1)	Nonposted
Configuration write (Type 0 and Type 1)	Nonposted
Message	Posted

TLP Request Types

- Memory
  - Transfer data to or from a location in the system memory map
  - A locked memory read transaction is defined but not supported by Qualcomm Technologies, Inc. (QTI) implementation
- Input/output
  - Transfer data to or from a location in the system input/output map
  - Input/output addressing is only used to support legacy devices
- Configuration
  - Transfer data to or from a location in the configuration space of a PCIe device
  - Used to discover device capabilities, program plug-and-play features, and check the status by the host
- Message
  - Provides an in-band messaging and event reporting mechanism without consuming either memory or input/output address resources

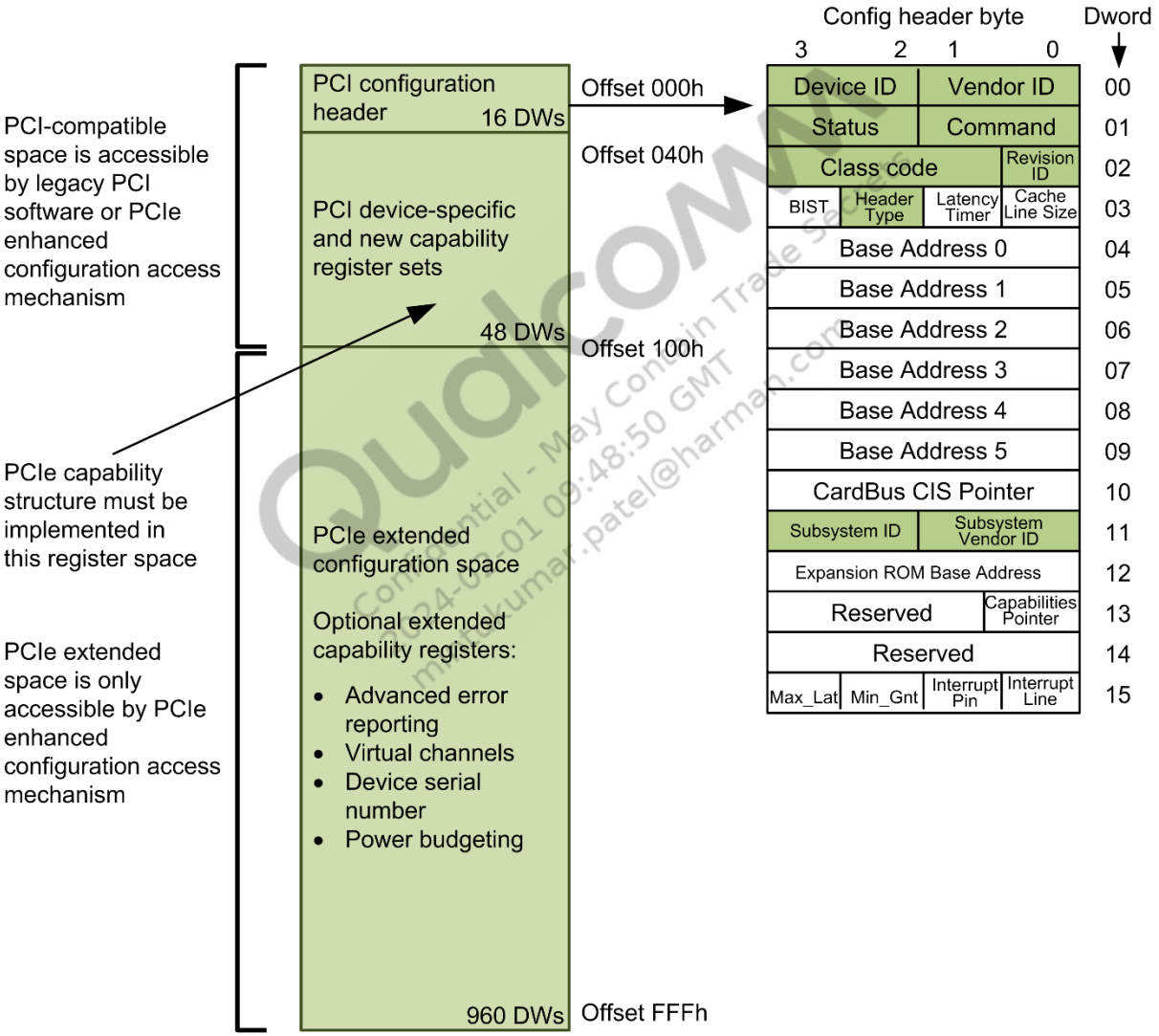
TLP Request Types (cont.)

- Each request type has one of these two characteristics:
  - Posted
    - Targeted device does not return a completion TLP to the requester
    - Improves performance but provides no feedback about whether the transaction has completed successfully or encountered an error
  - Nonposted
    - Requester sends a packet for which the targeted device should generate a response in the form of a completion TLP

TLP Routing and Addressing Rules

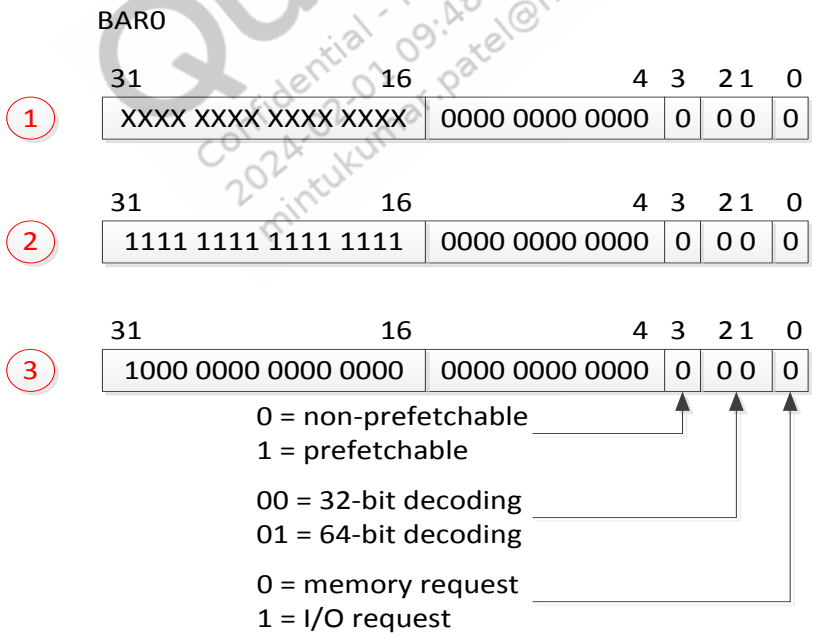
- Address
  - Used with memory and input/output requests
  - Two address formats are specified, a 64-bit format and a 32-bit format
  - Input/output requests use only 32-bit format
- ID
  - Used with configuration requests, ID routed messages, and completions
  - Uses the bus, device, and function numbers to specify the destination for the TLP
- Implicit
  - Special messages using implicit routing rule are defined to convey information related to, power management, interrupt handling, error handling, etc., between the RC and endpoints

Configuration Space



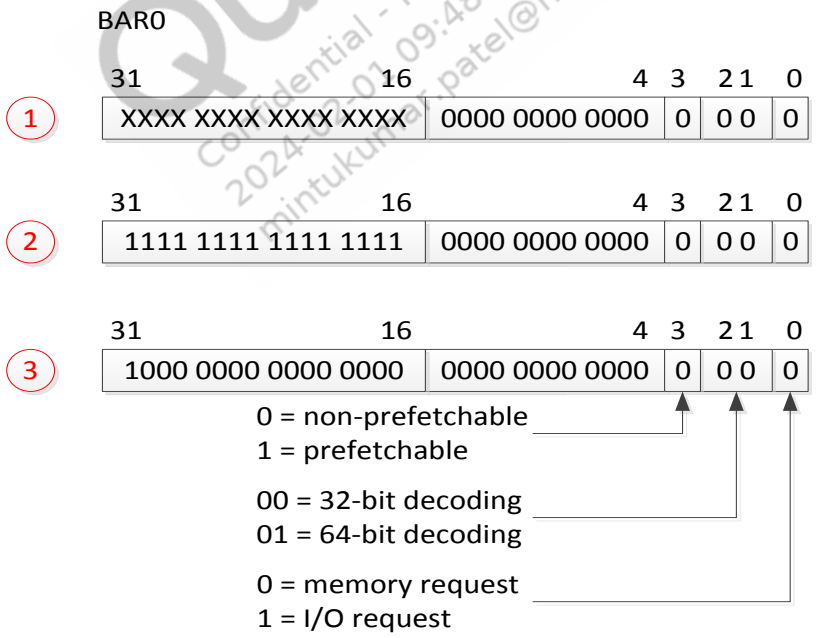
Base Address Registers (BARs) – Usage Example

- Bits 0 to 3 indicate the type of memory (or registers) present on the device
  - BAR0 in the example supports non-prefetchable, 32-bit decoding memory
- Software programs an all-1s pattern in BAR0 and reads it back
  - Writable bit positions change value from X to 1
  - From LSB to MSB, the software looks for the first writable bit position, bit 16 in this example, and determines that the memory (register) range covered by BAR0 is of size 2^{16} (64 KB)



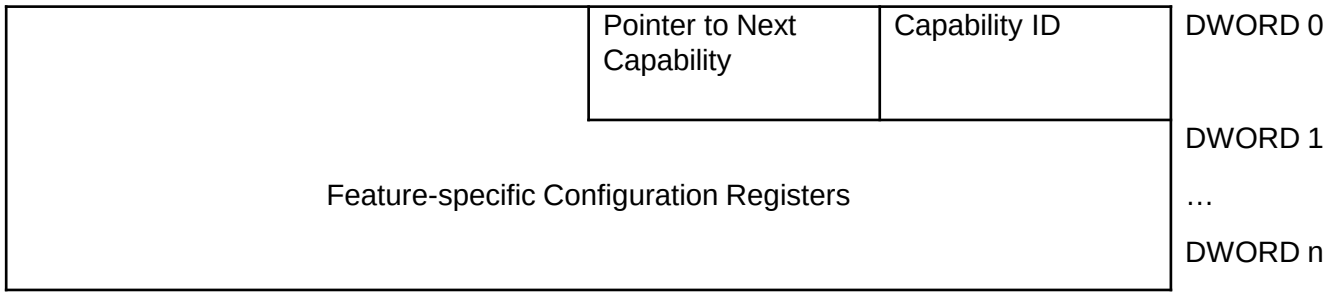
Base Address Registers (BARs) – Usage Example (cont.)

- Software finds an available address space of 64 KB, starting from address 0x80000000 in this example, and programs 0x10000000 into BAR0
  - Once the BARs are configured, the 64 KB memory (register) space on-device is mapped to 0x8000000000 to 0x8000FFFF in the system host processor PCIe address space



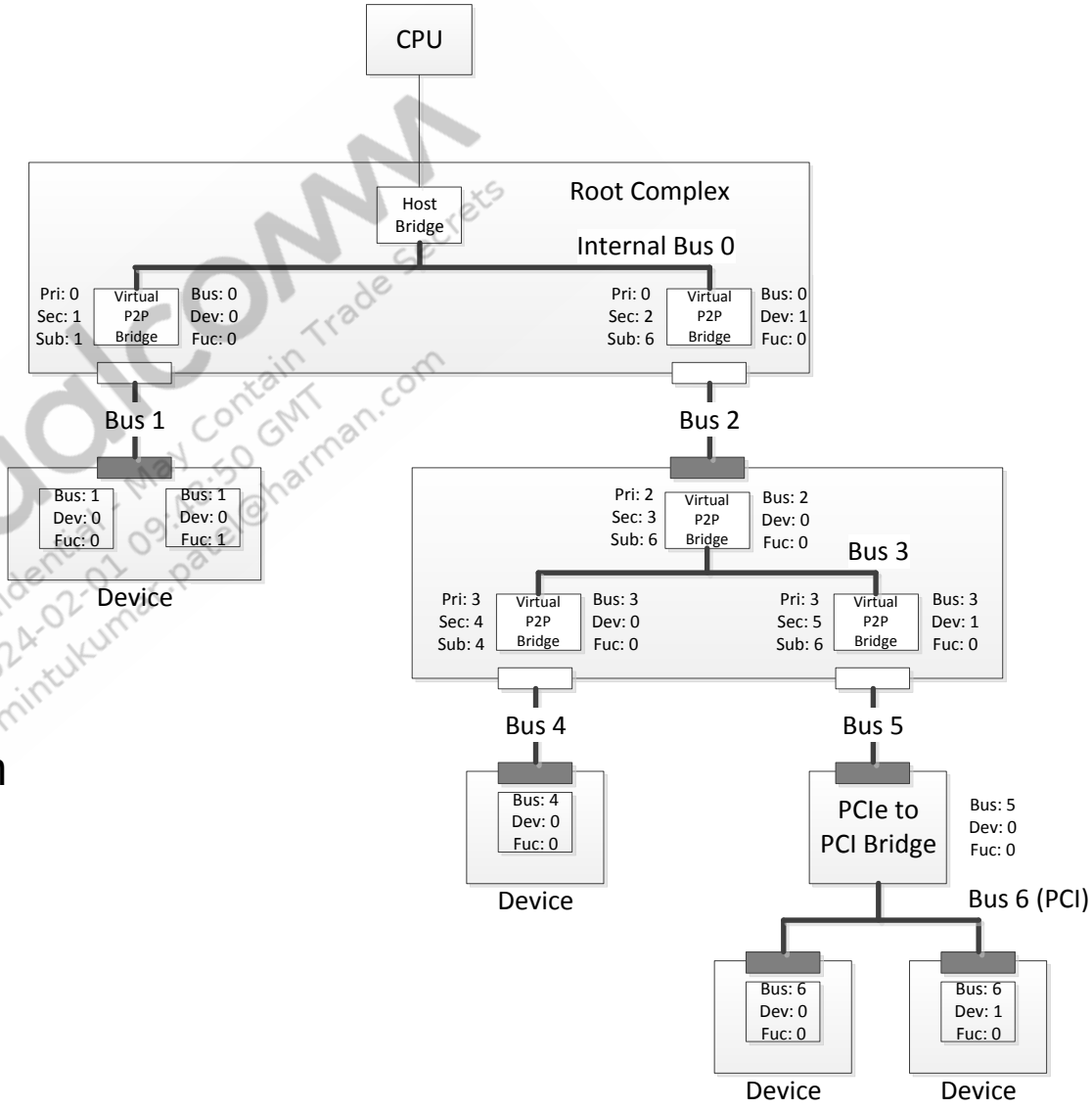
Capability List Entry

- Capability List bit (bit 4) in the Configuration Status register (byte offset 0x06) is set to 1 if the function implements the Capability List
- Capability Pointer register (byte offset 0x34) contains the address of the next entry of the Capability List
- First byte of the next entry of the Capability List is the Capability ID
  - Identifies the supported capability, such as PCI Express Capability register set (0x10), PCI Power Management interface (0x01), and Message Signaled Interrupts (0x05)
- Second byte from the next entry of the Capability List is the address of the next entry
  - If the value is 0, the list terminates



Enumeration Process

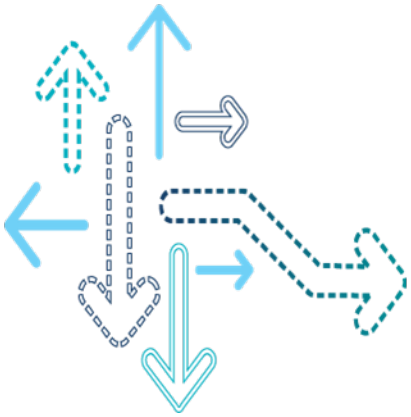
- Discovers if buses, devices, and functions exist in the system
- Assigns a Bus/Device/ Function (BDF) number to each discovered function for ID-based routing
- Primary bus number
  - Number of the bus toward the RC
- Secondary bus number
  - Number of the bus away from the RC
- Subordinate bus number
  - Highest bus number that exists on the downstream side



Interrupts

- Legacy PCI Interrupt
  - PCI bus defines four physical lines (INTA#, INTB#, INTC#, and INTD#) asserted by PCI devices to interrupt the system host processor
  - PCIe defines in-band messages that act as virtual INTx# wires to support legacy PCI devices
- Message Signaled Interrupt (MSI)
  - Eliminates the need for sideband signals
  - It is not based on Message TLP but on Memory Write TLP to a predetermined memory location

References



References

Documents	
QTI	
Application Note: Software Glossary for Customers	CL93-V3077-1
PCI Express Hardware and Software User Guide for APQ8084 and MSM8994 Linux	80-NH717-30

Questions?

https://support.cdmatech.com