

When below log is seen in kernel log, it means that PCIe 0 PHY fails to come up. It will cause that WLAN can't be enabled.

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[ 20.240414] msm_pcie_enable: PCIe: Assert the reset of endpoint of RC0.
[ 20.243640] msm_pcie_enable: PCIe: RC0: PCIE20_PARF_INT_ALL_MASK:
0x7f80c202
[ 20.254830] pcie_phy_init: PCIe PHY RC0 failed to come up!
[ 20.255649] msm_pcie_pm_resume: PCIe: RC0 fail to enable PCIe link in
resume.
[ 20.255652] msm_pcie_pm_control: PCIe: RC0: user failed to resume the
link.
[ 20.255654] cnss: Failed to resume PCI link with default option, err = -
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```

For such issue, it's mainly specific chipset issue. please follow steps as below to check:

1. Do CT scan to see if any pin is cracked.
2. PMIC L5B and L6B is the supply of PCIe 0 and 1. Check if they are well

RC	Rail	Voltage
RC0 (Gen3 power rail)	VREG_L6B_1P2 (PMIC) → VDD_A_PCIE_0_PLL_1P2	1.2 V
	VREG_L5B_0P88 (PMIC) → VDD_A_PCIE_0_CORE (SDM)	0.88 V
RC1 (Gen3 power rail)	VREG_L6B_1P2 (PMIC) → VDD_A_PCIE_1_PLL_1P2	1.2 V
	VREG_L5B_0P88 (PMIC) → VDD_A_PCIE_1_CORE (SDM)	0.88 V

3. For PHY fails to come up, need to check VDD_A_QREFS_0P875 pin is well or not. It's the supply of some internal PHYs like UFS, USB and PCIe. If it's cracked, it's expected that PCIe PHY fails to come up.
4. Check all VDD in the table on the right are well or not.

If one of them is cracked, it will impact L5B or L6B and then impact PCIe function.

PM8350	L5B	PL-N-1200_100-L512-1P0	LDO	PMIC	VPH → VIN_PM8350 → S11B → VDD_L3_L5	0.88000 V (0.83125 -- 0.91875)	1200 mA	OFF	VDD_A_CSI_0P9 VDD_A_DSI_0P9 VDD_A_DSI_PLL_0P9 VDD_A_PCIE_0_CORE VDD_A_PCIE_1_CORE VDD_A_QUINK_0_0P9 VDD_A_QUINK_1_0P9 VDD_A_QUINK_2_0P9 VDD_A_QREFS_0P875 VDD_A_SP_SENSOR VDD_A_UFS_0_CORE VDD_A_UFS_1_CORE VDD_A_USB_HS_CORE VDD_A_USB_SS_CORE
PM8350	L6B	PL-N-1200_100-L512-1P0	LDO	PMIC	VPH → VIN_PM8350 → S12B → VDD_L6_L9_L10	1.20000 V (1.15 -- 1.25)	1200 mA	OFF	DDRRPHY_VDDA_HV VDD_A_CSI_1P2 VDD_A_DSI_1P2 VDD_A_PCIE_0_PLL_1P2 VDD_A_PCIE_1_PLL_1P2 VDD_A_QUINK_HV_CK VDD_A_UFS_0_1P2 VDD_A_UFS_1_1P2 VDD_A_USB_SS_1P2 VDD_A_USB_SS_DP_1P2