Application Report
SNLA076A–October 2005–Revised April 2013

AN-1405 DP83848 Single 10/100 Mb/s Ethernet Transceiver Reduced Media Independent Interface™ (RMII™) Mode

ABSTRACT

This application report summarizes how a designer can take advantage of RMII mode of the DP83848 to provide lower cost system design.

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1 Introduction

National's DP83848 10/100 Mb/s single port Physical Layer device incorporates the low pin count Reduced Media Independent Interface (RMII) as specified in the RMII specification. RMII provides a lower pin count alternative to the IEEE 802.3 defined Media Independent Interface (MII) for connecting the DP83848 PHY to a MAC in 10/100 Mb/s systems.

2 Low Cost System Design with RMII

The Ethernet standard (IEEE 802.3u) defines the MII with 16 pins per port for data and control (8 data and 8 control). The RMII specification reduces the data interfaces from 4-bit (nibble) data to 2-bit (di-bit) data. In addition control is reduced to 3 signals (one of which is optional) and one clock). Thus the total signal connection is reduced to 7 pins (8 pins if RX_ER is required by the MAC).

In systems incorporating many MAC/PHY interfaces, such as switches or port-switched repeaters, the high number of pins can add significant costs as port count increases. For example, in a typical 24-port switch configuration, the RMII mode could reduce the number of MAC pins from 16 to 6 per port (plus a single clock), for a total savings of 239 pins.

While the RMII specification was originally created to address multi-port applications, the reduced connections in RMII can be useful to reduce pin count and signal routing for other applications as well. While the attached device is a switch or any other component with an embedded MAC, the attached device will be referred to as a MAC for the purposes of this document.

Figure 1 shows the RMII mode connection between a MAC and a DP83848 Ethernet Transceiver.

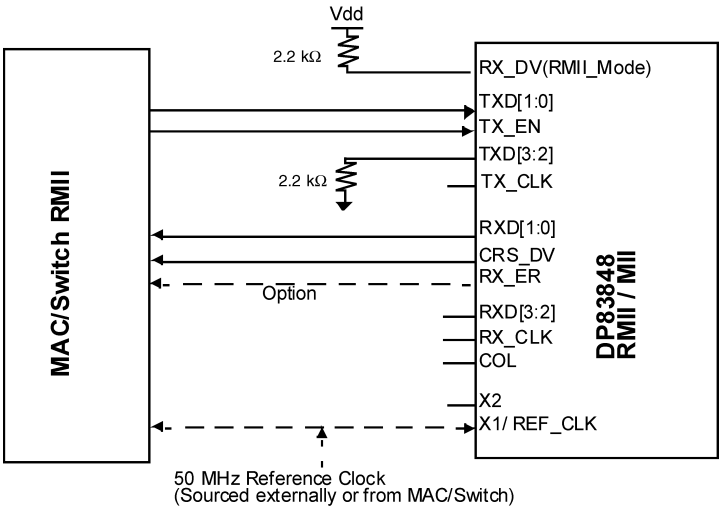

Figure 1. 10/100 Mb/s Twisted Pair Interface

2.1 RMII Mode Features

RMII mode reduces PHY interconnect while maintaining features currently available in the Physical Layer device:

- All the functionality of 802.3u MII
- Operation at either 10 or 100 Mb/s data rates
- Implementation of a single synchronous clock reference that is sourced from the MAC to the PHY (or from an external source), to simplify the clocking interface
- Support for existing features such as full-duplex capability in switches
- Simplified board layout (fewer high speed traces to route)

2.2 Additional Feature of the DP83848

In addition to RMII defined signals, the DP83848 supplies an RX_DV signal (receive data valid) that allows for a simpler method of recovering receive data without having to separate RX_DV from the CRS_DV indication. This is especially useful for systems that do not require CRS, such as systems that only support full-duplex operation. As described later in this document, RX_DV is also useful for Remote Loopback and Full-Duplex Extender operation.

3 Pin and Signal Definitions

Table 1 shows RMII mode pin definitions of the DP83848. Note that the following MII pins are not used in RMII mode:

- RX_CLK
- RXD[3:2]
- COL
- TXD[3:2]
- TX_ER
- TX_CLK

NOTE: TXD[3:2] should be pulled low to put these inputs in a known state.

Table 1. RMII Pin Descriptions

RMII Signal Name	Type	Pin No.	RMII Description
X1/REF_CLK	Input	34	Clock Input
TX_EN	Input	2	RMII Transmit Enable
TXD[0] TXD[1]	Input	3 4	RMII Transmit Data
RX_ER	Output	41	RMII Receive Error (optional connection to MAC)
RXD[0] RXD[1]	Output	43 44	RMII Receive Data
CRS_DV	Output	40	RMII Carrier Sense/Receive Data Valid

3.1 X1 (REF_CLK) — Reference Clock

REF_CLK is a continuous clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_ER. REF_CLK is sourced by the MAC or an external source. REF_CLK is an input to the DP83848 and may be sourced by the MAC or from an external source such as a clock distribution device.

The REF_CLK frequency shall be 50 MHz ± 50 ppm with a duty cycle between 35% and 65% inclusive. The DP83848 uses REF_CLK as the network clock such that no buffering is required on the transmit data path.

In the RMII mode, data is transferred 2-bits at a time using the 50MHz clock. Therefore, RMII mode requires a 50 MHz oscillator be connected to the device X1 pin.

Using a 50 MHz crystal is not supported. Table 2 shows the description of the Clock interface during the RMII mode.

Table 2. RMII Clock

Signal Name	Type	Pin No.	Description
X1/REF_CLK	Input	34	RMII Reference Clock
X2	Output	33	Floating
25MHz_OUT	Output	25	50MHz clock output

The 25MHz_OUT signal is a delayed version of the X1/REF_CLK input. While this clock may be used for other purposes, it should not be used as the timing reference for RMII control and data signals.

3.2 CRS_DV - Carrier Sense/Receive Data Valid

CRS_DV shall be asserted by the PHY when the receive medium is non-idle. The specifics of the definition of idle for 10BASE-T and 100BASE-X are contained in IEEE 802.3. CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. In 10BASE-T mode this occurs when squelch is passed. In 100BASE-X mode this occurs when 2 non-contiguous zeroes in 10 bits are detected.

As defined in the RMII Revision 1.2 specification, loss of carrier results in the deassertion of CRS_DV synchronous to the cycle of REF_CLK which presents the first di-bit of a nibble onto RXD[1:0] (that is, CRS_DV is deasserted only on nibble boundaries). If the DP83848 has additional bits to be presented on RXD[1:0] following the initial deassertion of CRS_DV, then the DP83848 asserts CRS_DV on cycles of REF_CLK which present the second di-bit of each nibble and deasserts CRS_DV on cycles of REF_CLK which present the first di-bit of a nibble. As a result, starting on nibble boundaries, CRS_DV toggles at 25MHz in 100Mb/s mode and 2.5MHz in 10Mb/s mode when CRS ends before RX_DV (that is, the DP83848 still has bits to transfer when the carrier event ends).

Alternatively, the device can be programmed to operate in an RMII Revision 1.0 compatible mode. In this mode, CRS_DV will still be asserted asynchronously with CRS, but will not be deasserted until the last data is transferred. In this mode, CRS_DV does not toggle at the end of the packet. This mode does not allow for accurate recovery of the CRS signal from CRS_DV, but does allow for a simpler MAC implementation.

During a false carrier event, CRS_DV will remain asserted for the duration of carrier activity.

The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] shall be “00” until proper receive signal decoding takes place (see definition of RXD[1:0] behavior).

Figure 2 shows CRS_DV formation for both RMII revision 1.2 and revision 1.0. The number of times CRS_DV may toggle at the end of the packet is dependent on how much data remains in the elasticity buffer following deassertion of CRS. The diagram shows two additional nibbles of data following CRS.

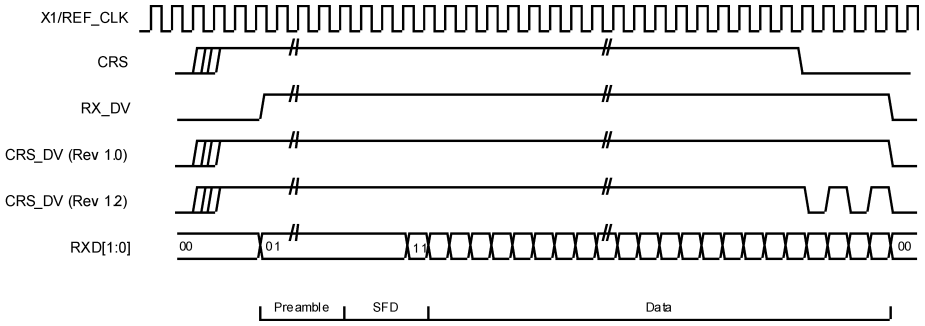

Figure 2. CRS_DV Generation

3.3 RXD[1:0] - Receive Data

RXD[1:0] transitions synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the DP83848. In some cases (for example, before data recovery or during error conditions) a pre-determined value for RXD[1:0] is transferred instead of recovered data. RXD[1:0] is “00” to indicate idle when CRS_DV is deasserted. Upon assertion of CRS_DV, the DP83848 ensures that RXD[1:0]=“00” until proper receive decoding takes place.

The DP83848 will always provide recovered data in nibbles, or pairs of di-bits. This is true for all data values beginning with preamble. Since CRS_DV is asserted asynchronously, the "00" data prior to preamble should not be assumed to be in di-bit pairs.

3.3.1 RXD[1:0] in 100Mb/s

For normal reception following assertion of CRS_DV, RXD[1:0] will be “00” until the receiver has detected a proper Start of Stream Delimiter. Upon detecting the SSD, the DP83848 will drive preamble (“01”) followed by the Start of Frame Delimiter (“01” “01” “01” “11”). The MAC should begin to capture data following the SFD.

If a receive error is detected, the RXD[1:0] is replaced with a receive stream of “01” until the end of carrier activity. By replacing the data in the remainder of the frame, the CRC check in the MAC will reject the packet as errored.

If False Carrier (Bad SSD) is detected, RXD[1:0] will be “10” until the end of the receive event. In this case, RXD[1:0] will transition from “00” to “10” without indicating preamble (“01”).

3.3.2 RXD[1:0] in 10Mb/s

Following assertion of CRS_DV, RXD[1:0] will be “00” until the DP83848 has recovered clock and is able to decode the receive data. Once valid receive data is available, RXD[1:0] will take on the recovered data values, starting with “01” for preamble.

As the REF_CLK frequency is 10 times the data rate in 10Mb/s mode, the value on RXD[1:0] may be sampled every 10th cycle by the MAC.

3.4 RX_ER - Receive Error

The DP83848 provides RX_ER as an output according to the rules specified in IEEE 802.3 (see Clause 24, Figure 24-11 - Receive State Diagram). RX_ER is asserted for one or more REF_CLK periods to indicate that an error (for example, a coding error or other error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY. RX_ER transitions synchronously with respect to REF_CLK.

Since the DP83848 corrupts RXD[1:0] by replacing data with a fixed pattern, the MAC is not required to use the RX_ER signal. Instead, errors will be detected by the CRC checking in the MAC.

3.5 TX_EN - Transmit Enable

TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] for transmission. TX_EN shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented. The MAC should assert TX_EN negated prior to the first REF_CLK rising edge following the final di-bit of a frame.

TX_EN shall transition synchronously with respect to REF_CLK.

3.6 TXD[1:0] - Transmit Data

TXD[1:0] shall transition synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the PHY.

In 10Mb/s operation, as the REF_CLK frequency is 10 times the data rate in 10Mb/s mode, the value on TXD[1:0] must be stable for 10 clocks, allowing the DP83848 to sample every 10th cycle.

3.7 RX_DV - Receive Data Valid

Although not part of the RMII specification, the DP83848 provides the RX_DV signal. RX_DV is the Receive Data Valid signal without combining with CRS. RX_DV is asserted with the first properly recovered data (preamble) or False carrier detection. It is deasserted following transfer of the final di-bit of recovered data. A full-duplex MAC may use this signal to avoid having to recover RX_DV from the CRS_DV signal.

3.8 Collision Detection

The RMII does not provide a Collision indication to the MAC. For half-duplex operation, the MAC must generate its own collision detection from the CRS_DV and TX_EN signals. To do this, the MAC must recover CRS from CRS_DV and logically AND this with TX_EN. Note that CRS_DV cannot be used directly since CRS_DV may toggle at the end of the frame to indicate deassertion of CRS.

4 Configuration of RMII Mode

To operate the DP83848 in RMII mode, a 50MHz external CMOS level Oscillator source must be provided to the RMII Reference CLOCK X1 (Pin 34). In addition, the DP83848 should be strapped to enter RMII mode at power-up or reset.

4.1 RMII Mode Selection

The MII_MODE Strap option determines the operating mode of the MAC Data interface. Default operation will enable normal MII Mode. Strapping MII_MODE (Pin 39) high configures the device to be in RMII mode of operation (see Table 3).

Table 3. Mode Selection

MAC Interface Mode	RMII Mode	RMII Mode Selection
RX_DV/MII_MODE (Pin 39)	1	0

The mode selection is accomplished by applying a pull-up resistor to the RX_DV/MII_MODE pin. The strap option is sampled at initial power-up or during Reset.

4.2 Register Configuration

RMII Mode and Bypass Register (RBR) configures features of the RMII mode of operation (see Table 4). When RMII mode is disabled, the RMII mode functionality is bypassed.

Table 4. RMII Mode and Bypass Register (RBR), address 0x17

Bit	Bit Name	Default	Description
15:6	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0
5	RMII_MODE	Strap, RW	**Reduced MII Mode:** 0 = Standard MII Mode 1 = Reduced MII Mode
4	RMII_REV1_0	0, RW	**Reduced MII Revision 1.0:** This bit modifies how CRS_DV is generated. 0 = (RMII Spec. Revision 1.2) CRS_DV will toggle at the end of a packet to indicate deassertion of CRS. 1 = (RMII Spec. revision 1.0). CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet.
3	RX_OVF_STS	0, RO	**RX FIFO Over Flow Status:** 0 = Normal 1 = Overflow detected
2	RX_UNF_STS	0, RO	**RX FIFO Under Flow Status:** 0 = Normal 1 = Underflow detected
1:0	ELAST_BUF[1:0]	01, RW	**Receive Elasticity Buffer.** This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at +/-50ppm accuracy for both RMII and Receive clocks. For greater frequency tolerance the packet lengths may be scaled (that is, for +/-100ppm, the packet lengths need to be divided by 2). 00 = 14 bit tolerance (up to 16800 byte packets) 01 = 2 bit tolerance (up to 2400 byte packets) 10 = 6 bit tolerance (up to 7200 byte packets) 11 = 10 bit tolerance (up to 12000 byte packets)

4.3 RMII Mode Programmable Elasticity Buffer

To tolerate potential frequency differences between the 50MHz reference clock and the recovered receive clock, the receive RMII mode function includes a programmable elasticity buffer.

For robust operation, the elasticity buffer is programmable to allow for minimizing propagation delay based on expected packet size and clock accuracy. This provides support for a rage of packet sizes including jumbo frames The elasticity buffer can detect both overrun and underrun conditions and will force Frame Check Sequence errors for packets which Overrun or Underrun the FIFO. Underrun and Overrun conditions can be reported in RMII mode and Bypass Register (RBR).

Table 5 indicates how to program the elasticity buffer FIFO (in 4-bit increments) based on expected maximum packet size and clock accuracy. It assumes both clocks (RMII Reference clock and far-end Transmitter clock) have the same accuracy.

Table 5. Supported Packet Sizes at ± 50ppm and ± 100ppm for Each Clock

Start Threshold RBR[1:0]	Latency Tolerance	Recommended Packet Size at ± 50ppm	Recommended Packet Size at ± 100ppm
1 (4-bits)	2 bits	2400 bytes	1200 bytes
2 (8-bits)	6 bits	7200 bytes	3600 bytes
3 (12-bits)	10 bits	12000 bytes	6000 bytes
0 (16-bits)	14 bits	16800 bytes	8400 bytes

4.4 RMII Loopback Operation

The DP83848 supports Loopback operation at the MAC Interface in RMII mode. The Loopback operation is enabled in the same manner as for MII operation, by setting the Loopback control bit in the BMCR register (address 0x00, bit 14). Since collision detection is handled by the MAC, the MAC must be sure to disable its collision detection during loopback.

5 Remode Loopback for Diagnostics

Since the RMII Transmit and Receive signals are synchronous to the same clock, it is possible to implement a Remote Loopback using external connections. This operation allows diagnostic testing where it may be desirable to receive data on the Physical Media and loop that data back to the transmitter, providing a remote loopback for the far-end link partner. The following connections need to be made external to the DP8384:

- Connect RXD[1:0] to TXD[1:0]
- Connect RX_DV to TX_EN

Note that CRS_DV cannot be used to frame the packet since it is asserted at CRS rather than at the first preamble data of the packet. In addition, the device needs to be configured for RMII mode. Figure 3 shows the connections.

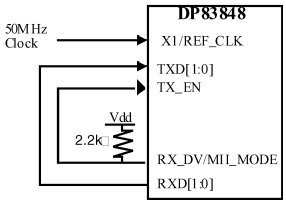

Figure 3. Remote Loopback Connection

6 Full-Duplex Extender Operation

Two DP83848 devices can be used to implement a simple full-duplex extender. A full-duplex extender allows a simple method of providing longer cabling distance than the standard 100 meters. By connecting two DP83848's in a back-to-back fashion at the RMII, packets received from one DP83848 may be transmitted directly by the other DP83848 without need for any additional buffering or control. This method will not work for half-duplex since there is not a MAC involved to handle recovery from collisions. In addition, both devices must be operating at the same data rate (that is, 10Mb/s or 100Mb/s).

The following connections need to be made to connect from each DP83848 to the other:

- Connect RXD[1:0] to TXD[1:0]
- Connect RX_DV to TX_EN

Figure 4 shows the connections.

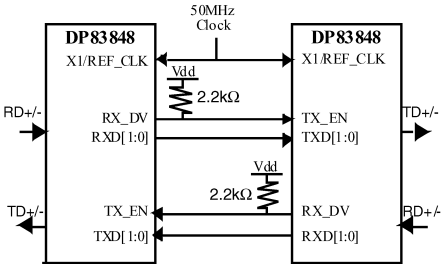

Figure 4. Full-Duplex Extender Connection

7 RMII Interface Timing Requirements

Figure 5 and Figure 6 show the timing requirements for the DP83848 in RMII mode. In addition, the diagrams show the approximate latency for transmit and receive data paths between the RMII and Physical layer for 100Mb/s operation.

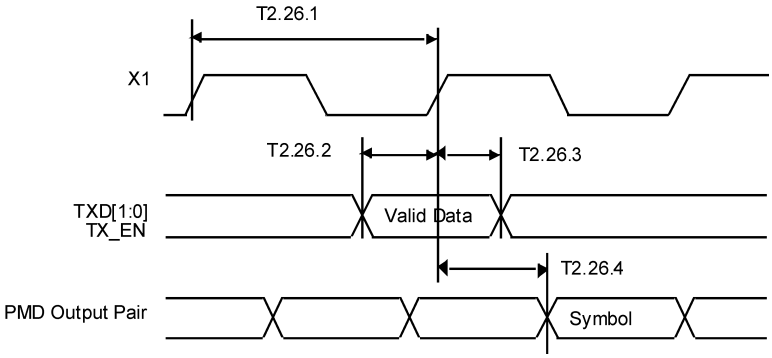

Figure 5. RMII Transmit Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T2.26.1	X1 Clock Period	50 MHz Reference Clock		20		ns
T2.26.2	TXD[1:0], TX_EN, Data Setup to X1 rising		4			ns
T2.26.3	TXD[1:0], TX_EN, Data Hold from X1 rising		2			ns
T2.26.4	X1 Clock to PMD Output Pair Latency	From X1 Rising edge to first bit of symbol		17		bits

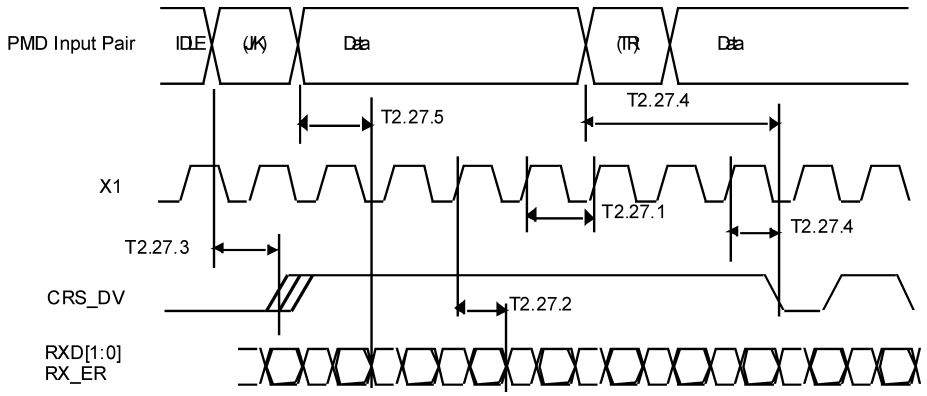

Figure 6. RMII Receive Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T2.27.1	X1 Clock Period	50 MHz Reference Clock		20		ns
T2.27.2	RXD[1:0], CRS_DV and RX_ER output delay from X1 rising		2		14	ns
T2.27.3	CRS ON delay	From JK symbol on PMD Receive Pair to initial assertion of CRS_DV		18.5		bits
T2.27.4	CRS OFF delay	From TR symbol on PMD Receive Pair to initial deassertion of CRS_DV		27		bits
T2.27.5	RXD[1:0] and RX_ER latency	From symbol on Receive Pair. Elasticity buffer set to default value (01)		38		bits

8 Summary

The DP83848 implements the RMII standard interface to provide a connection option that reduces the number of pins needed for a MAC to PHY interface. It allows the designer to minimize the cost of the system design while maintaining all the features of the IEEE 802.3 specification.

9 Reference

RMII Specification Rev 1.0

RMII Specification Rev 1.2

IEEE Standards 802.3-2002

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