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PRELIMINARY

CYW8x570

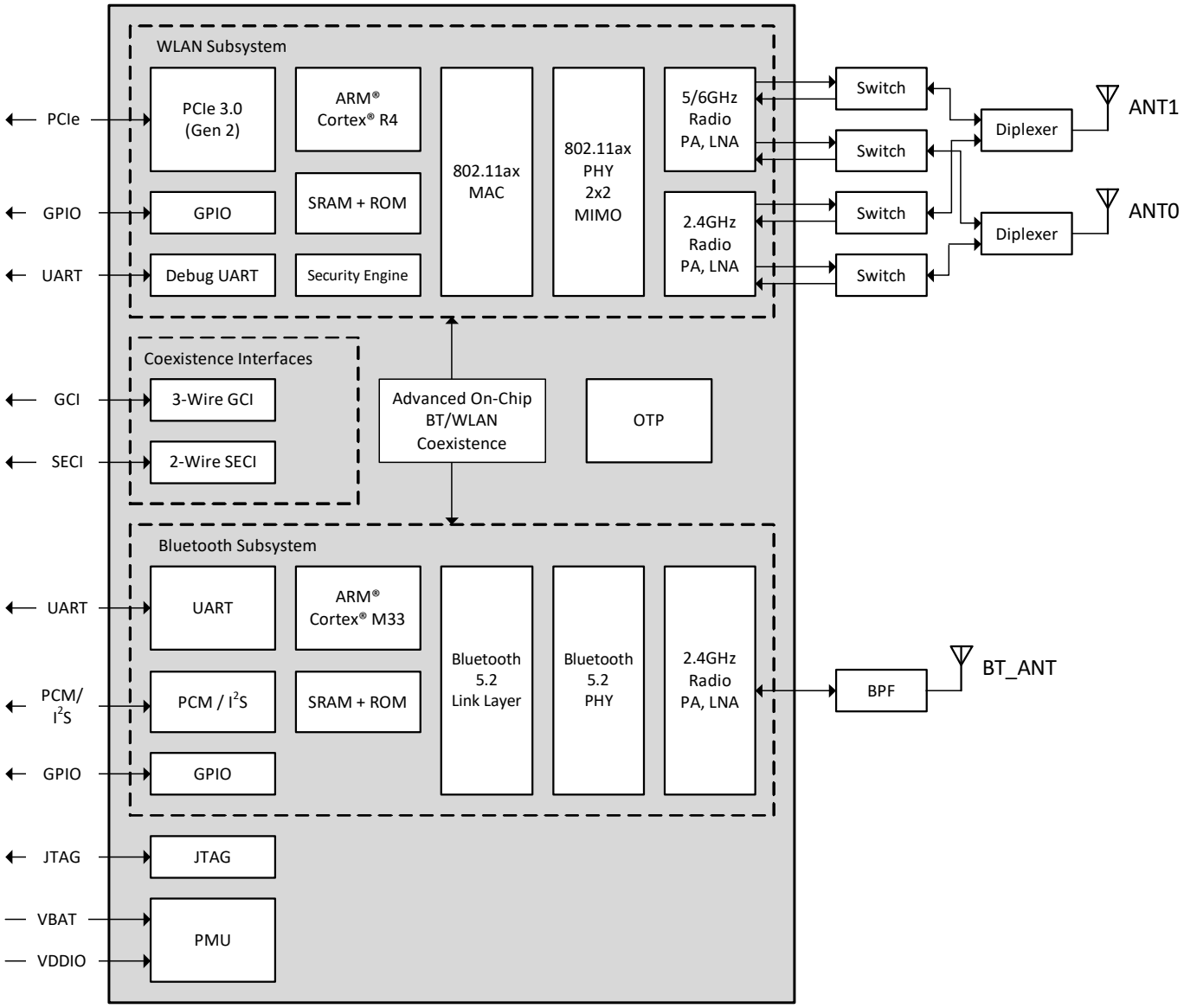
Single-chip Tri-band 802.11ax 2x2 MIMO Wi-Fi with Bluetooth 5.2 for Automotive Applications

The Cypress CYW8x570 single-chip device provides the highest level of integration for Automotive and Industrial IoT wireless systems with integrated tri-band 2x2 MIMO IEEE 802.11ax WLAN MAC/baseband/radio, Bluetooth 5.2 MAC/baseband/radio, and integrated Power Management Unit. WLAN and Bluetooth radios also include on-chip power amplifiers and low-noise amplifiers to further reduce the need for external components.

WLAN interfaces to host processor through a PCIe v3.0 Gen2 interface while Bluetooth host interface is provided through high-speed 4-wire UART interface. Additionally, the Bluetooth section supports PCM and I2S interfaces for audio applications. CYW8x570 is qualified to operate across Automotive Grade 3 (-40°C to +85°C) temperature range.

CYW89570 parts receive Automotive grade testing and CYW88570 parts receive Industrial grade testing. Both CYW89570 and CYW88570 parts are AEC Q-100 tested and manufactured in ISO9001/TS16949 certified fabrication facilities.

Figure 1. CYW8x570 Functional Block Diagram



Features

WLAN

- 802.11a/b/g/n/ac/ax compliant, Tri-band capable (2.4/5/6GHz)
- 5/6 GHz: 20/40/80-MHz channels, 1024-QAM, 2x2 MIMO providing up to 1.2Gbps PHY data rate
- 2.4 GHz: 20/40-MHz channels, 1024-QAM, 2x2 MIMO providing up to 574Mbps PHY date rate
- 802.11ax STA mode and Soft AP mode with 11ax scheduled access
- Supports 802.11d, h, k, r, v, w, ai
- Zero-wait dynamic frequency selection (DFS): Background channel availability check (CAC) scan for immediate switch to candidate DFS channel
- On-chip power amplifiers and low-noise amplifiers
- Supports 2 and 3-antenna configurations
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE
- Fast VSDB (Virtual Simultaneous Dual Band)
- Security:
  - WPA, WAPI STA, WPA2 (Personal) and WPA3 (Personal) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design
- Integrated Arm® Cortex ® R4 processor with tightly coupled memory for complete WLAN subsystem functionality. This architecture offloads the host processor completely from WLAN functionality.
- GPIOs: 15

Bluetooth

- Bluetooth 5.2 (BDR + EDR + BLE)
- All Bluetooth 5.0/5.1/5.2 optional features supported including LE-Audio
- Dedicated Bluetooth RF path for best WLAN-BT coexistence performance
- Bluetooth Class 1 or Class 2 transmitter operation
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Adaptive frequency hopping (AFH) for reducing radio frequency interference
- Interface support, host controller interface (HCI) using a high-speed UART interface and PCM/I2S for audio data
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound
- On-chip memory includes 512 KB SRAM and 2MB ROM
- GPIOs: 10

Interfaces

- PCIe Gen2 (3.0 Compliant) for WLAN: complies with PCI Express base specification revision 3.0 for ×1 lane and power management running at Gen2 speeds
- HCI-UART, PCM/I2S for BT

Coexistence

- Built-in advanced algorithms for BT/WLAN coexistence
- 2-wire SECI for external 3rd party BT/GPS/LTE radios

General

- Fully integrated programmable dynamic Power Management Unit
- Supports VBAT power supply range from 3.0 V to 4.8 V with internal regulator
- Supports 1.8V VDDIO
- Supports 1340 Bytes of OTP shared between BT and WLAN for storing board parameters
- Package: FCBGA 12x12mm (0.65mm ball pitch)
- 4-layer reference PCB design with no blind- and buried-vias, only through-hole via

Figure 2. CYW8x570 Functional Block Diagram—Three Antenna System

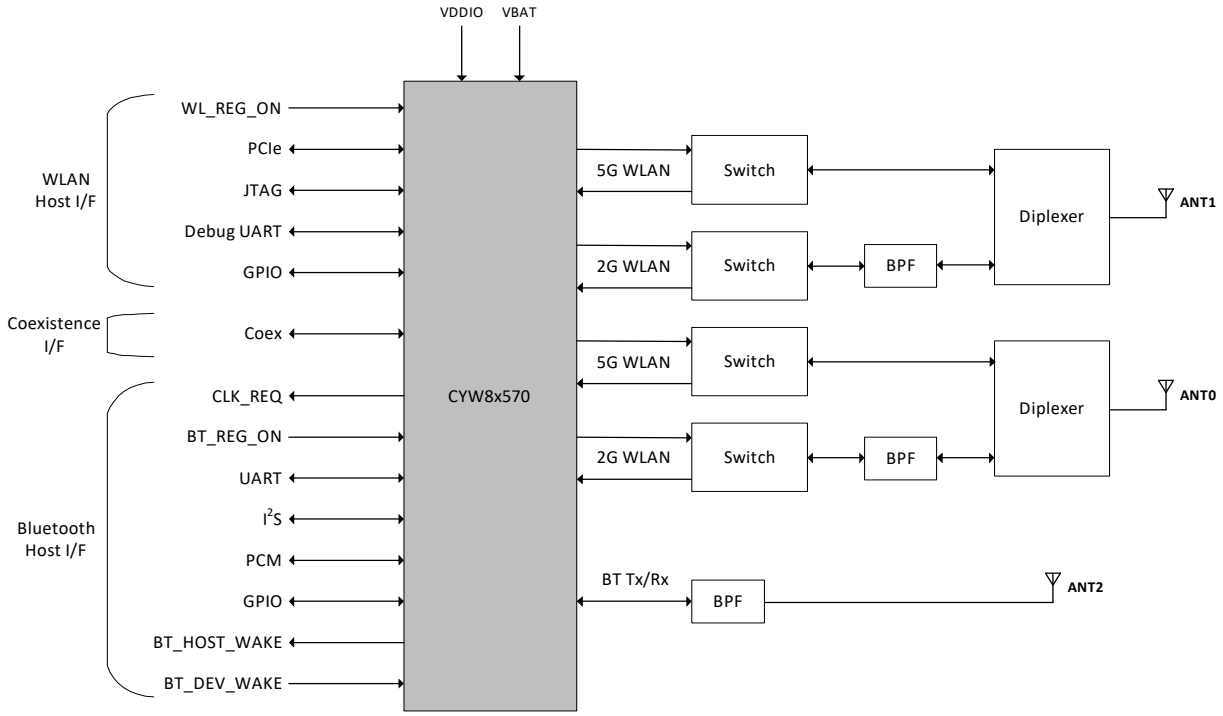
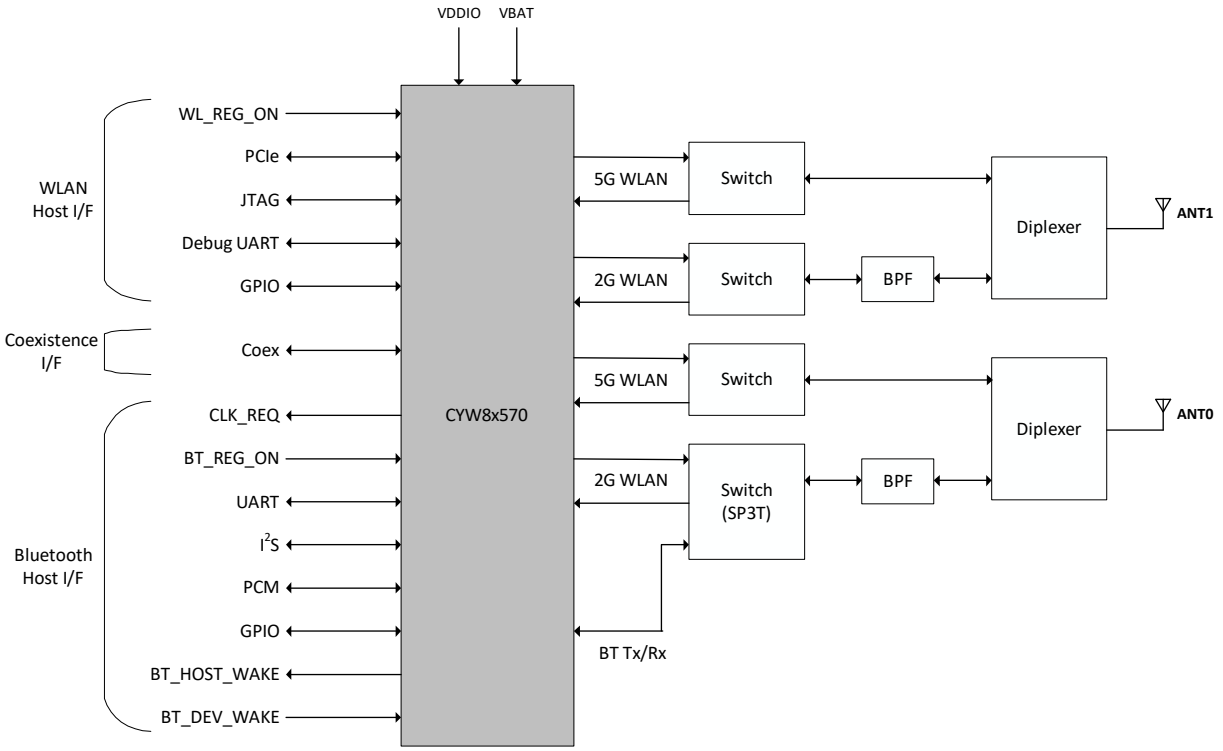


Figure 3. CYW8x570 Functional Block Diagram—Two Antenna System



Note Cypress recommends using a 3-antenna system to utilize the device's complete functionality: WLAN 2x2 MIMO in both 5 GHz and 2.4 GHz bands and Bluetooth concurrently

Contents

1. Overview

1.1 Overview

The Cypress CYW8x570 single-chip device provides the highest level of integration for Automotive Infotainment and Telematics systems, with integrated IEEE 802.11 a/b/g/n/ac/ax MAC/baseband/radio (dual-core 2×2 MIMO), Bluetooth 5.2+ Isochronous. It provides a small form-factor solution with minimal external components to drive down cost and allows for platform design flexibility in size, form, and function.

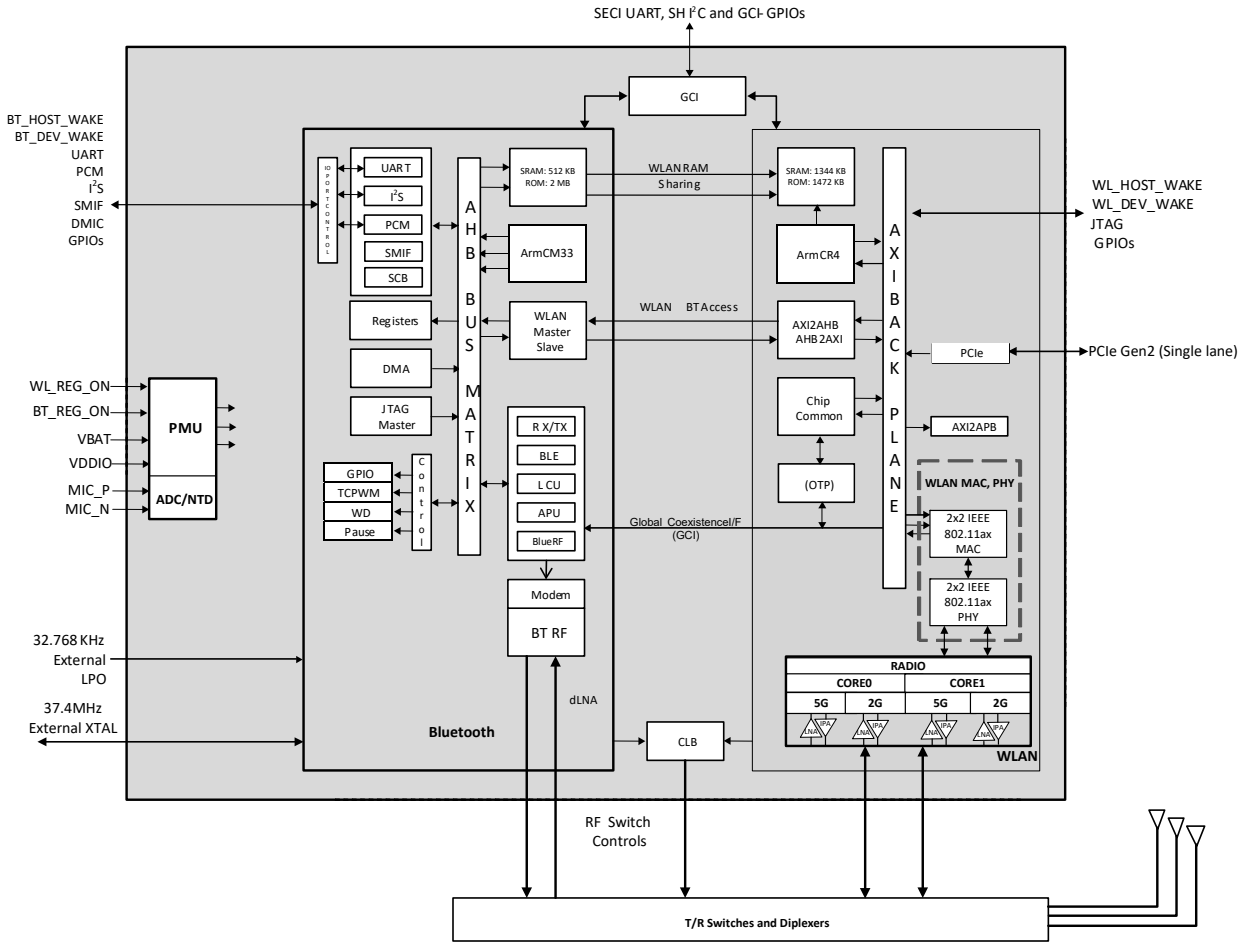
Table 1. Device Options and Features

Feature	FCBGA
Package ball count	289 balls
PCIe	Yes
UART	Yes
I^2S	Yes
GPIO	25

Figure 4 shows the interconnection of all the major physical blocks in CYW8x570.

The Interconnection interfaces are described in greater detail in the subsequent sections of this document.

Figure 4. CYW8x570 System Block Diagram



1.2 Standards Compliance

CYW8x570 supports the following standards:

- Bluetooth 2.1 + EDR, 3.0, 4.2, 5.0, 5.1, 5.2
- IEEE 802.11ax
- IEEE 802.11ac mandatory and optional requirements for 20 MHz, 40 MHz, and 80 MHz channels
- IEEE 802.11a/b/g/n
- IEEE 802.11d/h
- IEEE 802.11i
- Security:
  - WEP, WPA/WPA2/WPA3 personal, WMM, WMM-PS (U-APSD), WMM-SA, AES (hardware accelerator), TKIP (hardware accelerator), and CKIP (software support)
- IEEE 802.11r (fast roaming between APs)
- IEEE 802.11w (secure management frames)
- IEEE 802.11 extensions:
  - IEEE 802.11e QoS enhancements (In accordance with the WMM specification, QoS is already supported.)
  - IEEE 802.11h 5 GHz extensions
  - IEEE 802.11i MAC enhancements

2. Power Supplies and Power Management

2.1 Power Supply Topology

Two Buck regulators, multiple LDO regulators, and a power management unit (PMU) are integrated into CYW8x570. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.

CYW8x570 only requires two power supplies, VBAT and VDDIO, to be provided, with all additional voltages being generated by on-chip regulators.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The two core Buck regulators, CBUCK and ABUCK, power up when either BT_REG_ON or WL_REG_ON are asserted. All regulators, Buck and LDO, are powered down when both BT_REG_ON and WL_REG_ON are deasserted.

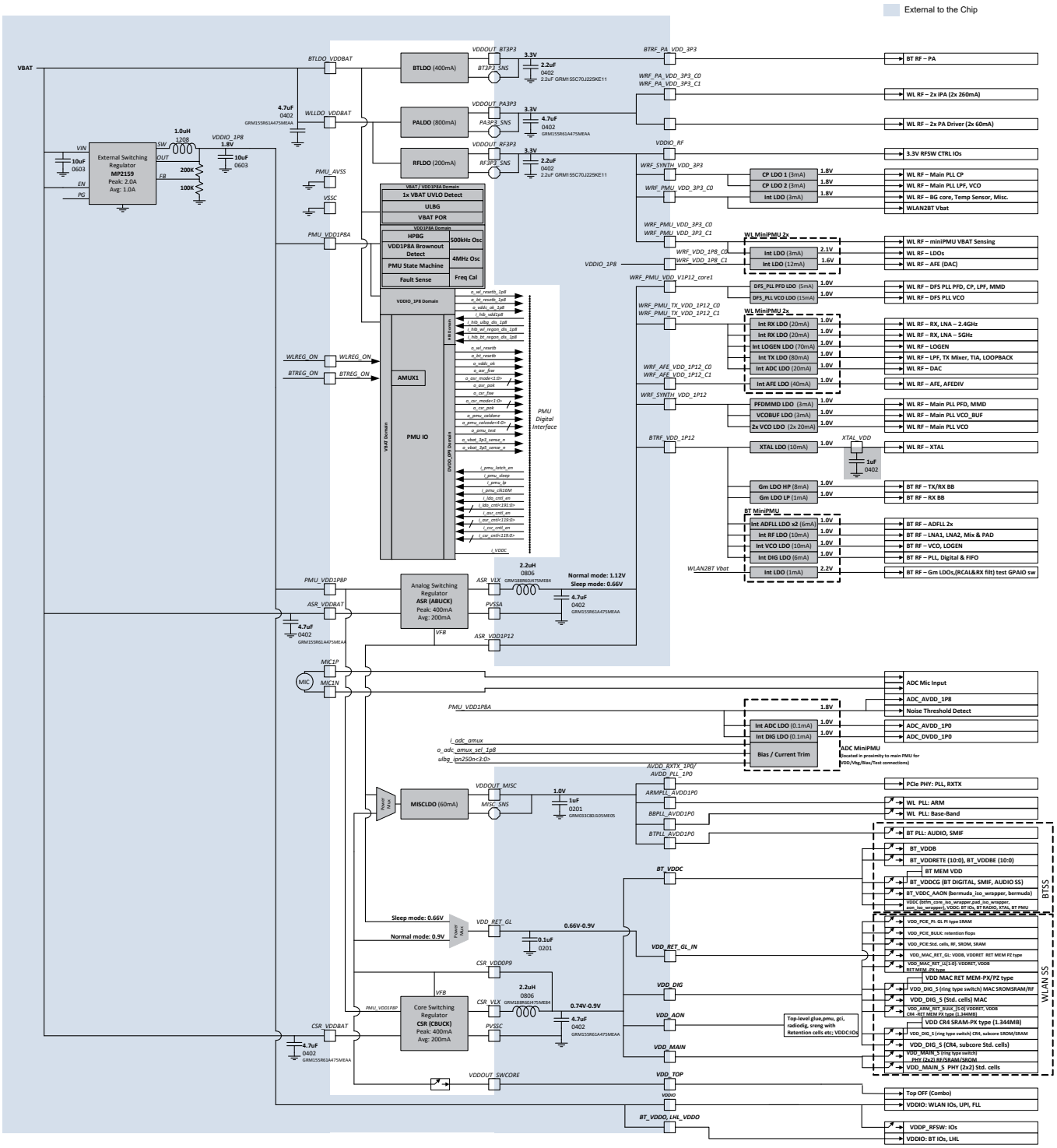
CYW8x570 allows for an extremely low power-consumption mode by completely shutting down the CBUCK and ABUCK regulators. In this extremely low power state, MEMLPLDO and LPLDO (which are a low-power linear regulators supplied by the system VDDIO supply) provide CYW8x570 with all the voltages it requires, thereby reducing leakage currents.

2.2 CYW8x570 PMU Features

- Core Switching Regulator (400 mA)
- Analog Switching Regulator (400 mA)
- BTLDO (300 mA)
- PALDO (800 mA)
- RFLDO (150 mA)
- VDDOUT_MISC (60 mA)

Figure 5 and WLAN Power Management on page 10 illustrate the typical power topology for CYW8x570. The shaded areas are external to CYW8x570.

Figure 5. Typical Power Topology



2.3 WLAN Power Management

CYW8x570 has been designed with the stringent performance requirements of automotive applications in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW8x570 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. CYW8x570 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting CYW8x570 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

CYW8x570 WLAN power states are described as follows:

- Active mode — All WLAN blocks in CYW8x570 are powered up and fully functional with active carrier sensing and frame transmission and reception. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Deep-sleep mode — Most of the chip including both analog and digital domains and most of the regulators are powered off. All main clocks (PLL, crystal oscillator, or TCXO) are shut down to reduce active power to the minimum. The PMU sequencer uses the 32.768 kHz LPO clock to keep track of time and wake up the chip and transition to Active mode as scheduled. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization. In Deep-sleep mode, the primary source of power consumption is leakage current.
- Power-down mode — CYW8x570 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

CYW8x570 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When CYW8x570 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows CYW8x570 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDIO remains applied to CYW8x570, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables CYW8x570 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When CYW8x570 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

2.6 Power-Up/Power-Down/Reset Circuits

CYW8x570 has two signals (see Table 2) that enable or disable Bluetooth and WLAN circuits and internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Power-Up Sequence and Timing on page 83.

Table 2. Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW8x570 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, all the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, all the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default and it can be disabled through programming.
BT_REG_ON	This signal is used by the PMU to power up the BT section. It is also OR-gated with the WL_REG_ON input to control the internal CYW8x570 regulators. When this pin is high, the regulators are enabled and the BT section is out of reset. When this pin is low, the BT section is in reset. If BT_REG_ON and WL_REG_ON are both low, all the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default and can be disabled through programming.

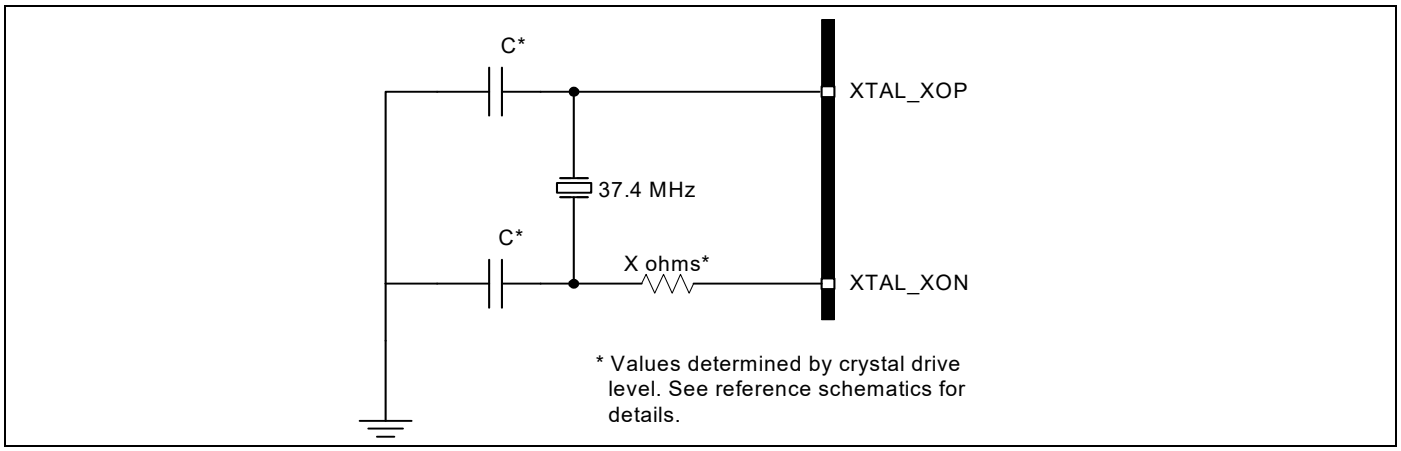
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. A 32.768 kHz clock is also required for low-power-mode timing.

3.1 Crystal Interface and Clock Generation

CYW8x570 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 6. Consult the reference schematics for the latest configuration.

Figure 6. Recommended Crystal Oscillator Configuration



A fractional-N synthesizer in CYW8x570 generates radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal oscillator interface are listed in Table 3.

Note Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

Table 3. Crystal Oscillator—Requirements and Performance

Parameter	Conditions/Notes	Crystal[1]			
		Min.	Typ.	Max.	Unit
Frequency	2.4G, 5G and 6G bands: IEEE 802.11ac/ax operation	–	37.4	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[2]	Without trimming	–20.0	–	20.0	ppm
Crystal load capacitance	–	–	12.0	–	pF
ESR	–	–	–	60.0	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	µW
Input impedance XTAL_XOP	Resistive	–	–	–	kΩ
	Capacitive	–	–	7.5	pF

Notes
1. Use XTAL_XOP and XTAL_XON.
2. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

3.2 External Frequency Reference

As an alternative to a crystal, an external precision frequency reference can be provided. The recommended default frequency is 37.4 MHz, and it must meet the requirements listed in Table 4.

The external frequency reference should be connected to the XTAL_XOP pin through an external 1000 pF coupling capacitor, as shown in Figure 7. The internal clock buffer connected to this pin will be turned OFF when CYW8x570 goes into sleep mode.

When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the WRF_XTAL_-VDD1P5 pin.

Figure 7. Recommended Circuit to Use with an External Reference Clock

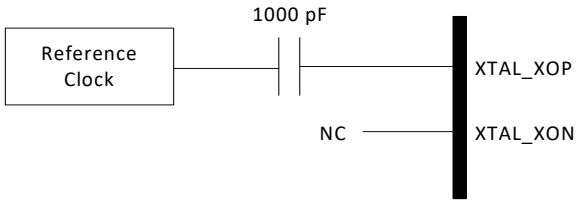


Table 4. External Clock—Requirements and Performance

Parameter	Conditions/Notes	External Frequency Reference			
		Min.	Typ.	Max.	Unit
Frequency	2.4G, 5G and 6G bands: IEEE 802.11ac/ax operation	–	37.4	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[3]	Without trimming	–20.0	–	20	ppm
Input impedance (XTAL_XOP)	Resistive	30.0	100	–	kΩ
	Capacitive	–	–	7.5	pF
XTAL_XOP Input low level	DC-coupled digital signal	0	–	0.2	V
XTAL_XOP Input high level	DC-coupled digital signal	1.0	–	1.26	V
XTAL_XOP input voltage (see Figure 7)	AC-coupled analog signal	400	–	1200	mV_{p-p}
Duty cycle	37.4 MHz clock	40.0	50.0	60.0	%
Phase Noise (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–136	dBc/Hz
Phase Noise[4] (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–137	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–144	dBc/Hz
Phase Noise[4] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–141	dBc/Hz
Phase Noise[4] (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–142	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–149	dBc/Hz
Phase Noise[4] (IEEE 802.11ac, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–150	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–157	dBc/Hz
Phase Noise[4] (IEEE 802.11ax, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–152	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–159	dBc/Hz

Notes
3. It is the responsibility of the equipment designer to select oscillator components that comply with these Specifications.
4. Assumes that external clock has a flat phase noise response above 100 kHz.

3.3 External 32.768 kHz Low-Power Oscillator

CYW8x570 requires an external low-frequency clock for low-power mode timing. An external 32.768 kHz precision oscillator which meets the requirements listed in Table 5 must be used.

Table 5. External 32.768 kHz Sleep Clock Specifications

Parameter	LPO Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30 – 70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[5]	> 100k	Ω
	< 5	pF
Clock jitter (during initial startup)	< 10,000	ppm

Note
5. When power is applied or switched off.

4. Bluetooth Subsystem Overview

The Cypress CYW8x570 is a Bluetooth 5.2 + EDR-compliant, baseband processor and 2.4 GHz transceiver. It features the highest level of integration and eliminates the need for all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth solution.

CYW8x570 is the optimal solution for any Bluetooth voice and/or data application. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high-speed UART and PCM for audio. CYW8x570 incorporates all Bluetooth 5.2 features including AoA/AoD direction finding, LE-Audio and LE Isochronous Channels.

The Bluetooth transmitter also features a power amplifier with programmable Class 1 and Class 2 capabilities.

4.1 Features

- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 4.0 + EDR features:
  - Adaptive frequency hopping (AFH)
  - Quality of service (QoS)
  - Extended synchronous connections (eSCO)—Voice Connections
  - Fast connect (interlaced page and inquiry scans)
  - Secure simple pairing (SSP)
  - Sniff subrating (SSR)
  - Encryption pause resume (EPR)
  - Extended inquiry response (EIR)
  - Link supervision timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.2, 5.0, 5.1, and 5.2 packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see Host Controller Power Management on page 18)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

4.2 Bluetooth Radio

CYW8x570 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless frequency band. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

4.2.1 Transmit

CYW8x570 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter is compatible with Bluetooth Low Energy specification. The transmitter PA can be programmed to provide Bluetooth class 1 or class 2 operation.

4.2.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

4.2.3 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

4.2.4 Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. For applications in which Bluetooth is integrated next to a cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

4.2.5 Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables CYW8x570 to be used in most applications with minimal off-chip filtering. For applications, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

4.2.6 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

4.2.7 Receiver Signal Strength Indicator

The radio portion of CYW8x570 provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

4.2.8 Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. CYW8x570 uses an internal RF and IF loop filter.

4.2.9 Calibration

The CYW8x570 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

5. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

5.1 Bluetooth 5.2 and 4.2 Features

The BBC supports all Bluetooth 5.2 and 4.2 features, with the following benefits:

- Dual-mode Bluetooth low energy (BT and BLE operation)
- BLE LE-2Mbps mode, LE-Long Range mode, Advertising Extensions, Slot Availability Masks
- Extended inquiry response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption pause resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure simple pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link supervision time out (LSTO): Additional commands added to HCI and link management protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

5.2 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth link controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

5.3 Test Mode Support

CYW8x570 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test mode, CYW8x570 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - Eight-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

5.4 Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core.

The power management functions provided by CYW8x570 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management

5.4.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

5.4.2 Host Controller Power Management

When running in UART mode, CYW8x570 may be configured so that dedicated signals are used for power management hand-shake between CYW8x570 and host. The basic power saving functions supported by those hand-shake signals include the standard Bluetooth defined power savings modes and standby modes of operation.

Table 6 describes the power-control hand-shake signals used with the UART interface.

Table 6. Power Control Pin Description

Signal	Type	Description
BT_DEV_WAKE	I	Bluetooth device wake-up: Signal from host to CYW8x570 indicating that the host requires attention. ■Asserted: The Bluetooth device must wake-up or remain awake. ■Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	O	Host wake up. Signal from CYW8x570 to the host indicating that CYW8x570 requires attention. ■Asserted: host device must wake-up or remain awake. ■Deasserted: host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ	O	CYW8x570 asserts CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock. CLK_REQ polarity is active-high.

Note Pad function Control Register is set to 0 for these pins. See DC Characteristics on page 54 for more details.

5.4.3 BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, CYW8x570 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When CYW8x570 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows CYW8x570 to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

  During the low-power shut-down state, provided VDDIO remains applied to CYW8x570, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables CYW8x570 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

  Two CYW8x570 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (XTAL_XOP) and the 32.768 kHz input (LPO_IN). When CYW8x570 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

5.4.4 Wideband Speech

CYW8x570 provides support for wideband speech (WBS) using on-chip SmartAudio® technology. CYW8x570 can perform subband codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 Kbps rate) transferred over the PCM bus.

5.4.5 Packet Loss Concealment

Packet Loss Concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream.

Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. CYW8x570 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 8 and Figure 9 show audio waveforms without and with Packet Loss Concealment. Cypress PLC/BEC algorithms also support wide band speech.

Figure 8. CVSD Decoder Output Waveform Without PLC

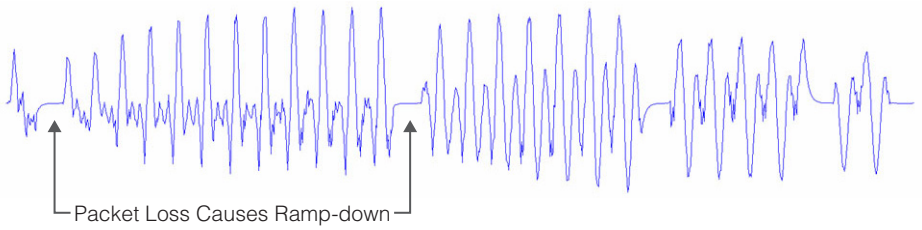
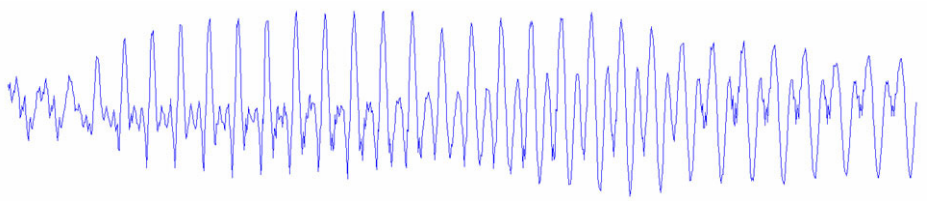


Figure 9. CVSD Decoder Output Waveform After Applying PLC



5.4.6 Audio Rate-Matching Algorithms

CYW8x570 has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth data rates.

5.4.7 Codec Encoding

CYW8x570 can support SBC and mSBC encoding and decoding for wideband speech.

5.4.8 Multiple Simultaneous A2DP Audio Stream

CYW8x570 has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

5.4.9 Burst Buffer Operation

CYW8x570 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

5.5 Adaptive Frequency Hopping

CYW8x570 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

5.6 Advanced Bluetooth/WLAN Coexistence

CYW8x570 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at Automotive infotainment applications such as WLAN + eSCO and WLAN + High Fidelity BT Stereo.

It is recommended that WLAN and Bluetooth have separate dedicated antennae for maximum simultaneous traffic. However, CYW8x570 is also capable of supporting platforms that share an antenna between WLAN and Bluetooth. Advanced Bluetooth/WLAN coexistence algorithms allow for simultaneous WLAN and Bluetooth reception and transmit antenna arbitration.

CYW8x570 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

CYW8x570 also supports Transmit Power Control on the WLAN STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core's channel information.

5.7 Fast Connection (Interlaced Page and Inquiry Scans)

CYW8x570 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

6. Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the Arm Cortex-M33 with embedded ICE-RT debug and JTAG interface units.

The Arm core is paired with a memory unit that contains 2 MB of ROM memory for program storage and boot ROM, and 512 KB of RAM for data scratch-pad and patch RAM code. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to CYW8x570 through the UART transports.

6.1 RAM, ROM, and Patch Memory

CYW8x570 Bluetooth core has 512 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 2 MB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

6.2 Reset

CYW8x570 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes High. If BT_REG_ON is low, then the POR circuit is held in reset.

7. Bluetooth Peripheral Transport Units

7.1 Media Transports

CYW8x570 supports HFP and A2DP codec controllers with optimized I^2S and PCM transports for Bluetooth audio.

HFP codec interface controller:

- Supported by PCM and I^2S transports and bi-directional operations.
- PCM
  - Sample rates 8k for NBS and 16k for WBS supported.
  - Dual stream use cases can concurrently use NBS and WBS.
  - Sample width is limited to 16-bits.
  - Synchronization clock width of 1 or 3 (short or long).
  - Bit clocks of 128k, 256k, 512k, 1024k and 2024k, the only difference being the number of 16bit slots.
  - HFP samples can be taken from any available slot. Slot 0 is the default slot.
- I^2S
  - Supports bit clocks of 256k (NBS) and 512K (WBS).
  - HFP samples can be taken from either left or right. Left is the default.

A2DP codec controller:

- Supported by I^2S transport in a single direction, either in or out but not both.
- Two channels, left and right. Mono is not supported.
- Sample rates: 44.1k or 48k.
- Sample width is limited to 16-bits.
- Supports bit clocks of 32 times the sample rate, 1.411200 (44.1k) or 1536000 (48k) and not adjustable.

7.1.1 PCM Interface

CYW8x570 supports two independent PCM interfaces that share the pins with the I^2S interfaces. The PCM Interface on CYW8x570 can connect to linear PCM codec devices in Master/Slave mode. In Master mode, CYW8x570 generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in Slave mode, these signals are provided by another master on the PCM interface and are inputs to CYW8x570.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

7.1.1.1 Slot Mapping

CYW8x570 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from a SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

7.1.1.2 Frame Synchronization

CYW8x570 supports both short and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

7.1.1.3 Data Formatting

CYW8x570 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, CYW8x570 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked Most Significant Bit (MSb) first.

7.1.1.4 Wideband Speech Support

When the host encodes WBS packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. CYW8x570 also supports slave transparent mode using a proprietary rate-matching scheme. In SBCcode mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

7.1.1.5 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

7.1.1.6 PCM Interface Timing

Short Frame Sync, Master Mode

Figure 10. PCM Timing Diagram (Short Frame Sync, Master Mode)

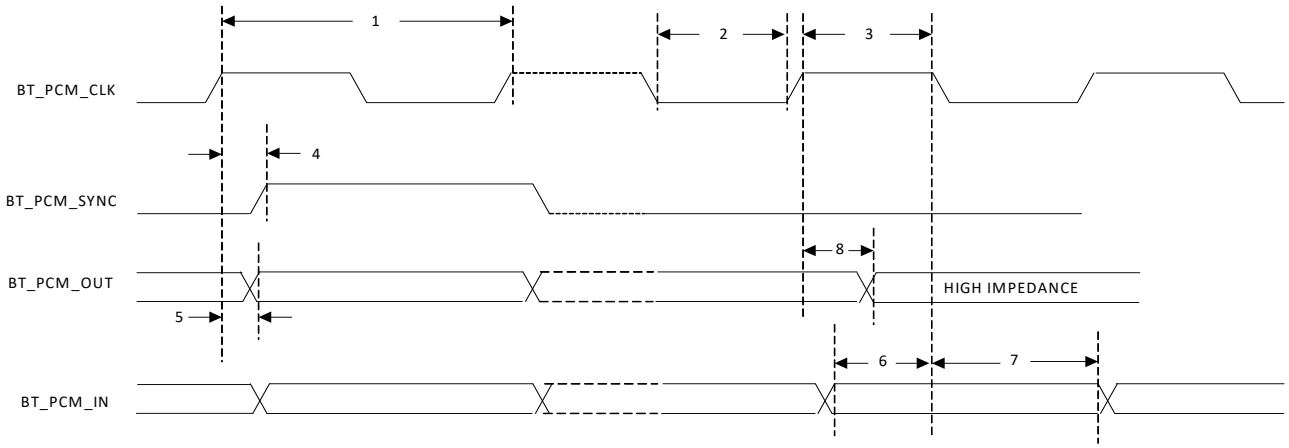


Table 7. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC delay	0	–	25.0	ns
5	BT_PCM_OUT delay	0	–	25.0	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

Short Frame Sync, Slave Mode

Figure 11. PCM Timing Diagram (Short Frame Sync, Slave Mode)

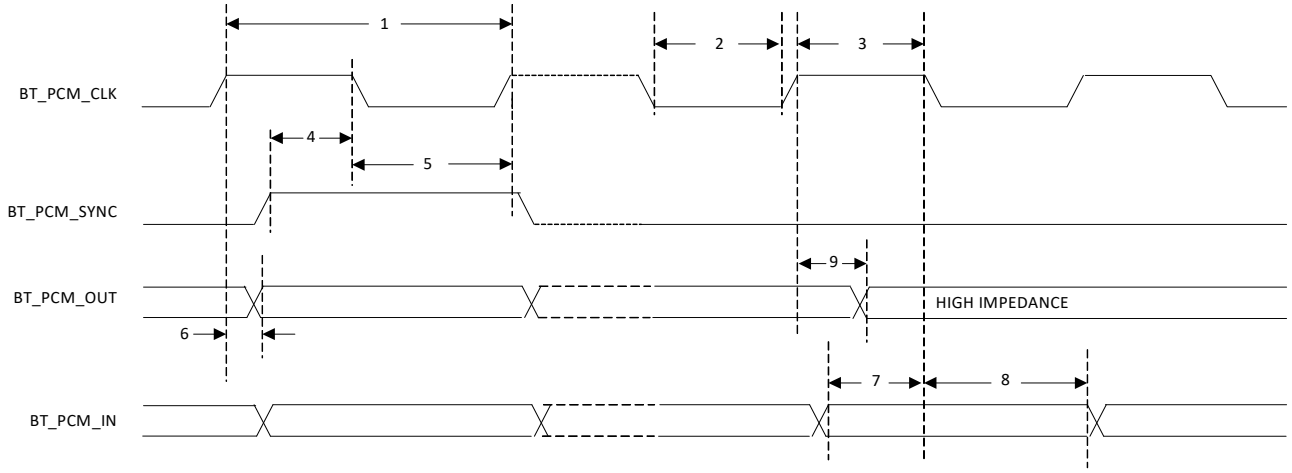


Table 8. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_OUT delay	0	–	25.0	ns
7	BT_PCM_IN setup	8.0	–	–	ns
8	BT_PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

Long Frame Sync, Master Mode

Figure 12. PCM Timing Diagram (Long Frame Sync, Master Mode)

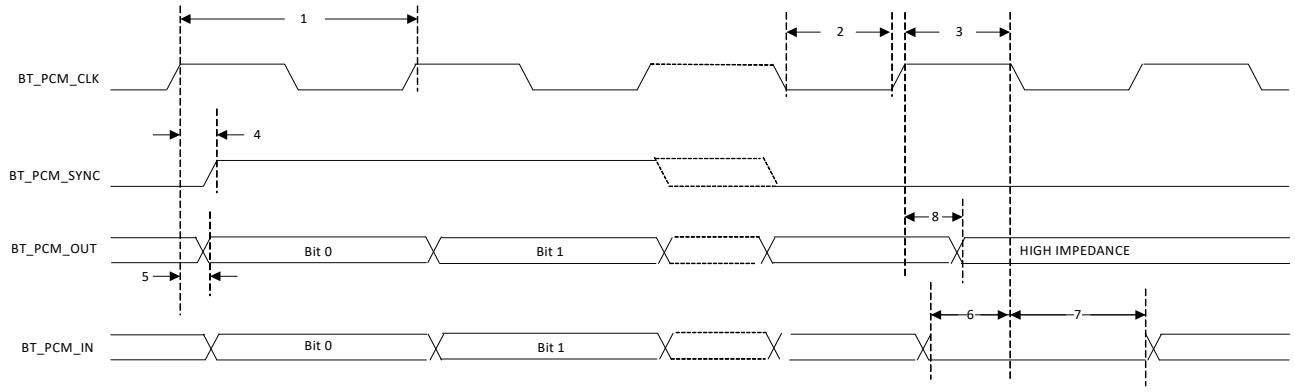


Table 9. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC delay	0	–	25.0	ns
5	BT_PCM_OUT delay	0	–	25.0	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

Long Frame Sync, Slave Mode

Figure 13. PCM Timing Diagram (Long Frame Sync, Slave Mode)

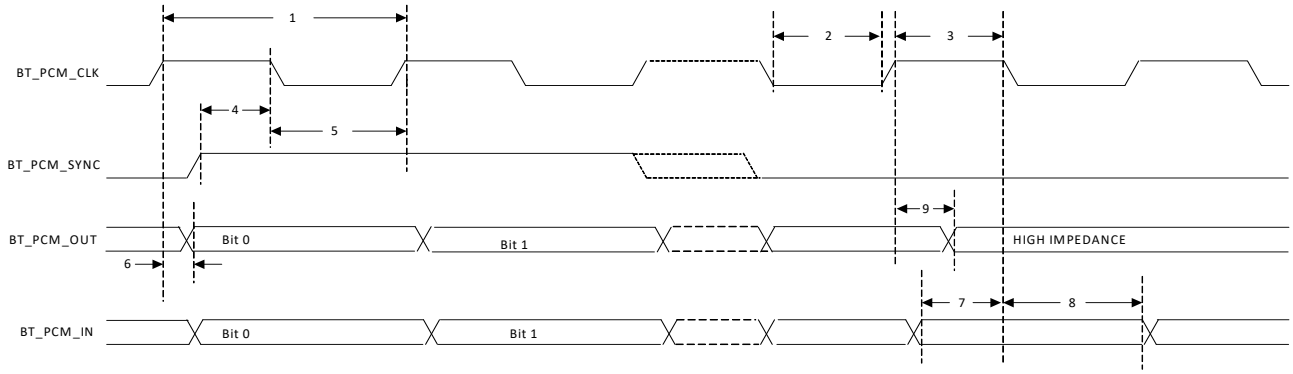


Table 10. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_OUT delay	0	–	25.0.	ns
7	BT_PCM_IN setup	8.0	–	–	ns
8	BT_PCM_IN hold	8.0.	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

Short Frame Sync, Burst Mode

Figure 14. PCM Burst Mode Timing (Receive Only, Short Frame Sync)

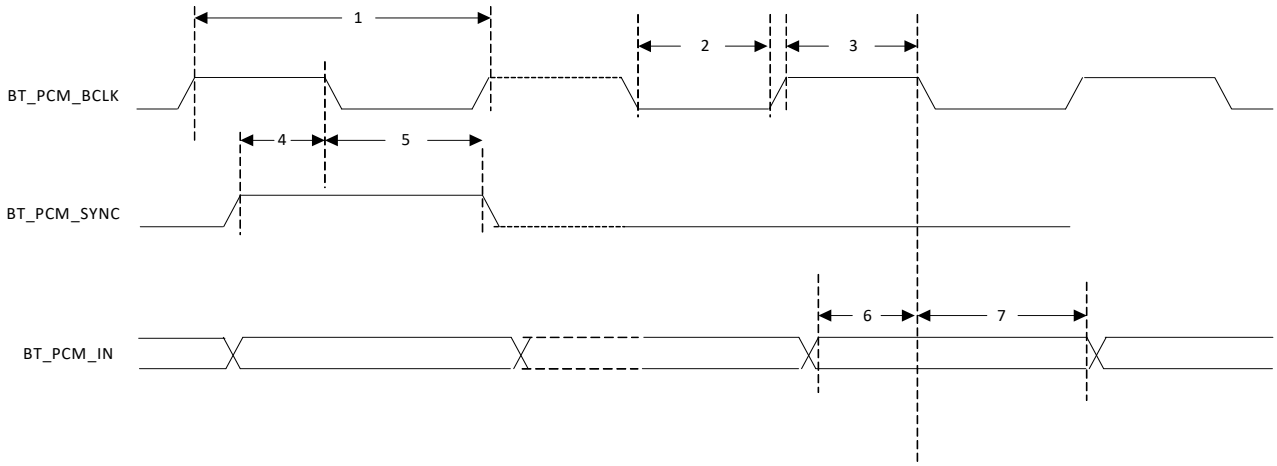


Table 11. PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24.0	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns

Long Frame Sync, Burst Mode

Figure 15. PCM Burst Mode Timing (Receive Only, Long Frame Sync)

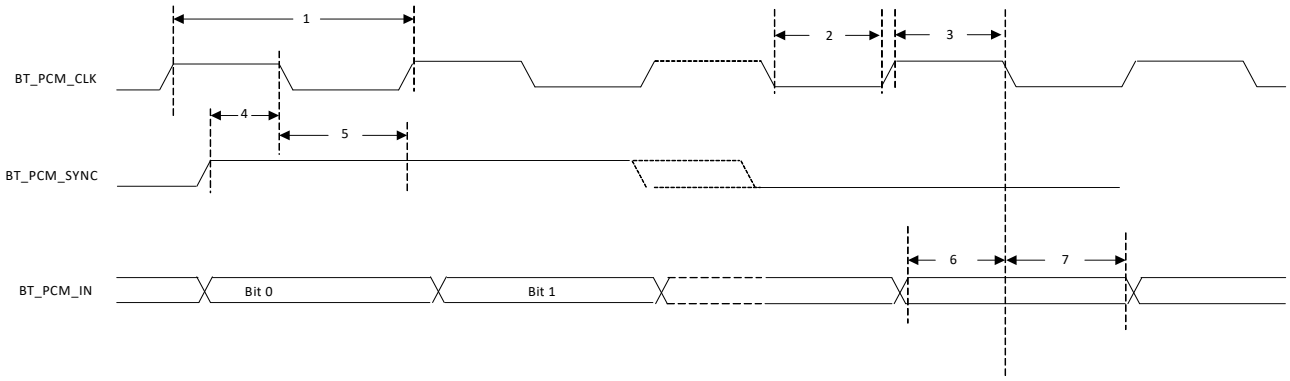


Table 12. PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24.0	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns

7.1.2 I²S Interface

CYW8x570 has the following I²S signals:

- I²S clock: BT_I2S_CLK
- I²S Word Select: BT_I2S_WS
- I²S Data Out: BT_I2S_DO
- I²S Data In: BT_I2S_DI

BT_I2S_CLK and BT_I2S_WS become outputs in Master mode and inputs in Slave mode, whereas BT_I2S_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSb of the left-channel data is aligned with the MSb of the I²S bus, in accord with the I²S specification. The MSb of each data word is transmitted one bit clock cycle after the BT_I2S_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when BT_I2S_WS is LOW, and right-channel data is transmitted when BT_I2S_WS is HIGH. Data bits sent by CYW8x570 are synchronized with the falling edge of BT_I2S_CLK and should be sampled by the receiver on the rising edge of BT_I2S_CLK.

7.1.2.1 I²S Timing

Note Timing values specified in Table 13 are relative to high and low threshold levels.

Table 13. Timing for I²S Transmitters and Receivers

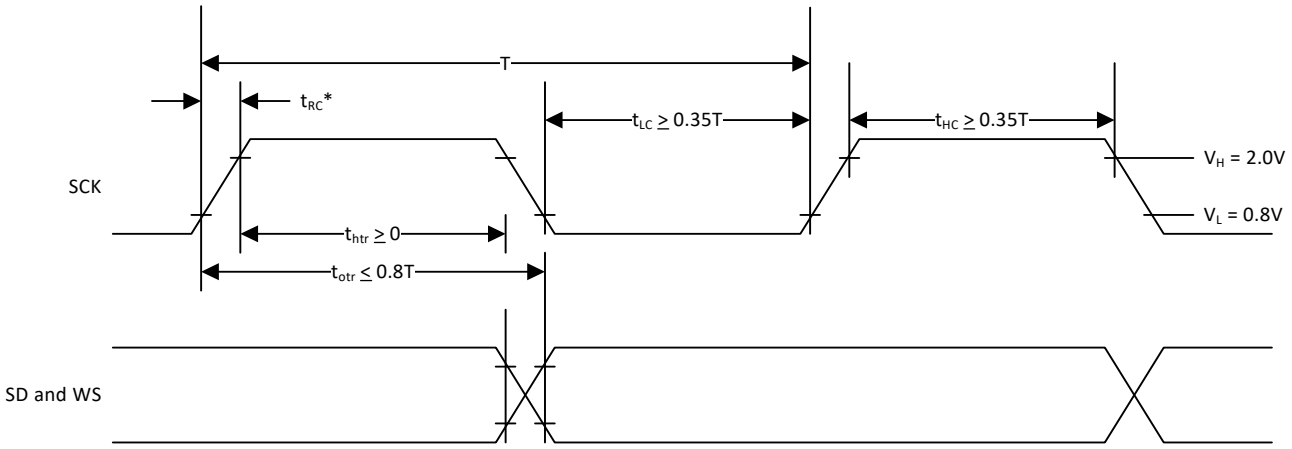
	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	[6]
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	[7]
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	[7]
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	[8]
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	[8]
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	[9]
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	[10]
Hold time t_{htr}	0	–	–	–	–	–	–	–	[9]
Receiver									
Setup time t_{sr}	–	–	–	–	$0.2T_r$	–	–	–	[11]
Hold time t_{hr}	–	–	–	–	$0.2T_r$	–	–	–	[11]

Notes

6. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
7. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
8. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
9. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
10. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
11. The data setup and hold time must not be less than the specified receiver setup and hold time.

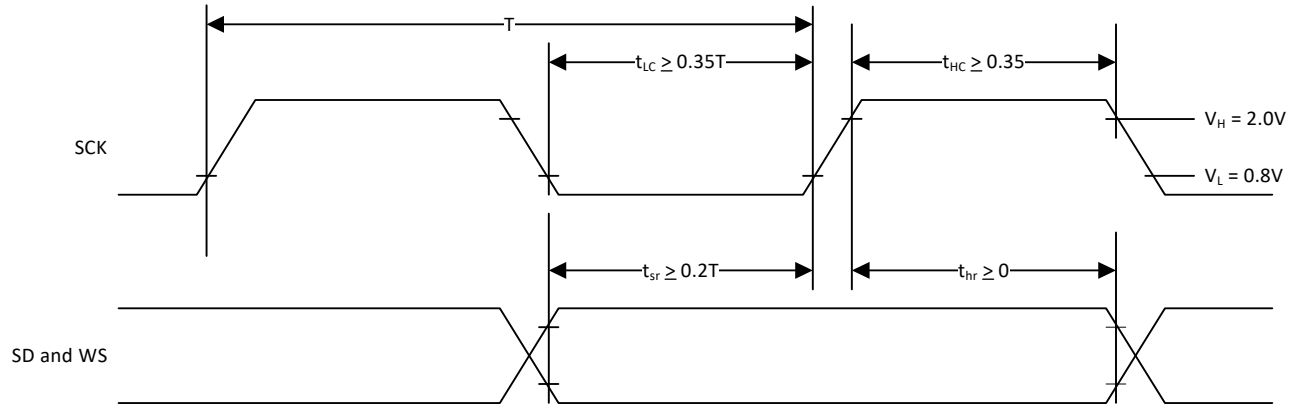
Note The time periods specified in Figure 16 and Figure 17 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 16. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 17. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

7.2 UART Interface

The CYW8x570 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 5.0 UART HCI specification. The default baud rate is 115.2 Kbaud.

The CYW8x570 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The CYW8x570 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 14. Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Figure 18. UART Timing

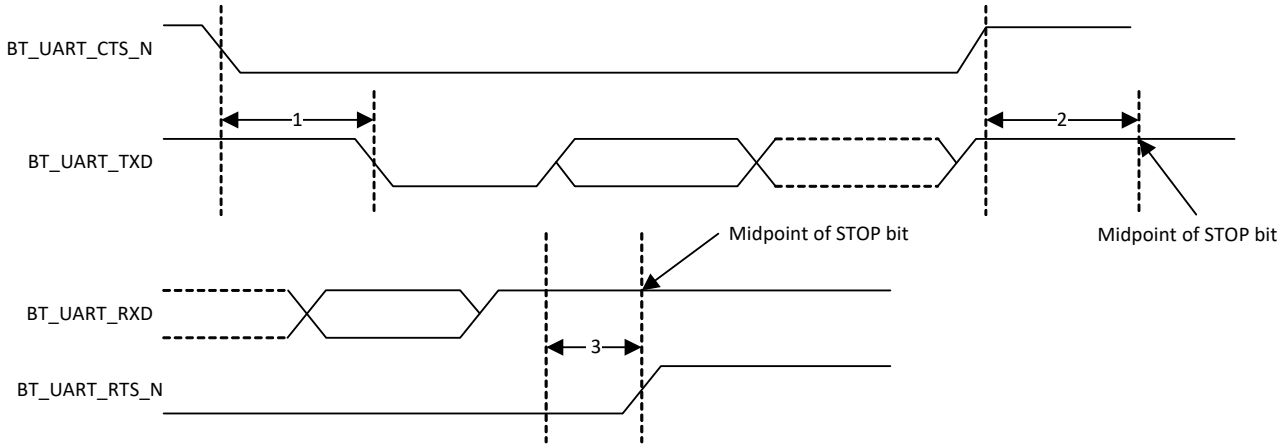


Table 15. UART Timing Specifications

Reference	Characteristics	Min	Typ	Max	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

8. WLAN Global Functions

8.1 WLAN CPU and Memory Subsystem

CYW8x570 WLAN section includes an integrated Arm Cortex-R4 32-bit processor with internal RAM and ROM. The on-chip memory for the CPU includes 1344 KB SRAM and 1472 KB ROM. The Arm Cortex-R4 processor implements the Arm v7-R architecture with support for the Thumb-2 instruction set.

Using multiple technologies to reduce cost, the Arm Cortex-R4 offers improved memory utilization, reduced pin overhead, and reduced silicon area. It supports independent buses for Code and Data access (ICode/DCode and system buses), integrated sleep modes, and extensive debug features including real-time tracing of program execution.

8.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal one-time programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design. Up to 1150 bytes of user-accessible OTP are available.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

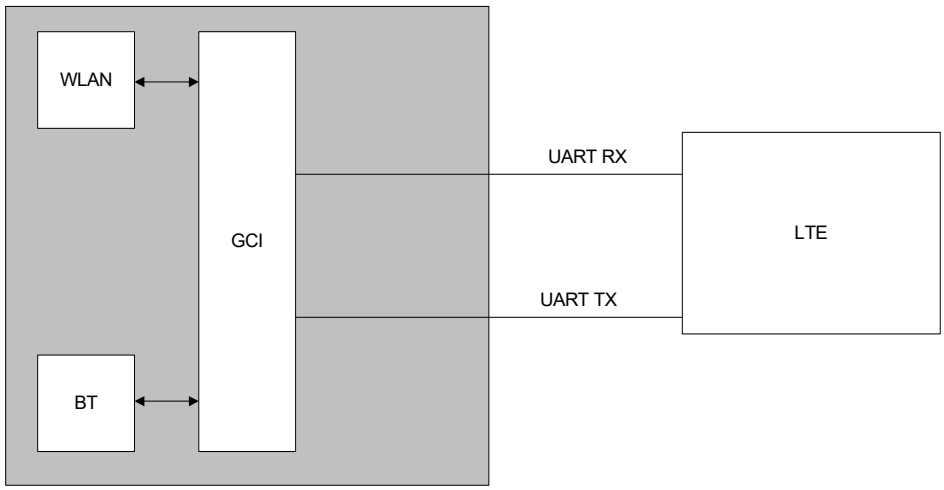
8.3 GPIO Interface

CYW8x570 has 15 GPIO pins in the WLAN section that can be used to connect to various external devices. Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions, see Table 19.

8.4 External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as LTE to manage wireless medium sharing for optimal performance. Figure 19 show the LTE coexistence interface (including UART). See Table 19 for further details on multiplexed signals, such as the GPIO pins.

Figure 19. Multipoint Global Coexistence Interface



Baud rates are derived from the crystal clock. For rates higher than a crystal_frequency/16, the baud rate is an integer divide of the crystal frequency. Table 16 shows the values for a 37.4 MHz crystal.

Table 16. Baud Rates for a 37.4 MHz Crystal

Division	XTAL	Baud Rate (Mbps)
12	37.4/12	3.116667
13	37.4/13	2.876923
14	37.4/14	2.671429
15	37.4/15	2.493333
16	37.4/16	2.3375

8.5 Debug UART Interface

One 2-wire UART interface can be enabled by software as an alternate function on GPIO pins. Refer to Table 19. Provided primarily for debugging during development, this UART enables CYW8x570 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

8.6 FAST UART Interface

A high-speed 4-wire CTS/RTS UART interface can be enabled by software as an alternate function on GPIO pins. Refer to Table 19. Provided primarily for control word exchange, this UART enables the chip to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

8.7 JTAG Interface

CYW8x570 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Cypress to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs. Refer to Table 19 for JTAG pin assignments.

8.8 CSC Interface

A proprietary Cypress Serial Control (CSC, an I^2C-compatible interface) slave interface is available as an alternate function on the GPIO lines. It supports data transfer rates up to 3.4 Mbps in high-speed mode. It can be primarily used to transfer data to a sensor hub in the host system. This interface supports device interrupts and 7-bit and 10-bit addressing to the processor. Based on the device-address matching, a device can be brought out of low-power state using this interface. This interface provides an internal FIFO depth of 32 bytes for both TX and RX with the ability to filter glitches on both clock and data lines.

9. WLAN Host Interface

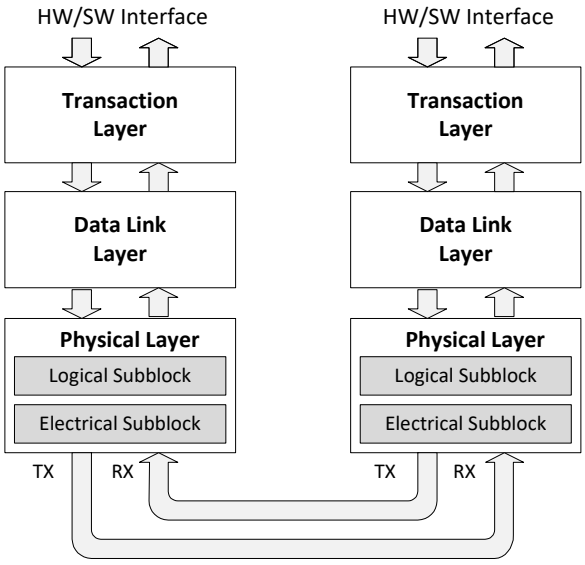
9.1 PCI Express Interface

The PCI Express (PCIe) core in CYW8x570 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the *PCI Express Base Specification v3.0* running at Gen2 speeds. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 20. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and CYW8x570 device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

Figure 20. PCI Express Layer Model



9.1.1 Transaction Layer Interface

The PCIe core employs a packet-based protocol to transfer data between the host and CYW8x570 device, delivering new levels of performance and features. The upper layer of the PCIe is the transaction layer. The transaction layer is primarily responsible for assembly and disassembly of transaction layer packets (TLPs). TLP structure contains header, data payload, and end-to-end CRC (ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with credit-based flow control of TLP, which eliminates wasted link bandwidth due to retries.

9.1.2 Data Link Layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

The data link layer packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgement, power management, and flow control.

9.1.3 Physical Layer

The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for Link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and CYW8x570 device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

9.1.4 Logical Subblock

The logical sub block primary functions are to prepare outgoing data from the data link layer for transmission and identify received data before passing it to the data link layer.

9.1.5 Scrambler/Descrambler

This PCIe PHY component generates pseudo-random sequence for scrambling of data bytes and the idle sequence. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding. On the receive side, descrambling is applied to characters after 8b/10b decoding. Scrambling may be disabled in polling and recovery for testing and debugging purposes.

9.1.6 8B/10B Encoder/Decoder

The PCIe core on CYW8x570 uses an 8b/10b encoder/decoder scheme to provide DC balancing, synchronizing clock and data recovery, and error detection. The transmission code is specified in the ANSI X3.230-1994, clause 11 and in IEEE 802.3z, 36.2.4.

Using this scheme, 8-bit data characters are treated as 3 bits and 5 bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the 12 special symbols included in the 8b/10b transmission code. These code groups are concatenated to form a 10-bit symbol, which is then transmitted serially. The special symbols are used for link management, frame TLPs, and DLLPs, allowing these packets to be quickly identified and easily distinguished.

9.1.7 Elastic FIFO

An elastic FIFO is implemented in the receiver side to compensate for the differences between the transmit clock domain and the receive clock domain, with worse case clock frequency specified at 600 ppm tolerance. As a result, the transmit and receive clocks can shift one clock every 1666 clocks. In addition, the FIFO adaptively adjusts the elastic level based on the relative frequency difference of the write and read clock. This technique reduces the elastic FIFO size and the average receiver latency by half.

9.1.8 Electrical Subblock

The high-speed signals utilize the common mode logic (CML) signaling interface with on-chip termination and deemphasis for best-in-class signal integrity. A deemphasis technique is employed to reduce the effects of intersymbol interference (ISI) due to the interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open “eye” at the detection point, thereby allowing the receiver to receive data with acceptable bit-error rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are deemphasized. Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the deemphasis values. The high-speed interface requires AC coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

9.1.9 Configuration Space

The PCIe function in CYW8x570 implements the configuration space as defined in the *PCI Express Base Specification v3.0*.

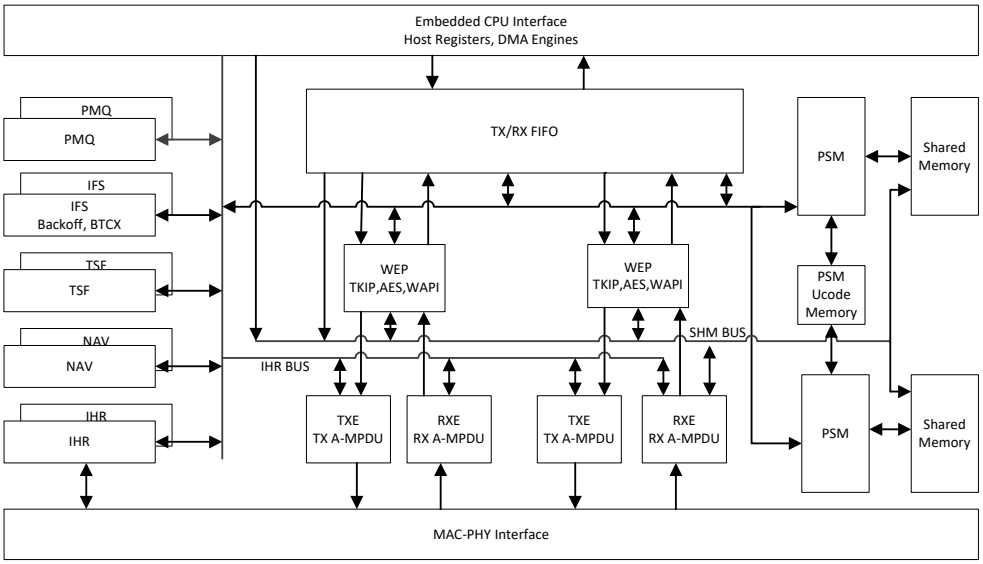
10. Wireless LAN MAC and PHY

10.1 IEEE 802.11ax MAC

The CYW8x570 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 21.

The following sections provide an overview of the important modules in the MAC.

Figure 21. WLAN MAC Architecture



The CYW8x570 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n.

The key MAC features include:

- Enhanced MAC for supporting IEEE 802.11ax and 802.11ac features.
- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT).
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation.
- Support for immediate ACK and Block-ACK policies.
- Interframe space timing support, including RIFS.
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges.
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification.
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware.
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management.
- Hardware offload engine for IEEE 802.11 to IEEE 802.3 header conversion for receive packets.
- Support for coexistence with Bluetooth and other external radios.
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality.
- Statistics counters for MIB support.

Programmable State Machine (PSM)

The PSM is a micro-coded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratch-pad, IHRs, or instruction literals, and the results are written into the shared memory, scratch-pad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

Wired Equivalent Privacy (WEP)

WEP engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

Transmit Engine (TXE)

The TXE constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

Receive Engine (RXE)

The RXE constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

Interframe Space (IFS) Timing

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

Timing Synchronization Function (TSF)

The TSF module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

Network Allocation Vector (NAV)

The NAV timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

10.2 IEEE 802.11ax/ac PHY

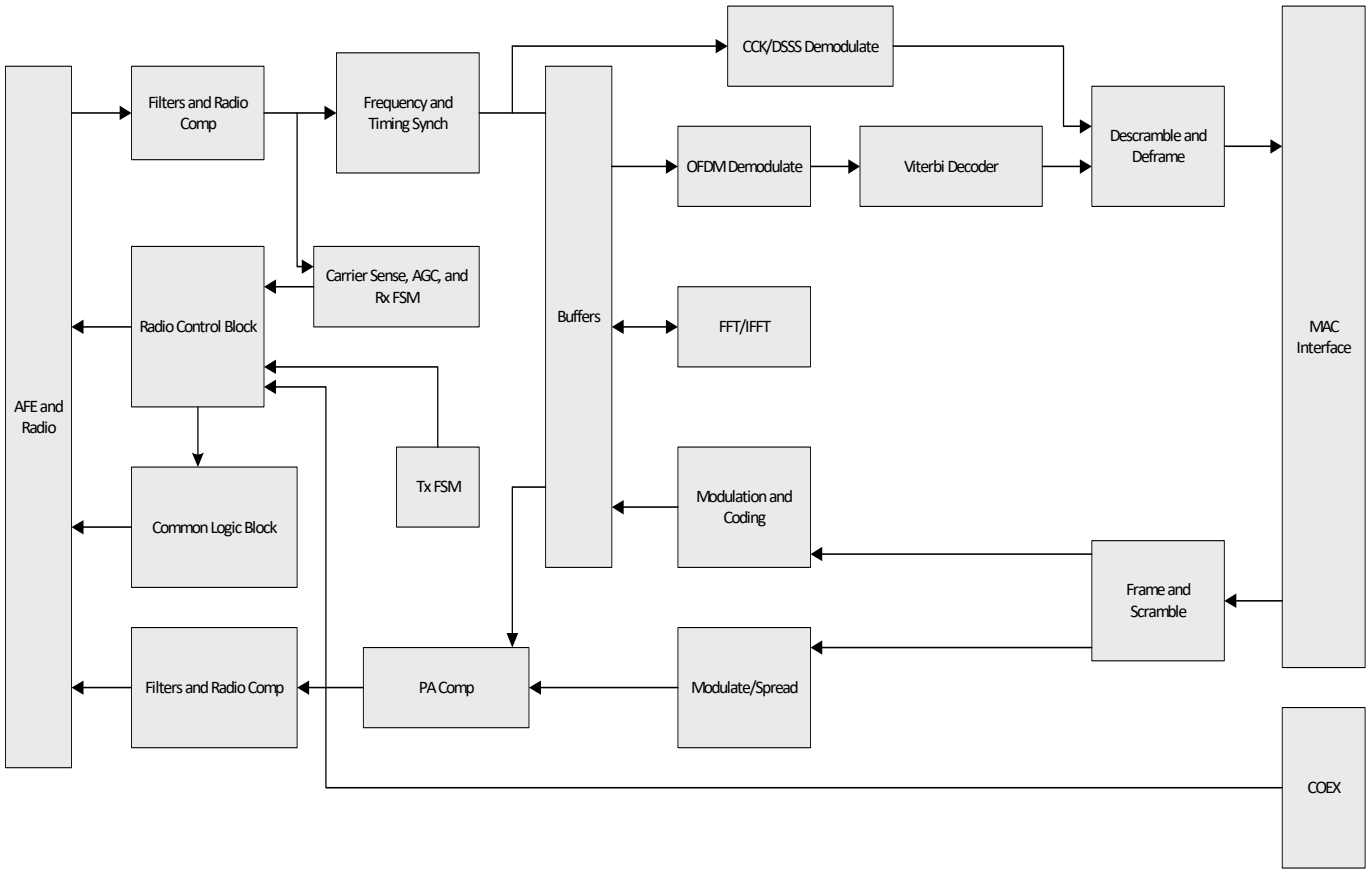
The CYW8x570 WLAN PHY is designed to comply with IEEE 802.11ax Draft, IEEE 802.11ac and IEEE 802.11a/b/g/n specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 1201.0 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT, and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, and channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for sharing an antenna between WL and BT.

The key PHY features include:

- Programmable data rates from MCS0–MCS9 in 20 MHz, 40 MHz, and 80 MHz channels, as specified in IEEE 802.11ac
- Improved performance with 2×2 channel smoothing support
- Short GI in TX and RX
- TX and RX LDPC for improved range and power efficiency
- Beamforming
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction
- Supports IEEE 802.11d/h for worldwide operation, designed to meet FCC and other worldwide regulatory requirements
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Algorithms to improve performance in presence of Bluetooth
- Closed loop-transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Available per-packet channel quality and signal strength measurements

Figure 22. WLAN PHY Block Diagram



11. WLAN Radio Subsystem

CYW8x570 includes an integrated tri-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems, and is hardware-ready for 6 GHz Wi-Fi 6E band. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5-7 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Twenty RF control signals are available (10 per core) to drive external RF switches and support optional external power amplifiers and low-noise amplifiers for each band. See the reference board schematics for further details.

CYW8x570 WLAN Radio has 2 Radio Cores for 2x2 MIMO operation with a shared RFPLL providing clock to both cores.

11.1 Receiver Path

CYW8x570 has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5-7 GHz U-NII band. An on-chip low-noise amplifier (LNA) in the 2.4 GHz path is shared between the Bluetooth and WLAN receivers, while the 5 GHz receive path has a dedicated on-chip LNA. Control signals are available that can support the use of optional external LNAs for each band.

11.2 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5-7 GHz U-NII bands, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output power while meeting IEEE 802.11a/b/g/n/ac/ax specifications without the need for external PAs. When using the internal PAs, closed-loop output power control is completely integrated. As an option, external PAs can be used for even higher output power, in which case the closed-loop power control is provided by means of a-band and g-band TSSI inputs from external power detectors.

11.3 Calibration

CYW8x570 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance, and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize the test time and cost in large volume production.

12. Pinout and Signal Descriptions

12.1 CYW8x570 FCFBGA Package Ball Map

Figure 23 shows the CYW8x570 FCFBGA Package Ball Map.

Figure 23. 12x12 mm FCFBGA Package Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	CSR_VDDBAT	CSR_VDDBAT	CSR_VLX	CSR_VLX	PVSSC	PVSSC	SMIF_SPHB_DQ2	SMIF_SPHB_CK	RF_SW_CTRL02	RF_SW_CTRL04	RF_SW_CTRL14	VDDP_RFSW	VDDIO_RFSW	RF_SW_CTRL16	WRF_PMU_VDD_3P3_C1	WRF_GND	WRF_GND	A
B	ASR_VDDBAT	ASR_VDDBAT	ASR_VDD1P12	CSR_VDD0P9	SMIF_SPHB_CS0_N	SMIF_SPHB_CS1_N	SMIF_SPHB_DQ3	SMIF_SPHB_DQ0	RF_SW_CTRL12	RF_SW_CTRL15	RF_SW_CTRL13	RF_SW_CTRL08	RF_SW_CTRL18	RF_SW_CTRL11	WRF_GND	WRF_GND	WRF_RFIN_5G_C1	B
C	ASR_VLX	ASR_VLX	ASR_VLX	VDDOUT_MISC	RF_SW_CTRL07	RF_SW_CTRL06	RF_SW_CTRL09	SMIF_SPHB_DQ1	GPIO_2	GPIO_11	RF_SW_CTRL17	GPIO_5	RF_SW_CTRL10	WRF_TSSI5G_OUT_C1	WRF_GND	WRF_GND	WRF_PAOUT_5G_C1	C
D	PVSSA	PVSSA	MISC_SNS	BTREG_ON	RF_SW_CTRL03	RF_SW_CTRL05	RF_SW_CTRL00	RF_SW_CTRL01	GPIO_8	GPIO_3	LHL_GPIO0	RF_SW_CTRL19	WRF_VDD_1P8_C1	WRF_GND	WRF_GND	WRF_PA_VDD_3P3_C1	WRF_GND	D
E	BTLDO_VDDBAT	BTLDO_VDDBAT	VDDOUT_SWCORE	PMU_AVSS	VDD_RET_GL	GPIO_9	GPIO_1	VDDIO	VSSC	VDD_AON	VSSC	WRF_GND	WRF_GND	WRF_GPAIO_TSSI2G_OUT_C1	WRF_GND	WRF_PA_VDD_3P3_C1	WRF_PAOUT_2G_C1	E
F	VDDOUT_BT3P3	VDDOUT_BT3P3	BT3P3_SNS	PMU_AVSS	WLREG_ON	GPIO_6	GPIO_7	VSSC	VDD_MAIN	VDD_AON	VDD_MAIN	WRF_GND	WRF_PMU_VDD_1P12_C1	WRF_GND	WRF_GND	WRF_GND	WRF_RFIN_2G_C1	F
G	VDDOUT_PA3P3	VDDOUT_PA3P3	VDDOUT_PA3P3	PA3P3_SNS	MIC_N	VSSC	GPIO_10	GPIO_12	GPIO_4	VDD_MAIN	VSSC	WRF_AFE_VDD_1P12_C1	WRF_SYNTH_VDD_1P12	WRF_GND	WRF_GND	WRF_GND	WRF_RFIN_5G_C0	G
H	WLLDO_VDDBAT	WLLDO_VDDBAT	WLLDO_VDDBAT	RF3P3_SNS	MIC_P	LHL_GPIO3	GPIO_0	JTAG_SEL	LHL_GPIO1	VDD_MAIN	VSSC	WRF_GND	WRF_VCO_VDD_1P12	WRF_VCO_VDD_3P3	WRF_GND	WRF_GND	WRF_PAOUT_5G_C0	H
J	VDDOUT_RF3P3	VDDOUT_RF3P3	PMU_VDD1P8	VSSC	LPO_IN	VSSC	VSSC	WLPLL_AVDD1P0	LHL_XTALI	VDD_TOP	VSSC	WRF_GND	WRF_SYNTH_VDD_3P3	WRF_PMU_VDD_3P3_C0	WRF_GND	WRF_PA_VDD_3P3_C0	WRF_GND	J
K	SDIO_CLK	SDIO_DATA_0	SDIO_DATA_2	SDIO_CMD	LHL_GPIO2	VDDIO_SD	VSSC	VDD_DIG	LHL_XTALO	VDD_TOP	VDD_TOP	WRF_AFE_VDD_1P12_C0	WRF_PMU_VDD_1P12_C0	WRF_VDD_1P8_C0	WRF_GND	WRF_PA_VDD_3P3_C0	WRF_PAOUT_2G_C0	K
L	PCIE_RDP	SDIO_DATA_1	SDIO_DATA_3	AVSS_PCIE	PCIE_PERST_L	VSSC	VDD_AON	LHL_VDDO	VDD_RET_GL_IN	BT_VDDC	VDD_DIG	WRF_TSSI5G_OUT_C0	WRF_GPAIO_TSSI2G_OUT_C0	BTRF_VSS	BTRF_VSS	WRF_GND	WRF_RFIN_2G_C0	L
M	PCIE_RDN	AVSS_PCIE	PCIE_TESTP	AVSS_PCIE	PCI_PME_L	VDD_DIG	VSSC	VDD_DIG	BT_GPIO_10	BT_VDDC	BT_GPIO_9	NC	BTRF_LDO_VDD_1P12	BTRF_VSS	BTRF_VSS	BTRF_VSS	BTRF_VSS	M
N	PCIE_TDP	AVSS_PCIE	PCIE_TESTN	AVSS_PCIE	PCIE_CLKREQ_L	VSSC	I2S_DI	VSSC	BTPLL_AVDD1P0	BT_VDDO_SMIF	VSSC	XTAL_GND	BTRF_TEST	BTRF_VSS	BTRF_VSS	BTRF_VSS	BTRF_RF_OP	N
P	PCIE_TDN	AVSS_PCIE	AVDD_TX_1P0	AVSS_PCIE	GPIO_13	BT_GPIO_19	I2S_DO	BT_UART_RXD	BT_GPIO_2	BT_GPIO_8	BT_GPIO_11	XTAL_GND	XTAL_GND	BTRF_VSS	BTRF_PAVDD_3P3	BTRF_VSS	BTRF_13DBM_OP	P
R	AVSS_PCIE	AVSS_PCIE	AVDD_PLL_1P0	AVDD_RX_1P0	BT_GPIO_18	GPIO_14	I2S_IRCK	BT_UART_CTS_N	BT_GPIO_3	BT_GPIO_7	BT_GPIO_20	XTAL_VDD_1P12	VDD_XTAL	XTAL_GND	BTRF_VSS	BTRF_VSS	BTRF_VSS	R
T	PCIE_REFCLKP	AVSS_PCIE	BT_GPIO_12	BT_GPIO_14	BT_GPIO_17	DMIC_DQ	I2S_SCK	BT_UART_RTS_N	BT_GPIO_4	BT_GPIO_6	BT_DEV_WAKE	XTAL_GND	XTAL_GND	XTAL_GND	XTAL_GND	BTRF_VSS	BTRF_20DBM_OP	T
U	PCIE_REFCLKN	AVSS_PCIE	BT_GPIO_13	BT_GPIO_15	BT_GPIO_16	DMIC_CK	I2S_MCK	BT_UART_TXD	BT_GPIO_5	BT_VDDO	BT_HOST_WAKE	XTAL_GND	XTAL_XOP	XTAL_XON	XTAL_GND	BTRF_VSS	BTRF_VSS	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

12.2 FCBGA Package Signal Descriptions

The signal name, type, and description of each pin in CYW8x570 is listed in Table 17. The symbols shown under Type indicate pin directions (I/O = Bidirectional, I = Input, O = Output, PWR = Power, GND =Ground, OD= Open-Drain) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 17. CYW8x570 FCBGA Signal Descriptions

Ball #	Ball Name	Type	Description
B15	WRF_GND	GND	WLAN Radio Ground
A16	WRF_GND	GND	WLAN Radio Ground
H13	WRF_VCO_VDD_1P12	PWR	WLAN Radio 1.12 V Supply
D17	WRF_GND	GND	WLAN Radio Ground
A17	WRF_GND	GND	WLAN Radio Ground
J17	WRF_GND	GND	WLAN Radio Ground
E13	WRF_GND	GND	WLAN Radio Ground
K14	WRF_VDD_1P8_C0	PWR	WLAN Radio 1.8 V Core0 Supply
H17	WRF_PAOUT_5G_C0	O	WLAN Radio Core0 5 GHz PA Output
L13	WRF_GPAIO_TSSI2G_OUT_C0	O	WLAN Radio 2.4 GHz TSSI Core0
E14	WRF_GPAIO_TSSI2G_OUT_C1	O	WLAN Radio 2.4 GHz TSSI Core1
H14	WRF_VCO_VDD_3P3	PWR	WLAN Radio 3.3 V Supply
G12	WRF_AFE_VDD_1P12_C1	PWR	WLAN Radio 1.12 V Core1 Supply
L12	WRF_TSSI5G_OUT_C0	O	WLAN Radio 5 GHz TSSI Core0
C15	WRF_GND	GND	WLAN Radio Ground
F13	WRF_PMU_VDD_1P12_C1	PWR	WLAN Radio 1.12 V Core1 Supply
F14	WRF_GND	GND	WLAN Radio Ground
B16	WRF_GND	GND	WLAN Radio Ground
G13	WRF_SYNTH_VDD_1P12	PWR	WLAN Radio 1.12 V Supply
B17	WRF_RFIN_5G_C1	I	WLAN Radio 5 GHz Core1 Receiver Input
D13	WRF_VDD_1P8_C1	PWR	WLAN Radio 1.8 V Core1 Supply
K16	WRF_PA_VDD_3P3_C0	PWR	WLAN Radio 3.3 V Core0 PA Supply
C16	WRF_GND	GND	WLAN Radio Ground
D15	WRF_GND	GND	WLAN Radio Ground
D16	WRF_PA_VDD_3P3_C1	PWR	WLAN Radio 3.3 V Core1 PA Supply
F16	WRF_GND	GND	WLAN Radio Ground
H15	WRF_GND	GND	WLAN Radio Ground
E16	WRF_PA_VDD_3P3_C1	PWR	WLAN Radio 3.3 V Core1 PA Supply
E17	WRF_PAOUT_2G_C1	O	WLAN Radio Core1 2.4 GHz PA Output
K17	WRF_PAOUT_2G_C0	O	WLAN Radio Core0 2.4 GHz PA Output
K13	WRF_PMU_VDD_1P12_C0	PWR	WLAN Radio 1.12 V Core0 Supply
G16	WRF_GND	GND	WLAN Radio Ground
H16	WRF_GND	GND	WLAN Radio Ground
K15	WRF_GND	GND	WLAN Radio Ground
J16	WRF_PA_VDD_3P3_C0	PWR	WLAN Radio 3.3 V Core0 PA Supply
L16	WRF_GND	GND	WLAN Radio Ground
J15	WRF_GND	GND	WLAN Radio Ground

Table 17. CYW8x570 FCBGA Signal Descriptions (Cont.)

Ball #	Ball Name	Type	Description
L17	WRF_RFIN_2G_C0	I	WLAN Radio 2.4 GHz Core0 Receiver Input
G15	WRF_GND	GND	WLAN Radio Ground
J13	WRF_SYNTH_VDD_3P3	PWR	WLAN Radio 3.3 V Supply
F15	WRF_GND	GND	WLAN Radio Ground
E15	WRF_GND	GND	WLAN Radio Ground
F17	WRF_RFIN_2G_C1	I	WLAN Radio 2.4 GHz Core1 Receiver Input
G14	WRF_GND	GND	WLAN Radio Ground
E12	WRF_GND	GND	WLAN Radio Ground
G17	WRF_RFIN_5G_C0	I	WLAN Radio 5 GHz Core0 Receiver Input
F12	WRF_GND	GND	WLAN Radio Ground
D14	WRF_GND	GND	WLAN Radio Ground
H12	WRF_GND	GND	WLAN Radio Ground
A15	WRF_PMU_VDD_3P3_C1	PWR	WLAN Radio 3.3 V Core1 Supply
J12	WRF_GND	GND	WLAN Radio Ground
J14	WRF_PMU_VDD_3P3_C0	PWR	WLAN Radio 3.3 V Core0 Supply
K12	WRF_AFE_VDD_1P12_C0	PWR	WLAN Radio 1.12 V Core0 Supply
C14	WRF_TSSI5G_OUT_C1	O	WLAN Radio 5 GHz TSSI Core0
C17	WRF_PAOUT_5G_C1	O	WLAN Radio Core1 5 GHz PA Output
U13	XTAL_XOP	I	Xtal Oscillator Input
U15	XTAL_GND	GND	Xtal Oscillator Ground
U14	XTAL_XON	O	Xtal Oscillator Output
R13	VDD_XTAL	PWR	Xtal Oscillator 1.0 V Supply
R12	XTAL_VDD_1P12	PWR	Xtal Oscillator 1.12 V Supply
T13	XTAL_GND	GND	Xtal Oscillator Ground
U12	XTAL_GND	GND	Xtal Oscillator Ground
P15	BTRF_PAVDD_3P3	PWR	BT Radio 3.3 V PA Supply
P16	BTRF_VSS	GND	BT Radio Ground
P14	BTRF_VSS	GND	BT Radio Ground
L14	BTRF_VSS	GND	BT Radio Ground
N16	BTRF_VSS	GND	BT Radio Ground
N14	BTRF_VSS	GND	BT Radio Ground
M17	BTRF_VSS	GND	BT Radio Ground
N15	BTRF_VSS	GND	BT Radio Ground
T16	BTRF_VSS	GND	BT Radio Ground
U16	BTRF_VSS	GND	BT Radio Ground
R15	BTRF_VSS	GND	BT Radio Ground
L15	BTRF_VSS	GND	BT Radio Ground
M14	BTRF_VSS	GND	BT Radio Ground
M15	BTRF_VSS	GND	BT Radio Ground
M16	BTRF_VSS	GND	BT Radio Ground
U17	BTRF_VSS	GND	BT Radio Ground
N13	BTRF_TEST	I/O	BT Radio Test Input/Output Pin

Table 17. CYW8x570 FCBGA Signal Descriptions (Cont.)

Ball #	Ball Name	Type	Description
N17	BTRF_RF_OP	O	BT Radio Output
R17	BTRF_VSS	GND	BT Radio Ground
P17	BTRF_13DBM_OP	O	BT Radio (13 DBM) Output
M13	BTRF_LDO_VDD_1P12	PWR	BT Radio 1.12 V Input Supply
R16	BTRF_VSS	GND	BT Radio Ground
T17	BTRF_20DBM_OP	O	BT Radio (20 DBM) Output
A6	PVSSC	GND	Ground Input of CSR Power Stage
G1	VDDOUT_PA3P3	PWR	3.3 V Output to Supply WLAN PA
E4	PMU_AVSS	GND	PMU Analog Ground
F3	BT3P3_SNS	I	Feedback Input of BT3P3 LDO
A1	CSR_VDDBAT	PWR	Battery Supply Input for CSR Power Stage
A2	CSR_VDDBAT	PWR	Battery Supply Input for CSR Power Stage
E3	VDDOUT_SWCORE	O	Power Switch Output Supply for VDD_TOP Power Supply Input
E5	VDD_RET_GL	O	Power Mux Output Supply for VDD_RET_GL_IN Power Supply Input
E1	BTLDO_VDDBAT	PWR	Battery Supply Input for BT PA LDO
E2	BTLDO_VDDBAT	PWR	Battery Supply Input for BT PA LDO
F1	VDDOUT_BT3P3	PWR	3.3 V Output to Supply BT PA
D1	PVSSA	GND	Ground Input of ASR Power Stage
G5	MIC_N	I	ADC Microphone Negative Input
F4	PMU_AVSS	GND	PMU Analog Ground
D3	MISC_SNS	I	Feedback Input of MISC LDO
D2	PVSSA	GND	Ground Input of ASR Power Stage
A5	PVSSC	GND	Ground Input of CSR Power Stage
B3	ASR_VDD1P12	I	Sense or Feedback Input of ASR Power Stage
F2	VDDOUT_BT3P3	PWR	3.3 V Output to Supply BT PA
G2	VDDOUT_PA3P3	PWR	3.3 V Output to Supply WLAN PA
A4	CSR_VLX	O	CSR Power Stage Output to Inductor
A3	CSR_VLX	O	CSR Power Stage Output to Inductor
J1	VDDOUT_RF3P3	PWR	3.3 V Output to Supply WLAN Radio
C1	ASR_VLX	O	ASR Power Stage Output to Inductor
J3	PMU_VDD1P8	PWR	1.8 V PMU Supply Input
C2	ASR_VLX	O	ASR Power Stage Output to Inductor
H1	WLLDO_VDDBAT	PWR	Battery Supply Input for WLAN PA and RF LDO
F5	WLREG_ON	I	Used by the PMU to power up or power down the internal CYW8x570 regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 KΩ pull-down resistor that is auto enabled/disabled by programming
B1	ASR_VDDBAT	PWR	Battery Supply Input for ASR Power Stage
H2	WLLDO_VDDBAT	PWR	Battery Supply Input for WLAN PA LDO and RF LDO
H3	WLLDO_VDDBAT	PWR	Battery Supply Input for WLAN PA LDO and RF LDO
B2	ASR_VDDBAT	PWR	Battery Supply Input for ASR Power Stage
H5	MIC_P	I	ADC Microphone Positive Input
J4	VSSC	GND	Core Ground for WLAN and BT

Table 17. CYW8x570 FCBGA Signal Descriptions (Cont.)

Ball #	Ball Name	Type	Description
C3	ASR_VLX		ASR Power Stage Output to Inductor
J2	VDDOUT_RF3P3	PWR	3.3 V Output to Supply WLAN Radio
D4	BTREG_ON	I	Used by the PMU to power up or power down the internal CYW8x570 regulators used by the BT section. When deasserted, this pin holds the BT section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming
B4	CSR_VDD0P9	I	Sense or Feedback Input of CSR Power Stage
H4	RF3P3_SNS	I	Feedback Input of RF3P3 LDO
C4	VDDOUT_MISC	O	Output of VDDOUT_MISC
G4	PA3P3_SNS	I	Feedback Input of PA3P3 LDO
G3	VDDOUT_PA3P3	PWR	3.3 V Output to Supply WLAN PA
N1	PCIE_TDP	O	PCIE Transmitter Differential Pair Positive Output
P1	PCIE_TDN	O	PCIE Transmitter Differential Pair Negative Output
T1	PCIE_REFCLKP	I	PCIE Differential Pair Clock Source (100 MHz) Positive Input.
U1	PCIE_REFCLKN	I	PCIE Differential Pair Clock Source (100 MHz) Negative Input.
L1	PCIE_RDP	I	PCIE Receiver Differential Pair Positive Input
M1	PCIE_RDN	I	PCIE Receiver Differential Pair Negative Input
N3	PCIE_TESTN	I/O	PCIE Test Differential Pair Negative Pin
M3	PCIE_TESTP	I/O	PCIE Test Differential Pair Positive Pin
R3	AVDD_PLL_1P0	PWR	1.0 V PCIE Analog Supply
P3	AVDD_TX_1P0	PWR	1.0 V PCIE Transmitter Supply Input
M2	AVSS_PCIE	GND	PCIE Analog Ground
R4	AVDD_RX_1P0	PWR	1.0 V PCIE Receiver Supply Input
J11	VSSC	GND	Core Ground for WLAN and BT

Table 17. CYW8x570 FCBGA Signal Descriptions (Cont.)

Ball #	Ball Name	Type	Description
D12	RF_SW_CTRL19	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file
B13	RF_SW_CTRL18	O	
C11	RF_SW_CTRL17	O	
A14	RF_SW_CTRL16	O	
B10	RF_SW_CTRL15	O	
A11	RF_SW_CTRL14	O	
B11	RF_SW_CTRL13	O	
B9	RF_SW_CTRL12	O	
B14	RF_SW_CTRL11	O	
C13	RF_SW_CTRL10	O	
C7	RF_SW_CTRL09	O	
B12	RF_SW_CTRL08	O	
C5	RF_SW_CTRL07	O	
C6	RF_SW_CTRL06	O	
D6	RF_SW_CTRL05	O	
A10	RF_SW_CTRL04	O	
D5	RF_SW_CTRL03	O	
A9	RF_SW_CTRL02	O	
D8	RF_SW_CTRL01	O	
D7	RF_SW_CTRL00	O	
G11	VSSC	GND	Core Ground for WLAN and BT
E10	VDD_AON	PWR	0.9 V Digital Core Supply for WLAN/BT
A13	VDDIO_RFSW	PWR	IO Supply for RF Switch Control Pads
E9	VSSC	GND	Core Ground for WLAN and BT
A12	VDDP_RFSW	O	VDDP Power Switch Output
E11	VSSC	GND	Core Ground for WLAN and BT
G6	VSSC	GND	Core Ground for WLAN and BT
J6	VSSC	GND	Core Ground for WLAN and BT
M7	VSSC	GND	Core Ground for WLAN and BT
J7	VSSC	GND	Core Ground for WLAN and BT
F8	VSSC	GND	Core Ground for WLAN and BT
N10	BT_VDDO_SMIF	PWR	1.8 V SMIF Interface IO Supply
A8	SMIF_SPHB_CK	O	SMIF Clock Output
B7	SMIF_SPHB_DQ3	I/O	SMIF Data Line 3
A7	SMIF_SPHB_DQ2	I/O	SMIF Data Line 2
C8	SMIF_SPHB_DQ1	I/O	SMIF Data Line 1
B8	SMIF_SPHB_DQ0	I/O	SMIF Data Line 0
B5	SMIF_SPHB_CS0_N	O	SMIF Chip Select0 Active-low Output
B6	SMIF_SPHB_CS1_N	O	SMIF Chip Select1 Active-low Output
H11	VSSC	GND	Core Ground for WLAN and BT
N6	VSSC	GND	Core Ground for WLAN and BT
L6	VSSC	GND	Core Ground for WLAN and BT

Table 17. CYW8x570 FCBGA Signal Descriptions (Cont.)

Ball #	Ball Name	Type	Description
K7	VSSC	GND	Core Ground for WLAN and BT
R8	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
U8	BT_UART_TXD	O	UART Serial Output. Serial data output for the HCI UART interface.
T8	BT_UART_RTS_N	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.
P8	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
R11	BT_GPIO_20	I/O	BT General Purpose I/O
P6	BT_GPIO_19	I/O	
R5	BT_GPIO_18	I/O	
T5	BT_GPIO_17	I/O	
U5	BT_GPIO_16	I/O	
U4	BT_GPIO_15	I/O	
T4	BT_GPIO_14	I/O	
U3	BT_GPIO_13	I/O	
T3	BT_GPIO_12	I/O	
P11	BT_GPIO_11	I/O	
M9	BT_GPIO_10	I/O	
M11	BT_GPIO_9	I/O	
P10	BT_GPIO_8	I/O	
R10	BT_GPIO_7	I/O	
T10	BT_GPIO_6	I/O	
U9	BT_GPIO_5	I/O	
T9	BT_GPIO_4	I/O	
R9	BT_GPIO_3	I/O	
P9	BT_GPIO_2	I/O	
T11	BT_DEV_WAKE	I/O	Bluetooth DEVICE WAKE
U11	BT_HOST_WAKE	I/O	Bluetooth HOST WAKE
U10	BT_VDDO	PWR	1.8 V IO Supply for BT GPIOs
M10	BT_VDDC	PWR	0.9 V Digital Core Supply for BT
R7	I2S_IRCK	I/O	I2S Word Clock or Left/Right Clock
T7	I2S_SCK	I/O	I2S Bit or Serial Clock
U7	I2S_MCK	I/O	I2S Master Clock
N7	I2S_DI	I/O	I2S Serial Data Input
P7	I2S_DO	I/O	I2S Serial Data Output
U6	DMIC_CK	I/O	Digital Mic Clock
T6	DMIC_DQ	I/O	Digital Mic Data
L10	BT_VDDC	PWR	0.9 V Digital Core Supply for BT
K6	VDDIO_SD	PWR	1.8 V IO Supply for WLAN GPIOs
L7	VDD_AON	PWR	0.9 V Digital Core Supply for WLAN/BT
F10	VDD_AON	PWR	0.9 V Digital Core Supply for WLAN/BT

Table 17. CYW8x570 FCBGA Signal Descriptions (Cont.)

Ball #	Ball Name	Type	Description
M5	PCI_PME_L	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3
N5	PCIE_CLKREQ_L	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.
L5	PCIE_PERST_L	I	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification v1.1
R6	GPIO_14	I/O	WLAN General Purpose I/O
P5	GPIO_13	I/O	
G8	GPIO_12	I/O	
C10	GPIO_11	I/O	
G7	GPIO_10	I/O	
E6	GPIO_9	I/O	
D9	GPIO_8	I/O	
F7	GPIO_7	I/O	
F6	GPIO_6	I/O	
C12	GPIO_5	I/O	
G9	GPIO_4	I/O	
D10	GPIO_3	I/O	
C9	GPIO_2	I/O	
E7	GPIO_1	I/O	
H7	GPIO_0	I/O	
E8	VDDIO	PWR	1.8 V IO Supply for WLAN GPIOs
H8	JTAG_SEL	I	JTAG Select Input: Pull high to select the JTAG interface. If the JTAG interface is not used this pin should be connected to ground.
J5	LPO_IN	I	External Sleep Clock Input (32.768 kHz)
J9	LHL_XTALI	I	32.768 KHz Crystal Oscillator Input
K9	LHL_XTALO	O	32.768 KHz Crystal Oscillator Output
L8	LHL_VDDO	PWR	1.8 V IO Supply for Miscellaneous GPIO
D11	LHL_GPIO0	I/O	Miscellaneous General Purpose I/O
H9	LHL_GPIO1	I/O	
K5	LHL_GPIO2	I/O	
H6	LHL_GPIO3	I/O	
N11	VSSC	GND	Core Ground for WLAN and BT
N8	VSSC	GND	
K8	VDD_DIG	PWR	0.9 V Digital Core Supply for WLAN
L11	VDD_DIG	PWR	
M6	VDD_DIG	PWR	
M8	VDD_DIG	PWR	

Table 17. CYW8x570 FCBGA Signal Descriptions (Cont.)

Ball #	Ball Name	Type	Description
F9	VDD_MAIN	PWR	0.9 V Digital Core Supply for WLAN
F11	VDD_MAIN	PWR	
G10	VDD_MAIN	PWR	
H10	VDD_MAIN	PWR	
L9	VDD_RET_GL_IN	PWR	0.9 V Digital Core Supply for WLAN
K11	VDD_TOP	PWR	0.9 V Digital Core Supply for WLAN/BT
K10	VDD_TOP	PWR	
J10	VDD_TOP	PWR	
J8	WLPLL_AVDD1P0	PWR	1.0 V WLPLL Analog Supply
N9	BTPLL_AVDD1P0	PWR	1.0 V BTPLL Analog Supply
N2	AVSS_PCIE	GND	PCIE Analog Ground
P2	AVSS_PCIE	GND	
R1	AVSS_PCIE	GND	
R2	AVSS_PCIE	GND	
T2	AVSS_PCIE	GND	
U2	AVSS_PCIE	GND	
L4	AVSS_PCIE	GND	
M4	AVSS_PCIE	GND	
N4	AVSS_PCIE	GND	
P4	AVSS_PCIE	GND	
T15	XTAL_GND	GND	Xtal Oscillator Ground
T12	XTAL_GND	GND	
R14	XTAL_GND	GND	
P12	XTAL_GND	GND	
P13	XTAL_GND	GND	
T14	XTAL_GND	GND	
N12	XTAL_GND	GND	

12.3 WLAN/BT GPIO Signals and Strapping Options

The pins listed in Table 18 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note Refer to the reference board schematics for more information.

12.3.1 Strapping Options

Table 18. GPIO Strap Pins

Ball/Bump Name	Default Pull During Strapping	All Packages
GPIO_1	1	1=PCIE 0 = RESERVED
GPIO_12	1	1=BT over UART 0=RESERVED

12.4 GPIO Alternative Signal Functions

Table 19. GPIO Alternative Signal Functions

Pin Name	HW Decided/Power ON Default	Same As Pin Function Name	GPIO-0	FAST_UART/ GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/I2C	BT-0	MISC-0	MISC-1
	Function Sel										
	0	1	2	3	4	5	6	7	8	9	10
GPIO_0	TRISTATE_IND	WL_HOST_WAKE/GPIO_0	GPIO_8	–	GCI_GPIO_0	GCI_GPIO_11	–	–	BT_DEV_WAKE	–	–
GPIO_1	TRISTATE_IND	WL_DEV_WAKE/GPIO_1	GPIO_9	–	GCI_GPIO_1	GCI_GPIO_12	–	–	BT_HOST_WAKE	RF_DISABLE_L	–
GPIO_2	JTAG_SEL ? Tessent TAPTCK : ARM DAP TCK[12]	GPIO_2	GPIO_10	FAST_UART_RX	GCI_GPIO_2	GCI_GPIO_13	UART_DBG_RX	–	BT_GPIO_2	DAP_SEL ? ARM DAP TCK : Tessent TAP TCK[12]	MUXED_RF_SW_CTRL0
GPIO_3	JTAG_SEL ? Tessent TAP TMS : ARM DAP TMS[12]	GPIO_3	GPIO_11	FAST_UART_TX	GCI_GPIO_3	GCI_GPIO_14	UART_DBG_TX	–	BT_GPIO_3	DAP_SEL ? ARM DAP TMS : Tessent TAP TMS[12]	MUXED_RF_SW_CTRL1
GPIO_4	JTAG_SEL ? Tessent TAP TDI : ARM DAP TDI[12]	GPIO_4	GPIO_12	FAST_UART_CTS_IN	GCI_GPIO_4	GCI_GPIO_15	–	–	BT_GPIO_4	DAP_SEL ? ARM DAP TDI : Tessent TAP TDI[12]	MUXED_RF_SW_CTRL2
GPIO_5	JTAG_SEL ? Tessent TAP TDO : ARM DAP TDO[12]	GPIO_5	GPIO_13	FAST_UART_RTS_OUT	GCI_GPIO_0	GCI_GPIO_5	–	–	BT_GPIO_5	DAP_SEL ? ARM DAP TDO : Tessent TAP TDO[12]	MUXED_RF_SW_CTRL3
GPIO_6	JTAG_SEL ? Tessent TAP TRST_L : ARM DAP TRST_L[12]	GPIO_6	GPIO_14	–	GCI_GPIO_1	GCI_GPIO_6	–	–	BT_GPIO_11	DAP_SEL ? ARM DAP TRST_L : Tessent TAP TRST_L[12]	MUXED_RF_SW_CTRL4
GPIO_7	TRISTATE_IND	GPIO_7	GPIO_15	–	GCI_GPIO_2	GCI_GPIO_7	–	–	BT_GPIO_7	–	SWD/JTAG SELECT.
GPIO_8	TRISTATE_IND	GPIO_8	GPIO_0	FAST_UART_CTS_IN	GCI_GPIO_3	GCI_GPIO_8	–	GSIO_SDI	BT_GPIO_8	–	–
GPIO_9	TRISTATE_IND	GPIO_9	GPIO_1	FAST_UART_RTS_OUT	GCI_GPIO_4	GCI_GPIO_9	–	GSIO_SDO	BT_GPIO_9	–	–
GPIO_10	TRISTATE_IND	GPIO_10	GPIO_2	FAST_UART_RX	GCI_GPIO_0	GCI_GPIO_10	UART_DBG_RX	GSIO_CSN	BT_GPIO_10	–	–
GPIO_11	TRISTATE_IND	GPIO_11	GPIO_3	FAST_UART_TX	GCI_GPIO_1	GCI_GPIO_11	UART_DBG_TX	GSIO_CLK	BT_GPIO_6		–
GPIO_12	TRISTATE_IND	WL_LED1/ GPIO_12	GPIO_4	–	GCI_GPIO_2	GCI_GPIO_12	–	–	BT_GPIO_12	–	–
GPIO_13	TRISTATE_IND	WL_LED0/ GPIO_13	GPIO_5	–	GCI_GPIO_3	GCI_GPIO_13	–	–	BT_GPIO_13	–	–
GPIO_14	TRISTATE_IND	GPIO_14	GPIO_6	–	GCI_GPIO_4	GCI_GPIO_14	–	–	BT_GPIO_14	–	–

Note
12. A ternary operator (condition ? value if condition is true: value if condition is false) is used to represent a conditional assignment.

12.5 I/O States

The following notations are used in Table 20 on page 52:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down
- Where applicable, the default value is shown in bold brackets (for example, **[default value]**)

Table 20. I/O States

Name	I/O	Keeper	Active Mode	Low-Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present	Power Rail
WL_REG_ON BT_REG_ON	I	N	I: PD Pull-down auto disabled	I: PD Pull-down auto disabled	I: PD (of 50K)	I: PD (of 50K)	I: PD (of 50K)	—
GPIO_0	I/O	Y	I/O: PU, PD, NoPull Programmable [PD]	I/O: PU, PD, NoPull Programmable [PD]	High-Z, NoPull	High-Z, NoPull	High Z, NoPull	VDDIO
GPIO_1	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High Z, NoPull	High-Z, NoPull	High Z, NoPull	VDDIO
GPIO_2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:PU	I:PU	VDDIO
GPIO_3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:PU	I:PU	VDDIO
GPIO_4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:PU	I:PU	VDDIO
GPIO_5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[13]	I: NoPull	VDDIO
GPIO_6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: PU	I:PU	VDDIO
GPIO_7	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_8	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO

Note
13. When JTAG is not enabled on the GPIO.

Table 20. I/O States (Cont.)

Name	I/O	Keeper	Active Mode	Low-Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present	Power Rail
GPIO_9	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_10	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_11	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	High Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_12	I/O	N	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	High Z, NoPull	High Z, NoPull	VDDIO
GPIO_13	I/O	N	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_14	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
RF_SW_CTRL_X	O	N	O: NoPull	O: NoPull	High-Z, NoPull	O: NoPull	O: NoPull	VDDIO_RF

Note
13. When JTAG is not enabled on the GPIO.

13. DC Characteristics

13.1 Absolute Maximum Ratings

Table 21. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for VBAT and PA driver supply	CSR_VDDBAT, ASR_VDDBAT, BTLDO_VDDBAT, WLLDO_VDDBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD, BT_VDDO, BT_VDDO_SMIF, LHL_VDDO, PMU_VDD1P8	–0.5 to 2.2	V
DC supply voltage for RF switch I/Os	VDDIO_RFSW	–0.5 to 3.9	V
DC supply voltage for core	VDD_AON, VDD_MAIN, VDD_DIG, VDD_RET_GL_IN, VDD_TOP, BT_VDDC	-0.5 to 1.1	V
Maximum undershoot voltage for I/O[14]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[14]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction temperature	T_j	125	°C

Note
14. Duration not to exceed 25% of the duty cycle.

13.2 Environmental Ratings

The environmental ratings are shown in Table 22.

Table 22. Environmental Ratings

Characteristic	Value	Unit	Conditions/Comments
Ambient Temperature (T_A)	–40 to +85	°C	Functional operation[15]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

Note
15. The device is functional across this range of temperature.The device autonomously monitors its junction temperature and employs transmit throughput throttling to regulate power dissipation and ensure that the junction temperature is held below maximum ratings for device reliability.

13.3 Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 23, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 23. Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	CSR_VDDBAT, ASR_VDDBAT, BTLDO_-VDDBAT, WLLDO_VDDBAT	3.0[16]	3.3	4.8[17]	V
DC supply voltage for core	VDD_AON, VDD_MAIN, VDD_DIG,VDD_RET_GL_IN, VDD_TOP,BT_VDDC	0.86	0.9	0.94	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD, BT_VDDO, BT_VDDO_SMIF, LHL_VDDO, PMU_VDD1P8	1.71	1.8	1.89	V
DC supply voltage for RF switch I/Os when supporting 3.3V RF_SW_CTRL pads	VDDIO_RFSW	3.13	3.3	3.47	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
Digital I/O Pins[18]					
For VDDIO, VDDIO_SD, BT_VDDO, BT_VDDO_SMIF = 1.8 V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
RF Switch Control Output Pins[18]					
For VDDIO_RFSW = 3.3 V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

Notes

16. CYW8x570 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2 V < VBAT < 4.5 V.
17. The maximum continuous voltage is 5.25 V. Voltage transients up to 6.0 V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5 V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.
18. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

13.4 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 24. ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	TBD	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	TBD	V

14. Bluetooth RF Specifications

Unless otherwise stated, limit values apply for the conditions specified in Table 25 and Table 26. Typical values apply for an ambient temperature of +25 °C.

Unless otherwise stated, the values in this section are design targets, to be confirmed by silicon characterization.

Figure 24 shows the RF port locations for testing Bluetooth in a system configuration with two antennas. Only one of the two system antennas is available to Bluetooth in this configuration and, thus, only one antenna is shown.

Figure 24. RF Port Locations for Bluetooth Testing in a Two-Antenna System

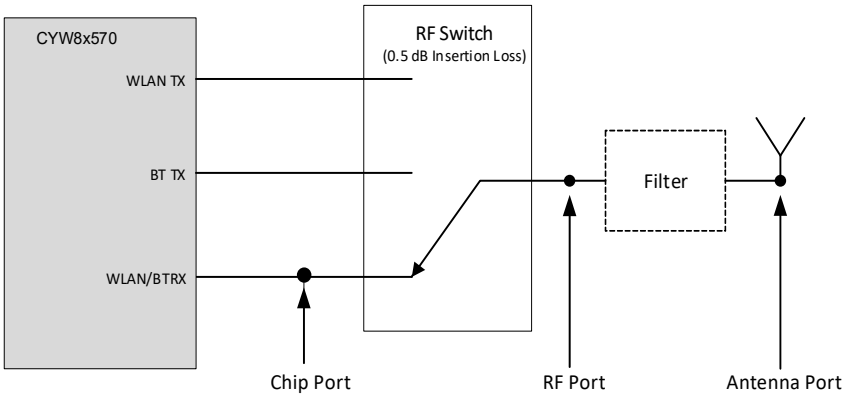
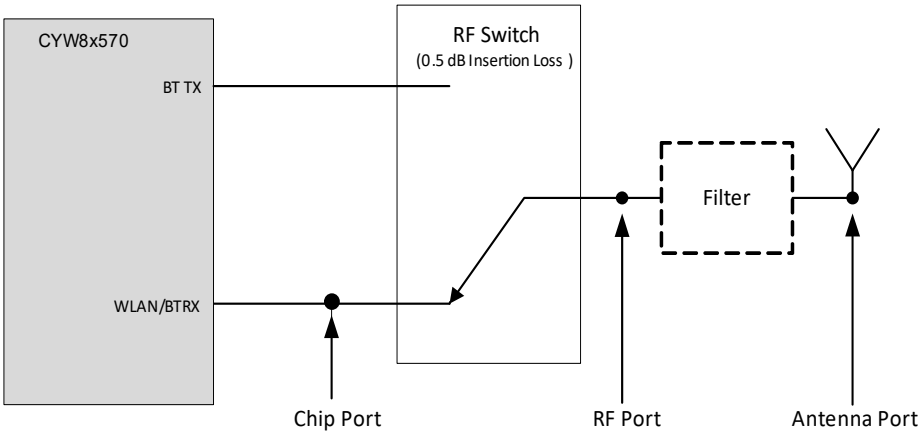


Figure 25 shows the RF port locations for testing Bluetooth in a system configuration with three antennas. In this system configuration, any one of the three system antennas can be used for Bluetooth.

Figure 25. RF Port Locations for Bluetooth Testing in a Three-Antenna System



Note All Bluetooth specifications are measured at the chip port unless otherwise specified.

Table 25. Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note The specifications in this table are measured at the chip port output unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Maximum input at antenna	–	–	–	–20	dBm
RX LO Leakage					
2.4 GHz band	–	–	–90.0	–80.0	dBm
Interference Performance[19]					
C/I co-channel	GFSK, 0.1% BER	–	–	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–	–30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20	dB
C/I co-channel	π/4-DQPSK, 0.1% BER	–	–	13.0	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–	–20.0	dB
C/I co-channel	8-DPSK, 0.1% BER	–	–	21.0	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	5.0	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–	–13.0	dB
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27.0	–	dBm
2498–3000 MHz	0.1% BER	–	–27.0	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer					
GFSK (1 Mbps)[20]					
698–716 MHz	WCDMA	–	–13.0	–	dBm

Notes
19. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
20. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = –84.5 dBm.
21. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
22. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.
23. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
24. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.
25. Bluetooth reference level for the wanted signal at the Bluetooth chip port = –79.5 dBm.

Table 25. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
776–849 MHz	WCDMA	–	–14.0	–	dBm
824–849 MHz	GSM850	–	–13.0	–	dBm
824–849 MHz	WCDMA	–	–14.0	–	dBm
880–915 MHz	E-GSM	–	–13.0	–	dBm
880–915 MHz	WCDMA	–	–13.0	–	dBm
1710–1785 MHz	GSM1800	–	–18.0	–	dBm
1710–1785 MHz	WCDMA	–	–17.0	–	dBm
1850–1910 MHz	GSM1900	–	–19.0	–	dBm
1850–1910 MHz	WCDMA	–	–19.0	–	dBm
1880–1920 MHz	TD-SCDMA	–	–20.0	–	dBm
1920–1980 MHz	WCDMA	–	–20.0	–	dBm
2010–2025 MHz	TD-SCDMA	–	–20.0	–	dBm
2500–2570 MHz	WCDMA	–	–26.0	–	dBm
2510 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2530 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2550 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2570 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2310 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2330 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2350 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2370 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2570–2620 MHz[23]	Band 38	–	–33.0	–	dBm
2545–2575 MHz[24]	XGP Band	–	–33.0	–	dBm
π/4-DPSK (2 Mbps)[20]					
698–716 MHz	WCDMA	–	–10.0	–	dBm
776–794 MHz	WCDMA	–	–10.0	–	dBm
824–849 MHz	GSM850	–	–11.0	–	dBm
824–849 MHz	WCDMA	–	–11.0	–	dBm
880–915 MHz	E-GSM	–	–10.0	–	dBm
880–915 MHz	WCDMA	–	–10.0	–	dBm
1710–1785 MHz	GSM1800	–	–16.0	–	dBm
1710–1785 MHz	WCDMA	–	–15.0	–	dBm
1850–1910 MHz	GSM1900	–	–17.0	–	dBm
1850–1910 MHz	WCDMA	–	–16.0	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18.0	–	dBm
1920–1980 MHz	WCDMA	–	–17.0	–	dBm

Notes
19. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
20. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = –84.5 dBm.
21. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
22. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.
23. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
24. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.
25. Bluetooth reference level for the wanted signal at the Bluetooth chip port = –79.5 dBm.

Table 25. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
2010–2025 MHz	TD-SCDMA	–	–19.0	–	dBm
2500–2570 MHz	WCDMA	–	–23.0	–	dBm
2510 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2530 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2550 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2570 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2310 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2330 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2350 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2370 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2570–2620 MHz[23]	Band 38	–	–33.0	–	dBm
2545–2575 MHz[24]	XGP Band	–	–33.0	–	dBm
8-DPSK (3 Mbps)[25]					
698–716 MHz	WCDMA	–	–13.0	–	dBm
776–794 MHz	WCDMA	–	–13.0	–	dBm
824–849 MHz	GSM850	–	–13.0	–	dBm
824–849 MHz	WCDMA	–	–14.0	–	dBm
880–915 MHz	E-GSM	–	–13.0	–	dBm
880–915 MHz	WCDMA	–	–13.0	–	dBm
1710–1785 MHz	GSM1800	–	–18.0	–	dBm
1710–1785 MHz	WCDMA	–	–17.0	–	dBm
1850–1910 MHz	GSM1900	–	–19.0	–	dBm
1850–1910 MHz	WCDMA	–	–19.0	–	dBm
1880–1920 MHz	TD-SCDMA	–	–19.0	–	dBm
1920–1980 MHz	WCDMA	–	–19.0	–	dBm
2010–2025 MHz	TD-SCDMA	–	–20.0	–	dBm
2500–2570 MHz	WCDMA	–	–23.0	–	dBm
2510 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2530 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2550 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2570 MHz[21]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2310 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2330 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2350 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2370 MHz[22]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2570–2620 MHz[23]	Band 38	–	–33.0	–	dBm
2545–2575 MHz[24]	XGP Band	–	–33.0	–	dBm

Notes
19. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
20. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = –84.5 dBm.
21. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
22. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.
23. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
24. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.
25. Bluetooth reference level for the wanted signal at the Bluetooth chip port = –79.5 dBm.

Table 25. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Spurious Emissions					
30 MHz–1 GHz		–	–95.0	-	dBm
1–12.75 GHz		–	–70.0	-	dBm
851–894 MHz		–	–147.0	–	dBm/Hz
925–960 MHz		–	–147.0	–	dBm/Hz
1805–1880 MHz		–	–147.0	–	dBm/Hz
1930–1990 MHz		–	–147.0	–	dBm/Hz
2110–2170 MHz		–	–147.0	–	dBm/Hz

Notes
19. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
20. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = –84.5 dBm.
21. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
22. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.
23. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
24. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.
25. Bluetooth reference level for the wanted signal at the Bluetooth chip port = –79.5 dBm.

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Table 26. Bluetooth Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note The specifications in this table are measured at the Chip port output unless otherwise specified.					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth		–	13.0	–	dBm
QPSK TX power at Bluetooth		–	9.0	–	dBm
8PSK TX power at Bluetooth		–	9.0	–	dBm
Power control step		–	4	–	dB
Note Output power is with TCA and TSSI enabled.					
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	0.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38.0	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–31.0	–20.0	dBm
|M – N| ≥ 2.5 MHz[26]		–	–43.0	–40.0	dBm
Out-of-Band Spurious Emissions					
TX harmonics (HD2, HD3, HD4) ■ Chip Pout = 13 dBm in BDR and BLE mode ■ Chip Pout = 10 dBm in BDR and BLE mode	HD2	–	-21	–	dBm
	HD3	–	-18	–	dBm
	HD4	–	-41	–	dBm

Note
26. The typical number is measured at ± 3 MHz offset.

Table 26. Bluetooth Transmitter RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
GLONASS BAND Spurious Emissions					
FDMA L1 Band 1598.0625-1606.375 MHZ	–	–	-156	–	dBm/Hz
FDMA L2 Band 1242.9375-1248.625 MHz	–	–	-162	–	dBm/Hz
CDMA L1 Signal 1202.025 MHz	–	–	-99	–	dBm/Hz
CDMA L2 Signal 1248.06 MHz	–	–	-162	–	dBm/Hz
CDMA L3 Signal 1202.025 MHz	–	–	-99	–	dBm/Hz
GPS Band Spurious Emissions					
CDMA L1 Signal 1575.42 MHz	–	–	-159	–	dBm/Hz
CDMA L2 Signal 1227.60 MHz	–	–	-162	–	dBm/Hz
Out-of-Band Noise Floor[27]					
65–108 MHz	FM RX	–	–150	–	dBm/Hz
776–794 MHz	CDMA2000	–	–150	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–150	–	dBm/Hz
925–960 MHz	E-GSM	–	–150	–	dBm/Hz
1570–1580 MHz	GPS	–	–150	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–147	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–145	–	dBm/Hz
2500–2570 MHz	Band 7	–	–133	–	dBm
2300–2400 MHz	Band 40	–	–133	–	dBm
2570–2620 MHz	Band 38	–	–136	–	dBm
2545–2575 MHz	XGP Band	–	–135	–	dBm

Note
27. Transmitted power in cellular and FM bands at the Bluetooth Antenna port. See Figure 24 for location of the port.

Table 27. Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72.0	–	µs
Initial carrier frequency tolerance	–	±25.0	±75.0	kHz
Frequency Drift				
DH1 packet	–	±8.0	±25.0	kHz
DH3 packet	–	±8.0	±40.0	kHz
DH5 packet	–	±8.0	±40.0	kHz
Drift rate	–	5.0	20.0	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[28]	140	155	175	kHz
10101010 sequence in payload[29]	115	135	–	kHz
Channel spacing	–	1	–	MHz

Notes
28. This pattern represents an average deviation in payload.
29. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 28. BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	–	2402		2480	MHz
RX sense[30]	GFSK, 0.1% BER, 1 Mbps	–	–95.5	–	dBm
TX power[31]	–	–	8.5	–	dBm
Mod Char: delta F1 average	–	225	255	275	kHz
Mod Char: delta F2 average	–	185	230	–	kHz
Mod Char: ratio	–	0.8	1.00	–	%

Notes
30. Dirty TX is off..
31. The BLE TX power cannot exceed 10 dBm EIRP specification limit. The front-end losses and antenna gain/loss must be factored in so as not to exceed the limit.

15. WLAN RF Specifications

15.1 Introduction

CYW8x570 includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radios.

Unless otherwise stated, limit values apply for the conditions specified in Table 30, Table 31, Table 32 and Table 33. Typical values apply for an ambient temperature +25 °C.

Unless otherwise stated, the values in this section are design targets, to be confirmed by silicon characterization.

Figure 26. 2.4 GHz WLAN Port Locations

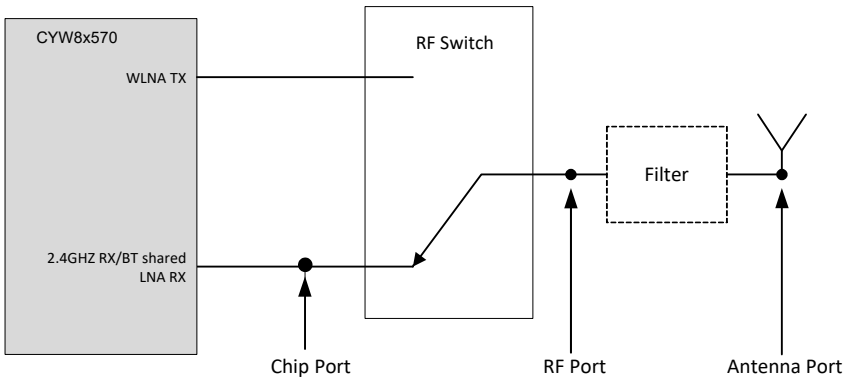
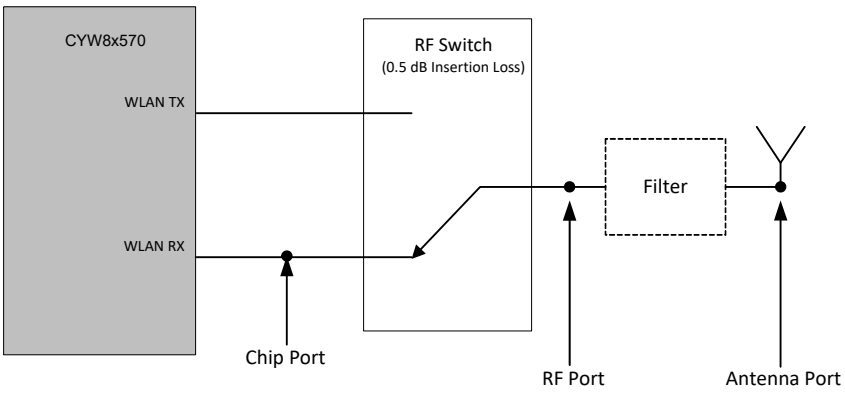


Figure 27. 5 GHz WLAN Port Locations



15.2 2.4 GHz Band General RF Specifications

Table 29. 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
TX/RX switch time	Including TX	–	–	5.0	µs
RX/TX switch time	Including TX	–	–	2.0	µs
Power-up and power-down ramp time	DSSS/CCK	–	–	–	–

15.3 WLAN 2.4 GHz Receiver Performance Specifications

Note The values in Table 30 are specified at the RF port unless otherwise noted.

Table 30. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Note		Min.	Typ.	Max.	Unit
Frequency range			2400	–	2500	MHz
Sensitivity						
Rx Sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU) [32], [33]	1 Mbps		–	-99.1	–	dBm
	2 Mbps		–	-96.1	–	dBm
	5.5 Mbps		–	-93.7	–	dBm
	11 Mbps		–	-90.7	–	dBm
Rx Sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU) [32], [34]	1 Mbps		–	-101.1	–	dBm/core
	2 Mbps		–	-97.6	–	dBm/core
	5.5 Mbps		–	-93.7	–	dBm/core
	11 Mbps		–	-90.7	–	dBm/core
Rx Sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU) [32], [33]	6 Mbps		–	-94.6	–	dBm
	9 Mbps		–	-93.1	–	dBm
	12 Mbps		–	-92.1	–	dBm
	18 Mbps		–	-89.6	–	dBm
	24 Mbps		–	-86.7	–	dBm
	36 Mbps		–	-83.4	–	dBm
	48 Mbps		–	-79.1	–	dBm
	54 Mbps		–	-77.6	–	dBm
Rx Sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU) [32], [34]	6 Mbps		–	-97.4	–	dBm/core
	9 Mbps		–	-94.9	–	dBm/core
	12 Mbps		–	-94.6	–	dBm/core
	18 Mbps		–	-92.1	–	dBm/core
	24 Mbps		–	-89.2	–	dBm/core
	36 Mbps		–	-85.9	–	dBm/core
	48 Mbps		–	-81.6	–	dBm/core
	54 Mbps		–	-80.1	–	dBm/core

Notes
32. Derate by TBD for -40 °C to TBD and by TBD for +85 °C to TBD.
33. Sensitivity with one Rx core active.
34. Sensitivity with two Rx core active and MRC combining (for Nss=1).
35. Sensitivity degradations for alternate settings in MCS modes. SGI: TBD dB drop.
36. Desired signal is at a power level 6 dB higher than the IEEE specification for the minimum sensitivity limit.
37. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
38. The minimum and maximum values shown have a 95% confidence level.

Table 30. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Note		Min.	Typ.	Max.	Unit
Rx Sensitivity IEEE 802.11n 20 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC. [32], [35], [34]	MCS0		–	-97.5	–	dBm/core
	MCS1		–	-94.9	–	dBm/core
	MCS2		–	-93.1	–	dBm/core
	MCS3		–	-90.0	–	dBm/core
	MCS4		–	-87.0	–	dBm/core
	MCS5		–	-82.8	–	dBm/core
	MCS6		–	-81.3	–	dBm/core
	MCS7		–	-79.8	–	dBm/core
	MCS8		–	-95.6	–	dBm/core
	MCS15		–	-77.1	–	dBm/core
Rx Sensitivity IEEE 802.11ax 20 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF, LDPC, non-STBC, and 20 MHz BW.[32], [35], [34]	MCS0, Nss=1		–	-97.7	–	dBm/core
	MCS7, Nss=1		–	-79.6	–	dBm/core
	MCS8, Nss=1		–	-75.6	–	dBm/core
	MCS9, Nss=1		–	-73.6	–	dBm/core
	MCS0, Nss=2		–	-95.5	–	dBm/core
	MCS7, Nss=2		–	-77.2	–	dBm/core
	MCS8, Nss=2		–	-73.5	–	dBm/core
	MCS9, Nss=2		–	-71.5	–	dBm/core
Rx Sensitivity IEEE 802.11ax HE-RE PPDU (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF. [[32], [35], [34]	RU242, MCS0, Nss=1		–	-95.4	–	dBm/core
	RU106, MCS0, Nss=1		–	-96.1	–	dBm/core
Rx Sensitivity IEEE 802.11ax HE-RE PPDU (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF. [32], [35], [34]	RU242, MCS0, Nss=1		–	-98.2	–	dBm/core
	RU106, MCS0, Nss=1		–	-98.9	–	dBm/core
Maximum Receiver Level @ 2.4 GHz	1, 2 Mbps (8% PER, 1024 octets)		–	-5	–	dBm/core
	5.5, 11 Mbps (8% PER, 1024 octets)		–	-5	–	dBm/core
	6-54 Mbps (10% PER, 1024 octets)		–	-10	–	dBm/core
	MCS0-MCS7 rates (10% PER, 4096 octets)		–	-10	–	dBm/core
	MCS8-MCS9 rates (10% PER, 4096 octets)		–	-10	–	dBm/core

Notes
32. Derate by TBD for -40 °C to TBD and by TBD for +85 °C to TBD.
33. Sensitivity with one Rx core active.
34. Sensitivity with two Rx core active and MRC combining (for Nss=1).
35. Sensitivity degradations for alternate settings in MCS modes. SGI: TBD dB drop.
36. Desired signal is at a power level 6 dB higher than the IEEE specification for the minimum sensitivity limit.
37. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
38. The minimum and maximum values shown have a 95% confidence level.

Table 30. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Note		Min.	Typ.	Max.	Unit
ACI/AACI/Jammer						
Adjacent Channel Rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level 6 dB higher than IEEE spec) [36]	Desired and interfering signal 30 MHz apart					
	1 Mbps	-74 dBm	–	48	–	dB
	Desired and interfering signal 25 MHz apart					
	11 Mbps	-70 dBm	–	44	–	dB
Adjacent Channel Rejection - OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as 3 dB higher than IEEE spec) [37]	6 Mbps	–79 dBm	–	30	–	dB
	54 Mbps	–62 dBm	–	15	–	dB
Adjacent Channel Rejection - 11n MCS0–7 in 20 MHz (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec) [37]	MCS0	–79 dBm	–	30	–	dB
	MCS7	–61 dBm	–	10	–	dB
Adjacent Channel Rejection - 11ax MCS0–9 in 20 MHz (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec) [37]	MCS0	–79 dBm	–	30	–	dB
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1024 octet PSDU for:(RxSens + 23 dB < Rxlevel < max. input level)		–	-80.0	–	dBm
Other RF Parameters						
Receiver cascaded noise figure	At maximum gain		–	4.0	–	dB
Input In-Band IP3	Maximum LNA gain		–	-16.0	–	dBm
	Minimum LNA gain		–	4.0	–	dBm
LPF 3 dB Bandwidth			5.0	–	40	MHz
Maximum Receiver Gain			–	65.0	–	dB
Gain control step			–	3.0	–	dB
Return loss	Zo = 50O, across the dynamic range		–	10.0	–	dB
RSSI accuracy [38]	Range 90 dBm to 30 dBm		-3.0	–	3	dB
	Range above 30 dBm		-5.0	–	5	dB

Notes
32. Derate by TBD for -40 °C to TBD and by TBD for +85 °C to TBD.
33. Sensitivity with one Rx core active.
34. Sensitivity with two Rx core active and MRC combining (for Nss=1).
35. Sensitivity degradations for alternate settings in MCS modes. SGI: TBD dB drop.
36. Desired signal is at a power level 6 dB higher than the IEEE specification for the minimum sensitivity limit.
37. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
38. The minimum and maximum values shown have a 95% confidence level.

15.4 WLAN 2.4 GHz Transmitter Performance Specifications

Note The values in Table 31 are specified at the RF port unless otherwise noted.

Table 31. WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Note	Min	Typ	Max	Unit
EVM not exceed @ output power					
TX power at the chip port for highest power level setting at 25 °C and VBAT = 3.3 V with spectral mask and EVM compliance [39]	DSSS- 1 Mbps	–	22.0	–	dBm
	DSSS- 11 Mbps	–	22.0	–	dBm
	OFDM - BPSK, R=3/4	–	21.0	–	dBm
	OFDM - QPSK, R=3/4	–	20.0	–	dBm
	OFDM - 16QAM, R=3/4	–	20.0	–	dBm
	OFDM - 64QAM, R=3/4	–	20.0	–	dBm
	OFDM - 64QAM, R=5/6	–	19.0	–	dBm
	OFDM - 256QAM, R=3/4	–	15.0	–	dBm
	OFDM - 256QAM, R=5/6	–	14.5	–	dBm
Carrier suppression		–	-45.0	–	dBc
TX power control dynamic range		–	32	–	dB
Gain control step		–	0.5	–	dB
Closed-loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies to TBD dBm to TBD dBm output power range.	–	±1.5	–	dB

Note
39. The TX power at the chip output port is controlled by firmware and is approximately TBD dB lower from the minimum numbers mentioned here, to account for closed loop TX power control variation and other factors.

15.5 WLAN 5 GHz Receiver Performance Specifications

Note The values in Table 32 are specified at the RF port unless otherwise noted.

Table 32. WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Note		Min.	Typ.	Max.	Unit
Sensitivity						
Rx Sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU)[40], [41]	6 Mbps		–	-95.9	–	dBm
	9 Mbps		–	-94.4	–	dBm
	12 Mbps		–	-92.9	–	dBm
	18 Mbps		–	-90.3	–	dBm
	24 Mbps		–	-87.3	–	dBm
	36 Mbps		–	-84.0	–	dBm
	48 Mbps		–	-79.1	–	dBm
	54 Mbps		–	-77.6	–	dBm
Rx Sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU) [40], [42]	6 Mbps		–	-99.4	–	dBm/core
	9 Mbps		–	-95.4	–	dBm/core
	12 Mbps		–	-94.9	–	dBm/core
	18 Mbps		–	-92.8	–	dBm/core
	24 Mbps		–	-89.8	–	dBm/core
	36 Mbps		–	-86.5	–	dBm/core
	48 Mbps		–	-81.6	–	dBm/core
	54 Mbps		–	-80.1	–	dBm/core
Rx Sensitivity IEEE 802.11n 20MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC [40], [42], [43]	MCS0		–	-98.5	–	dBm/core
	MCS1		–	-94.3	–	dBm/core
	MCS2		–	-93.3	–	dBm/core
	MCS3		–	-91.3	–	dBm/core
	MCS4		–	-87.7	–	dBm/core
	MCS5		–	-83.7	–	dBm/core
	MCS6		–	-82.2	–	dBm/core
	MCS7		–	-80.3	–	dBm/core
	MCS8		–	-96.7	–	dBm/core
	MCS15		–	-77.8	–	dBm/core

Notes

40. Derate by TBD for -40 °C to TBD and by TBD for +85 °C to TBD.
41. Sensitivity with one Rx core active.
42. Sensitivity with both Rx cores active and MRC combining (for Nss=1).
43. Sensitivity degradations for alternate settings in MCS modes. SGI: TBD dB drop.
44. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
45. The minimum and maximum values shown have a 95% confidence level.

Table 32. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Note		Min.	Typ.	Max.	Unit
Rx Sensitivity IEEE 802.11n 40 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC [40], [42], [43]	MCS0		–	-96.8	–	dBm/core
	MCS1		–	-93.0	–	dBm/core
	MCS2		–	-90.9	–	dBm/core
	MCS3		–	-87.4	–	dBm/core
	MCS4		–	-84.8	–	dBm/core
	MCS5		–	-80.8	–	dBm/core
	MCS6		–	-79.0	–	dBm/core
	MCS7		–	-77.3	–	dBm/core
	MCS8		–	-93.7	–	dBm/core
	MCS15		–	-74.8	–	dBm/core
Rx Sensitivity IEEE 802.11ac 20 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC [40], [42], [43]	MCS7, Nss=1		–	-77.4	–	dBm/core
	MCS8, Nss=1		–	-73.7	–	dBm/core
Rx Sensitivity IEEE 802.11ac 40 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC [40], [42], [43]	MCS7, Nss=1		–	-74.5	–	dBm/core
	MCS8, Nss=1		–	-70.9	–	dBm/core
	MCS9, Nss=1		–	-68.9	–	dBm/core
Rx Sensitivity IEEE 802.11ac 80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC [40], [42], [43]	MCS7, Nss=1		–	-71.8	–	dBm/core
	MCS8, Nss=1		–	-68.1	–	dBm/core
	MCS9, Nss=1		–	-66.0	–	dBm/core
Rx Sensitivity IEEE 802.11ax 20 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF, LDPC, non-STBC, and 20 MHz BW [40], [42], [43]	MCS0, Nss=1		–	-96.1	–	dBm/core
	MCS7, Nss=1		–	-77.5	–	dBm/core
	MCS8, Nss=1		–	-73.7	–	dBm/core
	MCS9, Nss=1		–	-71.6	–	dBm/core
	MCS11, Nss=1		–	-64.0	–	dBm/core
Rx Sensitivity IEEE 802.11ax 40 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF, LDPC, non-STBC, and 40 MHz BW [40], [42], [43]	MCS0, Nss=1		–	-93.5	–	dBm/core
	MCS7, Nss=1		–	-74.9	–	dBm/core
	MCS8, Nss=1		–	-70.9	–	dBm/core
	MCS9, Nss=1		–	-69.1	–	dBm/core
	MCS11, Nss=1		–	-61.5	–	dBm/core

Notes
40. Derate by TBD for -40 °C to TBD and by TBD for +85 °C to TBD.
41. Sensitivity with one Rx core active.
42. Sensitivity with both Rx cores active and MRC combining (for Nss=1).
43. Sensitivity degradations for alternate settings in MCS modes. SGI: TBD dB drop.
44. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
45. The minimum and maximum values shown have a 95% confidence level.

Table 32. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Note		Min.	Typ.	Max.	Unit
Rx Sensitivity IEEE 802.11ax 80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF, LDPC, non-STBC, and 80 MHz BW [40], [42], [43]	MCS0, Nss=1		–	-90.4	–	dBm/core
	MCS7, Nss=1		–	-71.6	–	dBm/core
	MCS8, Nss=1		–	-69.6	–	dBm/core
	MCS9, Nss=1		–	-65.9	–	dBm/core
	MCS11, Nss=1		–	-58.3	–	dBm/core
Rx Sensitivity IEEE 802.11ax HE-RE PPDU (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF [40], [42], [43]	RU242, MCS0, Nss=1		–	-96.1	–	dBm/core
	RU106, MCS0, Nss=1		–	-97.2	–	dBm/core
Rx Sensitivity IEEE 802.11ax HE-RE PPDU (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF [40], [42], [43]	RU242, MCS0, Nss=1		–	-97.9	–	dBm/core
	RU106, MCS0, Nss=1		–	-98.6	–	dBm/core
ACI/ AACI						
Adjacent Channel Rejection - OFDM (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as 3 dB higher than IEEE spec) [40]	6 Mbps	–79 dBm	–	25.0	–	dB
	54 Mbps	–62 dBm	–	5.0	–	dB
Adjacent Channel Rejection - MCS0–8 in 20 MHz (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec) [44]	MCS0	–79 dBm	–	25.0	–	dB
	MCS7	–61 dBm	–	5.0	–	dB
Adjacent Channel Rejection - MCS0–11 in 40 MHz (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec) [44]	MCS0, Nss=1	–76 dBm	–	24.0	–	dB
	MCS7, Nss=1	–58 dBm	–	5.0	–	dB
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1024 octet PSDU for:(RxSens + 23 dB < Rxlevel < max. input level)		–	-80.0	–	dBm

Notes
40. Derate by TBD for -40 °C to TBD and by TBD for +85 °C to TBD.
41. Sensitivity with one Rx core active.
42. Sensitivity with both Rx cores active and MRC combining (for Nss=1).
43. Sensitivity degradations for alternate settings in MCS modes. SGI: TBD dB drop.
44. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
45. The minimum and maximum values shown have a 95% confidence level.

Table 32. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Note		Min.	Typ.	Max.	Unit
Other RF Parameters						
Receiver cascaded noise figure	At maximum gain		–	4.0	–	dB
Input In-Band IP3	Maximum LNA gain		–	-16.0	–	dBm
	Minimum LNA gain		–	5.0	–	dBm
LPF 3 dB Bandwidth			5	–	40	MHz
Maximum Receiver Gain			–	–	–	dB
Gain control step			–	3.0	–	dB
Return loss	Zo = 50O, across the dynamic range		–	10.0	–	dB
RSSI accuracy [45]	Range 90 dBm to 30 dBm		-3	–	3	dB
	Range above 30 dBm		-5	–	5	dB

Notes
40. Derate by TBD for -40 °C to TBD and by TBD for +85 °C to TBD.
41. Sensitivity with one Rx core active.
42. Sensitivity with both Rx cores active and MRC combining (for Nss=1).
43. Sensitivity degradations for alternate settings in MCS modes. SGI: TBD dB drop.
44. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
45. The minimum and maximum values shown have a 95% confidence level.

15.6 WLAN 5 GHz Transmitter Performance Specifications

Note The values in Table 33 are specified at the RF port unless otherwise noted.

Table 33. WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition	EVM	Min	Typ	Max	Unit
EVM not exceed @ output power						
TX power at the chip port for highest power level setting at 25 °C and VBAT = 3.3 V with spectral mask and EVM compliance [46]	OFDM - BPSK, R=3/4	–8 dB	–	19.0	–	dBm
	OFDM - QPSK, R=3/4	–13 dB	–	19.0	–	dBm
	OFDM - 16QAM, R=3/4	–19 dB	–	19.0	–	dBm
	OFDM - 64QAM, R=3/4	–25 dB	–	19.0	–	dBm
	OFDM - 64QAM, R=5/6	–28 dB	–	17.0	–	dBm
	OFDM - 256QAM, R=3/4	–30 dB	–	13.0	–	dBm
	OFDM - 256QAM, R=5/6	–32 dB	–	12.5	–	dBm
Carrier suppression			–	-45.0	–	dBc
TX power control dynamic range			–	32	–	dB
Gain control step			–	0.5	–	dB
Closed-loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies to TBD dBm to TBD dBm output power range.		–	±1.5	–	dB

Note
46. The TX power at the chip output port is controlled by firmware and is approximately TBDdB lower from the minimum numbers mentioned herein, to account for closed loop TX power control variation and other factors.

15.7 General Spurious Emissions Specifications

Table 34. General Spurious Emissions Specifications

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
TX emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–85.0	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–31.0	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–81.0	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–86.0	–	dBm
RX standby emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–100.0	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–60.0	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–87.0	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–87.0	–	dBm

16. Internal Regulator Electrical Specifications

Functional operation is not guaranteed outside of the specification limits provided in this section.

16.1 Core Buck Switching Regulator

Table 35. Core Buck Switching Regulator Specifications

Specification	Symbol	Notes	Min.	Typ.	Max.	Unit
Input supply voltage	V_{BAT}	DC voltage range inclusive of disturbances.	3.0	3.3	4.8	V
Switching Frequency	F_{SW}	With calibration (PWM mode only)	3.04	3.2	3.36	MHz
		Programming range	2.8	–	5	
Output current	I_{OUT}	PWM mode. Peak rating 800 mA at Tj≤110 °C Max DC rating 650 mA at Tj 125 °C	–	–	400	mA
Output current limit	I_{OUT_LIMIT}	Peak inductor current	–	1.8	–	A
Output voltage	V_{OUT}	–	–	0.9	–	V
DC accuracy	$V_{OUT\_\Delta ERR}$	Includes line & load regulation.	–4	–	4.0	%
		After trim at PWM mode.	–2	–	2	
Ripple voltage[47]	ΔVOUT_R	PWM mode	–	5	10	mVpp
		PFM mode (Measure with 20 MHz BW limit at static load).	–	7	20	
Efficiency[47]	E_{FF_PWM}	PWM Peak efficiency at 200 mA. Inductor's DCR Typ = 114 mΩ, ACR Typ = 1Ω. Fsw = 3.2 MHz	–	89	–	%
	E_{FF_LPPFM}	LPPFM efficiency at 50 mA. Inductor's DCR Typ = 114 mΩ, ACR Typ=1 Ω.	–	89	–	%
Start-up time	T_{SU}	With VDDIO = 1.8V as always ON. Measure from rising edge of REG_ON to CSR_pok	–	420	–	µs
External inductor	L	Effective inductance	–	2.2	–	µH
External output capacitor[48]	C_o	Effective load capacitance	–	4.7	–	µF
External input capacitor[48]	C_{IN}	Effective load capacitance	–	4.7	–	µF

Notes

47. Efficiency numbers are assumed at typical condition (i.e. VBAT = 3.3 V, VDDIO =1.8 V, ASR VOUT =1.12 V, and CSR VOUT =0.9 V at room temp = 27 °C). Component parts used for L = 2.2 µH, and CO = 4.7 µF.
48. Min cap value refers to effective cap value after taking into account part-to-part tolerance, DC-bias, temperature and aging. Typ cap value refers to manufacturer nominal part value. Max cap value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there is any).

16.2 Analog Switching Regulator Specifications

Table 36. Analog Switching Regulator Specifications

Specification	Symbol	Notes	Min.	Typ.	Max.	Unit
Input supply voltage	V_{BAT}	DC voltage range inclusive of disturbances	3.0	3.3	4.8	V
Switching Frequency	F_{SW}	With calibration (PWM mode only)	3.04	3.2	3.36	MHz
		Programming range	2.8	–	5	
Output current	I_{OUT}	PWM mode. Peak rating 800mA at Tj≤110 °C Max DC rating 650mA at Tj 125 °C	–	–	400	mA
Output current limit	I_{OUT_LIMIT}	Peak inductor current	–	1.8	–	A
Output voltage	V_{OUT}	–	–	1.12	–	V
DC accuracy	$V_{OUT\_\Delta ERR}$	Includes line & load regulation.	–4	–	4.0	%
		After trim at PWM mode.	–2	–	2	
Ripple voltage[49]	$\Delta VOUT\_R$	PWM mode	–	5	10	mVpp
		PFM mode (Measure with 20 MHz BW limit at static load).	–	7	20	
Efficiency[49]	E_{FF_PWM}	PWM Peak efficiency at 200 mA. Inductor's DCR Typ=114 mΩ, ACR Typ=1 Ω. Fsw = 3.2 MHz	–	88	–	%
	E_{FF_LPPFM}	LPPFM efficiency at 50 mA. Inductor's DCR Typ = 114 mΩ, ACR Typ=1 Ω.	–	88	–	%
Start-up time	T_{SU}	With VDDIO = 1.8 V as always ON. Measure from rising edge of REG_ON to ASR_pok	–	450	–	µs
External inductor	L	Effective inductance	–	2.2	–	µH
External output capacitor[50]	C_o	Effective load capacitance	–	4.7	–	µF
External input capacitor[50]	C_{IN}	Effective load capacitance	–	4.7	–	µF

Notes

49. Efficiency numbers are assumed at typical condition (i.e. VBAT = 3.3 V, VDDIO =1.8 V, ASR VOUT =1.12 V, and CSR VOUT =0.9 V at room temp = 27 °C). Component parts used for L = 2.2 µH, and CO = 4.7 µF.
50. Min cap value refers to effective cap value after taking into account part-to-part tolerance, DC-bias, temperature and aging. Typ cap value refers to manufacturer nominal part value. Max cap value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there is any).

16.3 3.3 V LDO (VDDOUT_RF3P3)

Table 37. VDDOUT_RF3P3 Specifications

Specification	Symbol	Notes	Min.	Typ.	Max.	Unit
Input supply voltage	V_{BAT}	DC voltage range inclusive of disturbances.	3.0	3.3	4.8	V
Nominal output voltage	V_{OUT}	–	–	2.86	–	V
Output voltage programmability	–	Range	2.86	–	3.465	V
		Accuracy at any step	–4	–	4	%
Dropout voltage	–	Max load	200	–	–	mV
Output current	I_{OUT}	–	0.3	–	200	mA
Quiescent current	I_{Q_NoLoad}	I_{OUT} = 100 µA, V_{OUT} = 3.3 V	–	40	63	µA
	$I_{Q\_MaxLoad}$	I_{OUT} = 200 mA, V_{OUT} = 3.3 V	–	1.6	1.7	mA
Power-down Current	I_{Q_PD}	Typ at Ambient Temp 25 °C	–	16	–	nA
		Max at Ambient Temp 85 °C	–	–	13.8	µA
Line regulation	–	V_{BAT} from 3.5-5.5 V; I_{OUT} = 200 mA.	–	–	3.5	mV/V
Load regulation	–	Load from 1-200 mA; V_{BAT} = 3.3 V.	–	–	0.3	mV/mA
Load step error	–	Load from 1-100 mA in 1is at V_{BAT} = 3.3 V; C_o = 0.16 µF.	–	–	55	mV
PSRR	–	Freq from 100-100 kHz at max load. Freq at FSW at max load	20.0	–	–	dB
Turn-on time	T_{ON}	Measure from pµ signal to V_{OUT} = 3.2 V with reference ready. C_o= 2.2 µF	–	–	120	µs
Output current Limit	I_{OUT_LIMIT}	–	–	550	910	mA
In-rush current	I_{INRUSH}	–	–	68	116	mA
Output Capacitor[51]	C_o	See components section for details	–	2.2	–	µF

Note
51. Min cap value refers to effective cap value after taking into account part-to-part tolerance, DC-bias, temperature and aging. Typ cap value refers to manufacturer nominal part value. Max cap value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there is any).

16.4 3.3 V LDO (VDDOUT_BT3P3)

Table 38. VDDOUT_BT3P3 Specifications

Specification	Symbol	Notes	Min.	Typ.	Max.	Unit
Input supply voltage	V_{BAT}	DC voltage range inclusive of disturbances.	3.0	3.3	4.8	V
Nominal output voltage	V_{OUT}	–	–	2.86	–	V
Output voltage programmability	–	Range	2.86	–	3.465	V
		Accuracy at any step	–4	–	4	%
Dropout voltage	–	Max load	200	–	–	mV
Output current	I_{OUT}	–	0.2	–	400	mA
Quiescent current	I_{Q_NoLoad}	I_{OUT} = 200 µA, V_{OUT} = 3.3 V	–	77	124	µA
	$I_{Q\_MaxLoad}$	I_{OUT} = 400 mA, V_{OUT} = 3.3 V	–	3.3	–	mA
Power-down Current	I_{Q_PD}	Typ at Ambient Temp 25 °C	–	11	–	nA
		Max at Ambient Temp 85 °C	–	–	25	µA
Line regulation	–	V_{BAT} from 3.5-5.5 V; I_{OUT} = 400 mA.	–	–	3.5	mV/V
Load regulation	–	Load from 1-400 mA; V_{BAT} = 3.3 V.	–	–	0.3	mV/mA
Load step error	–	Load from 1-200.5 mA in 1ìs at V_{BAT} = 3.3 V; C_o = 0.16 µF.	–	–	100	mV
PSRR	–	Freq from 100-100 kHz at max load. Freq at FSW at max load	20.0	–	–	dB
Turn-on time	T_{ON}	Measure from pµ signal to V_{OUT} =3.3 V with reference ready. C_o= 2.2 µF	–	–	150	µs
Output current Limit	I_{OUT_LIMIT}	–	–	1060	1800	mA
In-rush current	I_{INRUSH}	–	–	155	220	mA
Output Capacitor[52]	C_o	See components section for details	–	2.2	–	µF

Note
52. Min cap value refers to effective cap value after taking into account part-to-part tolerance, DC-bias, temperature and aging. Typ cap value refers to manufacturer nominal part value. Max cap value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there is any).

16.5 3.3 V LDO_PA3P3

Table 39. 3.3 V LDO_PA3P3

Specification	Symbol	Notes	Min.	Typ.	Max.	Unit
Input supply voltage	V_{BAT}	Range	2.7	3.3	4.8	V
Nominal output voltage	V_{OUT}			2.86		V
Output voltage programmability	–	Range	2.86	–	3.465	V
Output voltage accuracy	–		-4	–	4	%
Dropout voltage	–	I_{OUT} = 800 mA	200	–	–	mV
Output current	I_{OUT}		0.4	–	800	mA
Quiescent current	$I_{Q(MIN)}$	I_{OUT} = 400 mA, V_{OUT} = 3.3 V	–	151	247	µA
	$I_{Q(MAX)}$	I_{OUT} = 800 mA, V_{OUT} = 3.3 V	–	6.5	6.8	mA
Power-down current	$I_{Q(PD)}$	Typ @ 25 °C	–	1.7	2.8	µA
		Max @ 125 °C	–	29	47	
Line regulation	–	3.5 V ≤ V_{BAT} ≤ 4.8 V, I_{OUT} = 800 mA, V_{OUT}=3.3 V	–	–	3.5	mV/V
Load regulation	–	1 mA ≤ I_{OUT} ≤ 800 mA, V_{BAT} = 3.3 V, V_{OUT} = 3.3V	–	–	0.3	mV/mA
Load step error	–	Load step from 1 mA to 400 mA in 1 µs, V_{BAT} = 3.3 V, V_{OUT} = 3.3 V,C_{OUT} = 4.7 µF	–	–	85	mV
PSRR	–	100 Hz ≤ f_{TEST} ≤ 100 kHz	20	–	–	dB
		I_{OUT} = 800 mA				
Turn-on time[53]	T_{ON}	Time from “pu” asserted to V_{OUT} = 3.2 V, C_{OUT} = 4.7 µF	–	125	–	µs
Output current limit	$I_{OUT(LIMIT)}$	V_{IN} = 5 V, V_{OUT} = 3.3 V, increase I_{OUT} until V_{OUT} = 3.2 V	–	2.8	3.6	A
In-rush current	I_{INRUSH}	C_{OUT} = 4.7 µF	–	236	266	mA
Output capacitor	C_{OUT}	See components section for details	–	4.7	–	µF

Note
53. Refer to register map for actual inrush delay setting.

16.6 1 V LDO (VDDOUT_MISC)

Table 40. VDDOUT_MISC Specifications

Specification	Symbol	Notes	Min.	Typ.	Max.	Unit
Input supply voltage	V_{IN}	Dropout voltage requirement must be met for performance.	–	1.12	–	V
Nominal output voltage	V_{OUT}	–	–	1.005	–	V
Output voltage programmability	–	Range	0.85	–	1.2	V
		Accuracy at any step	–4	–	4	%
Dropout voltage	–	Max load	50	–	–	mV
Output current	I_{OUT}	–	0.1	–	60	mA
Quiescent current	I_{Q_NoLoad}	No load	–	–	7	µA
	$I_{Q\_MaxLoad}$	Maximum load	–	–	2	mA
Power-down Current	I_{Q_PD}	V_{IN} = 1.12 V Typ at Junction Temp 25 °C, Max at Junction Temp 85 °C	–	1	14	µA
Bypass Current	I_{Q_byp}	V_{IN}= 0.8 V (Chip DS0) Typ at Junction Temp 25 °C, Max at Junction Temp 85 °C	–	–	1	µA
Line regulation	–	V_{IN} from (V_{OUT} + V_d) - 1.3 V; V_{IOUT} = 60 mA.	–	–	1	mV/V
Load regulation	–	Load from 1-60 mA; V_{IN} = 1.22 V.	–	–	125	mV/A
Load step error	–	Load from 1-60 mA in 100 ns V_{IN}=1.22 V; C_o = 0.5 µF effective.	–	–	40	mV
PSRR	–	Freq from 100-100 kHz at ½ max load. Freq at FSW at ½ max load	20.0	–	–	dB
Turn-on time	T_{ON}	Measure from pu signal to V_{OUT} = 1.0 V with reference ready. C_o = 1 µF	–	40	–	µs
In-rush current	I_{INRUSH}	C_o = 1 µF	–	–	60	mA
Output Capacitor[54]	C_o	See components section for details	–	1	–	µF

Note

54. Min cap value refers to effective cap value after taking into account part-to-part tolerance, DC-bias, temperature and aging. Typ cap value refers to manufacturer nominal part value. Max cap value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there is any).

17. System Power Consumption

17.1 WLAN Current Consumption

The WLAN current consumption measurements are shown in Table 41.

All values in Table 41 are with the Bluetooth core in reset (that is, Bluetooth is OFF).

Table 41. Typical WLAN Power Consumption

Mode	Bandwidth (MHz)	Band (GHz)	V_{bat} = 3.3V mA	V_{io} = 1.8V µA[55]
Sleep Modes				
OFF[56]	–	–	–	–
Sleep[57]	–	–	–	–
IEEE power save, DTIM 1 1 RX core[58]	20.0	2.4	2.6	210
IEEE power save, DTIM 3 1 RX core[58]	20.0	2.4	1.3	210
IEEE power save, DTIM 1 1 RX core[58]	20.0	5.0	2.1	215
IEEE power save, DTIM 3 1 RX core[58]	20.0	5.0	1.0	215
IEEE power save, DTIM 1 1 RX core[58]	40.0	5.0	2.3	215
IEEE power save, DTIM 3 1 RX core[58]	40.0	5.0	1.0	215
IEEE power save, DTIM 1 1 RX core[58]	80.0	5.0	3.0	215
IEEE power save, DTIM 3 1 RX core[58]	80.0	5.0	1.3	215
Active Modes				
Transmit				
CCK 1 chain[59]	20.0	2.4	320	33
MCS7, SGI[60], [61], [62]	20.0	2.4	271	33
MCS15, SGI[60], [61], [62]	20.0	5.0	523	33
6 Mbps	20.0	5.0	390	33
MCS8, Nss 1, HT20	20.0	5.0	357	33
MCS7[60], [61], [62]	40.0	5.0	392	33
MCS9, Nss 1, SGI[60], [61], [63]	40.0	5.0	375	33
MCS9, Nss 2, SGI[60], [61], [63]	40.0	5.0	702	33
MCS9, Nss 1, SGI[60], [61], [63]	80.0	5.0	414	33
MCS9, Nss 2, SGI[60], [61], [63]	80.0	5.0	772	33
Receive				
1 Mbps, 1 RX core	20.0	2.4	81	33
MCS7, HT20 1 RX core[64]	20.0	2.4	89	33
MCS15, HT20[64]	20.0	2.4	121	33
CRS 1 RX core[65]	20.0	2.4	80	33
6 Mbps	20.0	5.0	91	33

Notes
55. Specified with all pins idle (not switching) and not driving any loads.
56. WL_REG_ON, BT_REG_ON both low.
57. Idle, not associated, or inter-beacon.
58. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps. Average current over three DTIM intervals.
59. Output power per core at RF port = 21 dBm.
60. Duty cycle is 100%.
61. Measured using Packet engine test mode.
62. Output power per core at RF port = 17.5 dBm.
63. Output power per core at RF port = 14 dBm.
64. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
65. Carrier sense (CCA) when no carrier is present.

Table 41. Typical WLAN Power Consumption (Cont.)

Mode	Bandwidth (MHz)	Band (GHz)	V_{bat} = 3.3V mA	V_{io} = 1.8V µA[55]
Receive MCS7, SGI 1 RX core[64]	20.0	5.0	96	33
Receiver MCS15, SGI[64]	20.0	5.0	142	33
CRS 1 RX core[65]	20.0	5.0	84	33
Receive MCS 7, SGI 1 RX core[64]	40.0	5.0	120	33
Receive MCS 15, SGI[64]	40.0	5.0	198	33
CRS 1 RX core[65]	40.0	5.0	102	33
Receive MCS9, Nss 1, SGI[64]	80.0	5.0	172	33
Receive MCS9, Nss 2, SGI[64]	80.0	5.0	283	33
CRS 1 RX core[64]	80.0	5.0	140	33

Notes
55. Specified with all pins idle (not switching) and not driving any loads.
56. WL_REG_ON, BT_REG_ON both low.
57. Idle, not associated, or inter-beacon.
58. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps. Average current over three DTIM intervals.
59. Output power per core at RF port = 21 dBm.
60. Duty cycle is 100%.
61. Measured using Packet engine test mode.
62. Output power per core at RF port = 17.5 dBm.
63. Output power per core at RF port = 14 dBm.
64. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
65. Carrier sense (CCA) when no carrier is present.

17.2 Bluetooth Current Consumption

The Bluetooth and BLE current consumption measurements are shown in Table 42.

Note

- The WLAN core is in reset (WL_REG_ON = low) for all measurements provided in Table 42.
- The BT current consumption numbers are measured based on GFSK TX output power = 10 dBm

Table 42. Bluetooth and BLE Current Consumption

Operating Mode	VBAT (VBAT = 3.3V) Typical	VDDIO (VDDIO = 1.8V) Typical	Unit
Sleep	6.0	130	µA
Standard 1.28s inquiry scan	148.5	153	µA
500 ms sniff master	160	135	µA
DM1/DH1	25.0	0.05	mA
DM3/DH3	30.0	0.064	mA
DM5/DH5	30.0	0.068	mA
3DH5/3DH1 master	25.5	0.135	mA
SCO HV3 master	12.5	0.103	mA
BLE scan	160.5	153.3	µA
BLE adv. unconnectable 1 sec	68.5	138	µA
BLE connected 1 sec	60.0	153.3	µA

18. Interface Timing and AC Characteristics

18.1 PCI Express Interface Parameters

Table 43. PCI Express Interface Parameters

Parameter	Symbol	Comments	Minimum	Typical	Maxi-mum	Unit
General						
Baud rate	BPS	–	–	5	–	Gbaud
Reference clock amplitude	Vref	LVPECL, AC coupled	0.95	–	–	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80.0	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40.0	50.0	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	–	–	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	–	–	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	–	–	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	–	–	UI
Differential return loss	RLRX-DIFF	Differential return loss	10.0	–	–	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	–	–	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	–	–	10.0	ms
Signal detect threshold	VRX-IDLE-DET-DIFF p-p	Electrical idle detect threshold	65.0	–	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	–	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	–	–	600	mV
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	–	–	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	–	–	20.0	mV

Table 43. PCI Express Interface Parameters (Cont.)

Parameter	Symbol	Comments	Minimum	Typical	Maximum	Unit
Absolute delta of DC common-model voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-model voltage during L0 and electrical idle.	0	–	100	mV
Absolute delta of DC common-model voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	–	25.0	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	–	20.0	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	–	–	90.0	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80.0	–	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	–	–	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6.0	–	–	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	–	–	UI

18.2 JTAG Timing

Table 44. JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

19. Power-Up Sequence and Timing

19.1 Sequencing of Reset and Regulator Control Signals

CYW8x570 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 28, Figure 29, Figure 30, and Figure 31). The timing values indicated are minimum required values; longer delays are also acceptable.

19.1.1 Description of Control Signals

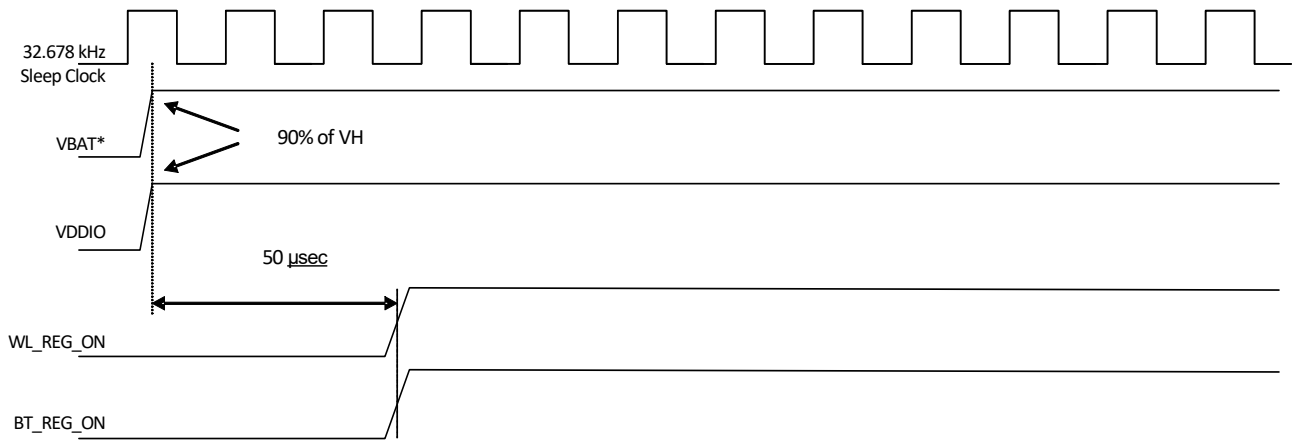
- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW8x570 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW8x570 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note

- CYW8x570 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating PCIe accesses.
- VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.

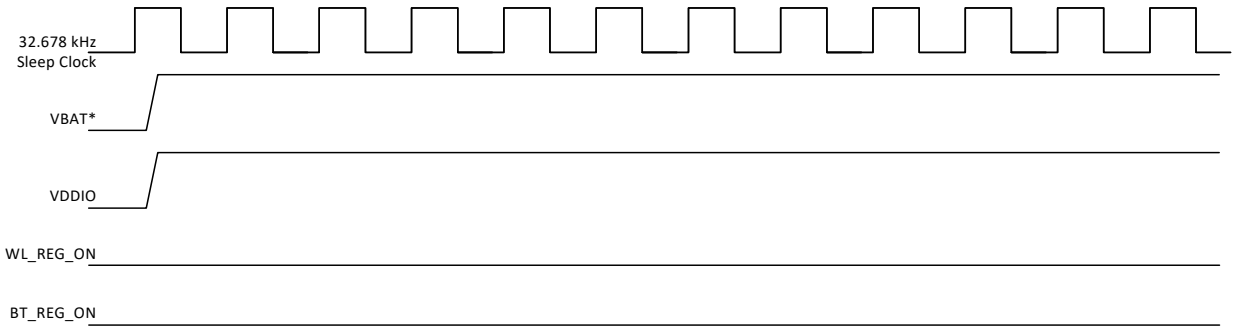
19.1.2 Control Signal Timing Diagrams

Figure 28. WLAN = ON, Bluetooth = ON



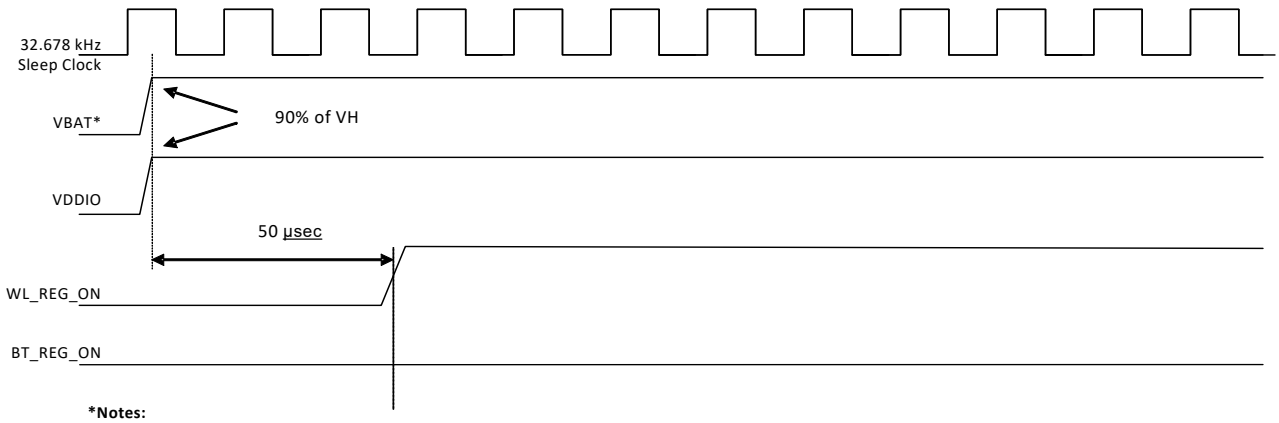
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 29. WLAN = OFF, Bluetooth = OFF



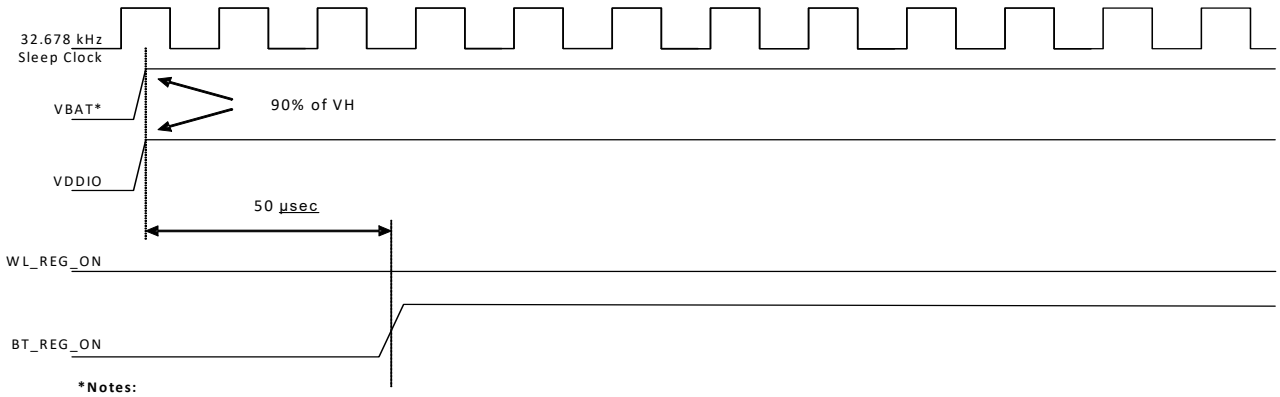
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 30. WLAN = ON, Bluetooth = OFF



***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

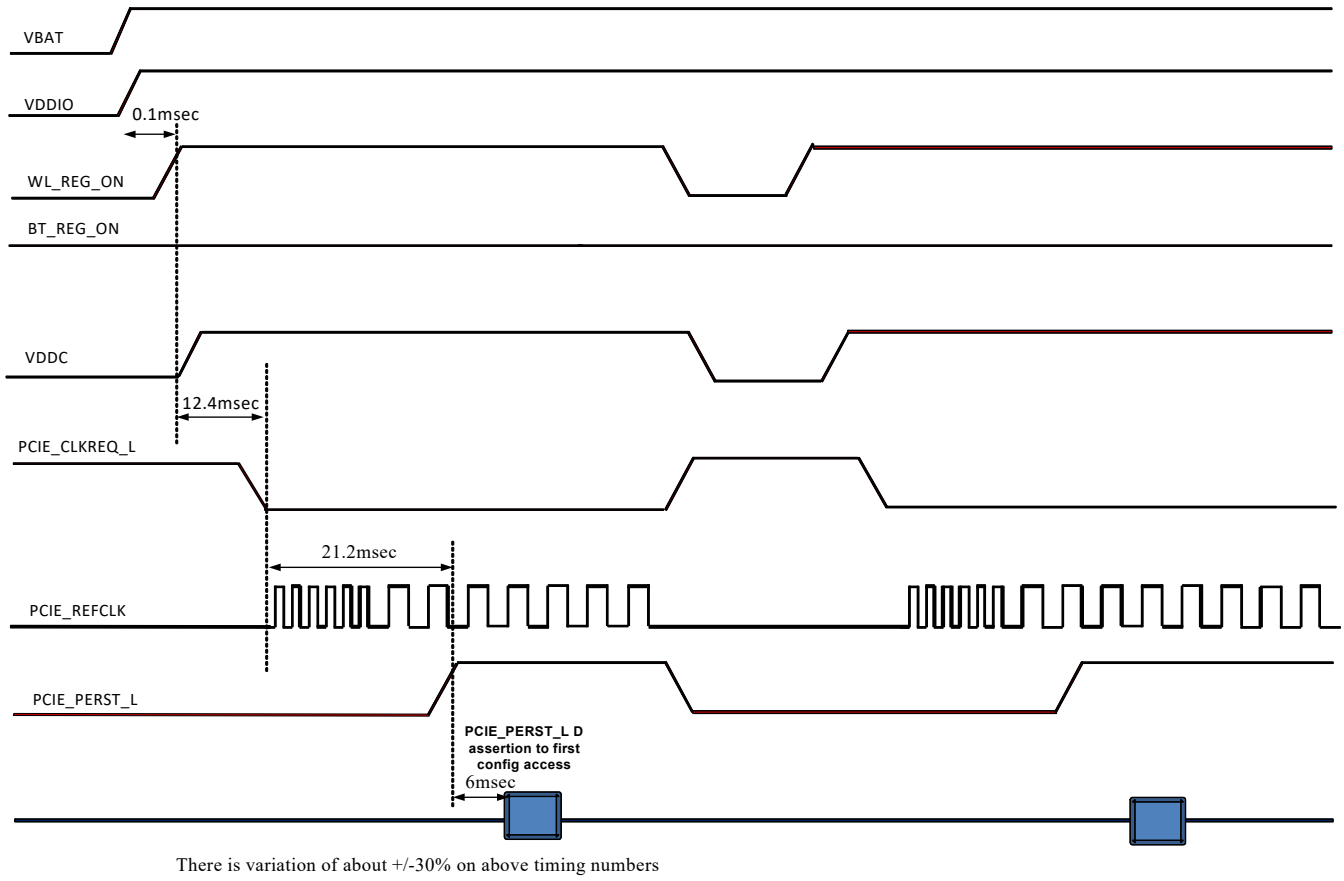
Figure 31. WLAN = OFF, Bluetooth = ON



***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 32 shows the WLAN boot-up sequence from power-up to firmware download.

Figure 32. WLAN Power-Up Sequence for PCIe Host



There is variation of about +/-30% on above timing numbers

20. Package Information

20.1 Package Thermal Characteristics

The information in Table 45 is based on the following conditions:

- Absolute junction temperature 125 °C limit is maintained through active thermal monitoring, throttling and turning off one of the TX chains, or both.

Table 45. FCBGA Package Thermal Characteristics

Characteristic	FCBGA
θ_{JA} (°C/W) (value in still air)	27.3
θ_{JB} (°C/W)	15.5
θ_{JC} (°C/W)	15.1
Ψ_{JT} (°C/W)	1.8
Ψ_{JB} (°C/W)	17.5
Maximum Junction Temperature T_j (°C)	123.22
Maximum Power Dissipation (W)	1.4

20.2 Junction Temperature Estimation and PSI_{JT} Versus $Theta_{JC}$

The package thermal characterization parameter PSI_{JT} (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) than using the junction-to-case thermal resistance parameter $Theta_{JC}$ (θ_{JC}). The reason for this is that θ_{JC} is based on the assumption that all the power is dissipated through the top surface of the package case. In actual applications, however, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account the power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

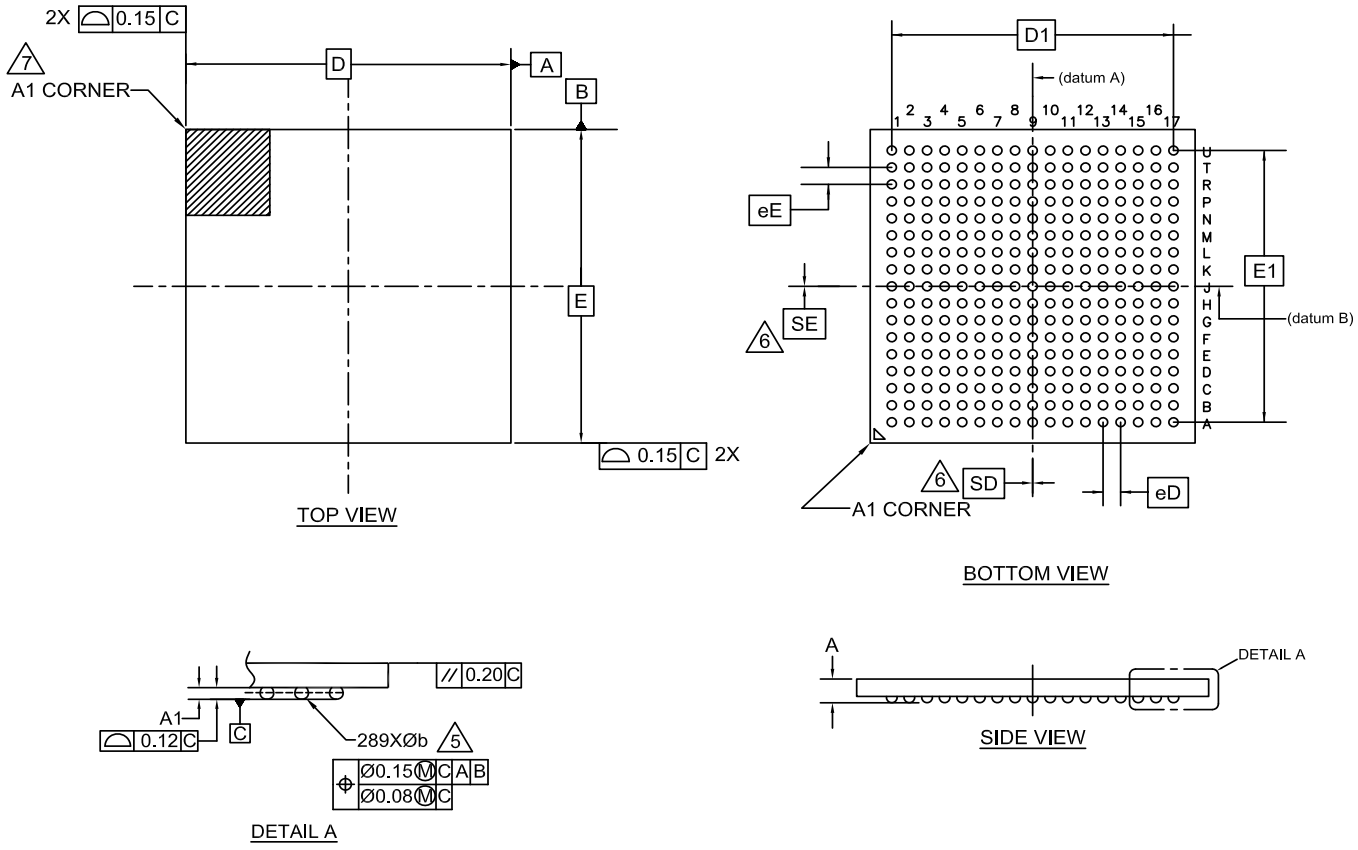
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

20.3 Environmental Characteristics

For environmental characteristics data, see Table 22.

21. Mechanical Information

Figure 33. Package Outline, 289 Ball FCFBGA 12 x12 x1.20 mm



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-------	-------	1.20
A1	0.22	-------	------
D	12.00 BSC		
E	12.00 BSC		
D1	10.40 BSC		
E1	10.40 BSC		
MD	17		
ME	17		
N	289		
Ø b	0.31	0.36	0.41
eD	0.65 BSC		
eE	0.65 BSC		
SD	0.00 BSC		
SE	0.00 BSC		

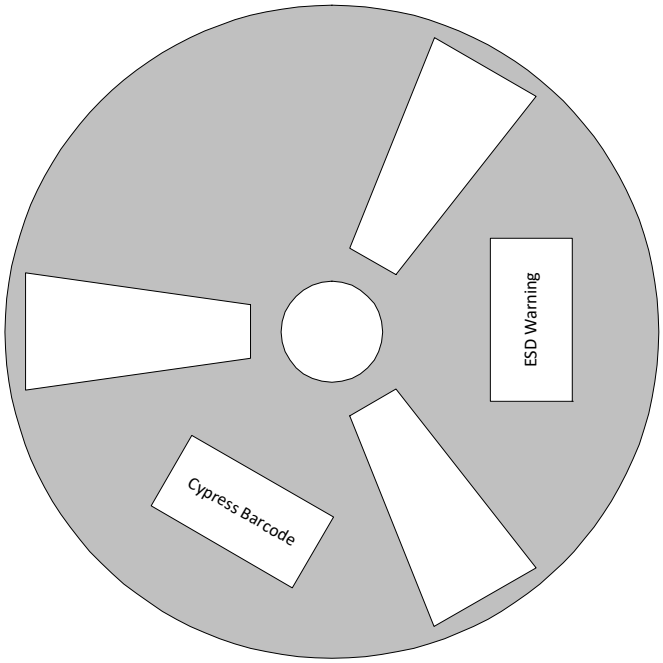
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A.

002-29083 *A

21.1 Tape, Reel, and Packing Specification

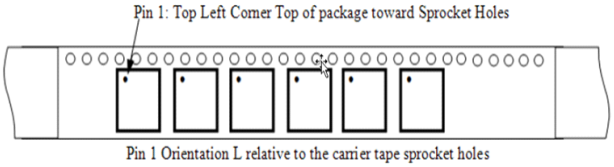
Figure 34. Reel, Labeling, and Packaging



Reel Diameter: 330 +/- 2.0 mm

Device Orientation/Mix Lot Number

Each reel may contain up to three lot numbers, independent of the date code. Individual lots must be labeled on the box, moisture barrier bag, and the reel.



22. Ordering Information

Table 46. Part Ordering Information

Part Number	Package	Description	Operating Ambient Temperature
CYW89570CFFBG	289-ball FCBGA (12mm x 12mm, 0.65mm pitch)	Tri-band 2.4/5/6GHz 802.11ax 2x2 MIMO WLAN and Bluetooth 5.2 Tray	–40 °C to +85 °C
CYW89570CFFBGT	289-ball FCBGA (12mm x 12mm, 0.65mm pitch)	Tri-band 2.4/5/6GHz 802.11ax 2x2 MIMO WLAN and Bluetooth 5.2 Tape and Reel	
CYW88570CFFBG	289-ball FCBGA (12mm x 12mm, 0.65mm pitch)	Tri-band 2.4/5/6GHz 802.11ax 2x2 MIMO WLAN and Bluetooth 5.2 Tray	
CYW88570CFFBGT	289-ball FCBGA (12mm x 12mm, 0.65mm pitch)	Tri-band 2.4/5/6GHz 802.11ax 2x2 MIMO WLAN and Bluetooth 5.2 Tape and Reel	

Note : CYW89570 parts receive Automotive grade testing and CYW88570 parts receive Industrial grade testing. Both CYW89570 and CYW88570 parts are AEC Q-100 tested and manufactured in ISO/TS16949 certified Fabrication facilities.

23. Additional Information

23.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: www.cypress.com/glossary.

Table 47. Acronyms Used in this Document

Term	Description
AES	Advanced Encryption Standard
AES-CTR	Advanced Encryption Standard-Counter Mode
ALU	Arithmetic logic unit
APB	advanced peripheral bus
APU	audio processing unit
CBC-MAC	Cipher Block Chaining Message Authentication Code
CCK	Complementary Code Keying
CCM	Counter with Cipher block chaining Message authentication code
CSC	Cypress Serial Control
CTS	Clear to Send
DMA	direct memory access
DSSS	Direct Sequence Spread Spectrum
DTE	Data Termination Equipment
EIR	Extended inquiry response
EPR	Encryption pause resume
ESR	Equivalent Series Resistance
eSCO	Extended synchronous connections
FEM	Front-End Module
FFT	Fast Fourier Transform
HCI	Host Control Interface
IRQ	interrupt request
JTAG	Joint Test Action Group
LCU	link control unit
LDO	low drop-out
LST	Link supervision timeout
LTE	Long Term Evolution
MIB	Management Information Base
MIC	Message Integrity Check
MSB	Most Significant Bit
OFDM	Orthogonal Frequency Division Multiplexing
PDM	pulse density modulation
PLL	phase locked loop
POR	power-on reset

Table 47. Acronyms Used in this Document (Cont.)

Term	Description
RTS	Request to Send
RX/TX	receive, transmit
SPI	serial peripheral interface
SP3T	Single Pole 3 Throw
SSP	Secure simple pairing
SSR	Sniff subrating
SWD	serial wire debug
TKIP	Temporal Key Integrity Protocol
TXOP	Transmit Opportunity
UART	universal asynchronous receiver/transmitter
WD	watchdog
WEP	wired equivalent privacy
WPA	Wi-Fi Protected Access
QoS	Quality of Service

23.2 References

The references in this section may be used in conjunction with this document.

Note
Cypress provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see IoT Resources).

For Cypress documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Bluetooth MWS Coexistence 2–wire Transport Interface Specification	–	www.bluetooth.com

23.3 IoT Resources

Cypress provides a wealth of data at www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (community.cypress.com)

Document History

Document Title: CYW8x570 Single-chip Tri-band 802.11ax 2x2 MIMO Wi-Fi with Bluetooth 5.2 for Automotive Applications Document Number: 002-29959			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	6838335	3/26/2020	Initial Release
*A	6909239	06/30/2020	Assorted Bluetooth Peripheral Transport Units section. Removed SDIO across all section in the datasheet. Updated Figure 5.Typical Power Topology. Corrected power-up-sequence timing Corrected WLAN Tx power control dynamic range in Figure 28, Figure 30 and Figure 31.
*B	6938425	07/30/2020	Updated typical input values of VBAT and VDDIO.

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