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Reduced Gigabit Media Independent Interface (RGMII)

Technical Data Sheet

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Proprietary Notice

Reduced Gigabit Media Independent Interface (RGMII)

Features

- Reduced GMII interface to physical layer
- Capable of working at 1 Gb/s, 100 Mb/s and 10 Mb/s data rates
- Selectable RGMII or reduced ten bit interface (RTBI) output
- Comma code-groups realignment in RTBI mode
- Optional registered DDR transmit output signals

Description

The Reduced Gigabit Media Independent Interface (RGMII) module provides an RGMII interface to an existing Ethernet MAC design with a GMII or TBI interface, for example the Gigabit Ethernet MAC (GEM) available from Cadence Design Foundry. The RGMII interface has been designed in accordance with the standards and specifications agreed in the Hewlett Packard document Reduced Gigabit Media Independent Interface (RGMII) Specifications. These are available for download at the following URLs http://www.hp.com/rnd/pdfs/RGMIIv1_3.pdf and http://www.hp.com/rnd/pdfs/RGMIIv2_0_final_hp.pdf

The RGMII module significantly reduces pin counts between the MAC and the physical layer. In applications where a number of Ethernet MAC and PHY interfaces are necessary, savings of up to 50% of the pin count are possible. This pin reduction is achieved by multiplexing data and control signals on both edges of the reference clocks. There are two modes of operation, RGMII mode and RTBI mode, with the current mode being selected by the `tbi` input signal.

- In RGMII mode, the number of data pins has been reduced from 8 to 4 for both receive and transmit, with a saving of 8 pins in total. This requires the use of both edges of the clock in order to maintain the bandwidth. In RTBI mode, the ten bit receive and transmit code groups are each split into two separate 5 bit groups and driven across the four data pins and the control pin, saving 10 pins in total.
- In RGMII mode, gmii_tx_er and gmii_tx_en are multiplexed over the rgmii_tx_ctl signal for transmission into a single clock period. Similarly for receive, gmii_rx_er and gmii_rx_dv have been encoded and multiplexed together into rgmii_rx_ctl. This saves another 2 pins.
- In RGMII mode, both gmii_col and gmii_crs from the PHY to the MAC can be decoded internally thus saving another 2 pins.

For 1 Gbit/s operation, clocks operate at 125 MHz. For 100 Mbit/s and 10 Mbit/s operation, clocks operate at 25 MHz and 2.5 MHz respectively.

The RGMII standard specifies a source synchronous clock with the data. It relies on the clock having a longer path delay than the data so that the data is resampled using the same edge of the clock on which it was generated.

In version 1.3 of the RGMII specification a 1.5 to 2ns clock delay is achieved through a PCB trace delay, in version 2.0 there is the option of introducing the delay on-chip at the source. Devices which support the internal delay are referred to as RGMII-ID.

Whether to support RGMII-ID is an implementation choice. The Cadence IP supports both versions of the specification.

Signal Interfaces

System Interface

Signal Name	I/O	Description
rgmii_tx_clk	I	RGMII transmit clock from system clock controller. This clock must also be sourced to the PHY.
rgmii_tx_clk_sig	I	rgmii_tx_clk clock used as signal to control multiplexer for rgmii_txd output data.
rgmii_tx_n_clk	I	RGMII transmit clock inverted.
rgmii_rx_clk	I	RGMII receive clock from the PHY.
rgmii_rx_n_clk	I	RGMII receive clock inverted.
rbc1_sig	I	rgmii_rx_clk timed signal indicating that rbc1 is active, used as signal to control TBI receive data alignment.
n_rgmii_txreset	I	Reset corresponding to rgmii_tx_clk. This signal should be asserted low asynchronously, and deasserted high synchronously with rgmii_tx_clk.
n_rgmii_tx_n_reset	I	Reset corresponding to rgmii_tx_n_clk. This signal should be asserted low asynchronously, and deasserted high synchronously with rgmii_tx_n_clk.
n_rgmii_rxreset	I	Reset corresponding to rgmii_rx_clk. This signal should be asserted low asynchronously, and deasserted high synchronously with rgmii_rx_clk.
n_rgmii_rx_n_reset	I	Reset corresponding to rgmii_rx_n_clk. This signal should be asserted low asynchronously, and deasserted high synchronously with rgmii_rx_n_clk.

MAC GMII Interface

Signal Name	I/O	Description
gmii_txd[7:0]	I	Transmit data signal generated by the MAC. This input must be synchronous with rgmii_tx_clk.
gmii_tx_en	I	Transmit enable signal generated by the MAC. This input must be synchronous with rgmii_tx_clk.
gmii_tx_er	I	Transmit error signal generated by the MAC. This input must be synchronous with rgmii_tx_clk.
gmii_rxd[7:0]	O	Receive data to the MAC. This output is generated synchronous to rgmii_rx_clk. In RTBI mode this output is

		driven low.
gmii_rx_dv	O	Receive data valid signal to the MAC to indicate that the value on gmii_rxd[7:0] is valid. This output is generated synchronous to rgmii_rx_clk. In RTBI mode this output is driven low.
gmii_rx_er	O	Receive error signal to the MAC to indicate that a code error has been detected at the PHY. This output is generated synchronous to rgmii_rx_clk. In RTBI mode this output is driven low.
gmii_col	O	Collision detect signal to the MAC to indicate the occurrence of transmission and reception at the same time in half duplex mode. This output is asserted asynchronously. In RTBI mode this output is driven low.
gmii_crs	O	Carrier sense indication to the MAC. This signal is asserted whenever the medium is in non-idle state. This signal is asserted asynchronously. In RTBI mode this output is driven low.

MAC TBI Interface

Signal Name	I/O	Description
tbi_tx_group[9:0]	I	10 bit code group for transmit path. This input must be synchronous with rgmii_tx_clk.
tbi_rx_group[9:0]	O	10 bit code group for receive path. This output is generated synchronous to rgmii_rx_clk. In RGMII mode this output is driven low.

PHY RGMII Interface

Signal Name	I/O	Description
rgmii_txd[3:0]	O	Transmit data signal to the PHY.
rgmii_tx_ctl	O	Transmit control signal to the PHY. In RTBI mode this is used for a fifth bit of data.
rgmii_rxd[3:0]	I	Receive data signal from the PHY.
rgmii_rx_ctl	I	Receive control signal from the PHY. In RTBI mode this is used for a fifth bit of data.

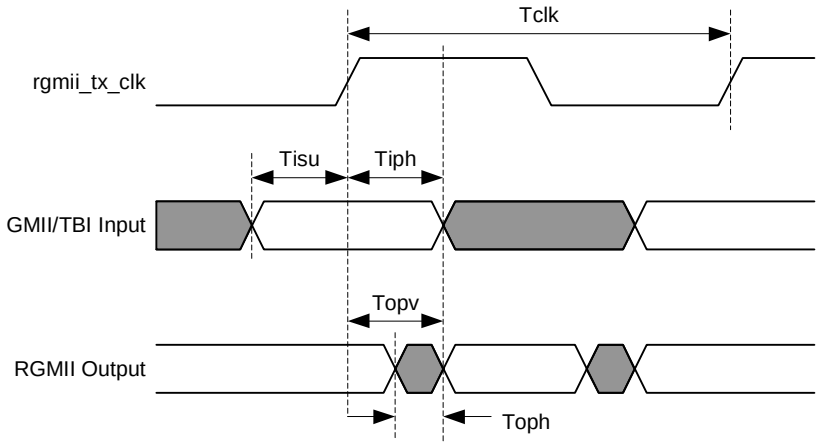
Control and Status Interface

Signal Name	I/O	Description
gmii_duplex_in	I	Signal from the MAC indicating current duplex mode. This is used to drive gmii_col low when in full duplex mode, which is indicated when this input is high.
tbi	I	Indicates RTBI mode when high. This asynchronous input is assumed static during operation.
gmii_gigabit	I	Input signal from the MAC indicating gigabit operation when high. This asynchronous input is assumed static during operation.
gmii_link_status	O	RGMII extracted link status signal. This output is generated synchronous to rgmii_rx_clk.
gmii_speed[1:0]	O	RGMII extracted signal indicating speed of operation. This output is generated synchronous to rgmii_rx_clk.
gmii_duplex_out	O	RGMII extracted signal indicating duplex mode. This output is generated synchronous to rgmii_rx_clk.

Timing Requirements

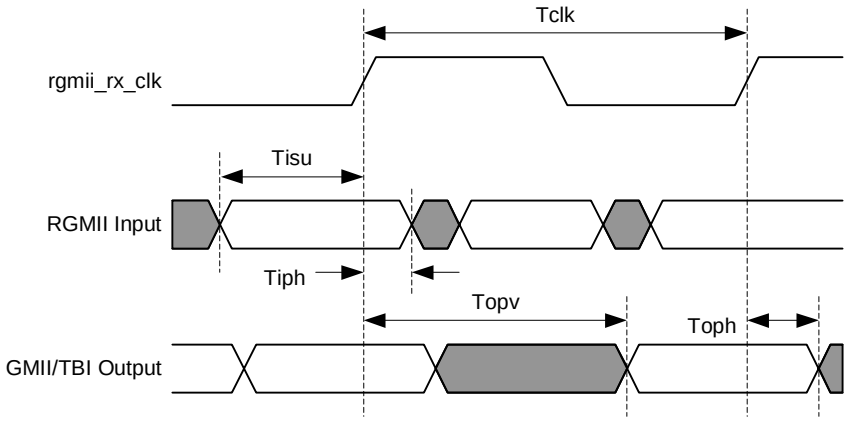
Transmit Path

Parameter	Description	Min	Max	Unit
Tclk	`rgmii_tx_clk` clock period	8	DC	ns
Tisu	GMII/TBI input set up prior to `rgmii_tx_clk`	2.8	—	ns
Tiph	GMII/TBI input data hold after `rgmii_tx_clk`	0.1	—	ns
Topv	RGMII output data valid after `rgmii_tx_clk`	—	0.85	ns
Toph	RGMII output data hold after `rgmii_tx_clk`	0	—	ns



Receive Path

Parameter	Description	Min	Max	Unit
Tclk	`rgmii_rx_clk` clock period	8	DC	ns
Tisu	RGMII input set up prior to `rgmii_rx_clk`	2.6	—	ns
Tiph	RGMII input data hold after `rgmii_rx_clk`	0.8	—	ns
Topv	GMII/TBI iutput data valid after `rgmii_rx_clk`	—	5.2	ns
Toph	GMII output data hold after `rgmii_rx_clk` TBI output data hold after `rgmii_rx_clk`	0.1 0.5	—	ns



Programming Interface

There is no programming or register map required for the RGMII module.

Physical Estimates

The physical estimates for the RGMII module are as follows:

Gate count	800
FF count	62
SOC internal pins	67
SOC external pins	10

Verification

All our IP modules are verified to one of the following levels:

- Gold IP has been to target silicon.
- Silver P has been to silicon in FPGA.
- Bronze IP has been verified in silicon with logical timing closure.
- In development IP has not yet been verified.

Please contact the IPGallery™ (ipgallery@cadence.com) for the latest verification information.

Deliverables

The full IP package comes complete with:

- Verilog HDL
- Envisia (BuildGates) and Synopsys Design Compiler synthesis scripts
- Verilog testbench
- *RGMII User's Guide* with full programming interface, parameterization instructions and synthesis instructions.