Function Block Documentation

Block: Ethernet Phy 100BASE-T1
Marvell 88Q1110

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Contents

1 Function Block Description (project independent)

[redacted]Introduction

This document describes the Marvell 88Q1110 Ethernet Phy circuit.

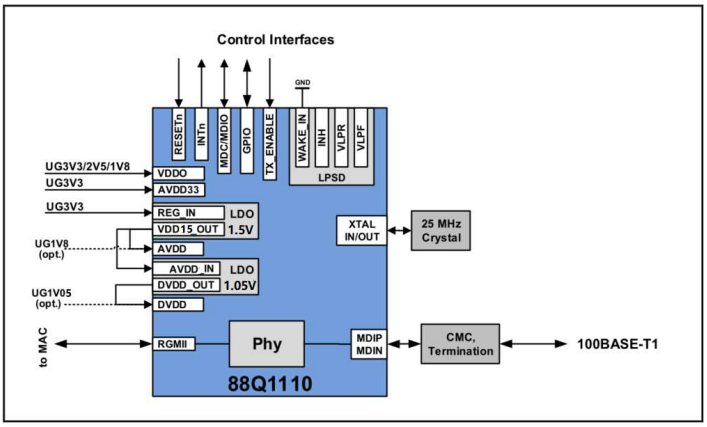
88Q1110 is IEEE 802.3bw compliant, and OPEN alliance TC1 &TC10 supported.

The interface to the MAC can be RGMII, RMII or MII.

For management access, a MDIO/MDC interface is available.

[redacted]Functional Description

[redacted]Block Diagram



Main Components:

- IC-SM MAV 88Q1110-B0-NYA2A000-#### (Harman PN: 4034301)
- 25 MHz crystal
- Common Mode Choke filter, Termination

[redacted]Feature Description

Features of the Marvell 88Q1110 100Base-T1 Ethernet Phy function block:

- One IEEE 802.3bw (100Base-T1) compliant automotive Ethernet PHY
- MAC interface could be RGMII, RMII, MII configurable by Hardware strap or SW configuration
- MDC/MDIO management interface according to IEEE802.3u, clause 45
- IO levels from 1.8V to 3.3V are supported for RGMII, MDC/MDIO and other control interfaces.
- HBM +/- 2kV ESD protection at the MDI pins

- Internal Regulator for generating the 1.5V and 1.05V core supplies. Optionally, the core supplies may be provided from an external regulator.
- By default, clocking is done by a 25MHz crystal connected to the IC.
  Optionally it is also possible to use an externally provided 25MHz clock signal instead of a crystal, special requirements regarding jitter and coupling has to be considered.
- The IC has support for Sleep mode / remote wakeup function. However, the required external circuit requires a 4MΩ resistor, which is electrically very critical and also in conflict with some customer requirements.
  Therefore it is not recommended to use this functionality and to select another IC in case a remote wakeup function is required.

[redacted] Configuration Settings

Bootstrap settings:

Configuration	88Q1110 Pin	Sampled Bit Definition	Register Affected	Pull-Up in Pad
PHYADR[0]	RXD[0]	PHYAD bit 0	None	Yes
PHYADR[1]	RXD[1]	PHYAD bit 1	None	Yes
PHYADR[2]	GPIO	PHYAD bit 2	None	Yes
Master/Slave configuration	RXD[2]	Auto-Negotiation off 0 – Master 1 – Slave	1.0834.14 7.0202.12	Yes
Mode	{RXC, RXD[3]}	11 – MII 10 – RGMII mode 1 01 – RMII 00 – RGMII mode 2	None	Yes
TC10 Sleep/Wake-up	RCLK	0 – Disable the TC10 Sleep/Wake-up feature 1 – Enable the TC10 Sleep/Wake-up feature	3.8707.0	Yes

[redacted] Interface Description

[redacted] Power Supply Requirements

In RGMII mode,

88Q1110 – RGMII to 100Base-T1

DVDD		AVDD15		AVDD33		VDDO		
Voltage (V)	Current (A)	Voltage (V)	Curren t (A)	Voltage (V)	Current (A)	Voltage (V)	Curren t (A)	Total Power (mW)
1.05	0.0096	1.5	0.0131	3.3	0.0107	3.3	0.0105	99.69

[redacted] Peripheral Signals and Interfaces

Signal Description:

Signal	Direction	Function	Port Type	Connects to
RESETn	I	Reset input low = Reset high = operation	LVCMOS3V3 or LVCMOS2V5 or LVCMOS1V8	Host controller
MDIO	IO	Management interface according to IEEE802.3u Clause 45		
MDC	I			
INTn	O	Interrupt output, active low		
TX_ENABLE	I	Enable input, active high		
GPIO	IO			
WAKE_IN / INH / VLPR / VLPF	I	Low Power Signal Detect (Remote wakeup circuit). Should not be used because of critical external circuit.	-	-
MDIP MDIN	IO	MDI interface	1000/100Base-T1	External
TXEN TXD[3..0] TXCLK RXDV RXD[3..0] RXCLK	I I I O O O	RGMII/RMII/MII interface	LVCMOS3V3 or LVCMOS2V5 or LVCMOS1V8	MAC

I = input, O =output, IO = input or output, PP = push-pull, OD = open drain

Details about the connections to the IOC/SoC (e.g. Port name) are described in the controller's chapter.

Electrical characteristics and requirements:

See the project specific chapters for detailed information.

[redacted] Power Dissipation

88Q1110 – RGMII to 100Base-T1

DVDD		AVDD15		AVDD33		VDDO		
Voltage (V)	Current (A)	Voltage (V)	Current (A)	Voltage (V)	Current (A)	Voltage (V)	Current (A)	Total Power (mW)
1.05	0.0096	1.5	0.0131	3.3	0.0107	3.3	0.0105	99.69

[redacted] Frequency overview

Device / Interface / Signal	Base Frequency
Crystal Oscillator	25 MHz
SGMII interface	1250 MHz symbol rate
RGMII interface clock 100 Mbps mode	25 MHz
RMII interface clock 100 Mbps mode	50Mhz
MII interface clock 100 Mbps mode	25Mhz

[redacted] Layout Requirements

[redacted] Power Supply

- Take care to have a good connection of power supply pins to the 100nF decoupling capacitors and to the planes. This shall have highest priority in the layout.
- Add planes for all power supply nets at the IC.

Commented [LL1]: Should be 1uF?

[redacted] MDIO/MDC interfaces

- See the project specific chapters.

[redacted] RGMII interface

- Single-ended impedance: 50 Ohm +/- 15%
- The following groups of 6 signals each shall be length matched:
  - TXC, TX_CTL, TXD[0..3]
  - RXC, RX_CTL, RXD[0..3]
- Intra-group length matching: < 30 ps
- Inter-group length matching: not needed
- Total length: keep as short as possible because of EMC.
- Separation to other nets: Clock signal (*CLK) shall have increased clearance: 3W
- Place series resistor as close as possible to the signal's drivers (see hints in schematic for direction).

- Minimize stubs.
- Place a ground stitching via for each signal when the reference ground layer changes. The stitching via must be placed as close as possible to the signal via.
- Try to avoid buried vias. If it cannot be avoided, add antipads on outer layers to minimize via capacitance.
- In case big pads have to be connected (e.g. LGA pads, MP's), add antipads on nearby layers to minimize pad capacitance.
- RGMII signals are very critical regarding EMC:
  - Try to place the parts in a way to have short connections.
  - Routing in inner layers may help due to shielding effect of outer layers

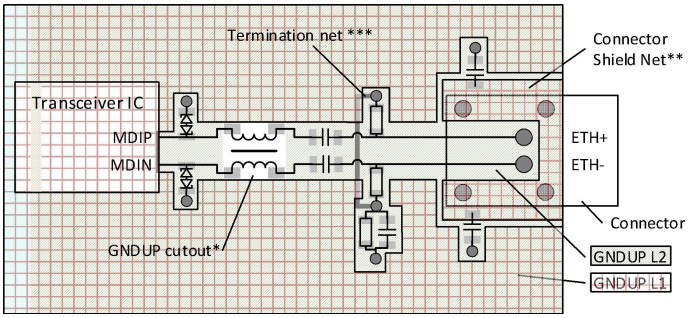
[redacted] SGMII interface

- Differential impedance: 100 Ohm +/- 15%
- Inter-pair length matching: not needed
- Intra-pair length matching: < 5mil
- Separation to other nets: >= 2W
- No stubs.
- No 90° corners.
- Try to route symmetrically where possible (e.g. at fan-out from components, placement of series capacitors, …)
- Place a ground stitching via for each signal when the reference ground layer changes. Place it as close as possible to the signal via.
- Try to avoid buried vias. If it cannot be avoided, add antipads on outer layers to minimize via capacitance.
- In case big pads have to be connected (e.g. LGA pads, MP's), add antipads on nearby layers to minimize pad capacitance.
- Antipads may be also required for other trace discontinuities (HP's, IC pins, series cap's, TH vias, Microvias). This needs to be decided individually based on measurement and/or simulation results.

[redacted] MDI interfaces

- Differential trace impedance: 100 Ohm+/-10%
- Route the differential pair traces as symmetrically as possible, since symmetry is critical to achieve the performance required by the IEEE Std 802.3bw specification.
  They shall be routed on outer layers, preferably without use of vias.
- Symmetry is also important for placement of the common mode choke, the termination resistors and the ESD diodes.

- Ground plane arrangement:

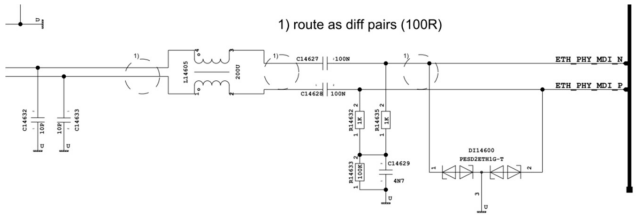


  - Under the common mode choke, a GND cutout* should be placed. This cutout shall cover the whole CMC area, and shall be applied on all layers. Also no other traces shall be in this area on all layers.
    If it is not possible to avoid that foreign traces cross this area, the GND cutout may be limited to L2 and L3 only (L3 needs to be free of foreign traces in this case).

  - The Connector Shield Net** shall be on L1 only.

  - The Termination net *** shall be routed preferably on the opposite layer than the MDI signal.

  - MDI interface schematics for reference:



[redacted]HSI Requirements

See the project specific chapters.

2 Project specific description

[redacted] Project TATA GEN3 Customer requirement

Ethernet feature is reserved for future EE architecture which will mate with TCU. Currently TCU connection is via USB.

Ethernet 100BaseT	PP	PP	PP	Design Package protection only for future usage if required

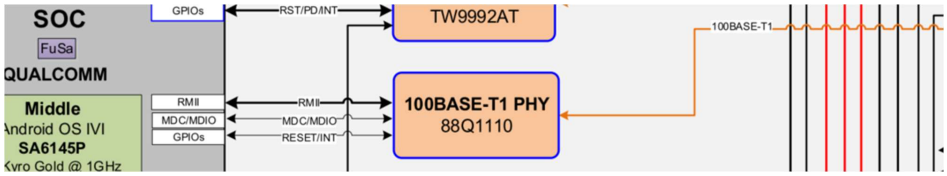
Ethernet	Standard	100BaseT1 (Vehicle Network) 100BaseTx (For DoIP)
	Communication Layer	AUTOSAR 4.4

In the TATA GEN3 project, the 88Q1110 IC variant, Rev. B0, is used.

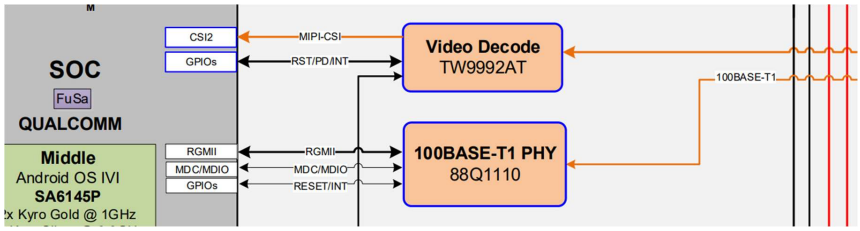
[redacted] Functional Description

Block diagram as below

MAC interface is RMII to reduce the SOC pins in B1/B2 version, but both Qualcom and 88Q1110 can only support RMII clock output, so the function is not workable. In B3, RGMII is used to correct the mistake.



B1/B2 SBD



B3 SBD

2.1.1.1 Configuration Settings

The device can be configured in two ways:
1. Hardware configuration strap options (unmanaged applications)
2.MDC/MDIO register writes (managed applications)

The Master/Slave configuration bits can be overwritten by software. PHYAD, RGMII/RMII/MII cannot be overwritten.

HW Bootstrap settings for B3:

PHY Address: 0x001

slave node

RGMII MODE 2

Disable TC10

As table below

88Q1110/88Q1111 Bootstrap and Schematics Checklist - MV-S111929-00

88Q1110 Configuration Summary				
GPIO	RXD[1]	RXD[0]	PHYAD[2:0] Value	Your PHYAD[2:0] Configuration
Pull-up / Unconnected	Pull-up / Unconnected	Pull-up / Unconnected	000	001
Pull-up / Unconnected	Pull-up / Unconnected	Pull-down	001	
Pull-up / Unconnected	Pull-down	Pull-up / Unconnected	010	
Pull-up / Unconnected	Pull-down	Pull-down	011	
Pull-down	Pull-up / Unconnected	Pull-up / Unconnected	100	
Pull-down	Pull-up / Unconnected	Pull-down	101	
Pull-down	Pull-down	Pull-up / Unconnected	110	
Pull-down	Pull-down	Pull-down	111	
Pull-up / Unconnected	Pull-up / Unconnected	Pull-down	<-- seen on schematics	

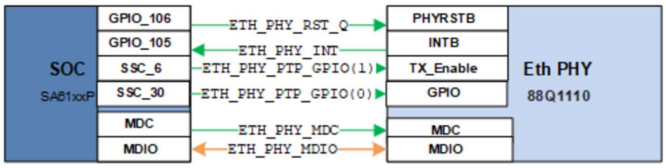
RXD[2]	Value	Definition	Your Configuration
Pull-up / Unconnected	1	Slave	Slave
Pull-down	0	Master	
Pull-up / Unconnected	<-- Seen on schematics		

RXC	RXD[3]	Value	Definition	Your Configuration
Pull-down	Pull-down	00	RGMII Mode 2	RGMII Mode 2
Pull-down	Pull-up / Unconnected	01	RMII	
Pull-up / Unconnected	Pull-down	10	RGMII Mode 1	
Pull-up / Unconnected	Pull-up / Unconnected	11	MII	
Pull-down	Pull-down	<-- Seen on schematics		

RCLK	Value	Definition	Your Configuration
Pull-up / Unconnected	1	Enable TC10 Sleep/Wake-up	
Pull-down	0	Disable TC10 Sleep/Wake-up	Disable TC10 Sleep/Wake-up
Pull-down	<-- Seen on schematics		

[redacted]Interface Description

2.1.2.1 B3 Peripheral Signals and Interfaces



Signal Description:

SOC (SA6145/50P)		Eth PHY (88Q1110)		From PHY view	
Pin	Signal	Pin	Signal	Type	Description
K34	SOC_RGMII_MDIO	MDIO	ETH_PHY_MDIO	I/O	Input / Output of Management Data

L33	SOC_RGMII_MDC	MDC	ETH_PHY_MDC	I	Management Data Clock.
J5	SOC_GPIO[106]	RESET	ETH_PHY_RST_Q	I	Hardware reset pin, low active
AL39	SOC_GPIO[105]	INT	ETH_PHY_INT_Q	O	Interrupt output, when 3.8312.11=1 means it is low active; when 3.8312.11=0 means it is high active
AR17	SOC_SSC(30)	GPIO	ETH_PHY_PTP_GPIO(0)	I/O/PU	PHY address Configuration pin，and this can be used as GPIO (reserved). Here reserved for PTP HW acceration.
AP22	SOC_SSC_QUP(1)_L4_SPI_CS1	TX_ENABLE	ETH_PHY_PTP_GPIO(1)	I	Reserved, IF TX_ENABLE is LOW, TX packages will be stopped after link up, but RX packages are still received normally. Here reserved for PTP HW acceration.

Commented [LL2]: Change pin connection in B3

I = input, O =output, IO = input or output, PP = push-pull, OD = open drain, boot = bootstrap function

Details about the connections to the IOC/SoC (e.g. Port name) are described in the controller's chapter.

[redacted] RGMII Interface

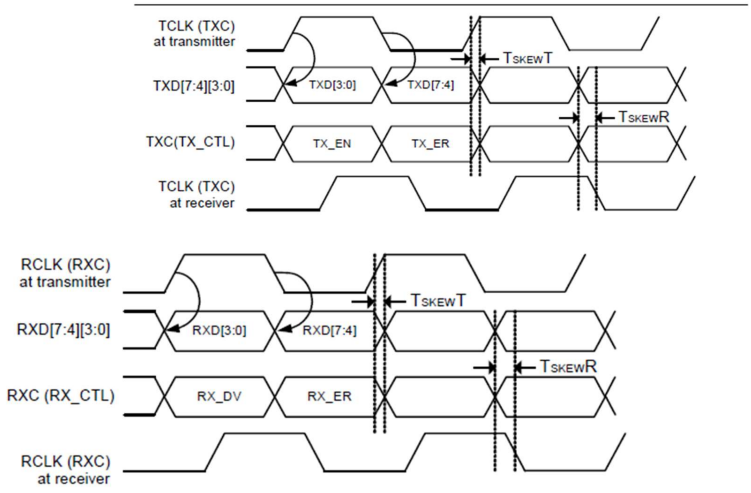
SOC (SA6145/50P)		Eth PHY (88Q1110)		From PHY view	
Pin	**Signal**	**Pin**	**Signal**	**Type**	**Description**
M32	SOC_RGMII_RX_CTL	RXC	ETH_PHY_RGMII_RXDV	O	Receive control signal to the MAC
N35	SOC_RGMII_TXC	RCLK	ETH_PHY_RGMII_RCLK	O	Output 50Mhz reference for both TX and RX
U33	SOC_RGMII_RXD0	RXD0	ETH_PHY_RGMII_RXD(0)	O	Transmit Data. Date is transmitted from PHY to MAC via RXD[3:0].
T32	SOC_RGMII_RXD1	RXD1	ETH_PHY_RGMII_RXD(1)	O	
R33	SOC_RGMII_RXD2	RXD2	ETH_PHY_RGMII_RXD(2)	O	
P32	SOC_RGMII_RXD3	RXD3	ETH_PHY_RGMII_RXD(3)	O	
U35	SOC_RGMII_TX_CTL	TXC	ETH_PHY_RGMII_TXEN	I	Transmit control signal from the MAC.
T36	SOC_RGMII_TXD0	TXD0	ETH_PHY_RGMII_TXD(0)	I	Data is received from TXD [3:0]
T34	SOC_RGMII_TXD1	TXD1	ETH_PHY_RGMII_TXD(1)	I	
R35	SOC_RGMII_TXD2	TXD2	ETH_PHY_RGMII_TXD(2)	I	
P34	SOC_RGMII_TXD3	TXD3	ETH_PHY_RGMII_TXD(3)	I	

5.7.1 RGMII AC Characteristics

Table 321: RGMII AC Characteristics
(This table is copied from the RGMII Specification. See the four timing modes discussed in Section 5.7.2, RGMII Delay Timing for Different RGMII Modes, on page 254).

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	–	–	ns
T_{CYCLE}	Clock Cycle Duration	36	40	44	ns
$T_{CYCLE\_HIGH100}$	High Time for 100BASE-T	16	20	24	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20% – 80%)	–	–	0.75	ns

Figure 38: RGMII Multiplexing and Timing



This figure is copied from the RGMII Specification. See the four timing modes discussed in Section 5.7.2, RGMII Delay Timing for Different RGMII Modes, on page 254.

Electrical characteristics and requirements:

Signal	Electrical characteristics / requirements	during reset	after reset release	during operation	remarks
ETH_PHY_RST_Q	V_{IL_max} = 0.54V V_{IH_min} = 1.26V V_{I_max} = V_{VDDO}+0,3V V_{I_min} = -0.3V V_{OH_min} = 1.4V V_{OL_max} = 0.4V @ I_{OL}=8mA	I, PU 4k7	I, PU 4k7	I, PU 4k7	
ETH_PHY_MDIO		I, PU 4k7	I, PU 4k7	IO, PU 4k7	
ETH_PHY_MDC		I	I	I	
ETH_PHY_INT_Q		I, PU 4k7	I, PU 4k7	I, PU 4k7	
ETH_PHY_RGMII_RXDV ETH_PHY_RGMII_RCLK ETH_PHY_RGMII_RX(3:0)		I I	I I	I I	

ETH_PHY_RGMII_TXEN ETH_PHY_RGMII_TCLK ETH_PHY_RGMII_TX(3:0)		I I I, IPU I, PU 4k7 I, PD 4k7	I O O O O	I O O O O	
MDIP MDIN	100Base-T1	inactive	IO	IO	External CMC filter and termination. Trace impedance 100Ω differential.

I = input, O =output, IO = input or output, PP = push-pull, OD = open drain, PU = pull-up, PD = pull-down

[redacted] HSI Requirements

2.1.4.1 HW reset

At startup of the system,

1. the SW shall initialize the PHY reset signal ETH_PHY_RST_Q (SOC_GPIO[106]) to “low” level
2. the SW shall set ETH_PHY_RST_Q (SOC_GPIO[106]) to “high” >= 10 ms after the Phy’s power supplies are stable and after it was initialized to low level..

The SW shall perform the following sequence in case a HW reset shall be performed during runtime:

1. The SOC shall set ETH_PHY_RST_Q (SOC_GPIO[106]) to “low” level
2. Wait for >= 10 ms
3. the SOC shall set ETH_PHY_RST_Q (SOC_GPIO[106]) to “high” level

2.1.4.2 Register settings

Refer to reference [3] for the registers setting.

2.1.4.3 PMA compliance test requirement

The 88Q1110 supports various test modes, which are needed to verify the compliance with IEEE802.3bw standard.

1. The SW shall provide a functionality that allows to enable all test modes described in the
   - 100BASE-T1 PMA/PMD Test Control Register, Device 1, Register 0x0836 [1].

Table 94: 100BASE-T1 PMA/PMD Test Control Register
Device 1, Register 0x0836

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	100BASE-T1 Test Mode Control	R/W	0x0	0x0	11x = Reserved 101 = Test mode 5 100 = Test mode 4 011 = Reserved 010 = Test mode 2 001 = Test mode 1 000 = Normal operation
12:0	Reserved	R/W	0x0000	0x0000	Set to 000000000000

2. The SW shall provide a functionality to configure the PHY in master mode 100BASE-T1 PMA/PMD Control Register, Device 1, Register 0x0834, bit 14 MASTER/SLAVE = 1 [1] for transmitter clock test.
3. The SW shall provide a functionality to configure the PHY in Slave mode (100BASE-T1 PMA/PMD Control Register, Device 1, Register 0x0834, bit 14 MASTER/SLAVE = 0 [1] for MDI Return Loss and MDI Mode Conversion Loss measurements.

Table 93: 100BASE-T1 PMA/PMD Control Register
Device 1, Register 0x0834

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MASTER-SLAVE Manual Configu-ration Enable	R/W	0x1	0x1	Value always 1, writes ignored
14	MASTER-SLAVE Configuration Value	R/W	Value con-figured.	Retain	1 = Configure PHY as Master 0 = Configure PHY as Slave
13:4	Reserved	RO	0x000	0x000	Set to 000000000000
3:0	Type Selection	R/W	0x0	0x0	0000 = 100BASE-T1

4. The SW shall provide a functionality to configure TX_TCLK enable or disable. Misc Test Device3,Register 0x861A bit15 TX_TCLK enable =1.

Table 157: Misc Test
Device 3, Register 0x861A

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TX_TCLK Enable	R/W	0x0	Retain	The transmit clock can be driven to the HSDACP/N pin. 1 = Enable 0 = Disable

Enabling of these function may be done e.g. via diagnostics or engineering interfaces.

2.1.4.4 Diagnostic

88Q1110 is able to do the cable quality diagnostic, shorts, cable impedance mismatch, bad connectors, termination mismatch and bad magnetics. setting register 3.8517.15 to 1. This bit will self clear when the test is completed. Register 3.8517.14 will be set to a 1 indicating that the TDR results in the registers are valid. Each time the VCT test is enabled, the results seen on the single channel are reported in register 3.8510

Table 140: Advanced VCT Control
Device 3, Register 0x8517

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Enable Test	R/W, SC	0x0	0x0	1 = Enable test 0 = Disable test This bit will self-clear when the test is completed.
14	Test Status	RO	0x0	0x0	1 = Test completed 0 = Test not started/in progress
13:11	Reserved	R/W	0x0	0x0	
10:8	Number of Sam-ple Averaged	R/W	6	Retain	0 = 2 samples 1 = 4 samples 2 = 8 samples 3 = 16 samples 4 = 32 samples 5 = 64 samples 6 = 128 samples 7 = 256 samples
7:6	Mode	R/W	0x0	Retain	00 = Maximum peak above threshold 01 = First or last peak above threshold. See register 3.851C.13. 10 = Offset 11 = Sample point at distance set by 3.8518.7:0
5:0	Peak Detection Hysteresis	R/W	0x03	Retain	0x00 = 0 mV 0x01 = 7.81 mV 0x3F = ± 492 mv

if 3.8510.15 is 1, this indicates the cable is open, otherwise if 3.8510.15 is 0, this indicates the cable is shorted. If the TDR test fails, it might be caused by 1 wire of a twisted pair being cut. To diagnose this case, set 3.851D.15 = 1 and run the TDR test again to check if there is an open on one wire of the pair.

Table 136: TDR Result
Device 3, Register 0x8510

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Amplitude	RO	0x00	Retain	The amplitude of reflected pulse 8'b1111_1111 = Maximum positive reflection 8'b1000_0000 = No reflection 8'b0000_0000 = Maximum negative reflection
7:0	Distance	RO	0x00	Retain	The distance of reflection

Table 146: TDR Threshold of Negative Threshold
Device 3, Register 0x851D

Bits	Field	Mode	HW Rst	SW Rst	Description
14:8	Negative Threshold 4	R/W	0x06	Retain	Negative threshold for distance > window3
7:0	Reserved	R/W	0xFF	Retain	

Refer to [3] for the source code of diagnostic functions.

```
// @desc: Virtual Cable Test (VCT) intended to find faults in cables and improper termination
// @param: phy - pointer to MRVL_DEV
// @param: pointer to distanceToFault
// @param: pointer to cableStatus
// @return: MRVL_APHY_STATUS - MRVL_APHY_STATUS_OK when measurement complete
//     In case method returns true, interpret results as follows:
//     cableStatus      distanceToFault     result
//     't'              0                   proper termination
//     'o'              value               open circuit at length "value"
//     's'              value               short circuit at length "value"
//     No other results possible
MRVL_APHY_STATUS getVCTReading(MRVL_DEV_PTR phy, double& distanceToFault, char& cableStatus)
{
```

2.1.4.5 SQI Report

There are SQI register to report the signal quality, the higher value the better quality. Refer to [3] for source code of following function.

```
  * getSQIReading_8Level
          Check signal quality
          Result range: 0-7.
          Higher value indicates better signal quality.
  * getSQIReading_16Level
          Check signal quality
          Result range: 0-15.
          Higher SQI resolution.
```

2.1.4.6 PTP setting(Not needed for TATA GEN3)

Firstly set LED and GPIO pin as GPIO function. And check the PTP registers setting in datasheet.

Table 160: PTP Control Register
Device 3, Register 0x8630

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Tx Side PTP's SFD Selection	R/W	0x0	Retain	Tx side PTP's SFD selection 1 = From tx_en 0 = From SFD
14	Tx Side PTP's Preamble Selection	R/W	0x1	Retain	Tx side PTP's preamble selection 1 = Enable detection of preemptable packets delimiter 0 = Disable detection of preemptable packets delimiter
13	Rx Side PTP's SFD Selection	R/W	0x0	Retain	Rx side PTP's SFD selection 1 = From rx_dv 0 = From SFD
12	Rx Side PTP's Preamble Selection	R/W	0x1	Retain	Rx Side PTP's Preamble Selection 1 = Enable detection of preemptable packets delimiter 0 = Disable detection of preemptable packets delimiter
11	Reserved		0x0	0x0	
10	PTP software reset	R/W, SC	0x0	Retain	1= software reset
9	PTP Power Down	R/W	0x1	Retain	1 = Power down 0 = Power up
8	Reserved	R/W	0x0	Retain	
7:6	PTP Event Request/Trigger Select For LED Pin	R/W	0x0	Retain	01 = Use LED pin for PTP output trigger pulse 10 = Use LED pin for PTP One Pulse Per Second (1PPS) output 11 = Use LED pin for PTP input trigger pulse
5:4	PTP Event Request/Trigger Select For GPIO Pin	R/W	0x0	Retain	01 = Use GPIO pin for PTP output trigger pulse 10 = Use GPIO pin for PTP for other functions 11 = Use GPIO pin for PTP input trigger pulse
3:1	Reserved	R/W	0x0	Retain	
0	Enable LED/GPIO for PTP Status	R/W	0x0	Retain	Used to bring PTP status to the LED pin.

3 References

No	Document name	Rev., Date
[1]	88Q1110_88Q1111 Datasheet MV-S111917-00D	May 11, 2021
[2]	Release_Notes_88Q1110_88Q1111_Rev_B0_TD_000818_02	Rev.2 Mar. 1, 2021
[3]	MRVL_Q111X_API_V_2_0_0	April12,2021

4 Change History

Date	By	Change Description
2021-4-28	Li,Ling	Initial version, HSI requirements open
2021-9-25	Li,Ling	Updated according to B3 schematic, RGMII interface is used instead of RMII