# PCI Configuration Space: -

PCI devices have a set of registers referred to as configuration space. These registers are then mapped to memory locations such as the I/O Address Space of the CPU. On PCI Express buses, this configuration space may be referred to as the the Extended Configuration Space. Every PCI device in the system, including the PCI-PCI bridges has a configuration space.

Size of configuration space in PCI – 256 bytes

Size of configuration space in PCIe – 2048 bytes

In PCI, configuration space of 256 bytes is addressed by using 8-bit PCI bus, 5-bit device and 3-bit function numbers for the device, it is commonly known as bus/device/funtion or BDF.

Diagram

Description automatically generated

Figure – 1

## Configuration header: -

Out of 256 bytes configuration space, first 64 bytes (00h – 3Fh) of configuration space are standardized, also called as “Configuration Header”.

In figure – 1, in 64 bytes configuration header, the black ones are read only and white ones are writable registers where the BSP code writes down the address details, configure this device and map it to a particular address space.

We can in 64 bytes configuration header, there resides PCI ID i.e., Vendor ID and Device ID registers, to identify the device.

If an Endpoint has 7 functionalities for example, then there will be 7 headers as shown in figure -1.

## 192 bytes (40h – FFh):-

The remaining 192 bytes (40h – FFh) out of 256 bytes represent user-definable configuration space, such as the information specific to PC card for use by its accompanying software.

# Permits Plug-And-Play: -

1. Base address registers allow an agent to be mapped dynamically into memory or I/O space.
2. A programmable interrupt-line setting allows a software driver to program a PC card with an IRQ upon power up.

[13-11-2021, 1:00:00]