Contents

[1. PCIe Introduction 2](#_Toc126529290)

[2. PIO and MMIO 2](#_Toc126529291)

[3. PCIe Lane Negotiation 2](#_Toc126529292)

# PCIe Introduction

The PCI Express bus is a backwards compatible, high performance, general purpose I/O interconnect bus, and was designed for a range of computing platforms. One of the key improvements of PCI Express, over the [PCI Local Bus](https://wiki.osdev.org/PCI), is that it now uses a serial interface (compared to the parallel interface used by PCI).

For specifications, refer - https://pcisig.com/specifications/

# PIO and MMIO

PIO and MMIO operate in different address spaces.

PIO –

PIO (port I/O) uses special assembly instructions to communicate with a dedicated IO bus. All devices attached to the PIO bus has a small 16-bit address.

MMIO –

In case of MMIO, device’s registers are also mapped into RAM’s address space.

# PCIe Lane Negotiation

* PCIe link between two devices can be 1 to 32.
* In multi lane link, packet data is stripped across lanes.
* Lane count is automatically negotiated during device initialization and also can be restricted by Endpoint due to this single lane device can be used in multi-lane slot
* Number of lanes in a link can also be reduced dynamically.