Course Code	**CS-531**
Course Title	**Advance Computer Architecture**
(TCH LCH CrHr)	(3 0 3)
Contact Hours	3 hours per week
Pre-requisite	None
Recommended Texts	1. Computer Organization and Architecture – Designing or Performance, 10th Edition, by Willian Stallings 2. Computer Architecture – A Quantitative Approach, 5th Edition, by John L. Hennessy and David A. Patterson 3. Structured Computer Organization, 5th Edition by Andrew S. Tanenbaum
Course Description	The course covers the topics of organization and architecture of computer systems hardware; instruction set architectures; addressing modes; register transfer notation; processor design and memory systems.
Course Objectives	• To enable students to understand the basic components of a computer system • To enable students to understand the issues that are limiting the performance of processor, caches and memories • To enable students to highlight architecture and organization parameters for processor performance • To enable students to understand the cycle of instruction execution in the pipeline of a processor
Course Outline	• Basic Components of Computer Systems • Underlining issues in multi-core and many-core systems • Issues of a cache system and distributed cache system • Different types of memories • Processor performance improvement • Instruction set architecture

Lecture Wise Distribution of the Contents

Lecture No.	Contents
L1-L3	Organization and Architecture Structure and Functions
L4-L6	History of Computers Evolution of Intel x86 Architecture Embedded Systems ARM Architecture

L6-L9	Designing for Performance Multicore, MICs and GPGPUs Amdahl's Law Little Law Basic measure of computer performance
L10-L12	Computer components Computer function Interconnection Structures Bus Interconnection Point-to-Point Interconnect PCI Express
L13-L15	Computer Memory System Cache Memory Principles Elements of cache Design
L16-L19	Mapping functions Replacement algorithms Pentium 4 cache organization
L19-L22	Semiconductor main memory Error Correction
L23-L25	DDR DRAM Flash Memory Newer Nonvolatile Solid-State Memory Technologies
L26-L29	Magnetic Disk RAID Solid State Drives
L30-L33	Optical Memory Magnetic Tape Machine instruction characteristics
L34-L36	Types of operands Types of operations Addressing modes Instruction format
L37-L39	Processor organization Register organization Instruction cycle Instruction pipelining
L40-L42	Instruction execution characteristics The use of large register file Compiler-based register optimization Reduced instruction set architecture RISC pipelining MIPS R4000 SPARC

	RISC vs CISC controversy
L43-L44	Instruction level parallelism Design issues Intel core microarchitecture ARM Cortex-A8, Coretex-M3
L45	Revision