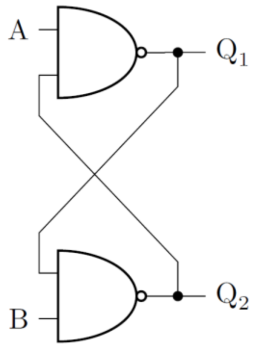
MANAGEMENT AND ANALYSIS OF PHYSICS DATASET (MOD. A)

Memory Elements
Sequential Circuits

Memory elements

- If both inputs are at 1, the circuit keep memory of the previous state

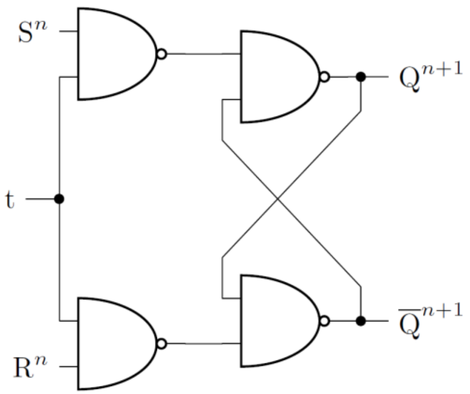


A	B	Q_2	Q_1
0	0	1	1
1	0	1	0
0	1	0	1
1	1	X	$\overline{X}$

- Latch

Memory elements

- Flip-flop set-reset (S-R)
  - A synchronization input t is added
  - If t is not present the output doesn't change



S^n	R^n	Q^{n+1}	$\overline{Q}^{n+1}$
0	0	Q^n	$\overline{Q}^n$
1	0	1	0
0	1	0	1
1	1	-	-

$$Q^{n+1} = \left(Q\,\overline{S}\,\overline{R} + S\,\overline{R}\right)^n = \left(S + Q\,\overline{R}\right)^n$$
$$S\,R = 0$$

Memory elements

- Flip-flop J-K
  - It removes the forbidden state
- Flip-flop D
  - Only one input
- How to build J-K and D?

J^n	K^n	Q^{n+1}	$\overline{Q}^{n+1}$
0	0	Q^n	$\overline{Q}^n$
1	0	1	0
0	1	0	1
1	1	$\overline{Q}^n$	Q^n

$$Q^{n+1} = \left(Q\,\overline{J}\,\overline{K} + J\,\overline{K} + \overline{Q}\,J\,K\right)^n = \left(Q\,\overline{K} + \overline{Q}\,J\right)^n$$

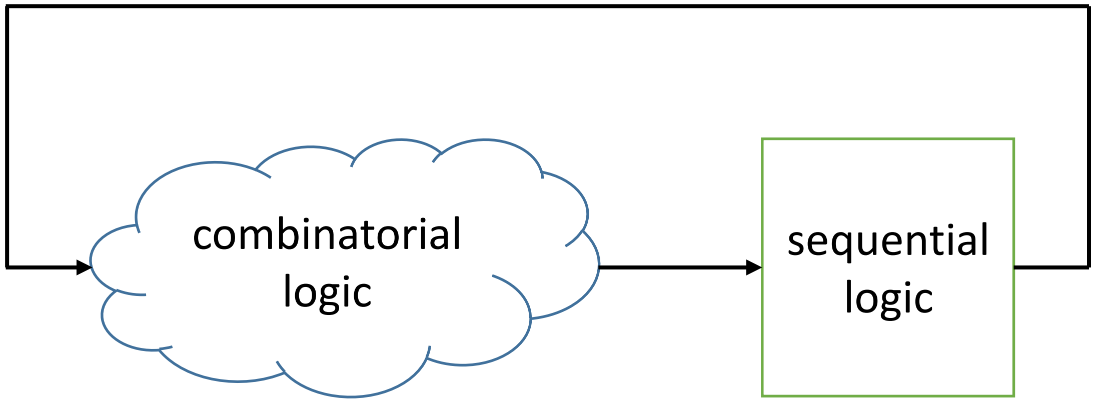
D^n	Q^{n+1}	$\overline{Q}^{n+1}$
0	0	1
1	1	0

$$Q^{n+1} = D^n$$

Memory elements

- Usually, memory elements are controlled by logic functions

a_0^n	a_1^n	Q^n	Q^{n+1}	S^n	R^n	J^n	K^n	D^n
0	0	0	0	0	X	0	X	0
1	0	0	0	0	X	0	X	0
0	1	0	1	1	0	1	X	1
1	1	0	1	1	0	1	X	1
0	0	1	0	0	1	X	1	0
1	0	1	1	X	0	X	0	1
0	1	1	0	0	1	X	1	0
1	1	1	1	X	0	X	0	1



$$Q^{n+1} = \left(a_0 Q + a_1 \overline{Q}\right)^n$$

$$S = a_1 \overline{Q} \qquad J = a_1$$
$$R = \overline{a_0} Q \qquad K = \overline{a_0}$$

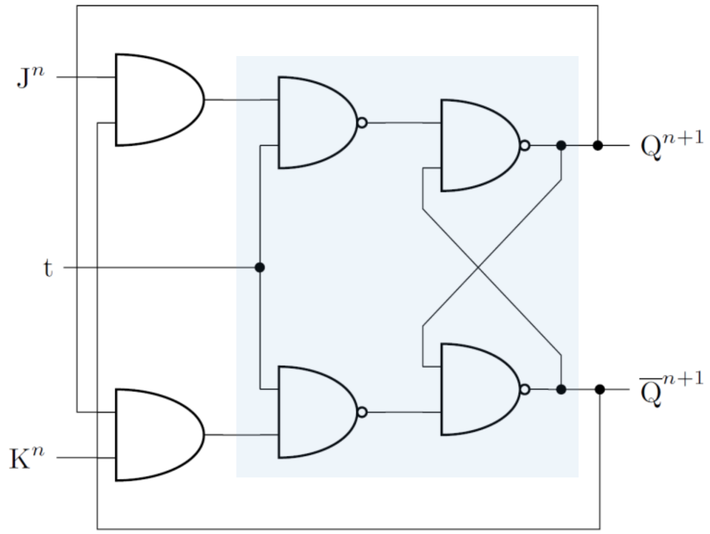
Memory elements

$$S = a_1\overline{Q}$$
$$R = \overline{a_0}Q$$

$$J = a_1$$
$$K = \overline{a_0}$$

$$\Rightarrow$$

$$S = J\overline{Q}$$
$$R = KQ$$

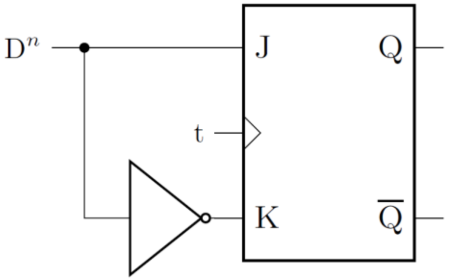


$$J = a_1$$
$$K = \overline{a_0}$$

$$D = a_0Q + a_1\overline{Q}$$

$$\Rightarrow$$

$$J = D$$
$$K = \overline{D}$$



Exercises

- Make a J-K flip-flop from a D flip-flop
- Find the truth table of the flip-flop with the following equation
  $Q^{n+1} = [Q \oplus (M \oplus N)]^n$
- Make the above flip-flop from a J-K flip-flop

Counters and registers

Decimal counter

- Design a 0-9 counter
- $A^{n+1} = \left[\overline{A}\right]^n$
- $B^{n+1} = \left[B\left(\overline{A}\right) + \overline{B}\left(A\,\overline{D}\right)\right]^n$
- $C^{n+1} = \left[C\left(\overline{A} + \overline{B}\right) + \overline{C}\left(A\,B\right)\right]^n$
- $D^{n+1} = \left[D\left(\overline{A}\right) + \overline{D}\left(A\,B\,C\right)\right]^n$
- 4 FF J-K and 3 logic ports (assuming the complement of each variable is available)

D^n	C^n	B^n	A^n	D^{n+1}	C^{n+1}	B^{n+1}	A^{n+1}
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

Johnson counter

- It is a counter without switching incertitude because it changes only one bit at a time
- m-bit Johnson counter -> sequence of $2m$ numbers
- If we use the redundant terms, we get

$$A^{n+1} = \overline{C^n}$$
$$B^{n+1} = A^n$$
$$C^{n+1} = B^n$$

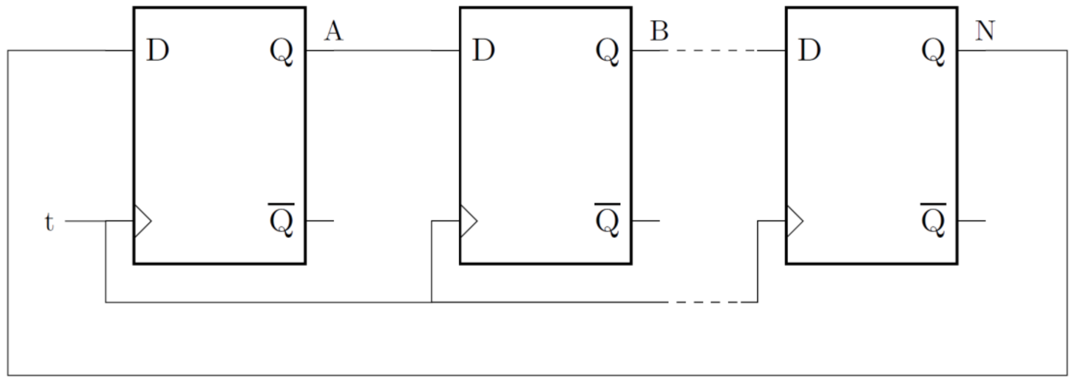
- It nicely corresponds to a D flip-flop chain, but if the system starts by chance from a redundant term, it never get out!
- We need to avoid that making the schematics a little bit more complex

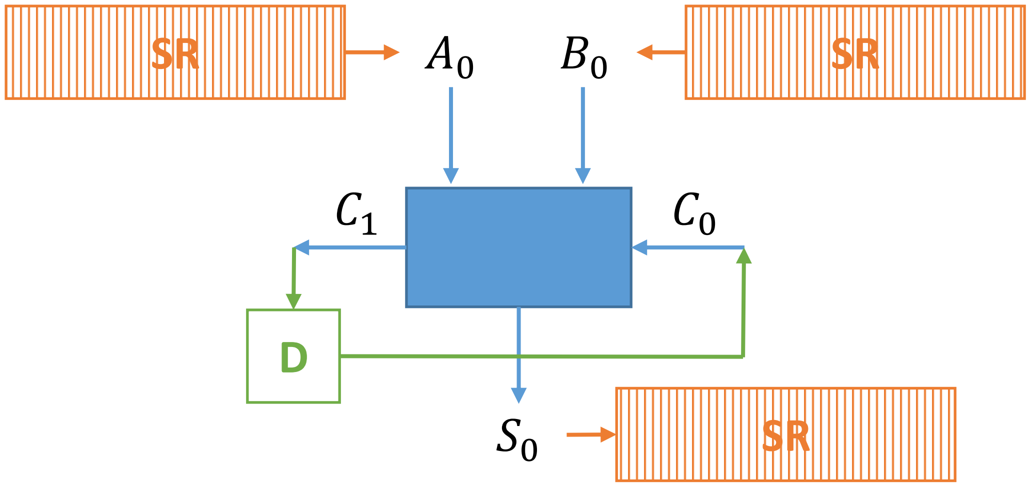
$$A^{n+1} = \overline{C^n}$$
$$B^{n+1} = [A(B + \overline{C})]^n$$
$$C^{n+1} = B^n$$

A^n	B^n	C^n	A^{n+1}	B^{n+1}	C^{n+1}
0	0	0	1	0	0
1	0	0	1	1	0
1	1	0	1	1	1
1	1	1	0	1	1
0	1	1	0	0	1
0	0	1	0	0	0

Shift register

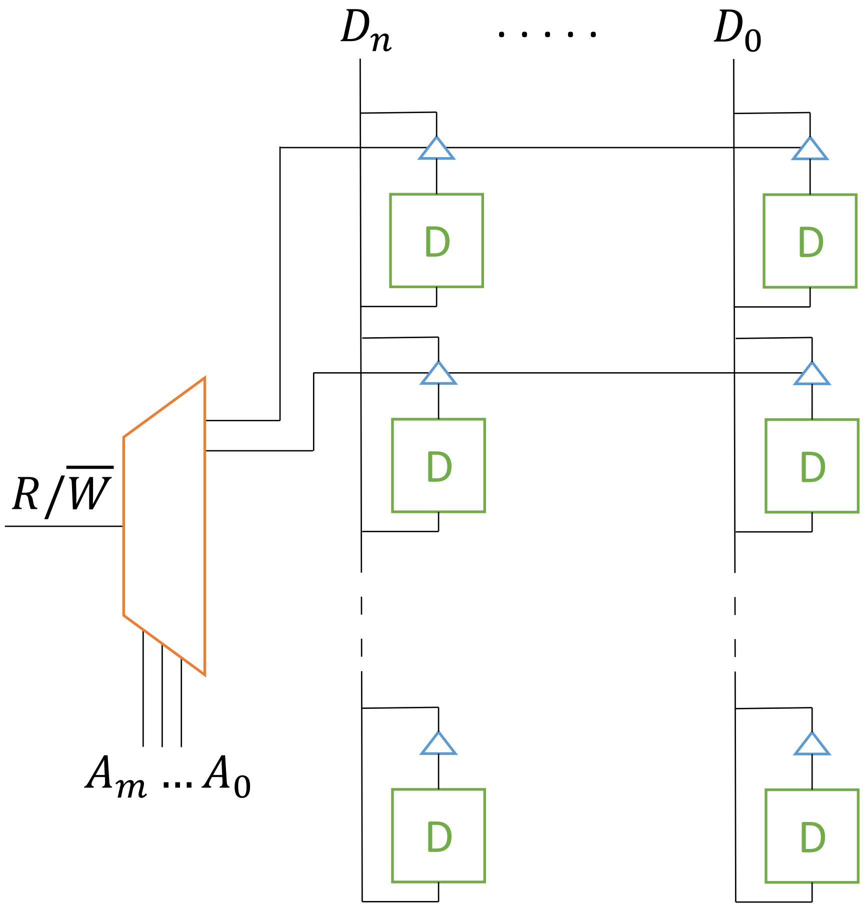
- It is used to shift a signal
- Its design can be obtained by the sequential table
- Without feedback can be used to access in parallel to a serial data or to serialize a parallel data
- Each cell can have a multiplexer to choose if shifting the bit or loading a new bit





Memory

- It can be seen as an array of FF
- A decoder is used for addressing the data row
- A tristate allows read/write operation
- Memory size = data width x $2^{\text{address width}}$
- Random Access Memory (RAM)
  - If Read Only is called ROM
  - It can contain a truth table -> It implements any combinatorial function (one for each data bit)



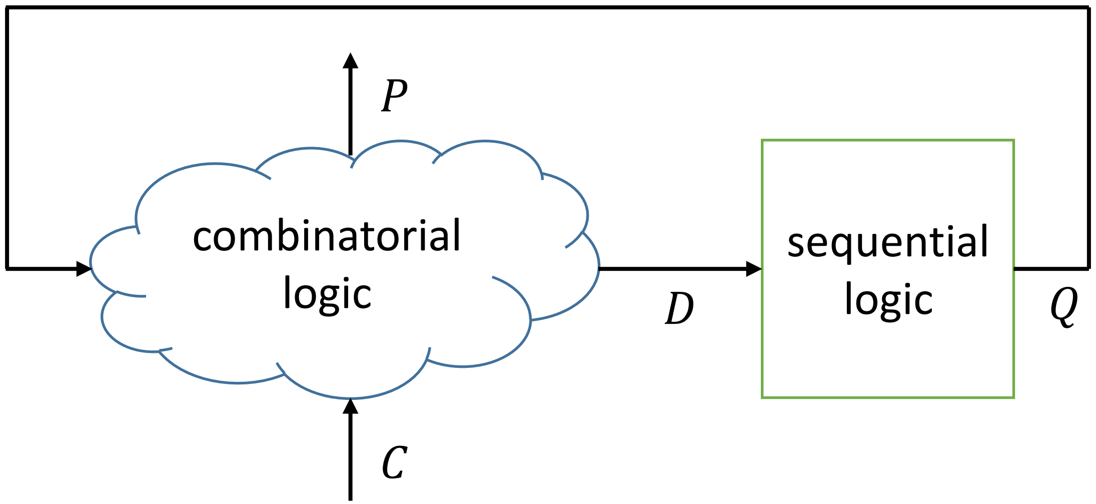
Exercises

- Design a 4-bit down counter
- Design an n-bit shift register that starts from a state where all the bits are equal to zero: 00…0 -> 10…0 -> 01…0, etc.

State machines

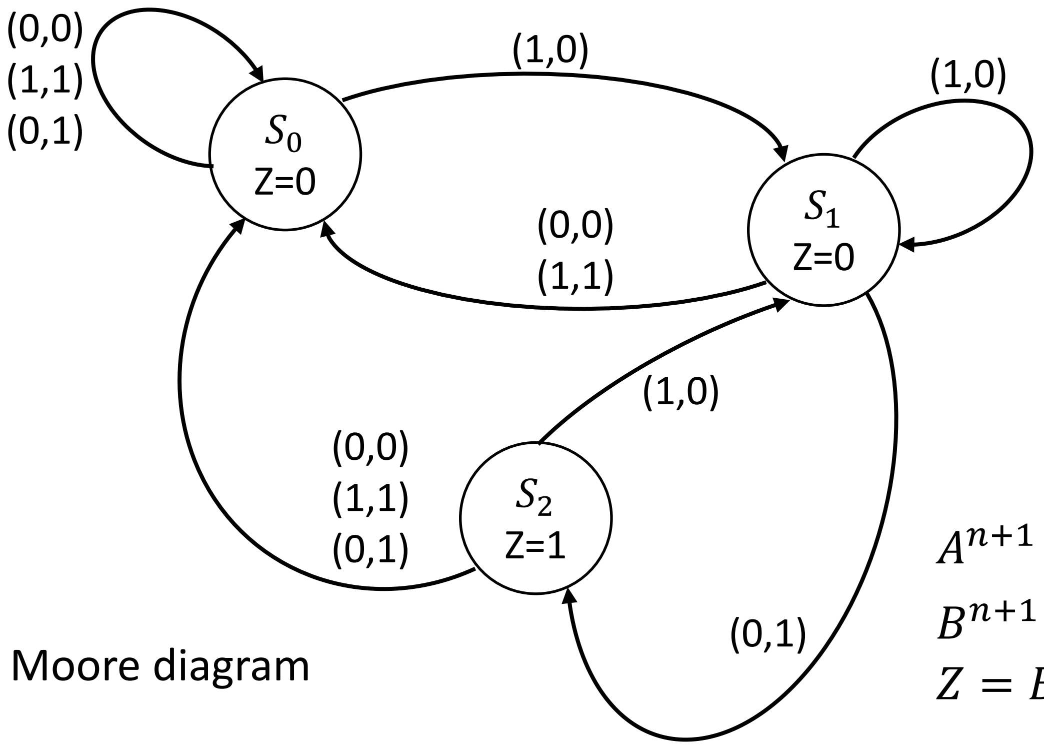
State machine

- A general schema for functions that control sequential logic take into account external signals C and produce control signals P
  - Mealey state machine: P is function of C and Q
  - Moore state machine: P is only function of Q
- Moore outputs are synchronous



State machine

- Find the transition (1,0) -> (0,1) of two bits (M,N)



Moore diagram

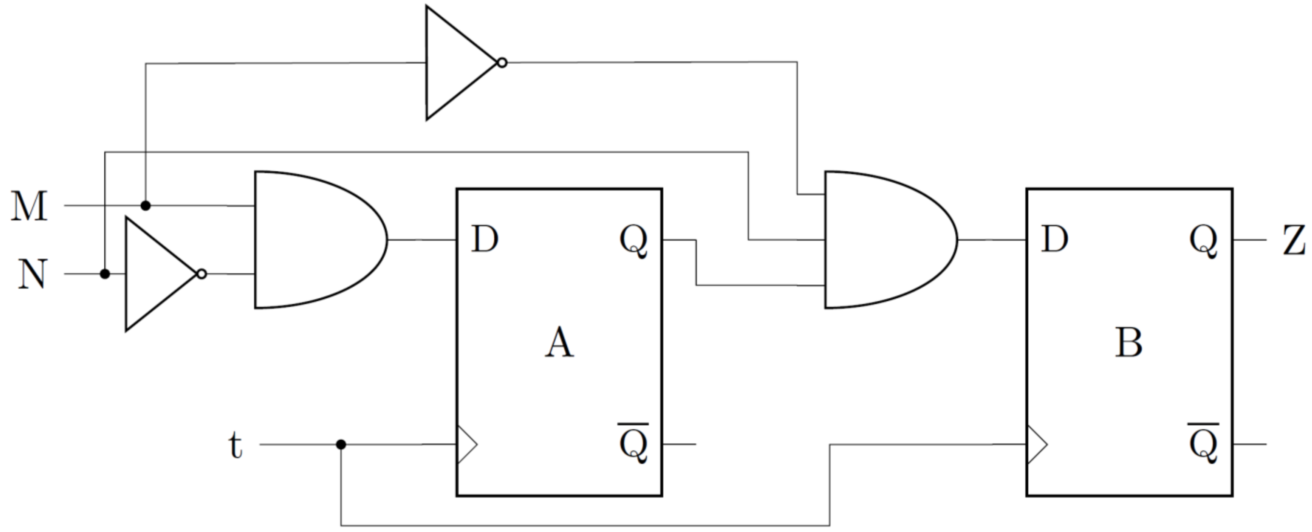
$$A^{n+1} = \left(M\,\overline{N}\right)^n$$
$$B^{n+1} = \left(A\,\overline{M}\,N\right)^n$$
$$Z = B$$

M	N	A^n	B^n	A^{n+1}	B^{n+1}	Z
0	0	0	0	0	0	0
1	0	0	0	1	0	0
0	1	0	0	0	0	0
1	1	0	0	0	0	0
0	0	1	0	0	0	0
1	0	1	0	1	0	0
0	1	1	0	0	1	1
1	1	1	0	0	0	0
0	0	0	1	0	0	0
1	0	0	1	1	0	0
0	1	0	1	0	0	0
1	1	0	1	0	0	0

State machine

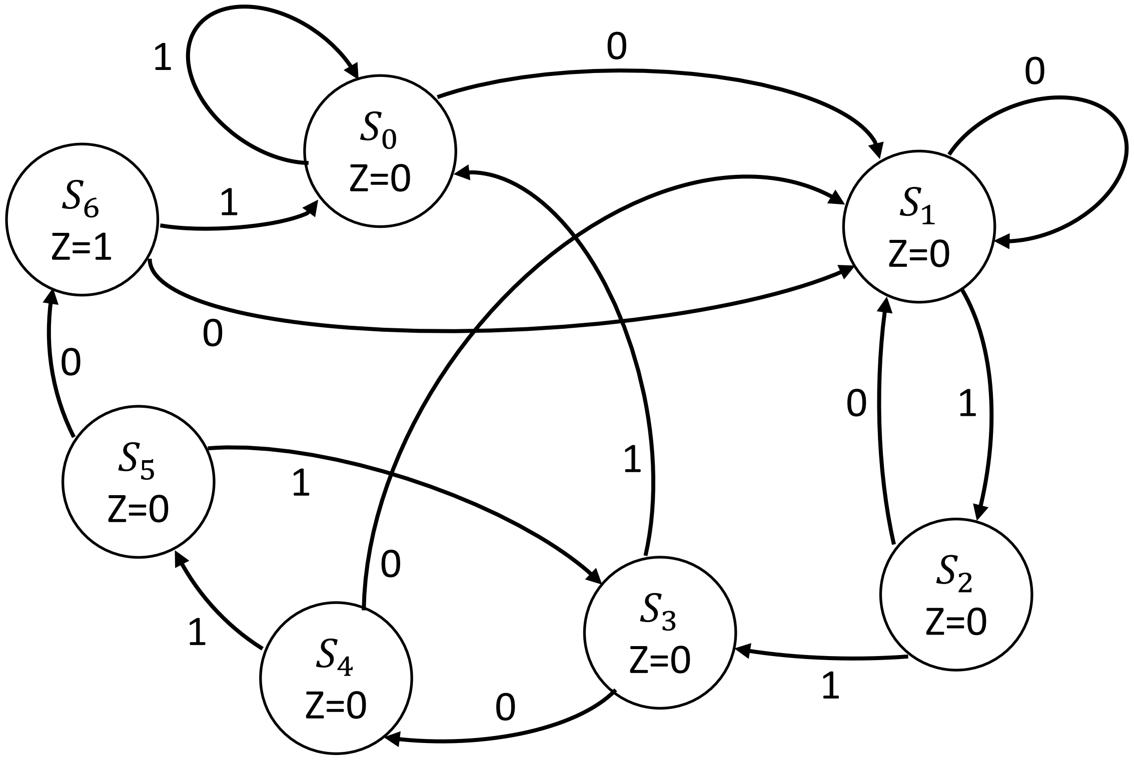
- Find the transition (1,0) -> (0,1) of two bits (M,N)

$$A^{n+1} = \left(M\,\overline{N}\right)^{n}$$
$$B^{n+1} = \left(A\,\overline{M}\,N\right)^{n}$$
$$Z = B$$



State machine

- Find the sequence …011010… on a data line M



M	A^n	B^n	C^n	A^{n+1}	B^{n+1}	C^{n+1}
0	0	0	0	1	0	0
1	0	0	0	0	0	0
0	1	0	0	1	0	0
1	1	0	0	0	1	0
0	0	1	0	1	0	0
1	0	1	0	1	1	0
0	1	1	0	0	0	1
1	1	1	0	0	0	0
0	0	0	1	1	0	0
1	0	0	1	1	0	1
0	1	0	1	0	1	1
1	1	0	1	1	1	0
0	0	1	1	1	0	0
1	0	1	1	0	0	0

Exercises

- Complete the previous example designing the state machine circuit with the use of J-K flip-flops
- Design a controller for an elevator
  - The elevator can be at one of the three floors: Ground, First and Second
  - There is a button that controls the elevator, and it has two possible values: up and down
  - The elevator goes up one floor every time you set the button to “up”, and goes down one floor every time you set the button to “down”
  - There are two lights in a row in the elevator that indicate the current floor: both lights off (00) indicates the ground floor; the left light off and right light on (01) indicates the first floor; the right light off and left right on (10) indicates the second floor