

APR

Meng-Chih, Chang
Media IC & System Lab

Outline

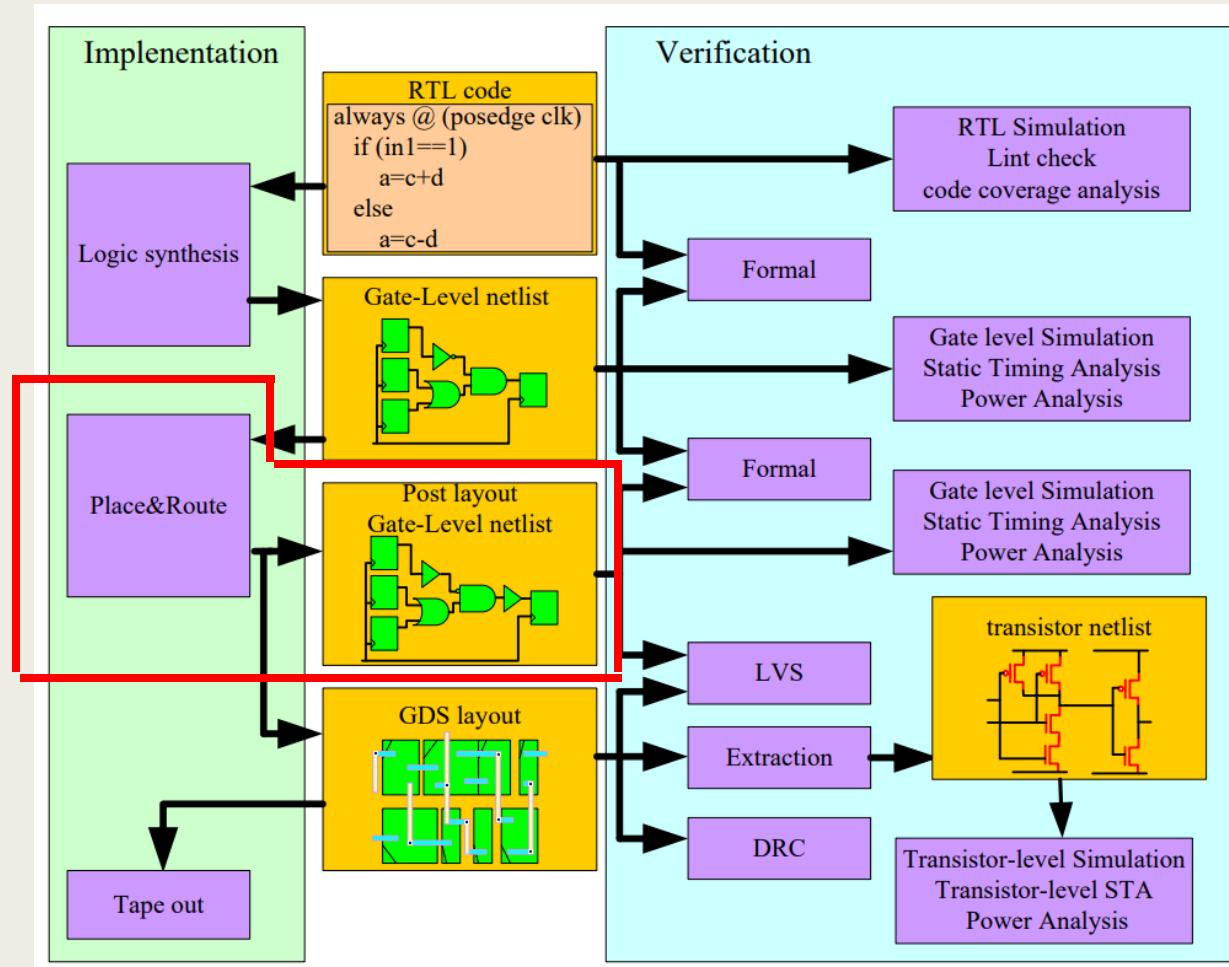
- Introduction
- Initial step
- Floor plan
- Power plan
- Power route
- Placement
- CTS
- Route
- Post processing
- Post-layout simulation
- Reference

Outline

- Introduction
- Initial step
- Floor plan
- Power plan
- Power route
- Placement
- CTS
- Route
- Post processing
- Post-layout simulation
- Reference

Introduction

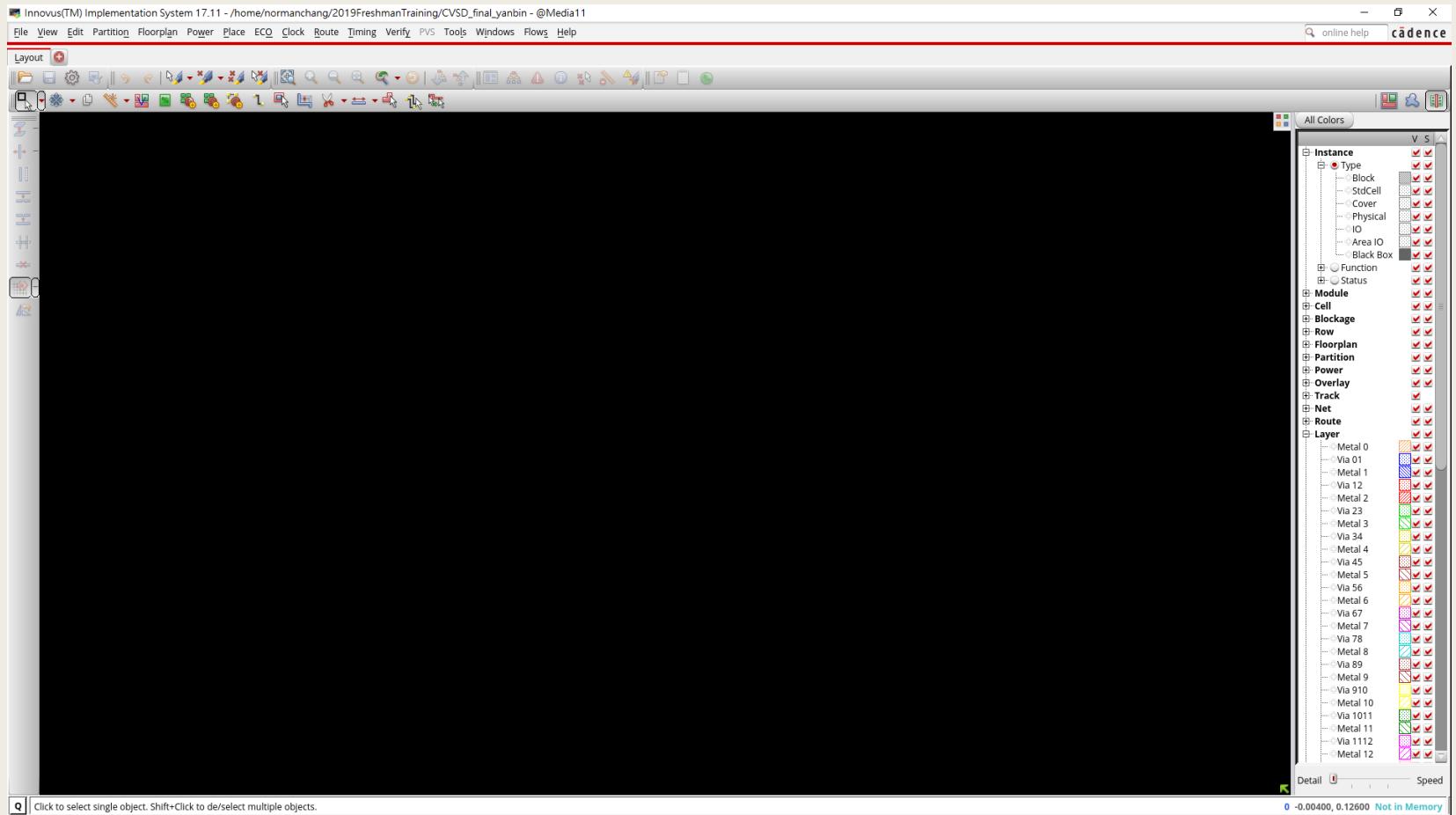
- What's APR?
 - *Automatic Place & Route*



Introduction

- Brief introduction of tool
 - *Cadence Innovus*

cadence®



Introduction

■ Some manipulation

- z: zoom in (equal to mouse wheel)
- shift + z: zoom out (equal to mouse wheel)
- press mouse wheel: drag
- shift + mouse wheel: horizontal shift
- control + mouse wheel: vertical shift
- select an object + delete: delete the object

Introduction

- Before start the whole flow:
 - I'll use *Italic Type* to indicate it's a selectable option.
 - I'll use underline type to indicate you need to fill it.

Outline

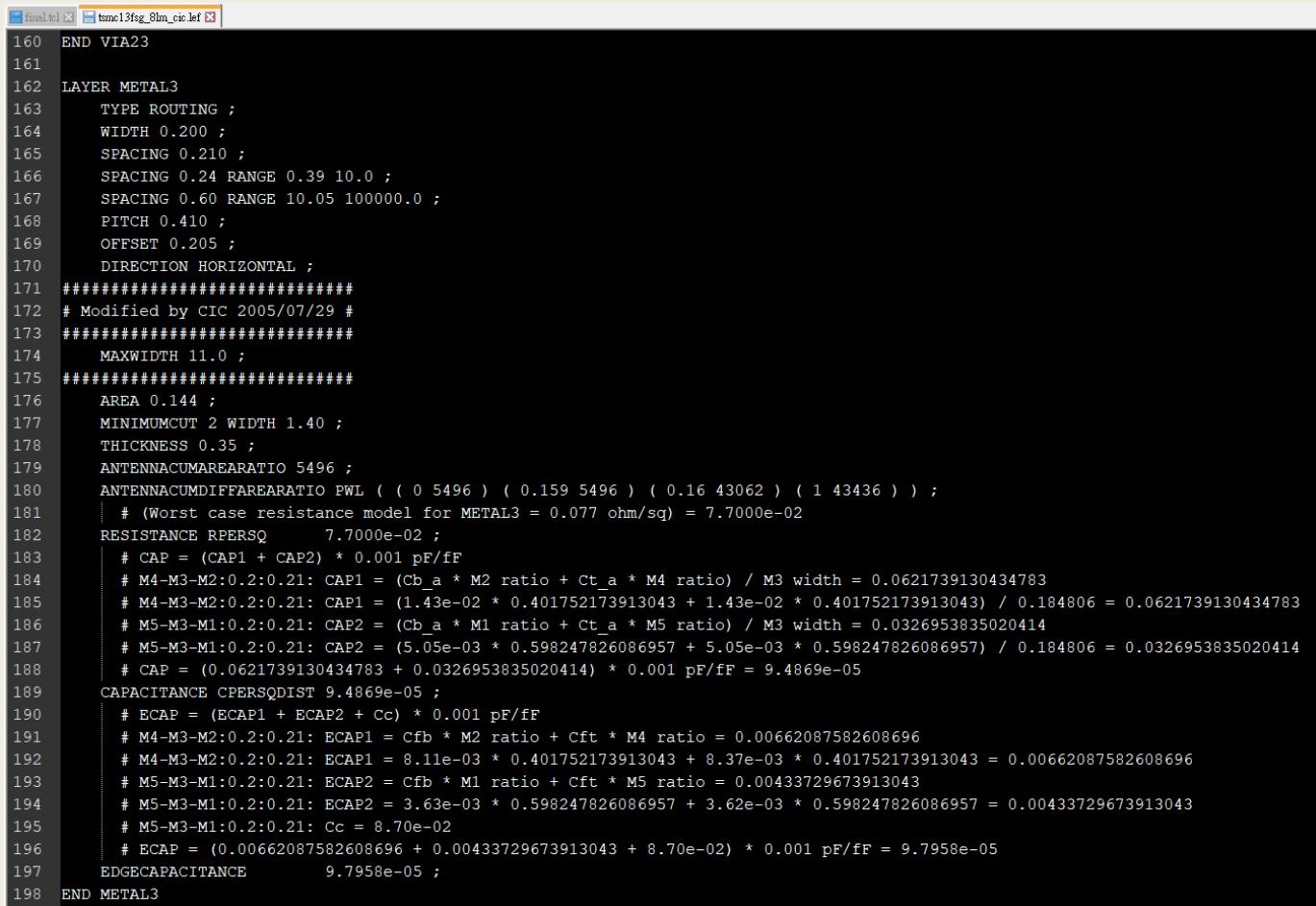
- Introduction
- Initial step
- Floor plan
- Power plan
- Power route
- Placement
- CTS
- Route
- Post processing
- Post-layout simulation
- Reference

Initial Step

- File preparing:
 - Verilog file after synthesis
 - sdc file
 - lef file
 - MMMC.view
 - (optional) tcl file

Initial Step

- What's lef file?
 - *Contain process technology information*



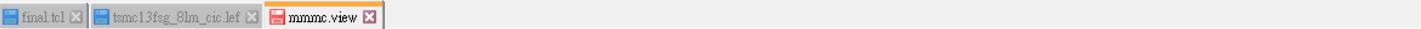
The screenshot shows a terminal window with two tabs: 'final.tcl' and 'tsmc13fsg_8lm_cic.lef'. The 'tsmc13fsg_8lm_cic.lef' tab is active and displays the following content:

```
160 END VIA23
161
162 LAYER METAL3
163     TYPE ROUTING ;
164     WIDTH 0.200 ;
165     SPACING 0.210 ;
166     SPACING 0.24 RANGE 0.39 10.0 ;
167     SPACING 0.60 RANGE 10.05 100000.0 ;
168     PITCH 0.410 ;
169     OFFSET 0.205 ;
170     DIRECTION HORIZONTAL ;
171 ######
172 # Modified by CIC 2005/07/29 #
173 #####
174     MAXWIDTH 11.0 ;
175 #####
176     AREA 0.144 ;
177     MINIMUMCUT 2 WIDTH 1.40 ;
178     THICKNESS 0.35 ;
179     ANTENNACUMAREARATIO 5496 ;
180     ANTENNACUMDIFFAREARATIO PWL ( ( 0 5496 ) ( 0.159 5496 ) ( 0.16 43062 ) ( 1 43436 ) ) ;
181     # (Worst case resistance model for METAL3 = 0.077 ohm/sq) = 7.7000e-02
182     RESISTANCE RPERSQ    7.7000e-02 ;
183     # CAP = (CAP1 + CAP2) * 0.001 pF/fF
184     # M4-M3-M2:0.2:0.21: CAP1 = (Cb_a * M2 ratio + Ct_a * M4 ratio) / M3 width = 0.0621739130434783
185     # M4-M3-M2:0.2:0.21: CAP1 = (1.43e-02 * 0.401752173913043 + 1.43e-02 * 0.401752173913043) / 0.184806 = 0.0621739130434783
186     # M5-M3-M1:0.2:0.21: CAP2 = (Cb_a * M1 ratio + Ct_a * M5 ratio) / M3 width = 0.0326953835020414
187     # M5-M3-M1:0.2:0.21: CAP2 = (5.05e-03 * 0.598247826086957 + 5.05e-03 * 0.598247826086957) / 0.184806 = 0.0326953835020414
188     # CAP = (0.0621739130434783 + 0.0326953835020414) * 0.001 pF/fF = 9.4869e-05
189     CAPACITANCE CPERSQDIST 9.4869e-05 ;
190     # ECAP = (ECAP1 + ECAP2 + Cc) * 0.001 pF/fF
191     # M4-M3-M2:0.2:0.21: ECAP1 = Cfb * M2 ratio + Cft * M4 ratio = 0.00662087582608696
192     # M4-M3-M2:0.2:0.21: ECAP1 = 8.11e-03 * 0.401752173913043 + 8.37e-03 * 0.401752173913043 = 0.00662087582608696
193     # M5-M3-M1:0.2:0.21: ECAP2 = Cfb * M1 ratio + Cft * M5 ratio = 0.00433729673913043
194     # M5-M3-M1:0.2:0.21: ECAP2 = 3.63e-03 * 0.598247826086957 + 3.62e-03 * 0.598247826086957 = 0.00433729673913043
195     # M5-M3-M1:0.2:0.21: Cc = 8.70e-02
196     # ECAP = (0.00662087582608696 + 0.00433729673913043 + 8.70e-02) * 0.001 pF/fF = 9.7958e-05
197     EDGECAPACITANCE      9.7958e-05 ;
198 END METAL3
```

Initial Step

■ What's MMMC file?

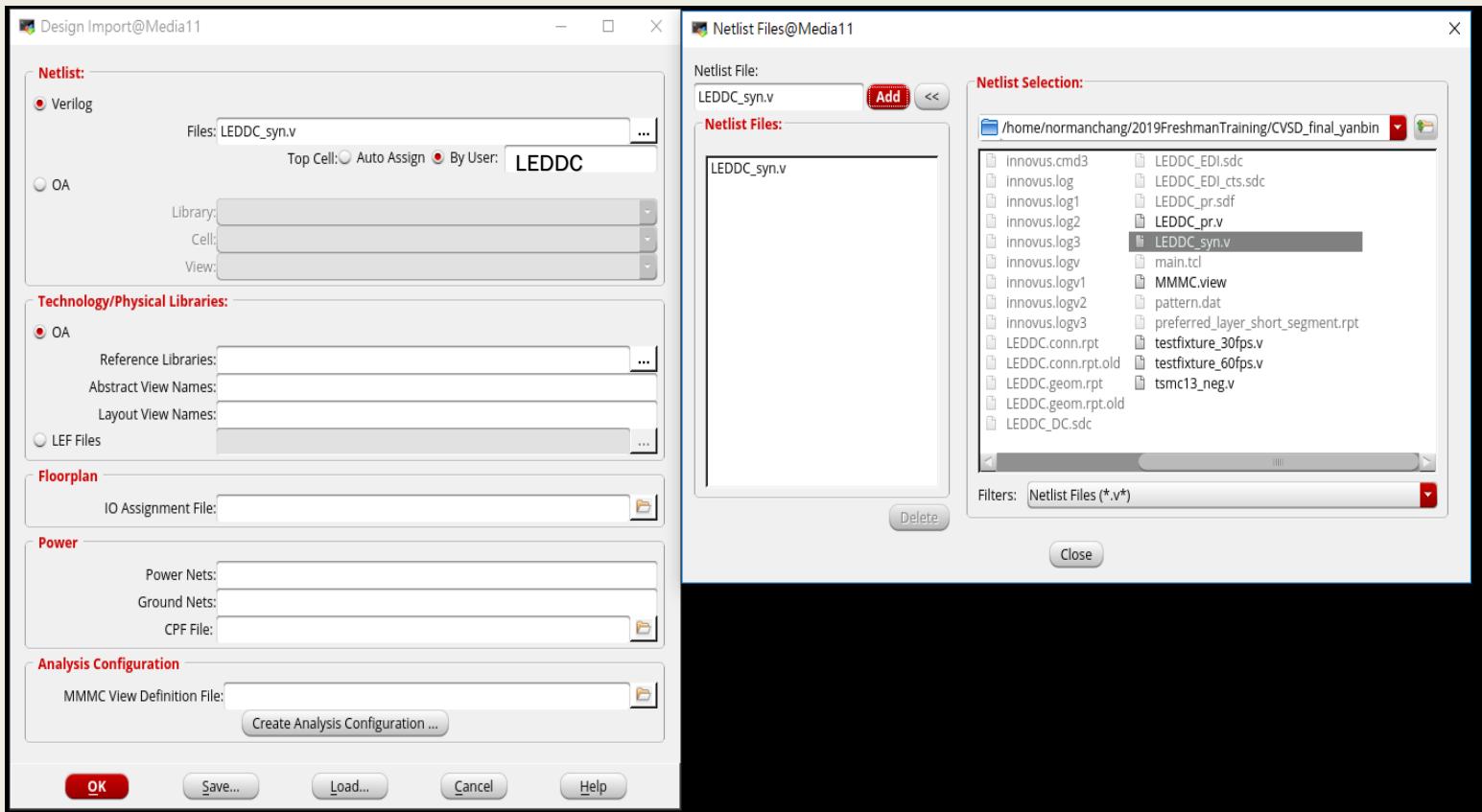
- *Multi-Mode Multi Corner*
- *Similar to sdc file*



```
final.tcl x tsmc13fsg_8lm_cic_left x mmmc.view x
1 # Version:1.0 MMMC View Definition File
2 # Do Not Remove Above Line
3
4 create_rc_corner -name RC_corner -cap_table {library/tsmc013.capTbl} -preRoute_res {1.0} -preRoute_cap {1.0} \
5           -preRoute_clkres {0.0} -preRoute_clkcap {0.0} -postRoute_res {1.0} -postRoute_cap {1.0} \
6           -postRoute_xcap {1.0} -postRoute_clkres {0.0} -postRoute_clkcap {0.0} \
7           -qx_tech_file {library/tsmc13_8lm.cl/icecaps_8lm.tch}
8
9 create_library_set -name lib_max -timing {library/lib/slow.lib
10          ./Memory/sram_1024x8_t13/sram_1024x8_t13_slow_syn.lib
11          library/lib/tpz013g3wc.lib} -si {library/celtic/slow.cdB}
12
13 create_library_set -name lib_min -timing {library/lib/fast.lib
14          ./Memory/sram_1024x8_t13/sram_1024x8_t13_slow_syn.lib
15          library/lib/tpz013g3lt.lib} -si {library/celtic/fast.cdB}
16
17 create_constraint_mode -name func_mode -sdc_files {CLE_DC.sdc}
18 create_constraint_mode -name scan_mode -sdc_files {CLE_scan.sdc}
19
20 create_delay_corner -name Delay_Corner_max -library_set {lib_max} -rc_corner {RC_corner}
21 create_delay_corner -name Delay_Corner_min -library_set {lib_min} -rc_corner {RC_corner}
22
23 create_analysis_view -name av_func_mode_max -constraint_mode {func_mode} -delay_corner {Delay_Corner_max}
24 create_analysis_view -name av_func_mode_min -constraint_mode {func_mode} -delay_corner {Delay_Corner_min}
25
26 create_analysis_view -name av_scan_mode_max -constraint_mode {scan_mode} -delay_corner {Delay_Corner_max}
27 create_analysis_view -name av_scan_mode_min -constraint_mode {scan_mode} -delay_corner {Delay_Corner_min}
28
29 set_analysis_view -setup {av_func_mode_max av_scan_mode_max} -hold {av_func_mode_min av_scan_mode_min}
30
```

Initial Step

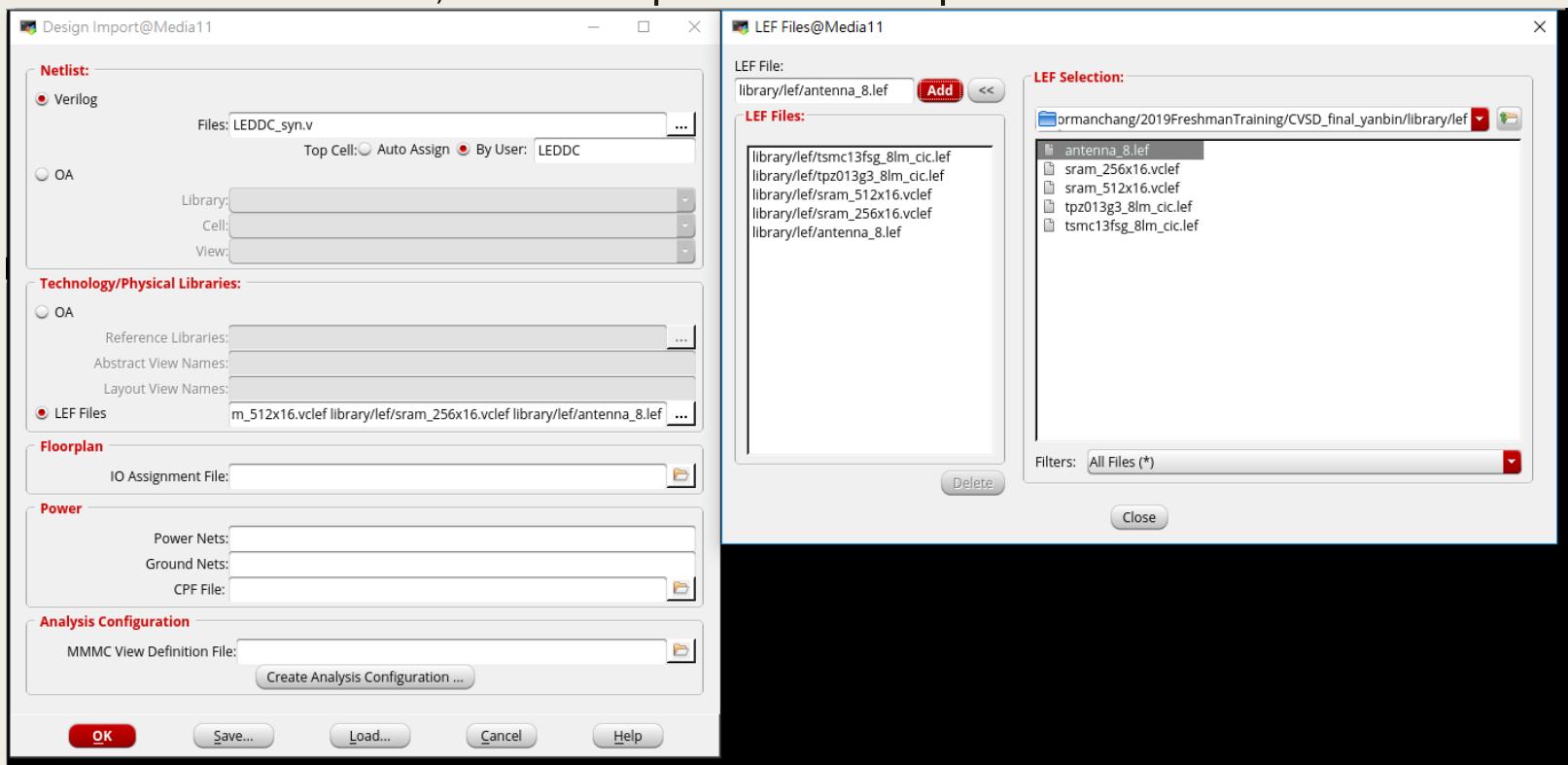
- 1. File → Import Design → Netlist → *Verilog* → Files → ... →
select your file and click Add
- 2. Select By User, fill your_design_name



Initial Step

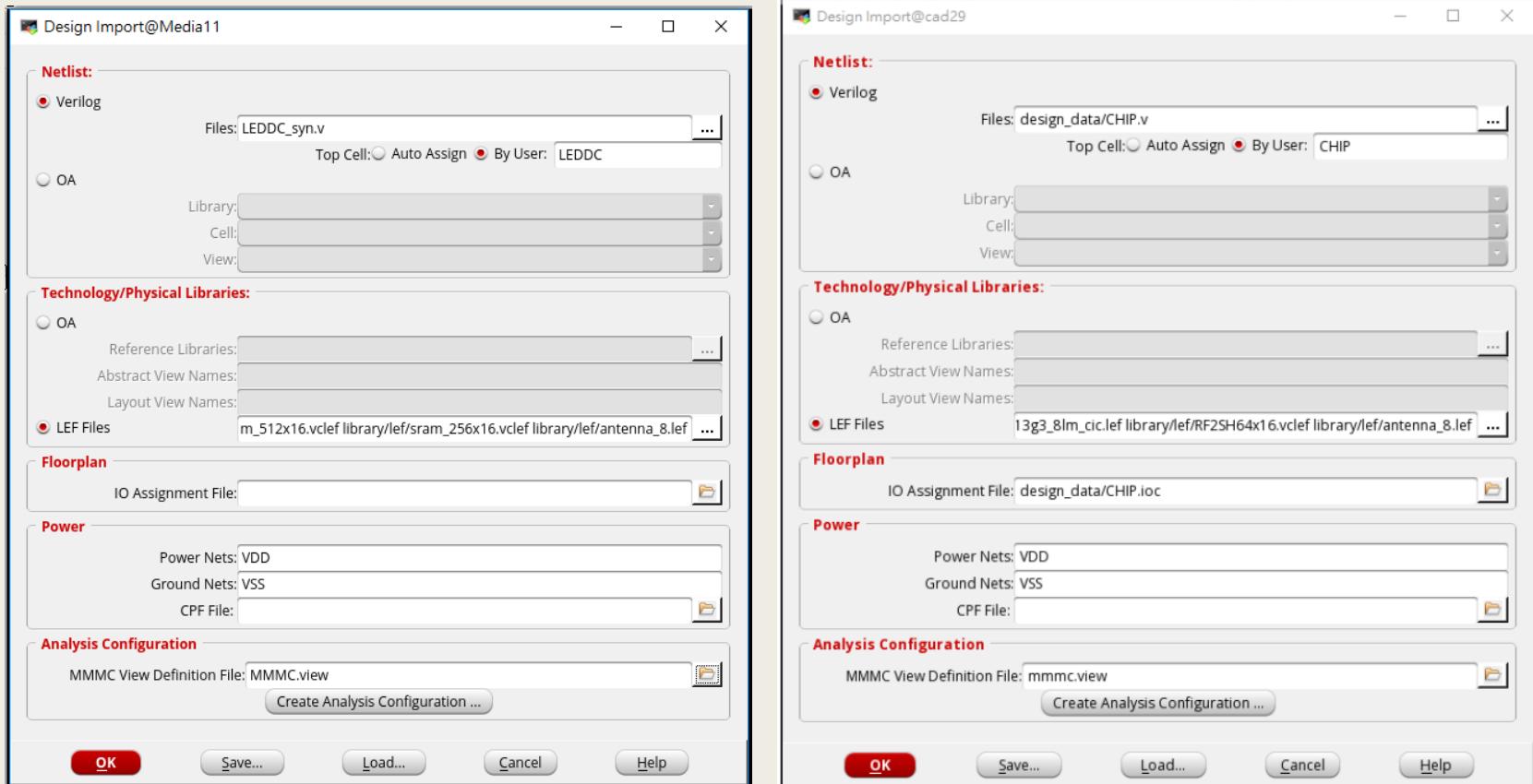
- 3. Load process file
- *LEF Files* → ... → Filters: *All Files (*)* → add lef files

※ *tsmc13fsg_8lm_cic.lef* contain all process technology information, must be place at first place



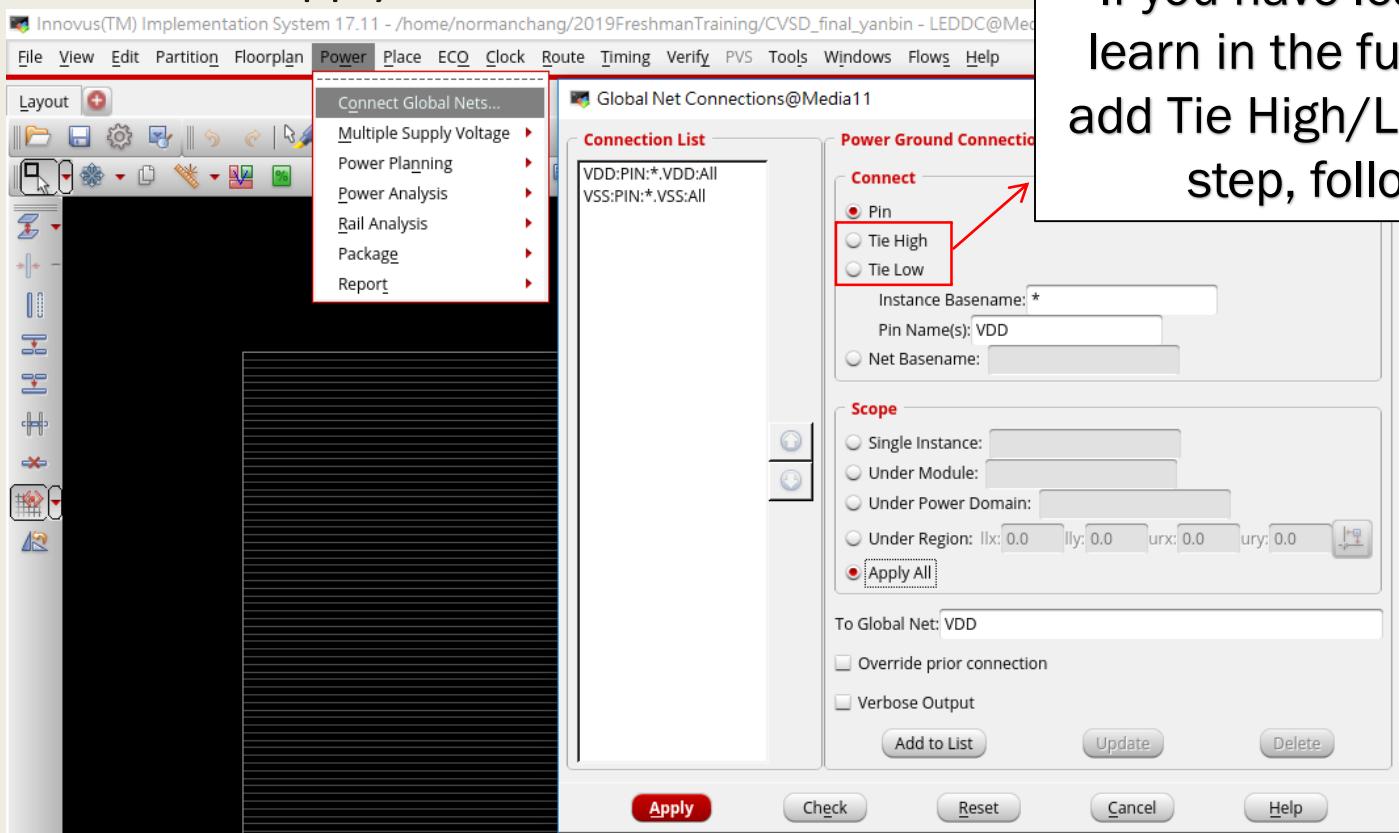
Initial Step

- 4. (Optional) IO Assignment File → add IO file
- 5. Power → Power Nets: VDD; Ground Nets: VSS
- 6. MMC view... → load MMMC.view



Initial Step

- 7. Connect global power
- Power → Connect Global Nets → Pin Name(s): VDD; Scope: *Apply All*; To Global Net: VDD → Add to List → Do it again but change VDD to VSS → Apply



If you have learned or learn in the future that add Tie High/Low at this step, follow it.

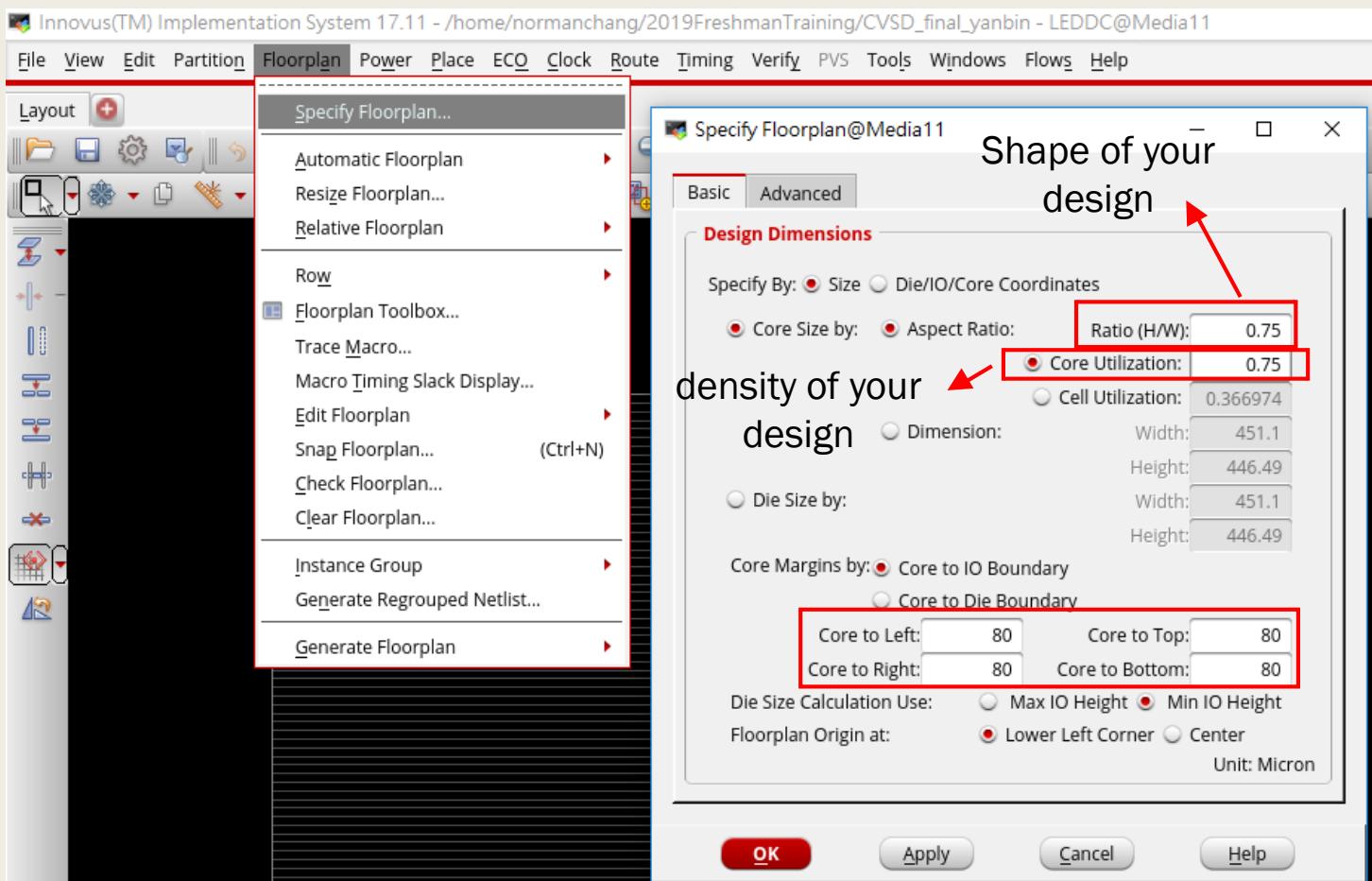
Initial Step

- 8. (Optional) Specify scanchain:
 - *innovus > specifyScanChain scanx -start your_input_name/C –stop your_output_name/I*
 - *innovus > scanTrace*
- Ex:

```
innovus 12> specifyScanChain scan1 -start ipad_test_si1/C -stop opad_test_so1/I
innovus 13> specifyScanChain scan2 -start ipad_test_si2/C -stop opad_test_so2/I
innovus 14> specifyScanChain scan3 -start ipad_test_si3/C -stop opad_test_so3/I
innovus 15> specifyScanChain scan4 -start ipad_test_si4/C -stop opad_test_so4/I
innovus 16> specifyScanChain scan5 -start ipad_test_si5/C -stop opad_test_so5/I
innovus 17> scanTrace
*** Scan Trace Summary (runtime: cpu: 0:00:00.0 , real: 0:00:00.0):
Successfully traced 5 scan chains (total 545 scan bits).
*** Scan Sanity Check Summary:
*** 5 scan chains passed sanity check.
innovus 18> █
```

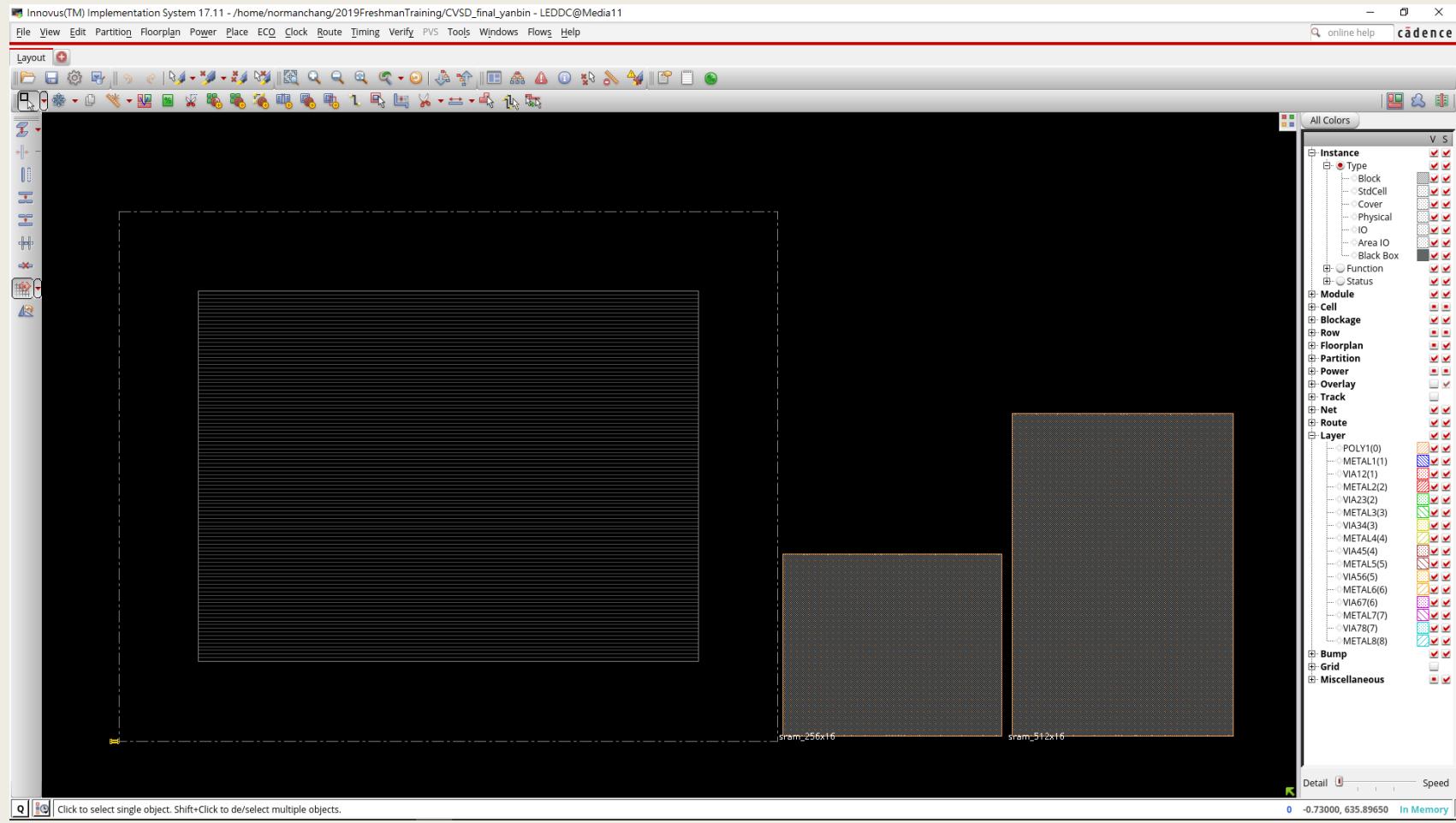
Initial Step

- 9. Decide the overview of you design.
- Floorplan → Specify Floorplan... → ...



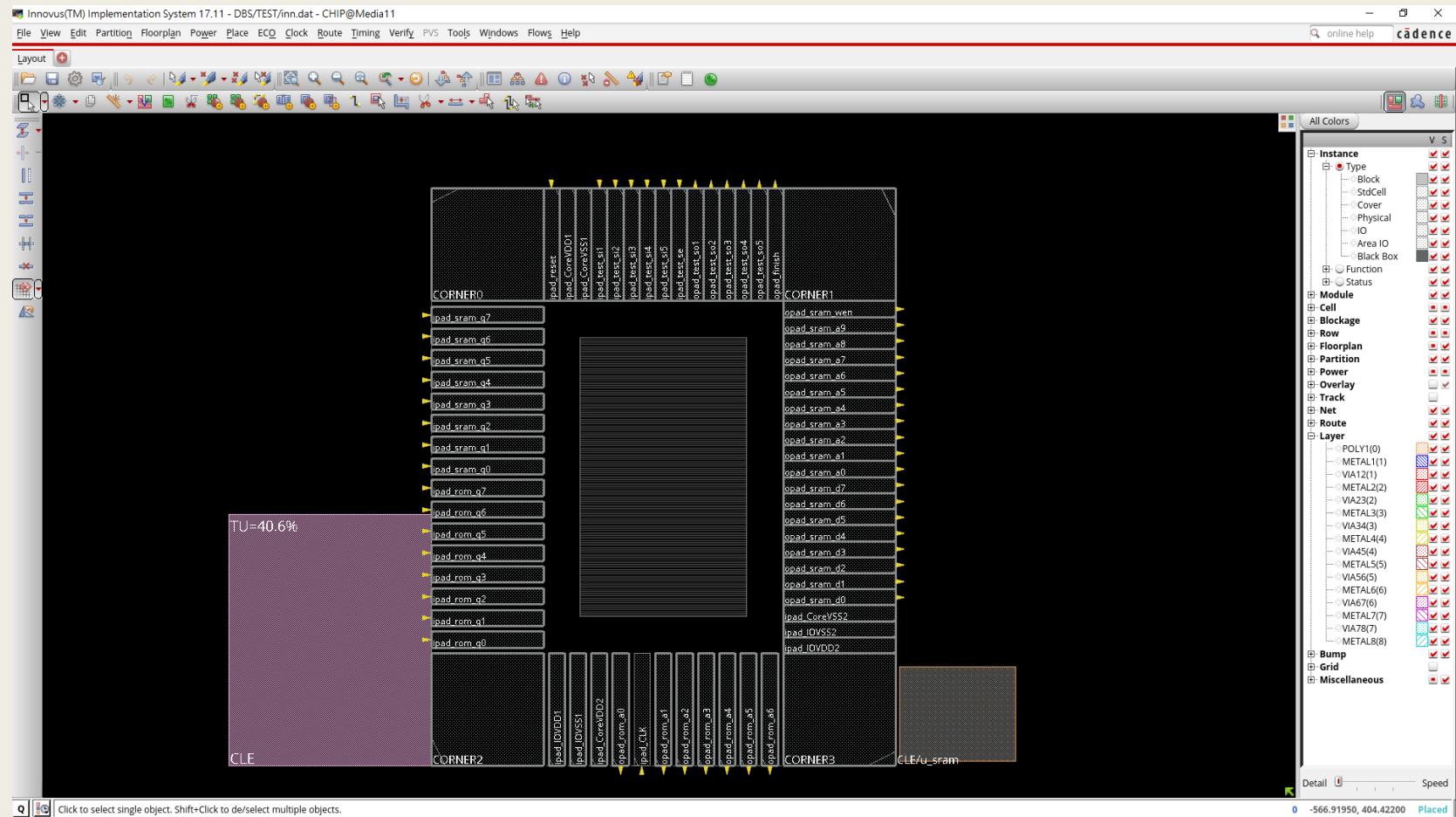
Initial Step

- w/o iopad:



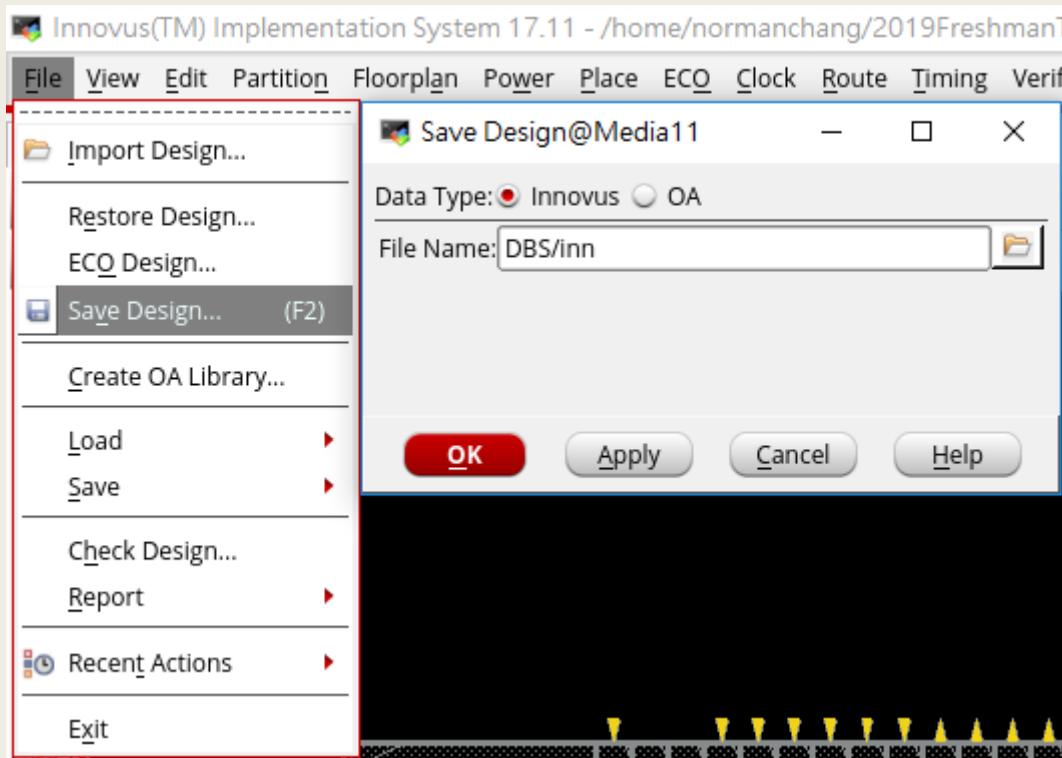
Initial Step

- w/ iopad:



Initial Step

- 10. File → Save Design... → *Innovus: DBS/inn*
- 11. File → Save Design... → *Innovus: DBS/inn*
- 12. File → Save Design... → *Innovus: DBS/inn*



Outline

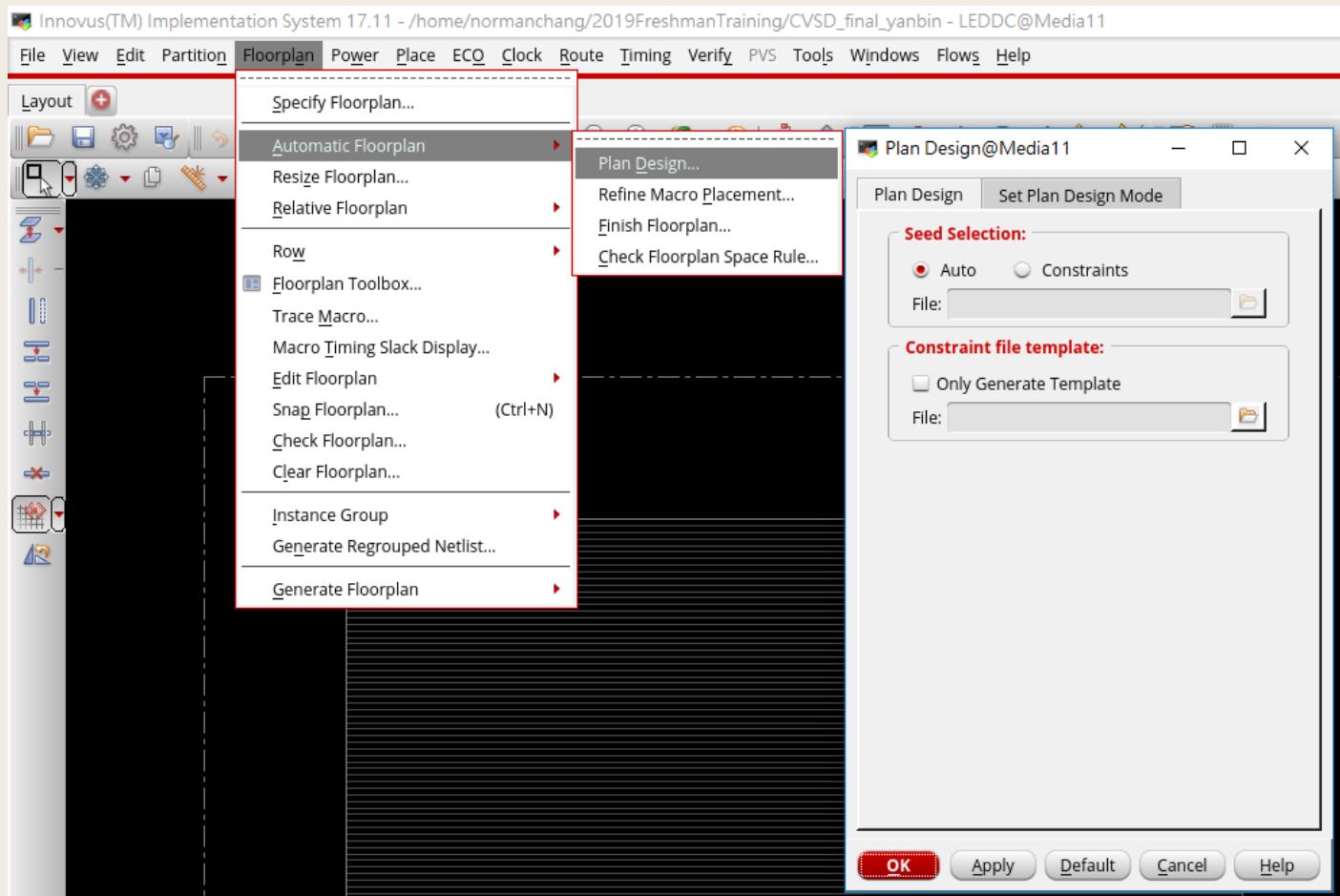
- Introduction
- Initial step
- Floor plan**
- Power plan
- Power route
- Placement
- CTS
- Route
- Post processing
- Post-layout simulation
- Reference

Floor Plan

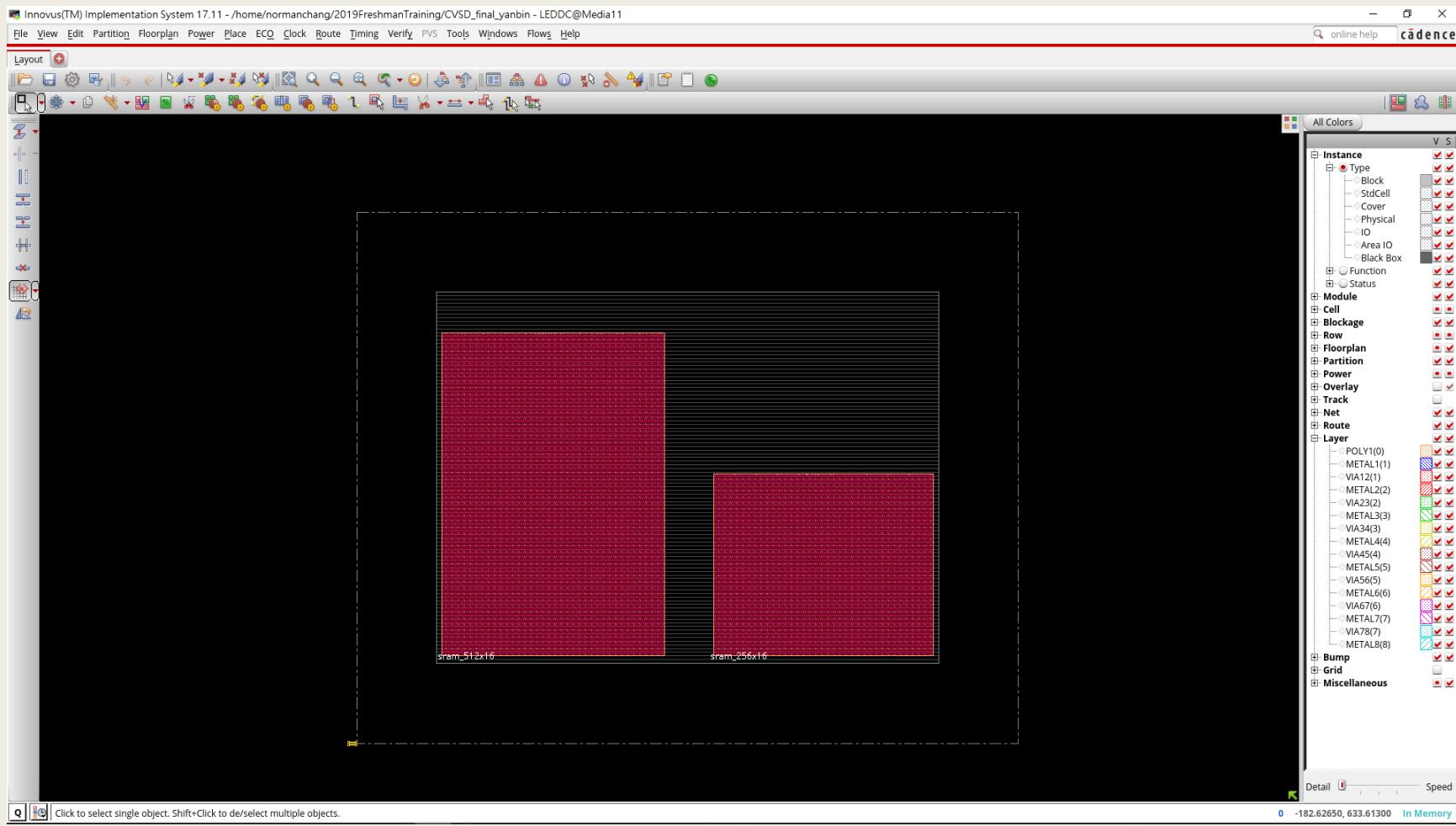
- In this stage, we are going to decide how to place the basic things.

Floor Plan

- 1. Place our modules
- Floorplan → Automatic Floorplan → Plan Design...

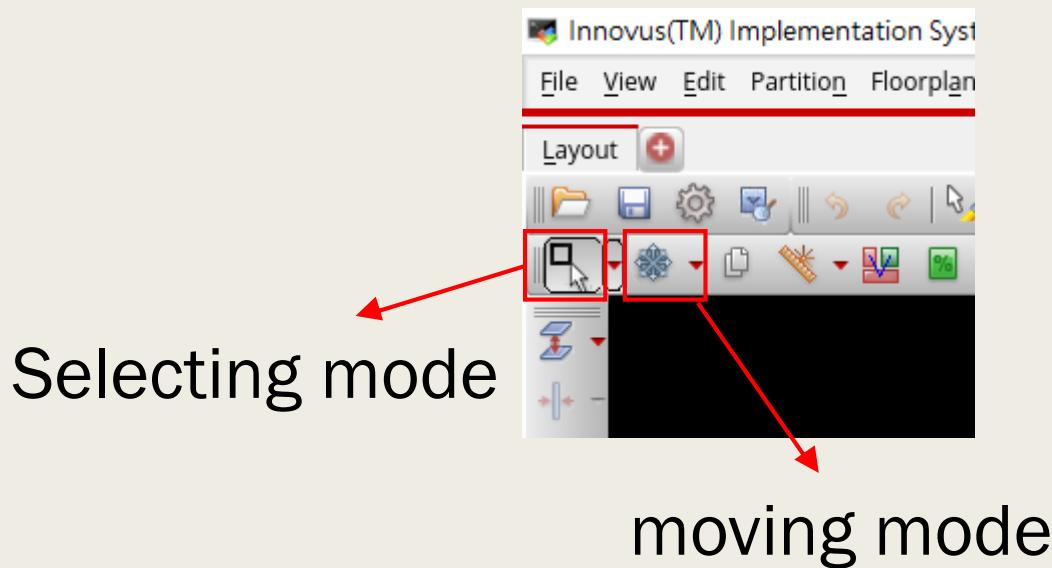


Floor Plan



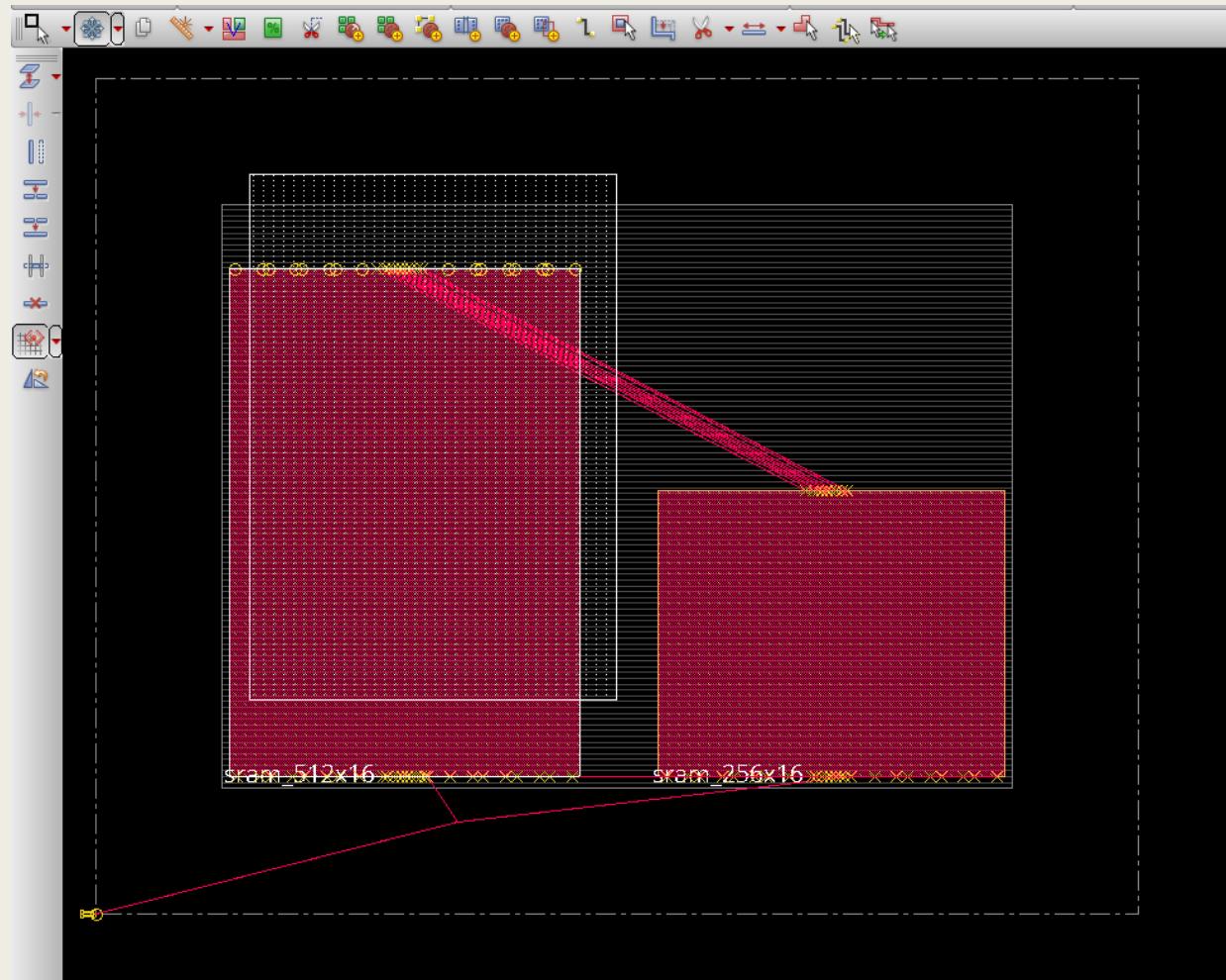
Floor Plan

- Change location and orientation of modules



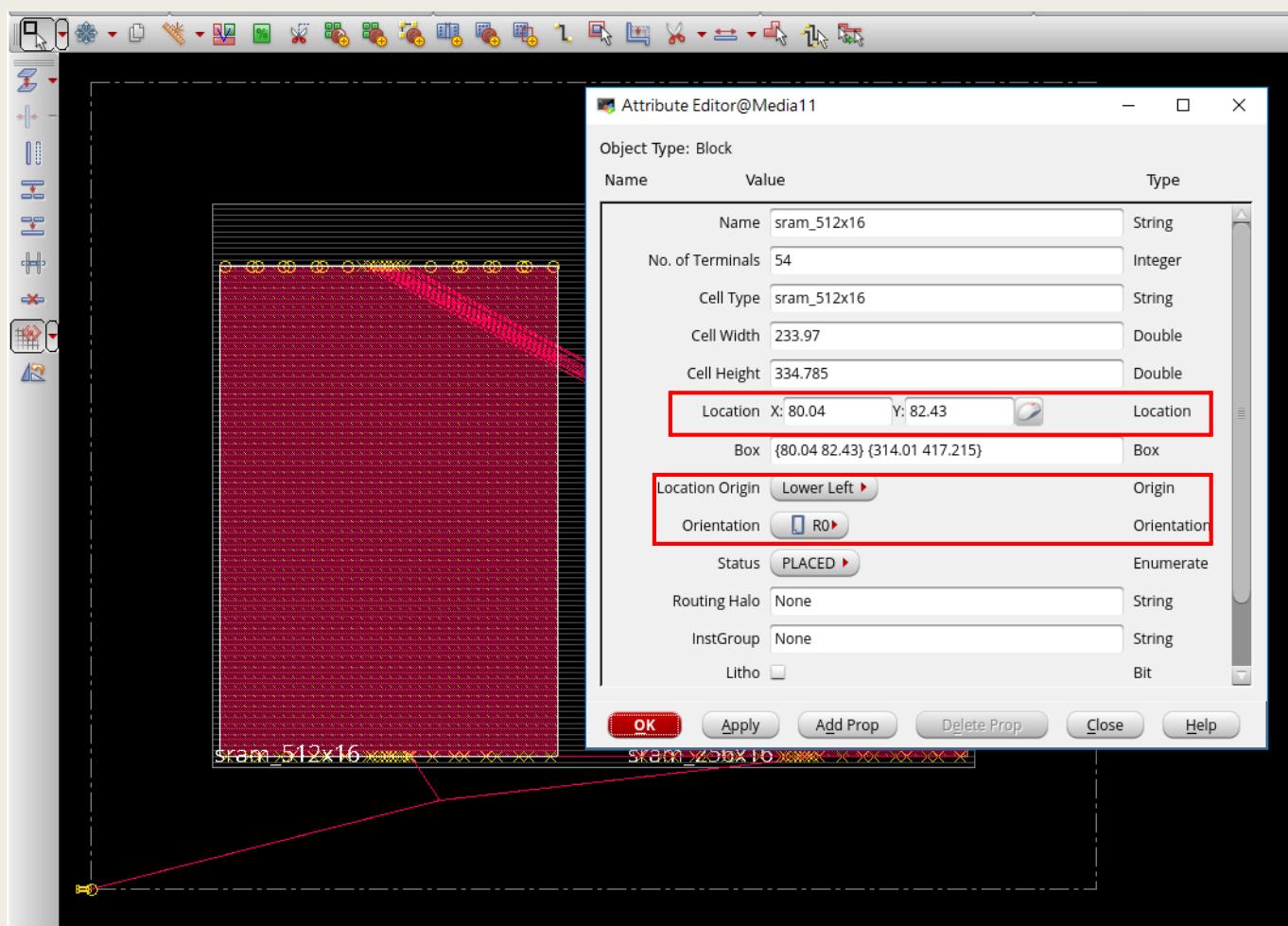
Floor Plan

- In moving mode:



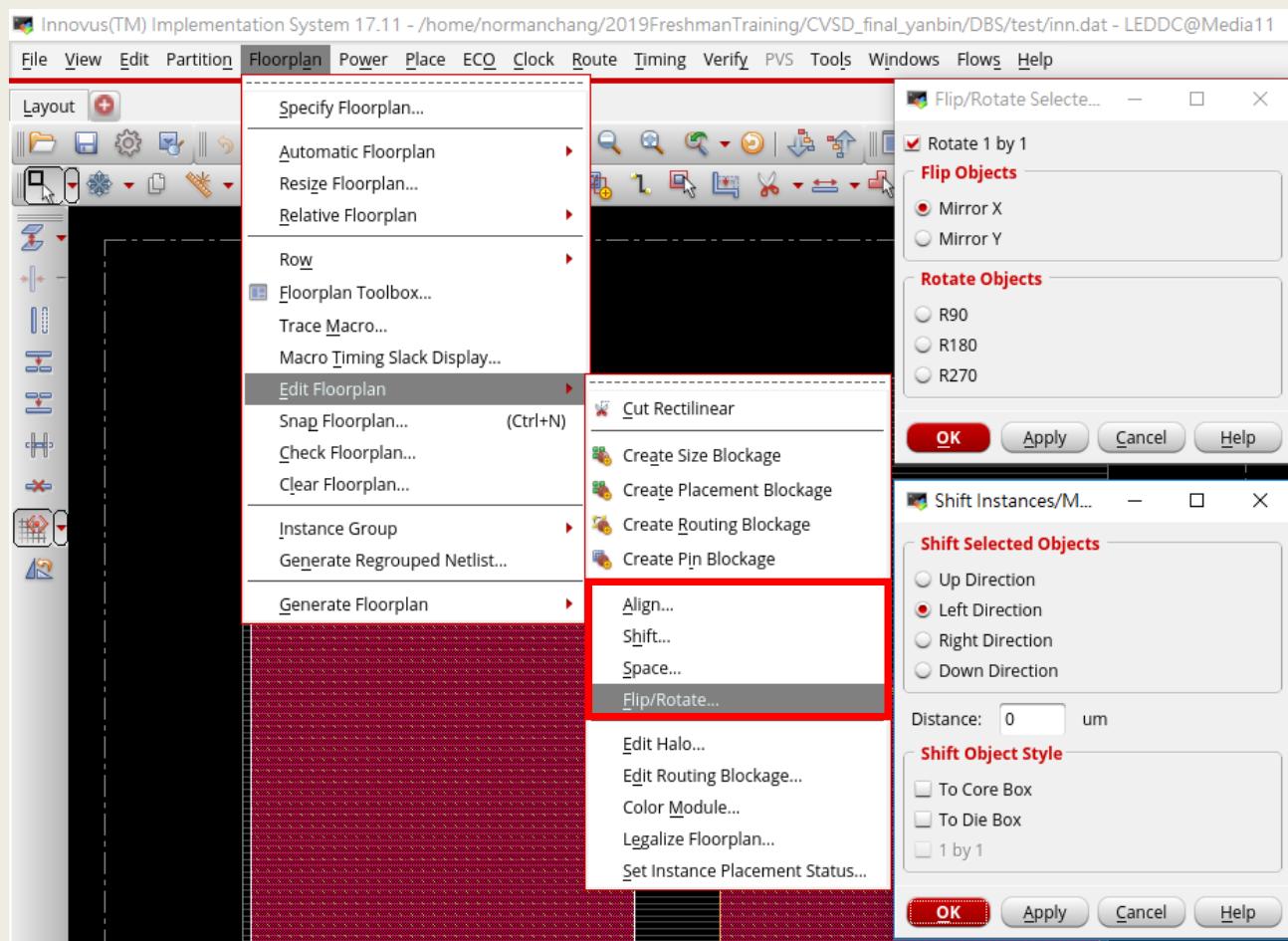
Floor Plan

- Enter selecting mode and select a module, click it twice to open Attribute Editor window



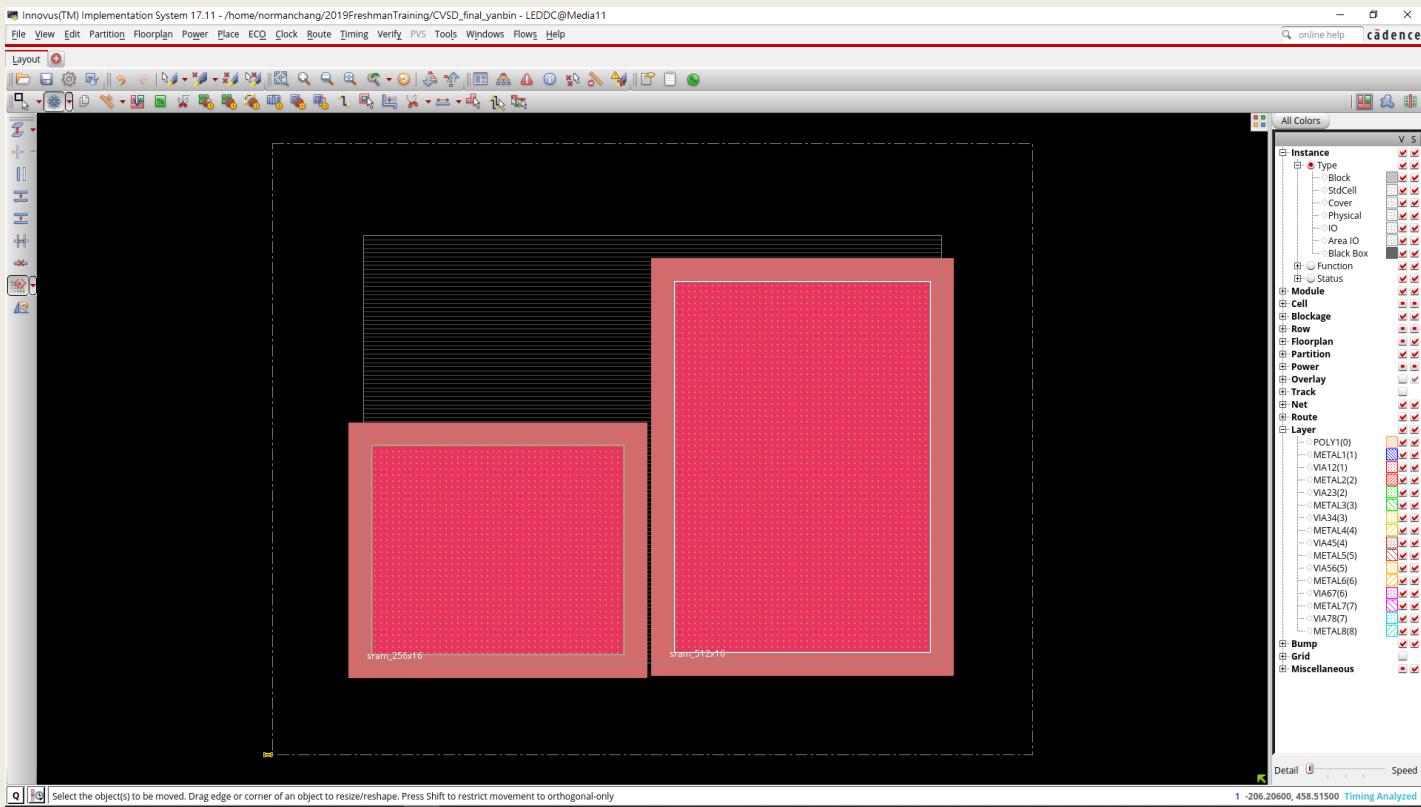
Floor Plan

- Or you can: Floorplan → Edit Floorplan →
- In this way you can do some coarse adjustment.



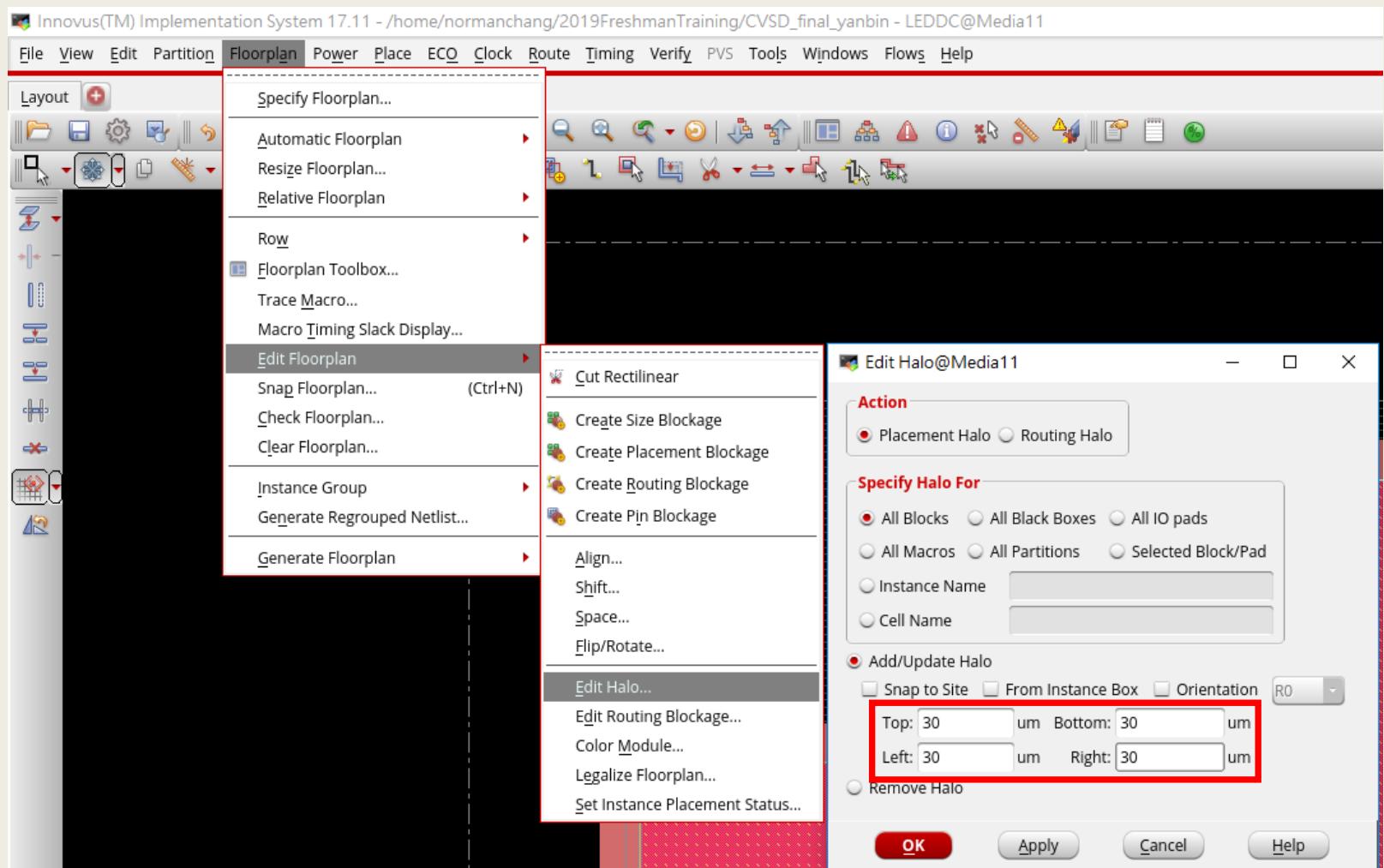
Floor Plan

- 2. Added Halo
- Why?
 - There will not have any basic cell placed inside Halo, leaving more space for routing. ~~Your module need it's own little space.~~



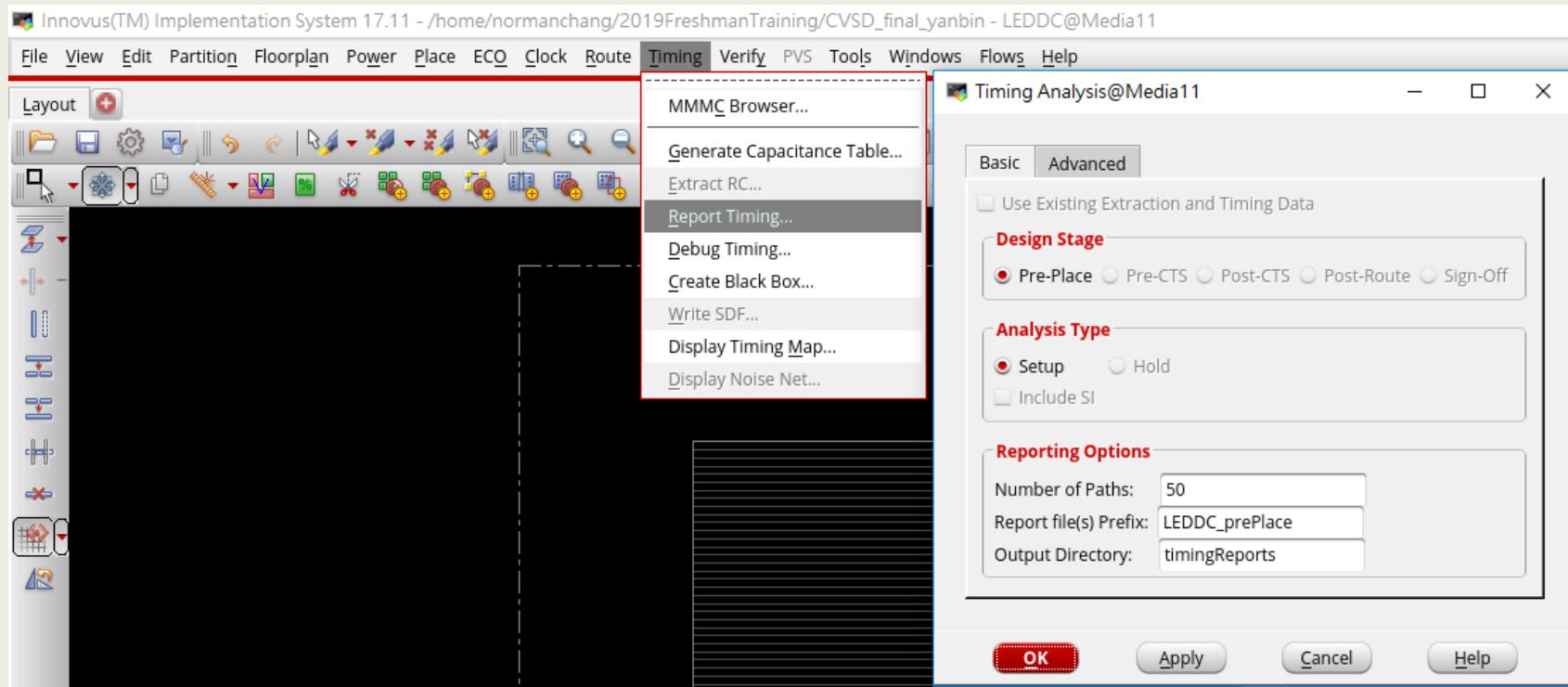
Floor Plan

- Floorplan → Edit Floorplan → Edit Halo



Floor Plan

- 3. Pre-Place timing analysis: Timing → Report Timing → OK



Floor Plan

- Your WNS and TNS should greater than (or equal to) 0.
 - *WNS: Worst Negative Slack*
 - *TNS: Total Negative Slack*
- If any one fails, change your RTL design...

```
timeDesign Summary
-----
Setup views included:
AV_func_max

+-----+-----+-----+
|      Setup mode   |    all    | reg2reg | default |
+-----+-----+-----+
|          WNS (ns):|  0.668  |  0.668  |  1.700  |
|          TNS (ns):|  0.000  |  0.000  |  0.000  |
| Violating Paths:|     0    |     0    |     0    |
|      All Paths:  | 1228   | 1179   |  391   |
+-----+-----+-----+
Density: 0.000%
```

Floor Plan

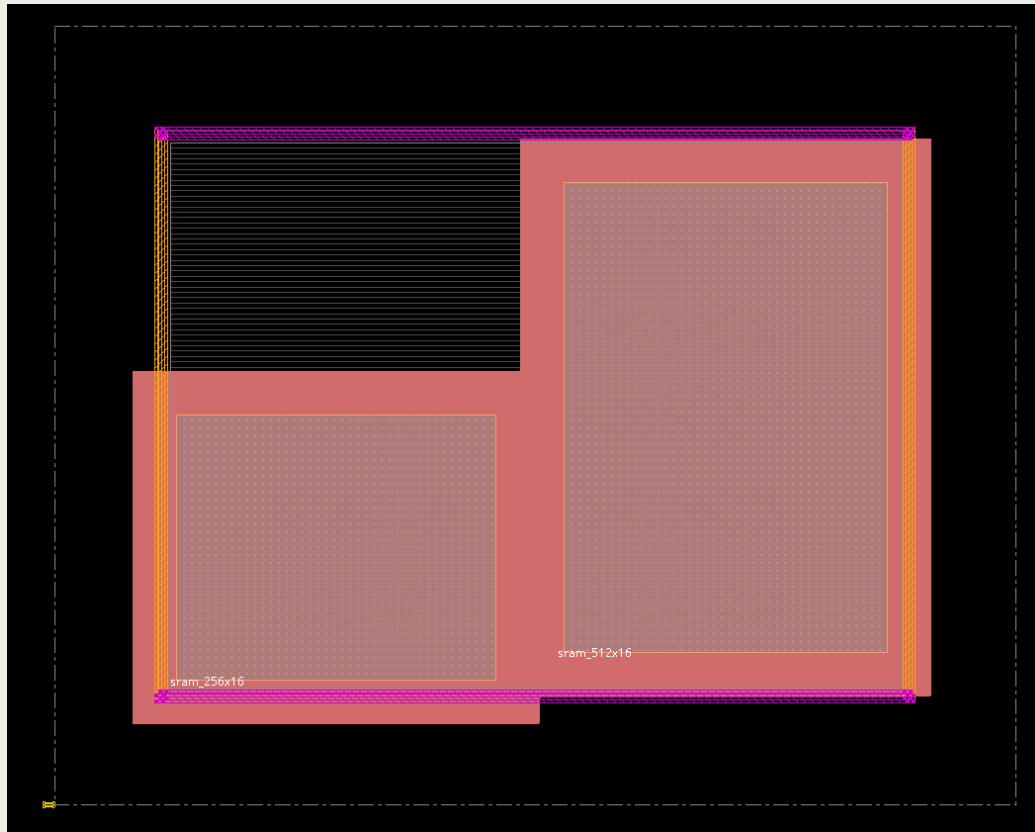
- 4. Save file: File → Save Design... → *Innovus: DBS/floorplan*

Outline

- Introduction
- Initial step
- Floor plan
- Power plan**
- Power route
- Placement
- CTS
- Route
- Post processing
- Post-layout simulation
- Reference

Power Plan

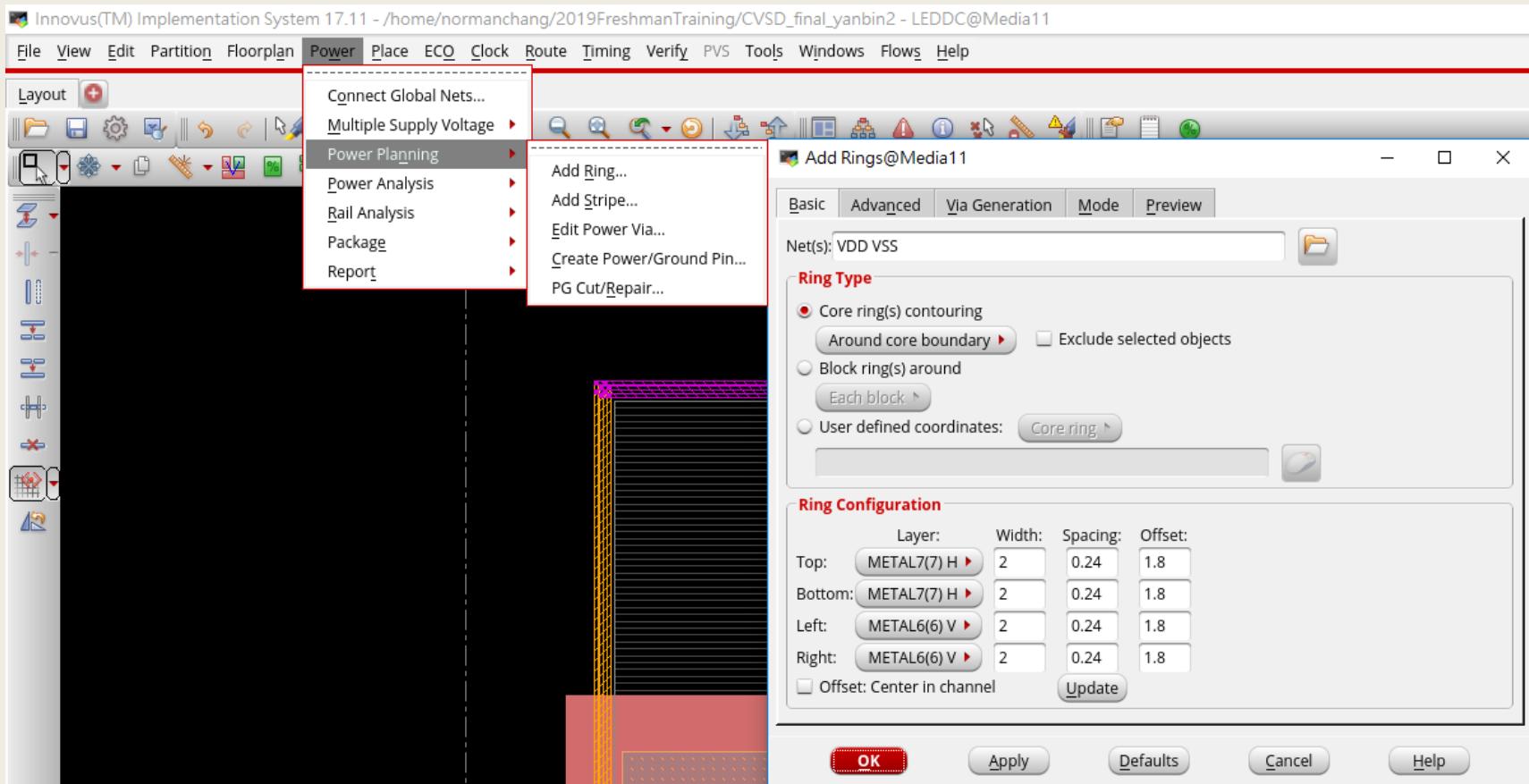
- 1. Create Power Ring
- Why?
 - *To give power to chip*



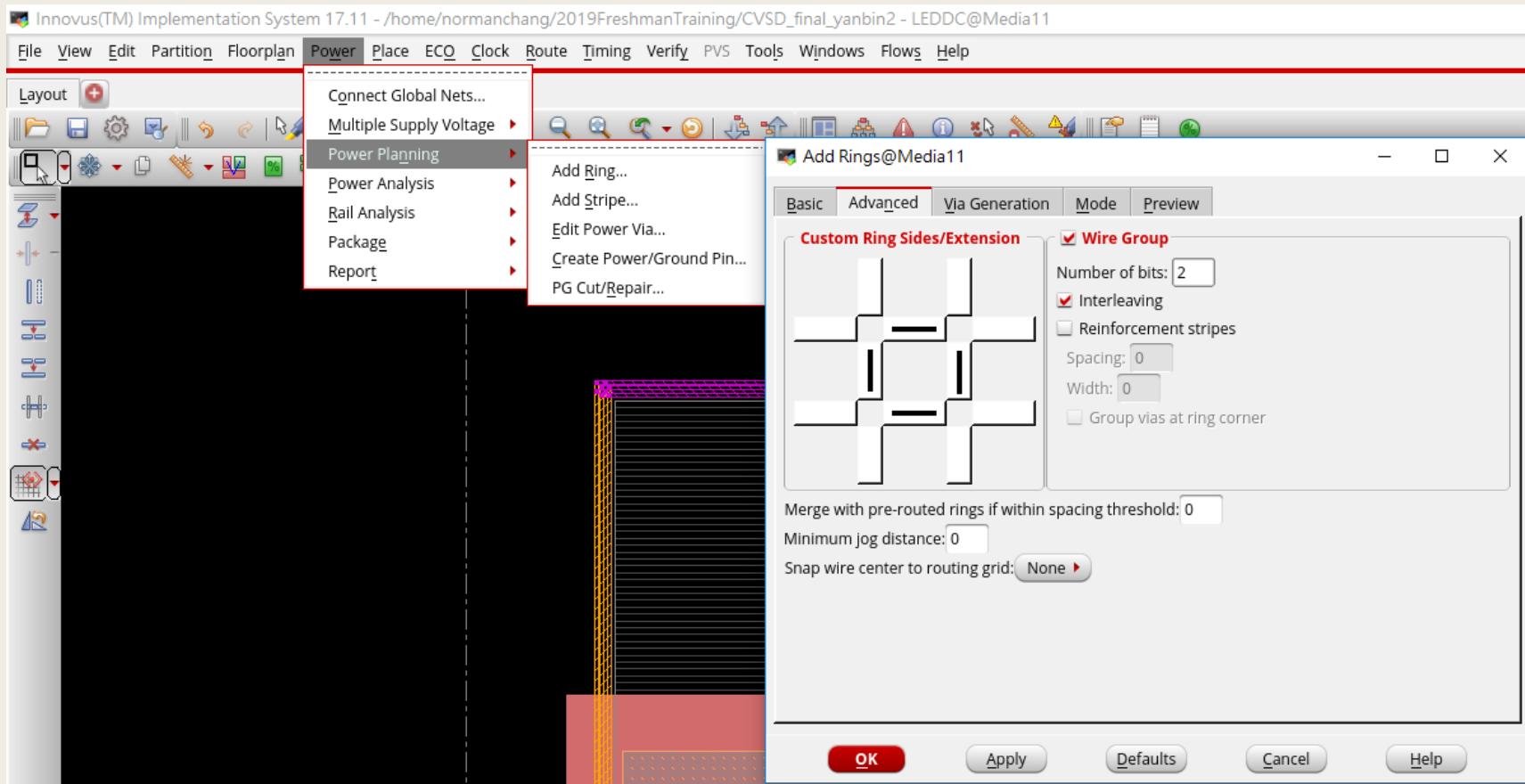
Power Plan

- Power → Power Planning → Add Rings → Basic
 - Nets: VDD VSS
 - In Ring Configuration, change Top & Bottom to *METAL7*, Left & Right to *METAL6*;
 - Set Width to 2 and click update
- Change to Advanced
 - Select *Wire Group*, set Numbers of Bits to 2
 - Select *Interleaving*

Power Plan

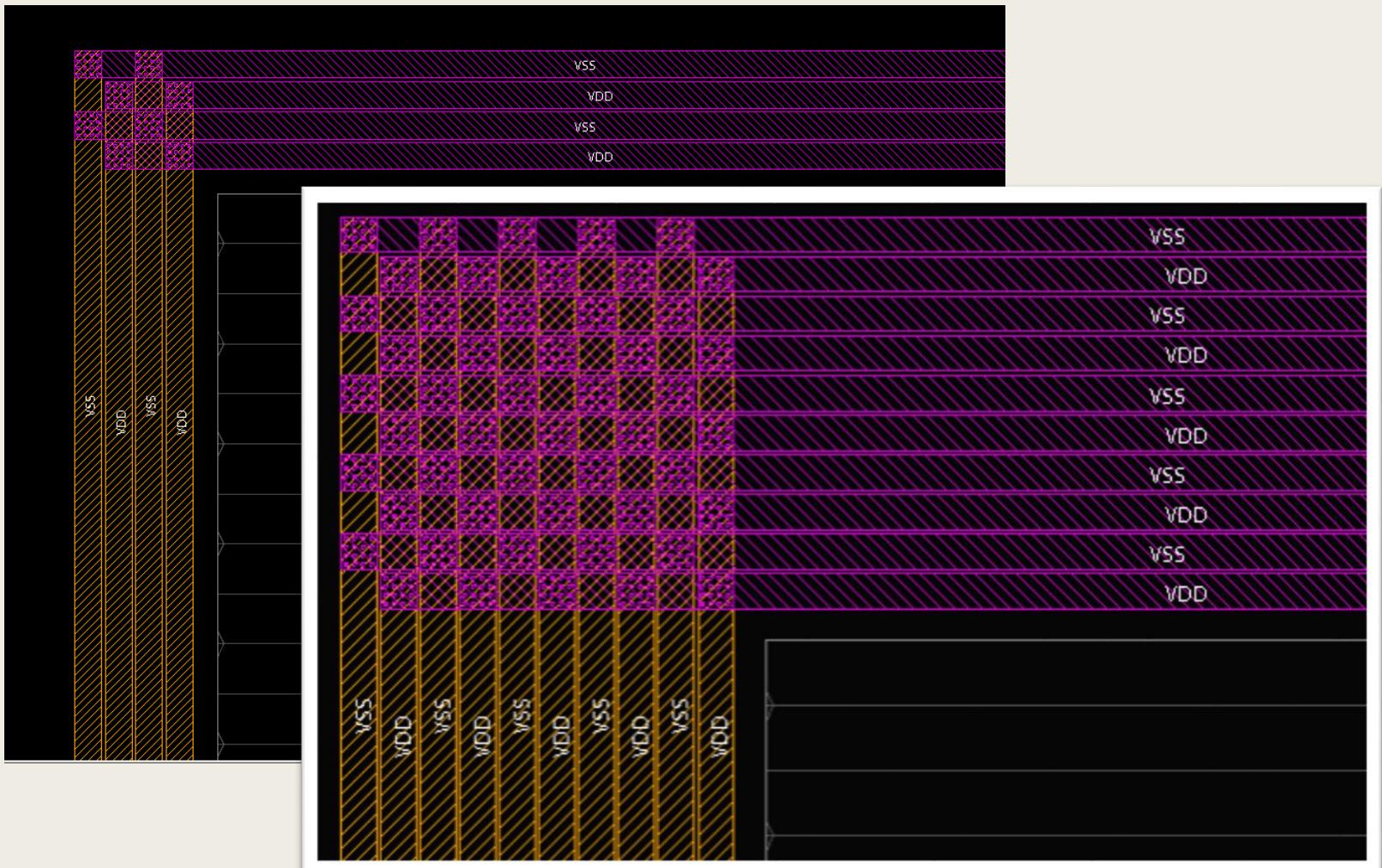


Power Plan



Power Plan

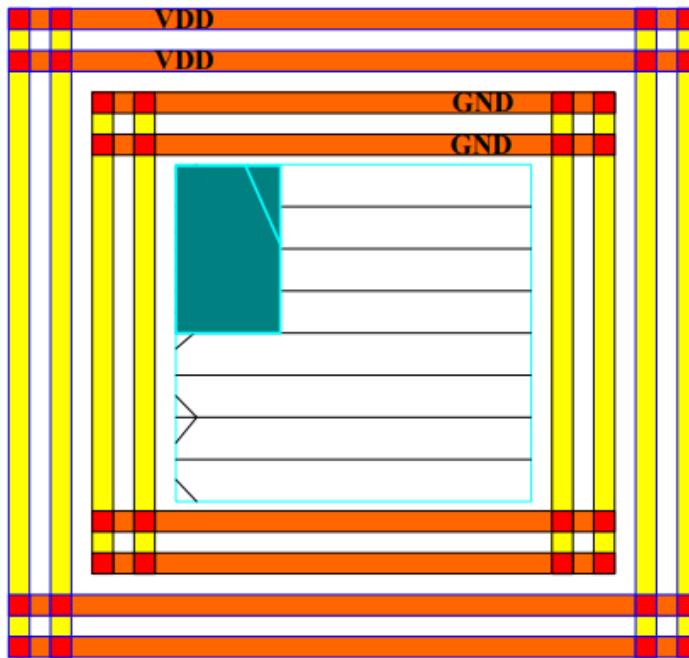
- Number of bits



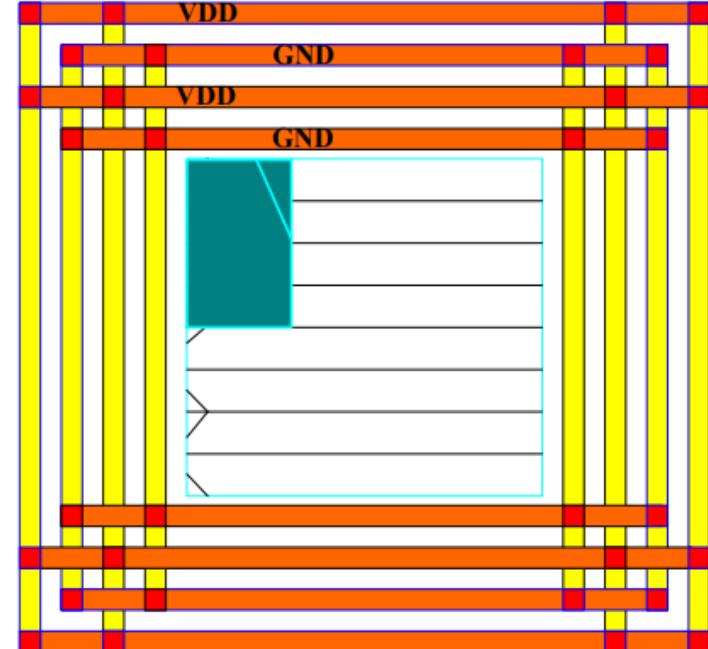
Power Plan

- What's *Interleaving*?

- ✓ Use wire group
no interleaving
- ✓ number of bits = 2



- ✓ Use wire group
- ✓ interleaving
- ✓ number of bits = 2



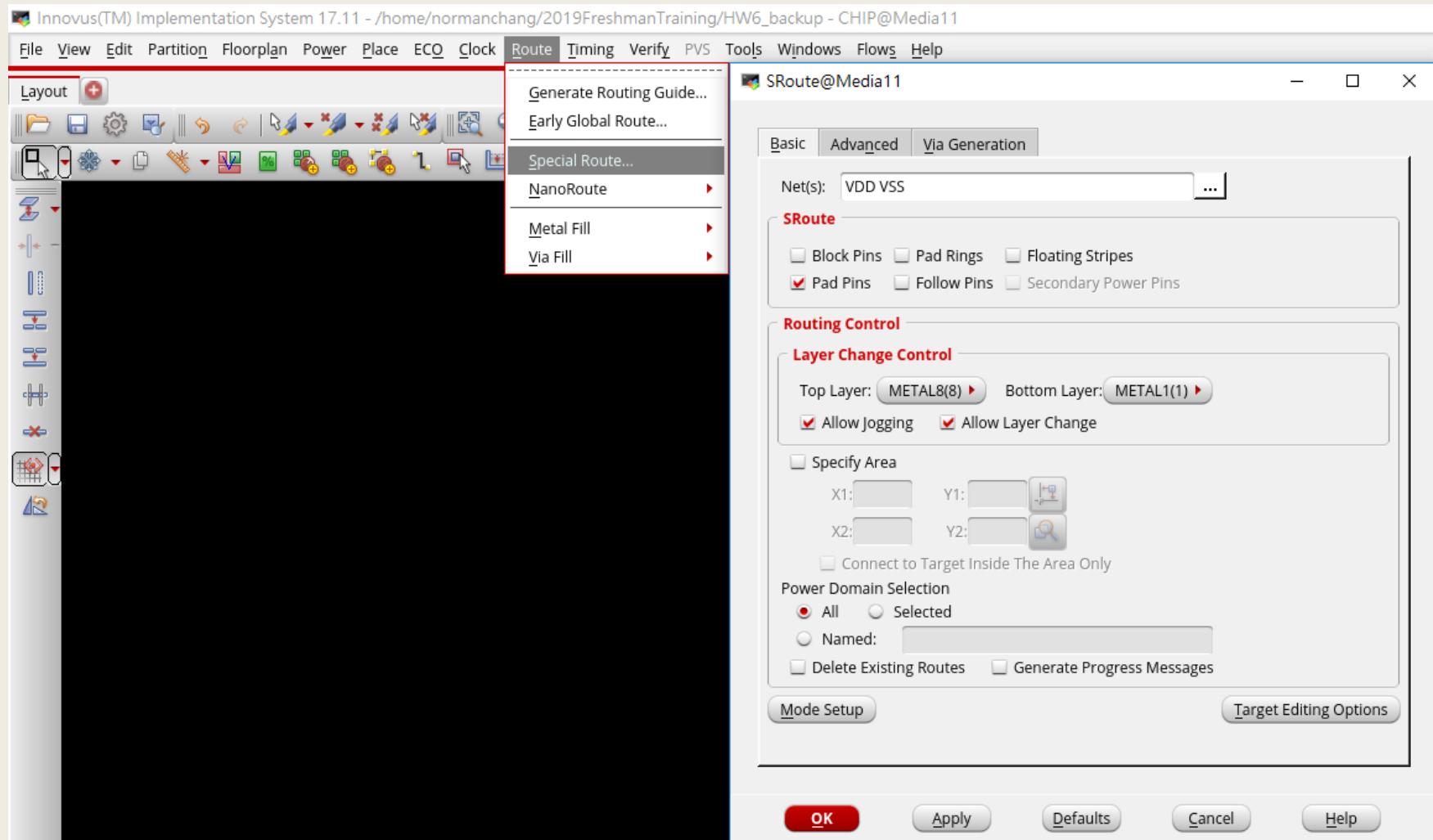
Power Plan

- 2. (Optional) Add power pad
- Why?
 - *Connect power ring with iopad.*

Power Plan

- Route → Special Route → Basic
 - Net(s): VDD VSS
 - In SRoute, only select *Pad Pins*
- Change to Advanced
 - Select *Pad Pins*
 - In Number of Connections to Multiple Geometries, select *All*
- Change to Via Generation
 - In Make Via Connection To, only select *Core Ring*
- Click Apply to see if there is any wrong. If not, click OK to confirm.

Power Plan



Power Plan

The image displays two side-by-side windows of the SRoute software interface, both titled "SRoute@Media11".

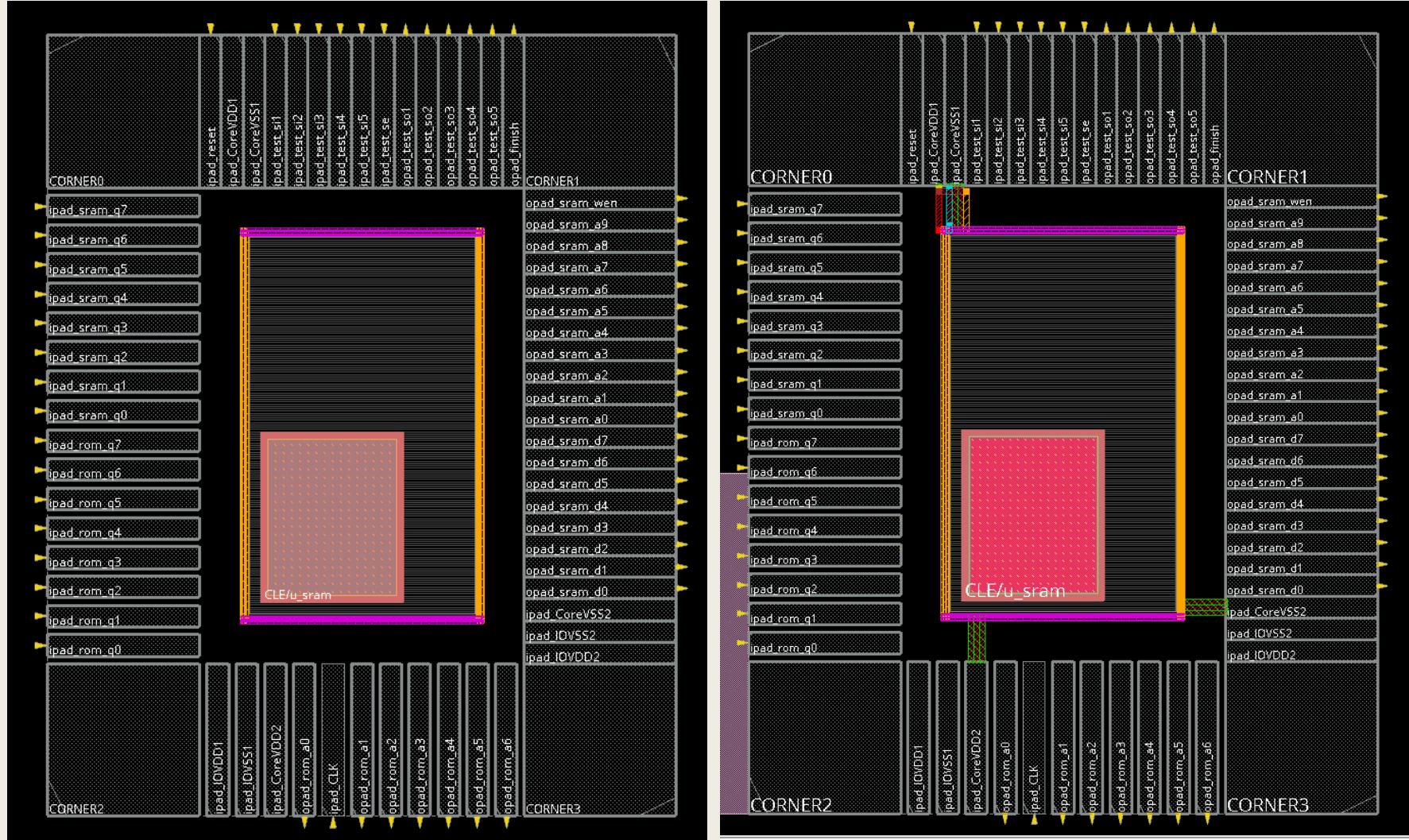
Left Window (Pad Pins Tab):

- Pad Pins:**
 - Route Only to Pins with Width: 0
 - Route Only to Pins on Layers Between:
Lowest: METAL1(1) Highest: METAL8(8)
- Number of Connections to Multiple Ports:**
 - One
 - All
- Number of Connections to Multiple Geometries:**
 - One
 - All
 - On Preferred Routing Direction
- Minimum Via Width Percent between Pad and Ring:** 20 %
- Connect to Pad Pins on:**
 - Bottom Side
 - Top Side
 - Left Side
 - Right Side
- Connect to Aligned Block Pins
- Target Selection and Extension Control:**
 - Target Selection:
 - Block Ring
 - Ring
 - Ring Pin
 - Follow Pin
 - Stripes
 - Block Pin
 - Extension Control:
 - Nearest Target

Right Window (Via Generation Tab):

- Specify Layer Ranges:**
 - Crossover Connection:
Top Stack Via Layer: METAL8(8) Bottom Stack Via Layer: METAL1(1)
 - Target Connection:
Top Stack Via Layer: METAL8(8) Bottom Stack Via Layer: METAL1(1)
- Check Standard Cell Geometry
- Split vias longer than 0 into smaller vias
with center-to-center step of 0 and height -1
and bottom/left edge offset of -1
- Make Via Connections To:**
 - Pad Ring/Pin
 - Stripe
 - Block Pin
 - Core Wire
 - IO Wire
 - Core Ring
 - Block Ring
 - Block Wire
 - Follow Pin
 - No Shape

Power Plan



Power Plan

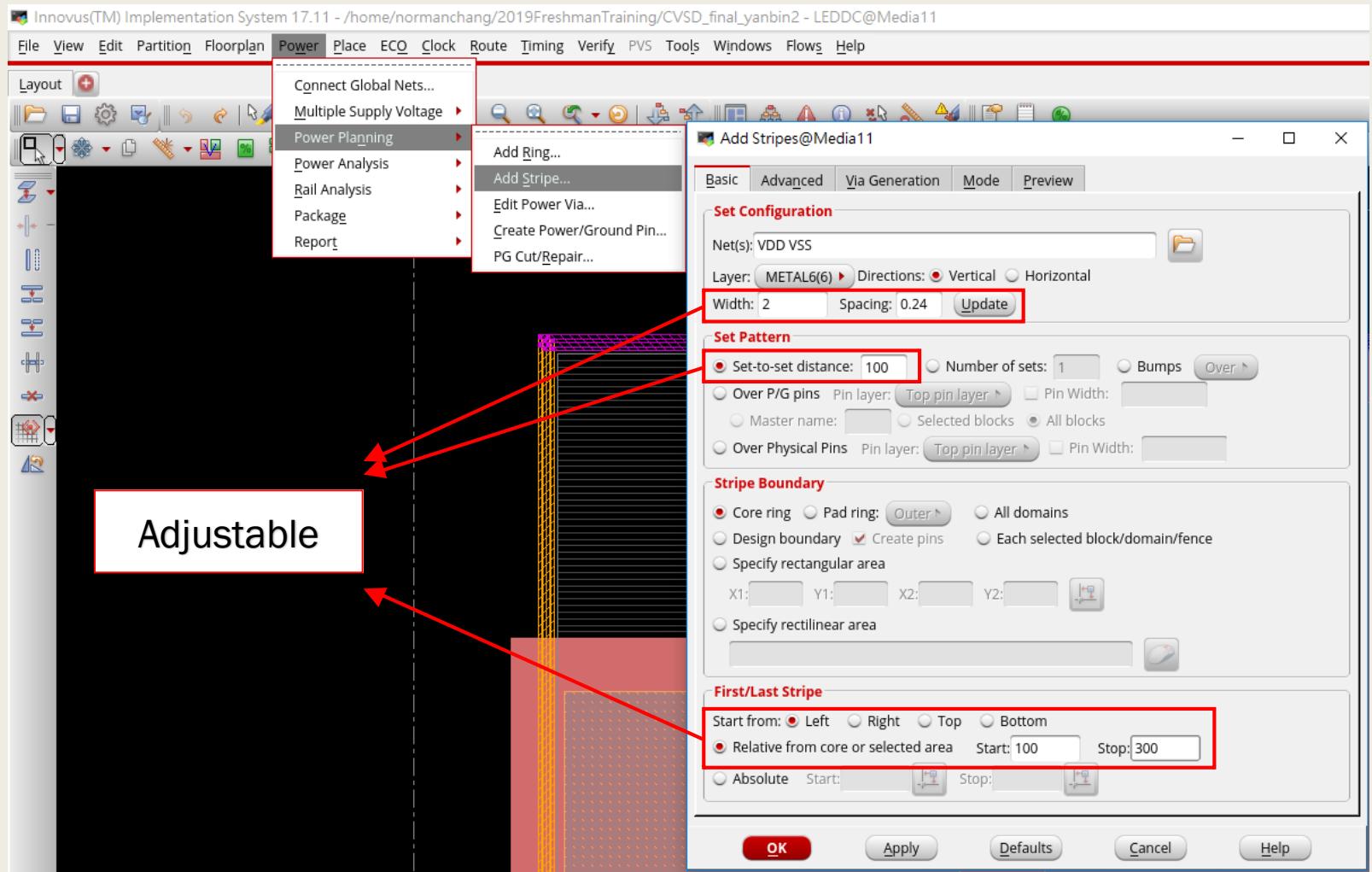
- 3. Add stripe
- Why?
 - *The deeper part of your design may not have enough power from power ring, so you need to add stripe to boost the voltage.*
 - *Vertical stripe is recommended.*

Power Plan

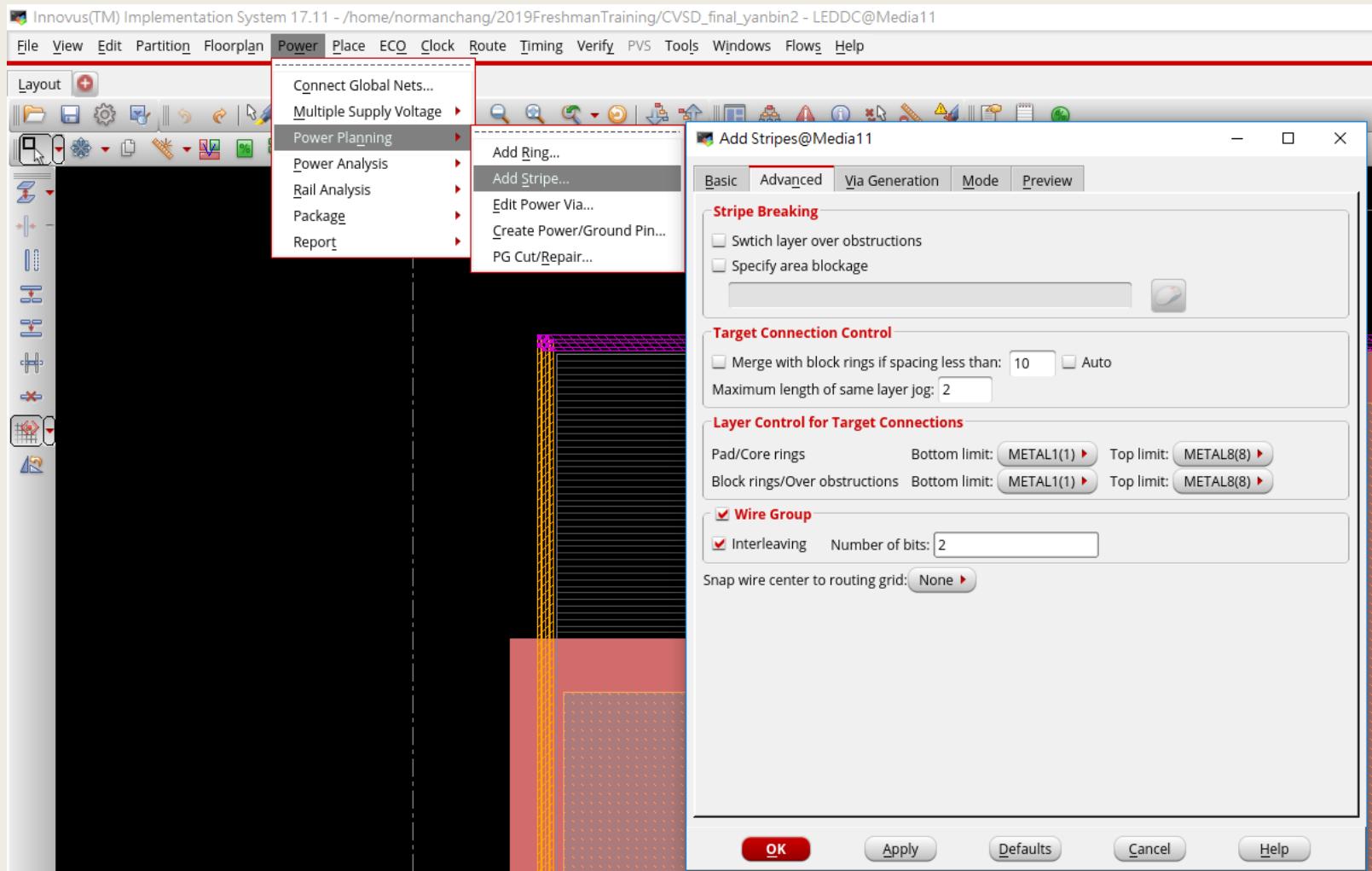
- Power → Power Planning → Add Stripe → Basic
 - Nets: VDD VSS
 - Layers: METAL6 and select *Vertical*; METAL7 and select *Horizontal*
 - Set Width to 2(adjustable) and click Update
 - In Set Pattern, select *Set-to-set distance* and input 100(adjustable)
 - In First/Last stripe: select *Left* or *Right* if use Vertical; select *Top* or *Bottom* if use horizontal;
 - Select *Relative from core or selected area*
 - Start: adjustable; Stop: adjustable
- Change to Advanced
 - Select *Wire Group*
 - Select *Interleaving*, and set Number of Bits to 2
- Click Apply to see the result. If it's ok, then click OK to confirm.

Power Plan

In figure:

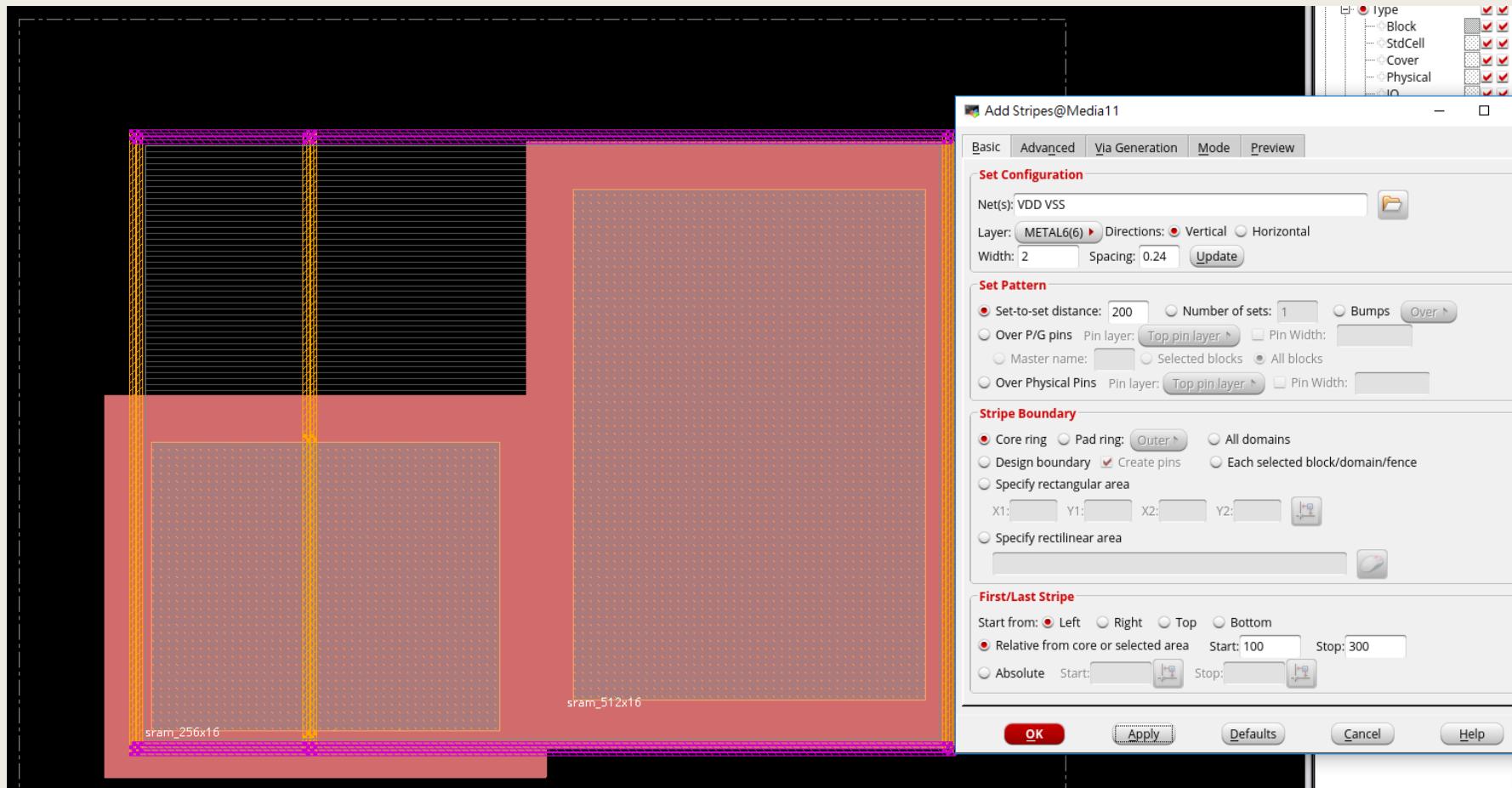


Power Plan



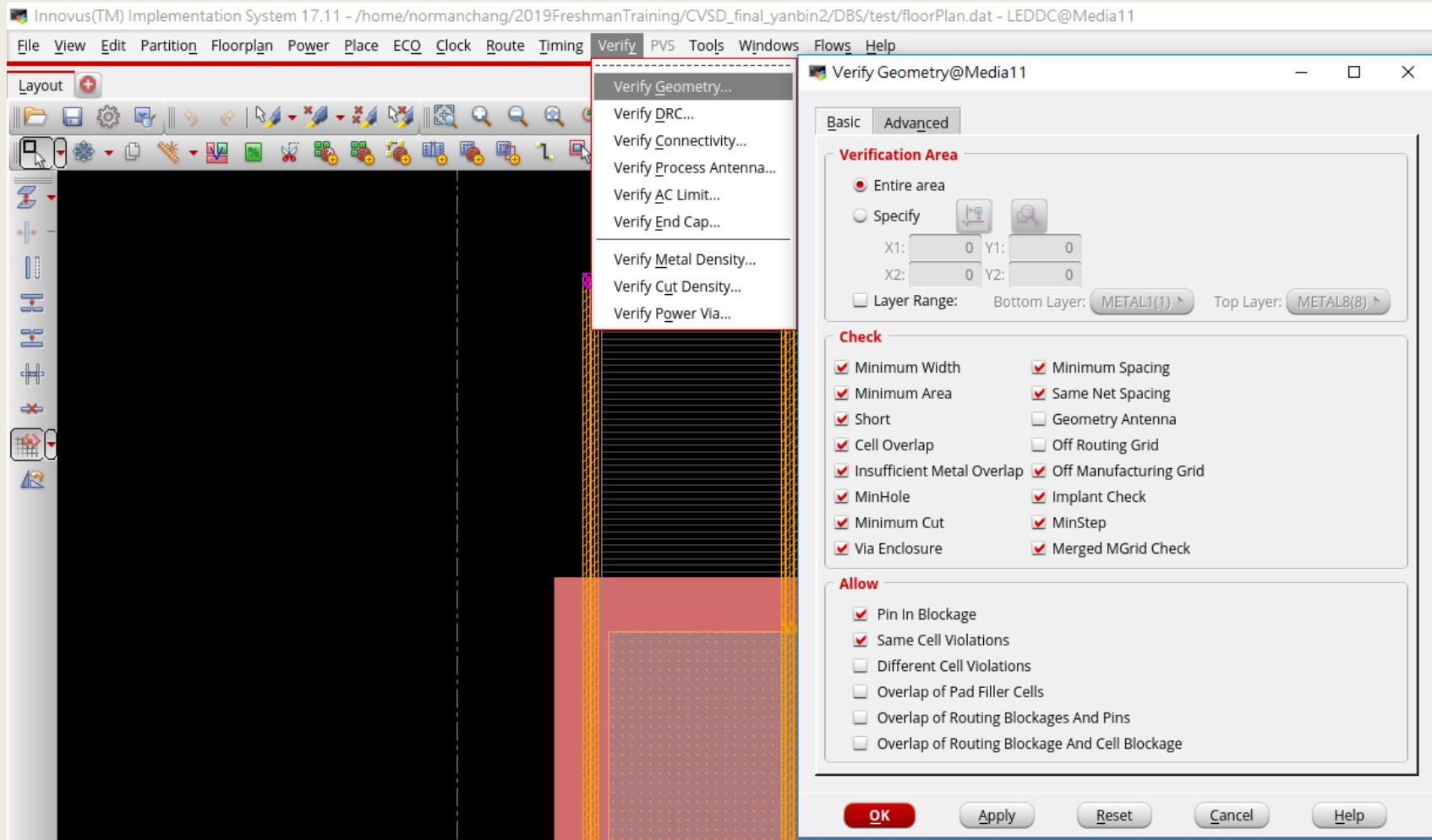
Power Plan

- Different setting:



Power Plan

- 4. Verify → Verify Geometry ... → OK



Power Plan

- To check is there any violation, i.e. Design Rule Check(DRC).

```
innovus 94> *** Starting Verify Geometry (MEM: 1490.6) ***

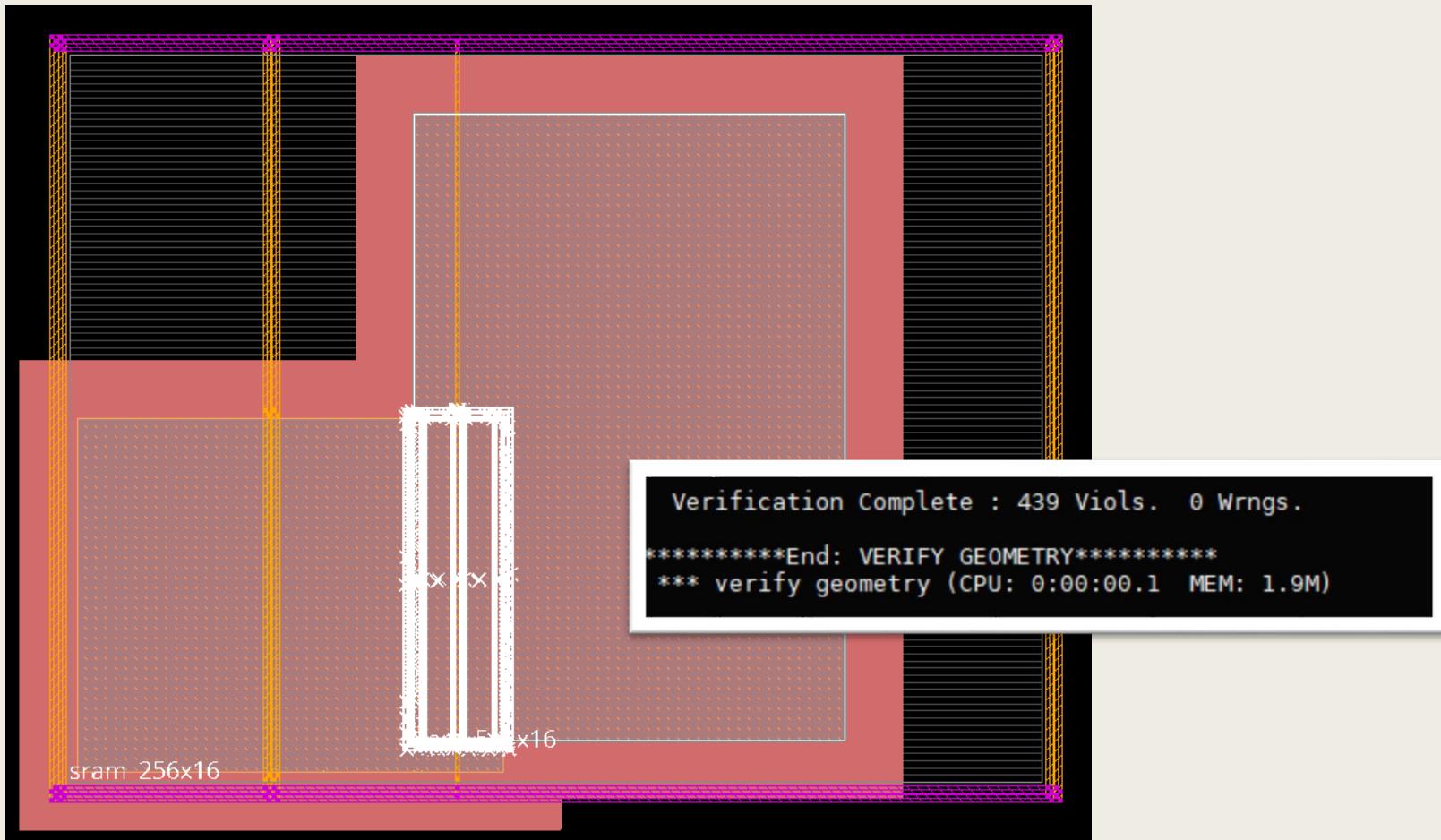
**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works
in this release but will be removed in future release. Please update your script to use the new
command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 8320
**WARN: (IMPVFG-198): Area to be verified is small to see any runtime gain from multi-cpus. Us
e setMultiCpuUsage command to adjust the number of CPUs.
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 87.0M)

innovus 94> █
```

Power Plan

- There should not have any X on the window.
- For example, if someone retarded overlap two modules...



Power Plan

- 4. Save file: File → Save Design... → *Innovus: DBS/powerplan*

Outline

- Introduction
- Initial step
- Floor plan
- Power plan
- Power route**
- Placement
- CTS
- Route
- Post processing
- Post-layout simulation
- Reference

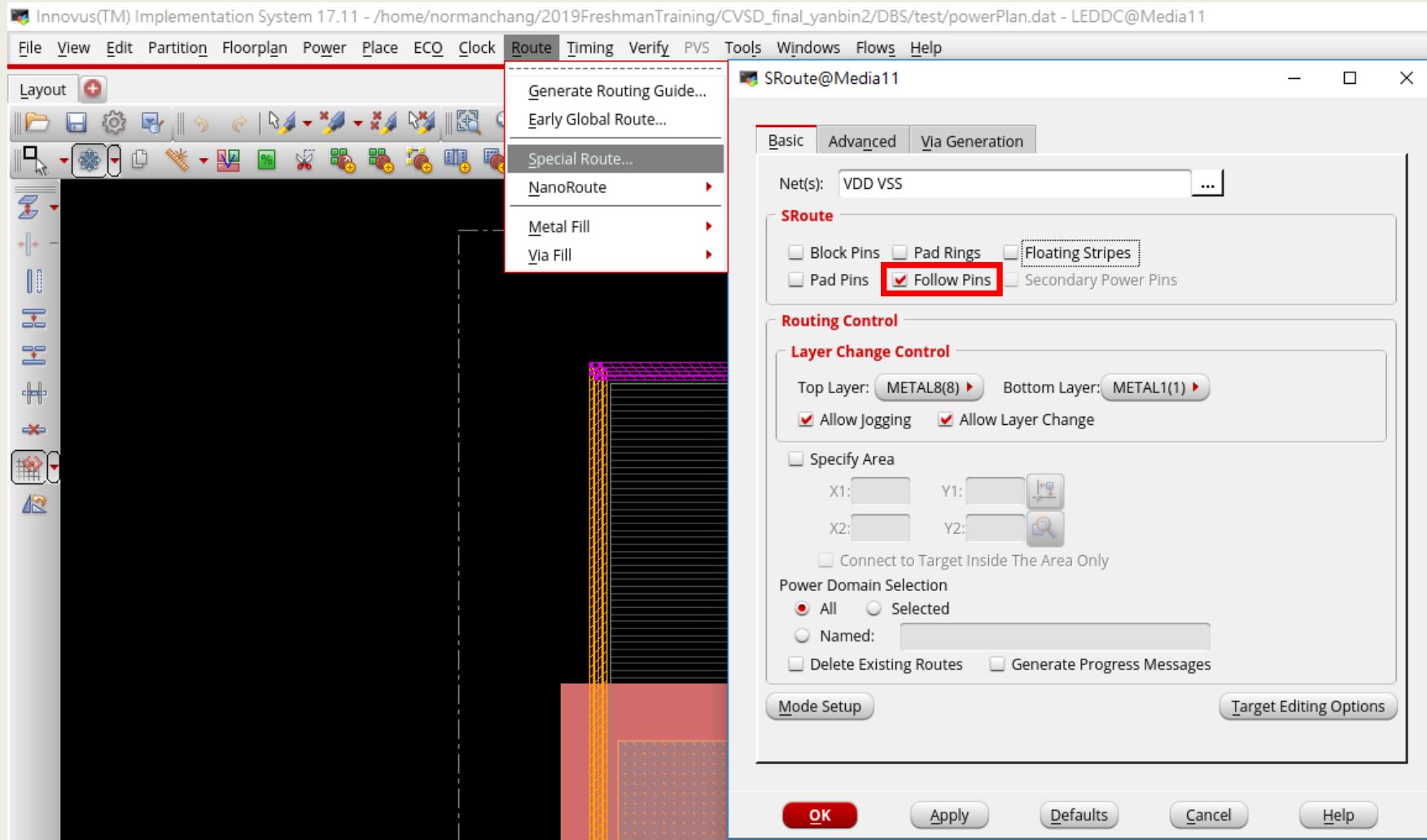
Power Route

- What's power route?
 - *Connect all cell to power ring*

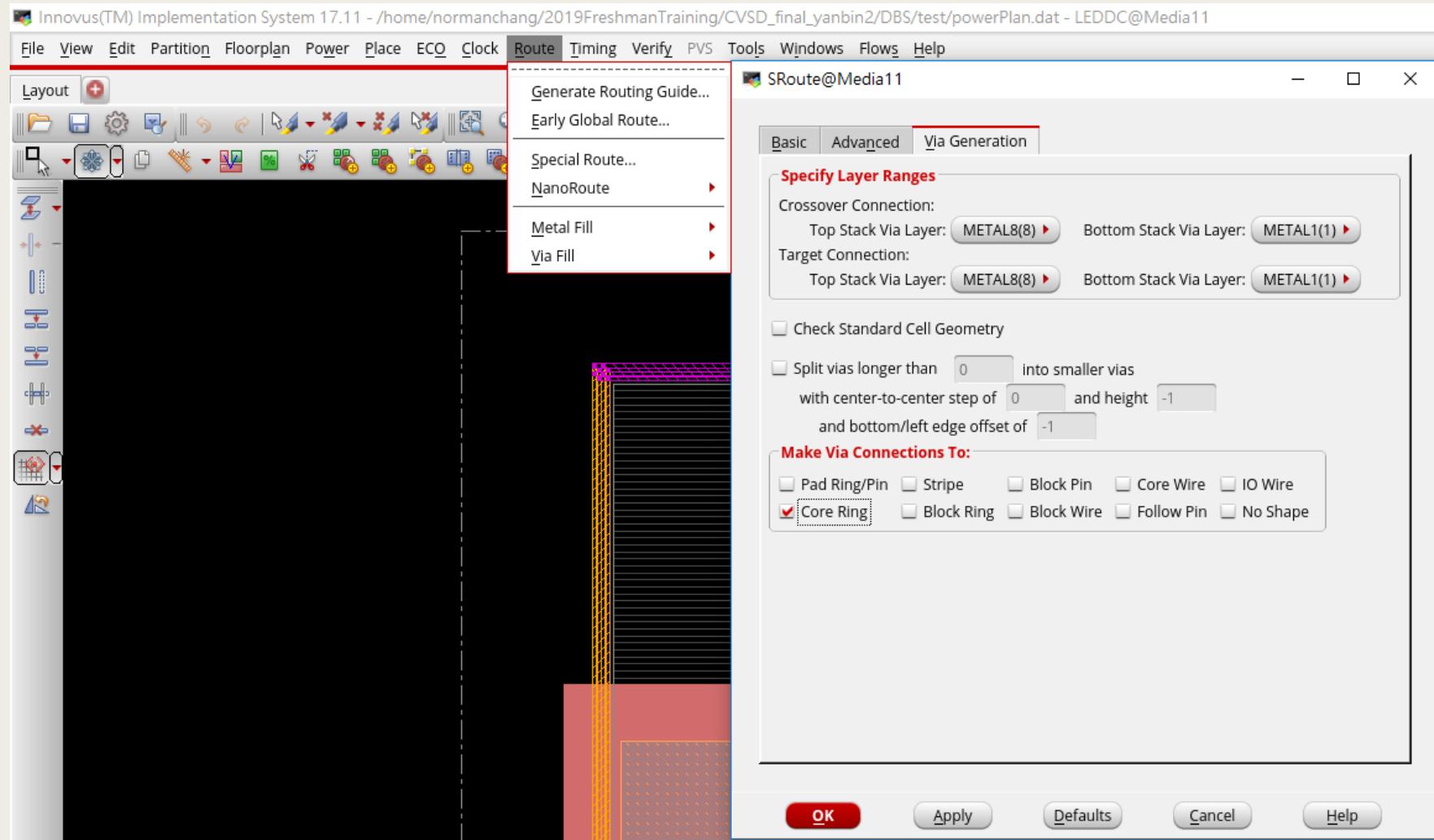
Power Route

- 1.Route → Special Route → Basic
 - Net(s): VDD VSS
 - In SRoute, only select *Follow Pins*
- Change to Via Generation
 - In Make Via Connection To, only select *Core Ring*
- Click OK.

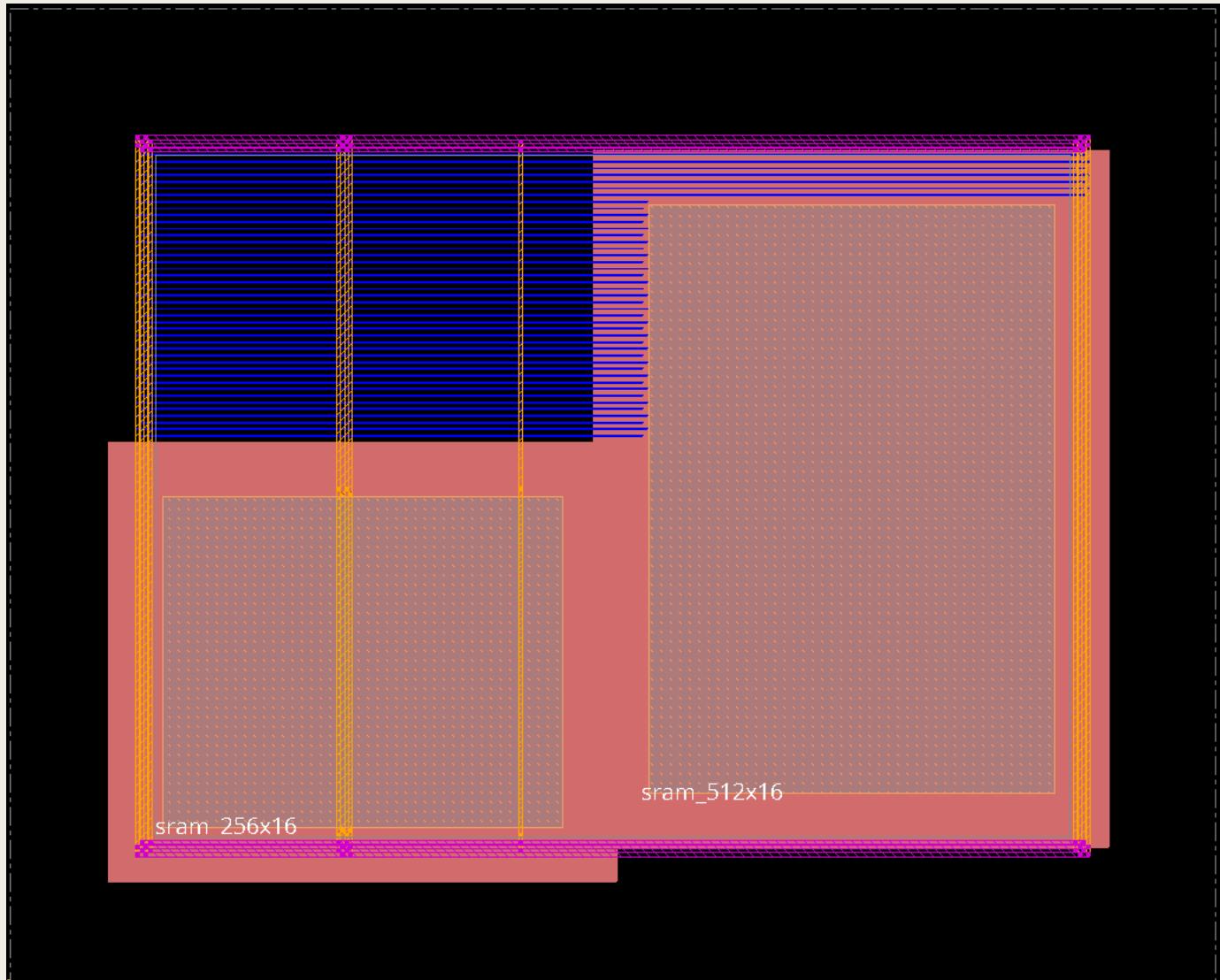
Power Route



Power Route

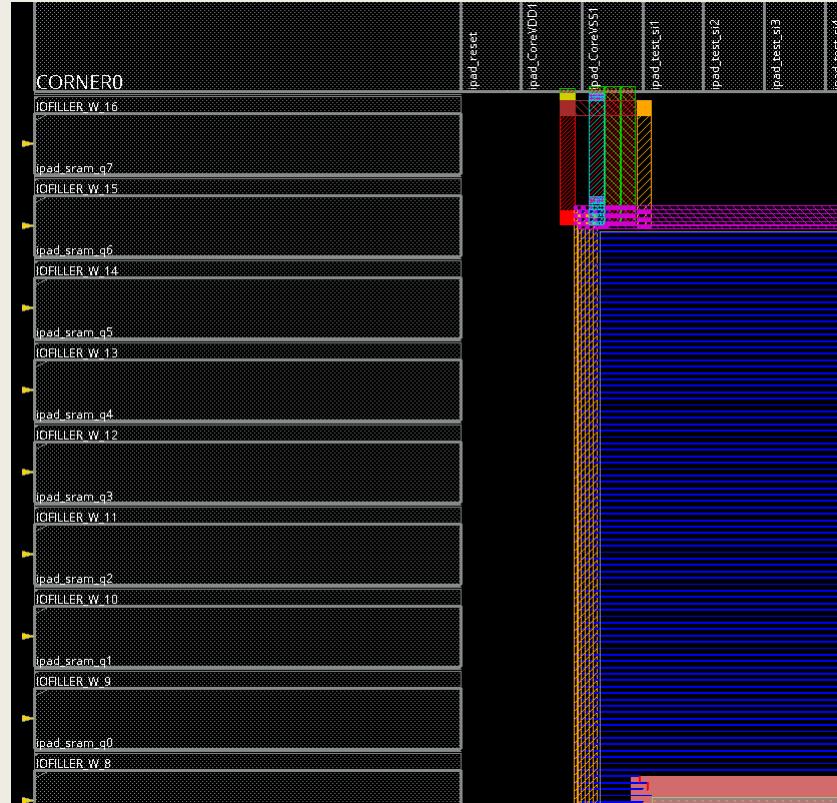
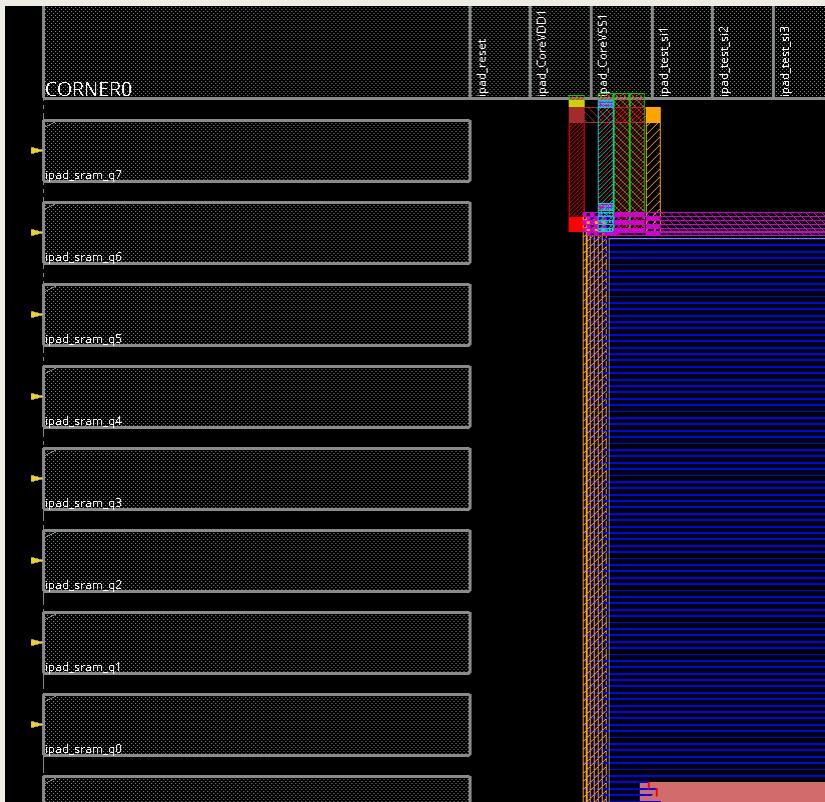


Power Route



Power Route

- 2. (Optional) Add IO Filler
 - Why?
 - *To fill the empty space of IO pad.*



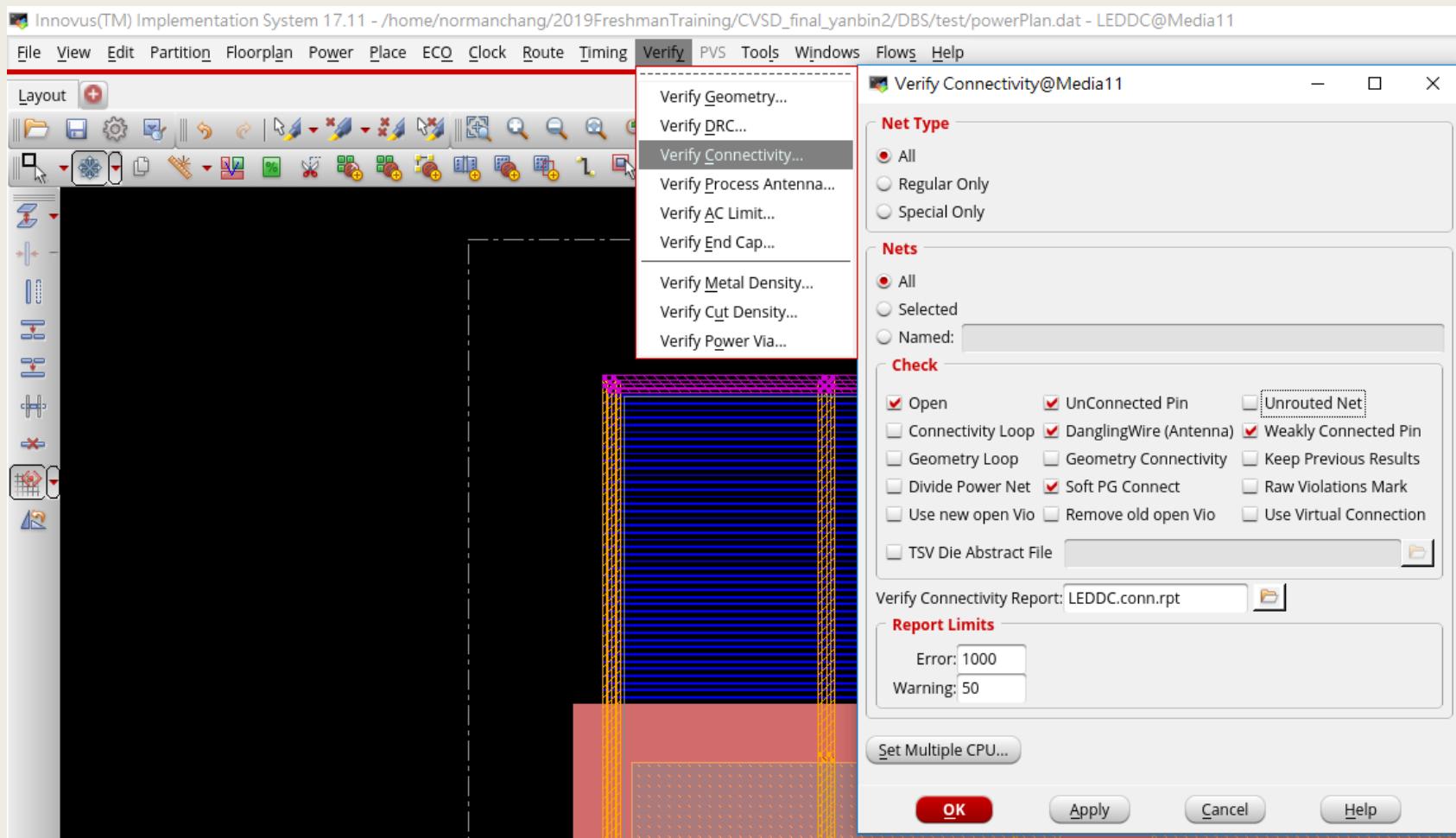
Power Route

- innovus > source addIoFiller_tpz.cmd

```
innovus 76> source addIoFiller_tpz.cmd
**WARN: (IMPFP-127): Incorrect LEF/OA class of cell 'PFEED20Z', expected cell with class 'PAD SPACER'.
Added 0 of filler cell 'PFEED20Z' on top side.
Added 0 of filler cell 'PFEED20Z' on left side.
Added 0 of filler cell 'PFEED20Z' on bottom side.
Added 0 of filler cell 'PFEED20Z' on right side.
**WARN: (IMPFP-127): Incorrect LEF/OA class of cell 'PFEED10Z', expected cell with class 'PAD SPACER'.
Added 0 of filler cell 'PFEED10Z' on top side.
Added 17 of filler cell 'PFEED10Z' on left side.
Added 12 of filler cell 'PFEED10Z' on bottom side.
Added 0 of filler cell 'PFEED10Z' on right side.
**WARN: (IMPFP-127): Incorrect LEF/OA class of cell 'PFEED5Z', expected cell with class 'PAD SPACER'.
Added 0 of filler cell 'PFEED5Z' on top side.
Added 0 of filler cell 'PFEED5Z' on left side.
Added 0 of filler cell 'PFEED5Z' on bottom side.
Added 0 of filler cell 'PFEED5Z' on right side.
**WARN: (IMPFP-127): Incorrect LEF/OA class of cell 'PFEED1Z', expected cell with class 'PAD SPACER'.
Added 0 of filler cell 'PFEED1Z' on top side.
Added 34 of filler cell 'PFEED1Z' on left side.
Added 12 of filler cell 'PFEED1Z' on bottom side.
Added 0 of filler cell 'PFEED1Z' on right side.
**WARN: (IMPFP-127): Incorrect LEF/OA class of cell 'PFEED0_1Z', expected cell with class 'PAD SPACER'.
Added 0 of filler cell 'PFEED0_1Z' on top side.
Added 51 of filler cell 'PFEED0_1Z' on left side.
Added 72 of filler cell 'PFEED0_1Z' on bottom side.
Added 0 of filler cell 'PFEED0_1Z' on right side.
**WARN: (IMPFP-127): Incorrect LEF/OA class of cell 'PFEED0_01Z', expected cell with class 'PAD SPACER'.
Added 0 of filler cell 'PFEED0_01Z' on top side.
Added 85 of filler cell 'PFEED0_01Z' on left side.
Added 76 of filler cell 'PFEED0_01Z' on bottom side.
Added 0 of filler cell 'PFEED0_01Z' on right side.
**WARN: (IMPFP-127): Incorrect LEF/OA class of cell 'PFEED0_005Z', expected cell with class 'PAD SPACER'.
Added 0 of filler cell 'PFEED0_005Z' on top side.
Added 10 of filler cell 'PFEED0_005Z' on left side.
Added 8 of filler cell 'PFEED0_005Z' on bottom side.
Added 0 of filler cell 'PFEED0_005Z' on right side.
innovus 77> ■
```

Power Route

- 3. Verify → Verify Connectivity...
 - In Check, un-choose *Unrouted Net*



Power Route

- There should not have any violation and X on the screen.

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Mon Jul  8 16:19:13 2019

Design Name: LEDDC
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (664.2400, 537.1000)
Error Limit = 1000; Warning Limit = 50
Check all nets
Use 7 pthreads

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Mon Jul  8 16:19:13 2019
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 8.000M)
```

Power Route

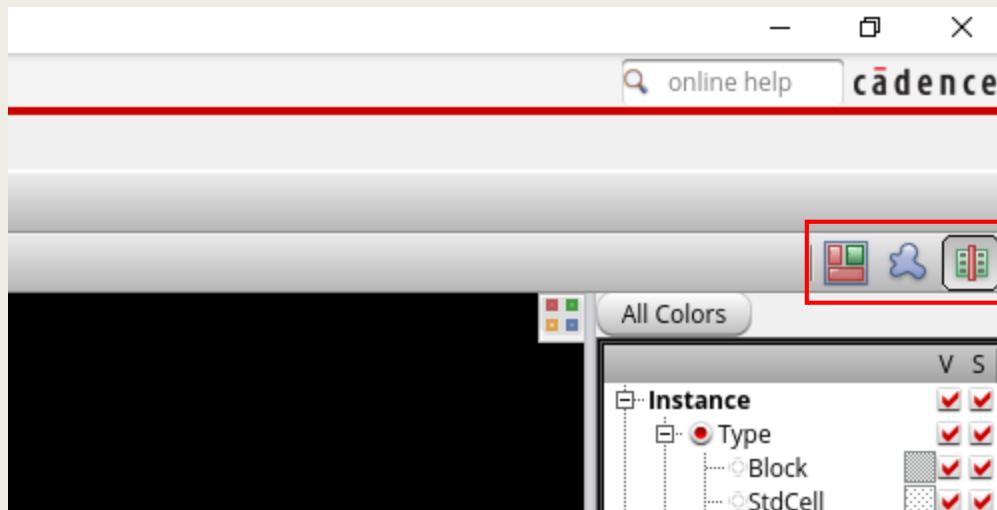
- 4. Verify geometry again
 - Verify → Verify Geometry ... → OK
- 5. Save file: File → Save Design... → *Innovus: DBS/powerroute*

Outline

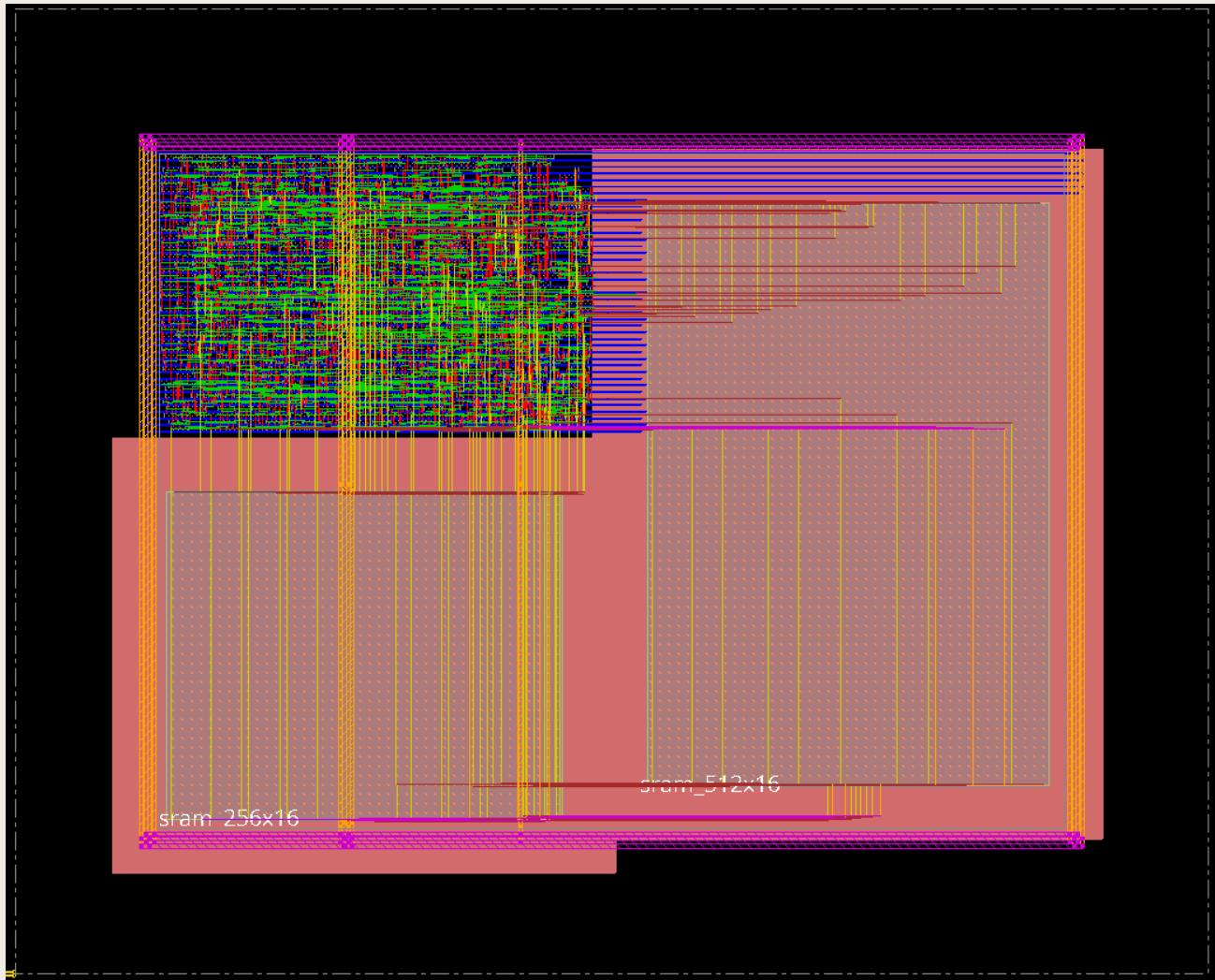
- Introduction
- Initial step
- Floor plan
- Power plan
- Power route
- Placement**
- CTS
- Route
- Post processing
- Post-layout simulation
- Reference

Placement

- In this stage, we are going to place all standard cells.
- 1. In Innovus command line:
 - Innovus > createBasicPathGroups –expanded
 - Innovus > get_path_groups
 - Innovus > place_opt_design
- After the processing has finished, change to Physical View to see how the cells are placed.

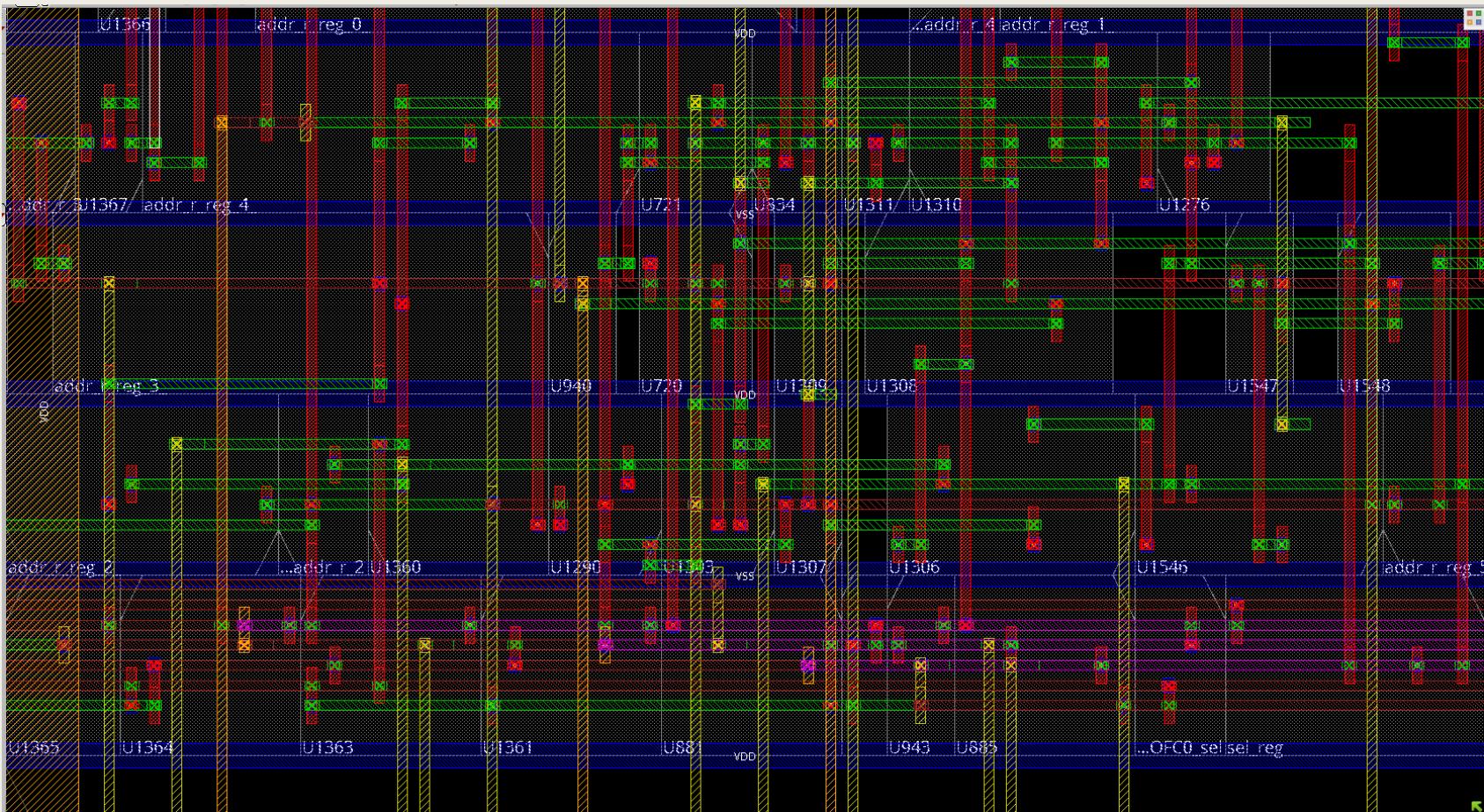


Placement



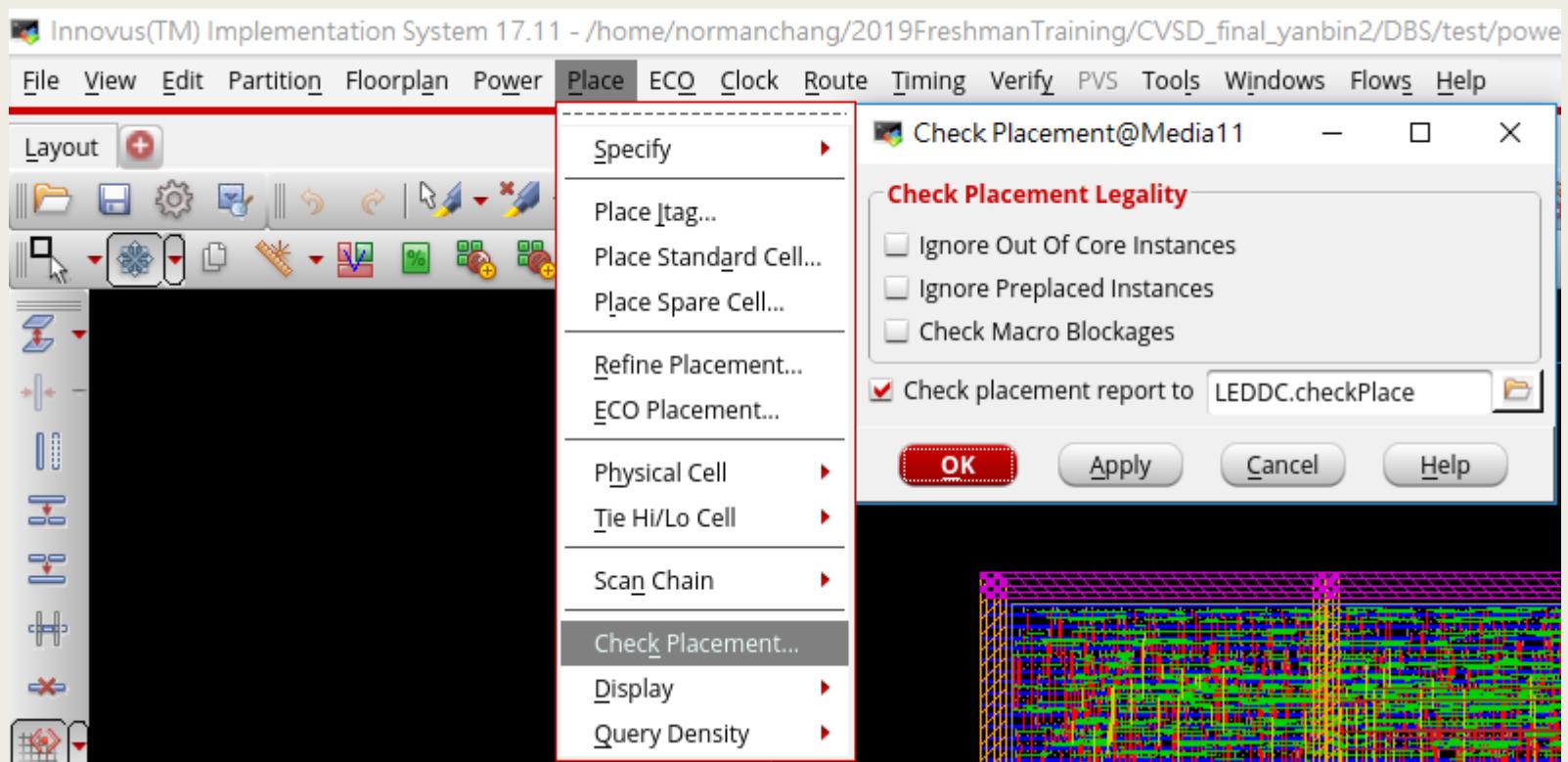
Placement

- A closet view



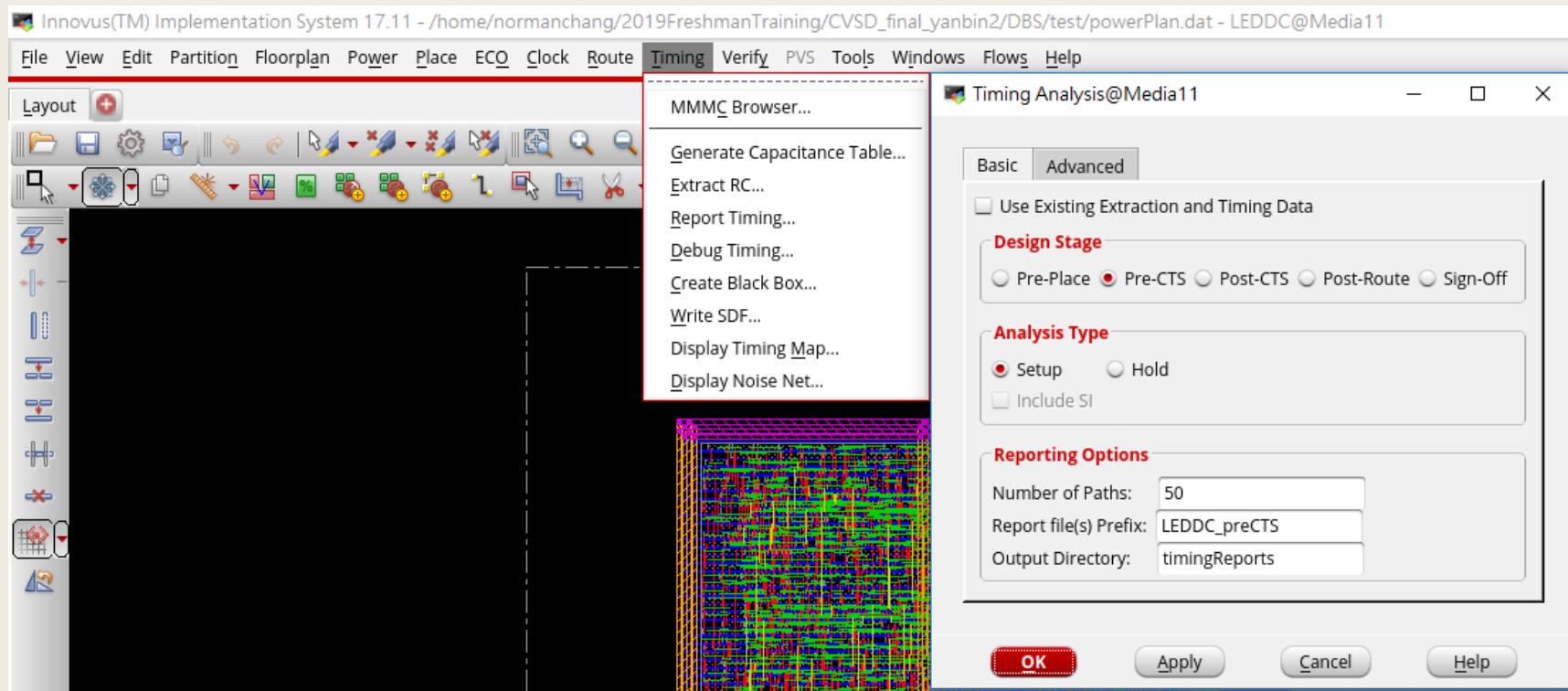
Placement

- 2. We still need to check whether the placement is ok or not.
- Place → Check Placement... → OK
 - *If the placement is ok, there should not have X on the screen.*



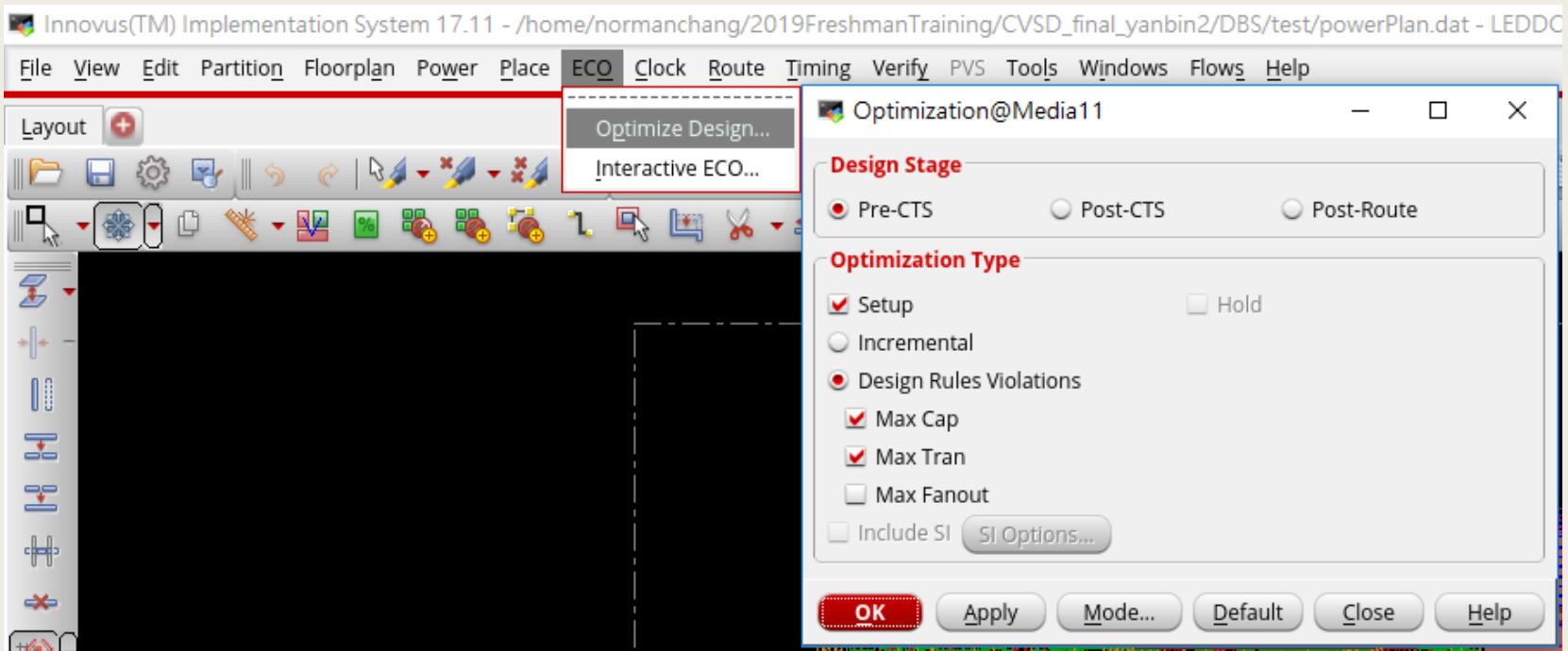
Placement

- 3. Check if there is any timing violation
- Timing → Report Timing → *Pre-CTS* → *Setup* → OK



Placement

- Your WNS should greater or equal to 0.
- If not: ECO → Optimize Design... → *Pre-CTS* → *Setup* → OK
- Do this step until the WNS is greater or equal to 0.
- If it always fails, go back to floorplan stage and change something like ration or utilize, or shift modules a little.



Placement

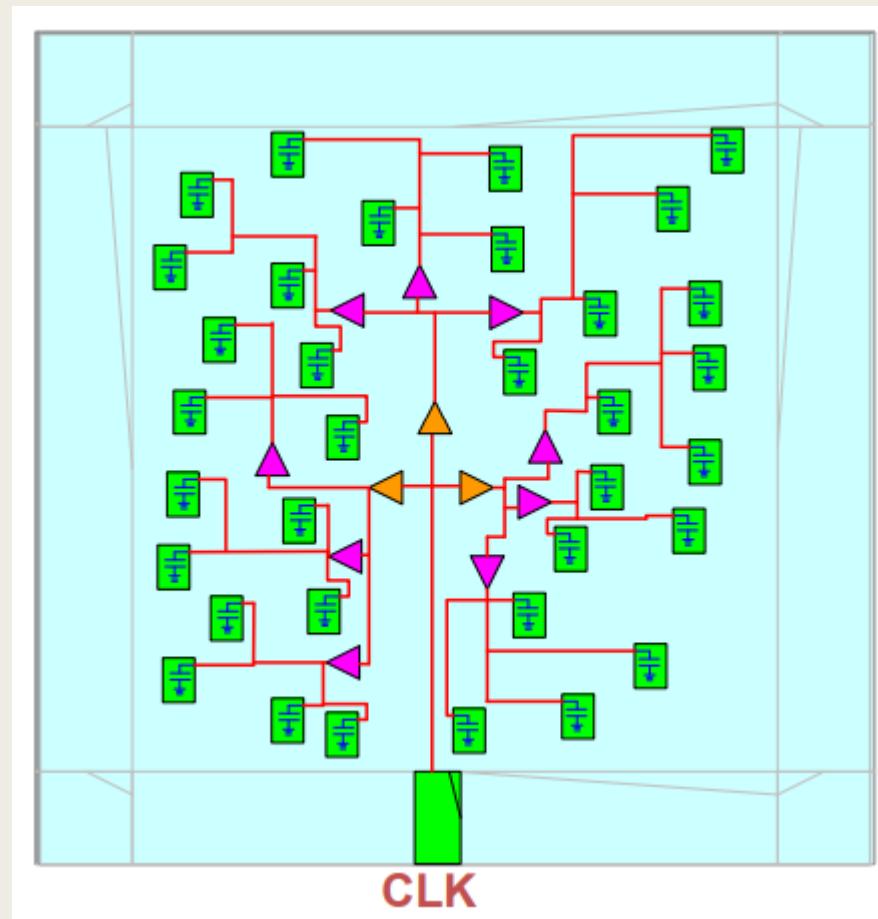
- 4. Save file: File → Save Design... → *Innovus: DBS/place*

Outline

- Introduction
- Initial step
- Floor plan
- Power plan
- Power route
- Placement
- CTS**
- Route
- Post processing
- Post-layout simulation
- Reference

Clock Tree Synthesis

- Clock Tree Synthesis, CTS:
 - *Create clock*



Clock Tree Synthesis

- 1. Before starting, we need to remove the latency part in origin sdc file
 - *Because we're going to use real clock, we don't need the simulation anymore.*
- Delete the latency and uncertainty in origin sdc file, and store it as a new file named ***your_ori_sdc_name_cts.sdc***.

```
final.tcl | tel_innovus.tcl | mmnc_view | LEDCC_EDI.sdc
1 # operating conditions and boundary conditions #
2
3 create_clock -name DCK -period 1300 [get_ports DCK]
4 create_clock -name GCK -period 4.50 [get_ports GCK]
5
6 set_clock_uncertainty 0.1 [all_clocks]
7 set_clock_latency 1.0 [all_clocks]
8
9
10 #Don't touch the basic env setting as below
11 set_input_delay -max 1.0 -clock DCK [remove_from_collection [all_inputs] [get_ports {DCK}]] [get_ports {GCK}]
12 set_input_delay -min 0.0 -clock DCK [remove_from_collection [all_inputs] [get_ports {DCK}]] [get_ports {GCK}]
13 set_input_delay -max 1.0 -clock GCK [get_ports Vsync]
14 set_input_delay -min 0.0 -clock GCK [get_ports Vsync]
15
16 set_output_delay -max 1.0 -clock GCK [get_ports OUT*]
17 set_output_delay -min 0.0 -clock GCK [get_ports OUT*]
18
19 set_load 0.1 [all_outputs]
20 set_drive 0.1 [all_inputs]
21
22 set_operating_conditions -max_library slow -max slow
23 set_max_fanout 6 [all_inputs]
24
25
26 #set_interactive_constraint_modes func_mode
27 set_false_path -from DCK -to GCK
28 set_false_path -from GCK -to DCK
29
```



```
LEDCC_EDI_cts.sdc
1 # operating conditions and boundary conditions #
2
3 create_clock -name DCK -period 1300 [get_ports DCK]
4 create_clock -name GCK -period 4.50 [get_ports GCK]
5
6
7
8
9
10 #Don't touch the basic env setting as below
11 set_input_delay -max 1.0 -clock DCK [remove_from_collection [all_inputs] [get_ports {DCK}]] [get_ports {GCK}]
12 set_input_delay -min 0.0 -clock DCK [remove_from_collection [all_inputs] [get_ports {DCK}]] [get_ports {GCK}]
13 set_input_delay -max 1.0 -clock GCK [get_ports Vsync]
14 set_input_delay -min 0.0 -clock GCK [get_ports Vsync]
15
16 set_output_delay -max 1.0 -clock GCK [get_ports OUT*]
17 set_output_delay -min 0.0 -clock GCK [get_ports OUT*]
18
19 set_load 0.1 [all_outputs]
20 set_drive 0.1 [all_inputs]
21
22 set_operating_conditions -max_library slow -max slow
23 set_max_fanout 6 [all_inputs]
24
25
26 #set_interactive_constraint_modes func_mode
27 set_false_path -from DCK -to GCK
28 set_false_path -from GCK -to DCK
29
```

Clock Tree Synthesis

- 2. In Innovus command line:

- Innovus > update_constraint_mode -name CM_func -sdc_files *your_ori_sdc_name_cts.sdc*

```
innovus 154> update_constraint_mode -name CM_func -sdc_files LEDDC_EDI_cts.sdc
Reading timing constraints file 'LEDDC_EDI_cts.sdc' ...
Current (total cpu=0:32:21, real=4:35:06, peak res=1582.0M, current mem=1267.1M)
**WARN: (TCLCMD-1013): The SDC set_operating_conditions assertion is not supported. Please use the Innovus setOpCond command to
he setAnalysisMode command to control single vs. bestCase/worstCase vs. on-chip variation timing analysis. (File LEDDC_EDI_cts.sdc)

Number of path exceptions in the constraint file = 2
Number of paths exceptions after getting compressed = 2
INFO (CTE): Reading of timing constraints file LEDDC_EDI_cts.sdc completed, with 1 WARNING
Ending "Constraint file reading stats" (total cpu=0:00:00.0, real=0:00:00.0, peak res=1275.5M, current mem=1275.5M)
Current (total cpu=0:32:21, real=4:35:06, peak res=1582.0M, current mem=1275.5M)
innovus 155> █
```

- If you have scan chain, remember to change both sdc file:

- Innovus > update_constraint_mode -name func_mode -sdc_files *your_ori_sdc_name_DC_cts.sdc*
 - Innovus > update_constraint_mode -name scan_mode -sdc_files *your_ori_sdc_name_scan_cts.sdc*

Clock Tree Synthesis

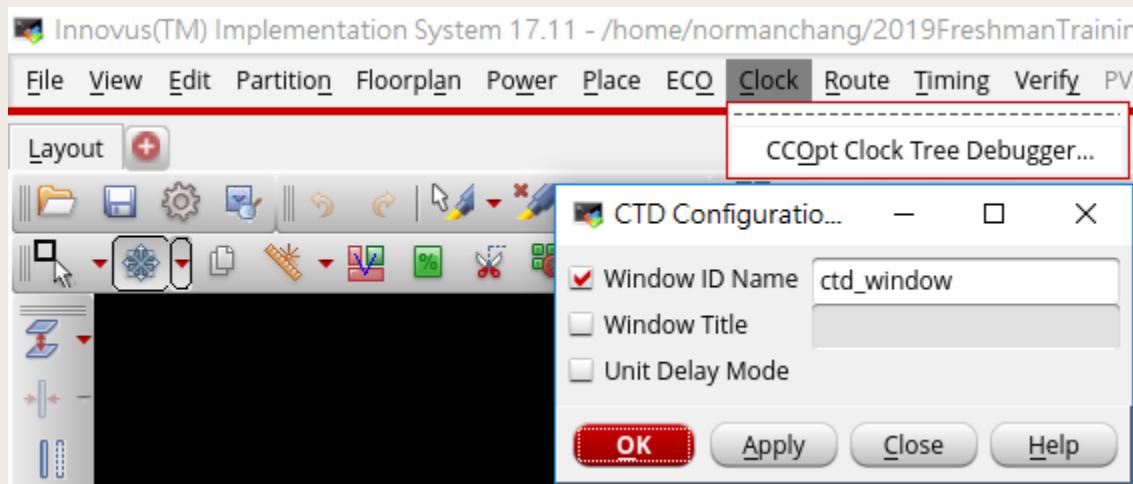
- 3. Create the spec file of CT and start CTS
- In Innovus command line:
 - Innovus > create_ccopt_clock_tree_spec -file ./copt.spec
 - Innovus > source ./ccopt.spec
 - Innovus > ccopt_design -cts
- Result

```
Logging CTS constraint violations...
No violations found.
Logging CTS constraint violations done.
Tidy Up And Update Timing done. (took cpu=0:00:00.6 real=0:00:00.2)
Runtime done. (took cpu=0:00:14.9 real=0:00:09.3)
Runtime Summary
=====
Clock Runtime: (58%) Core CTS          5.36 (Init 1.09, Construction 2.69, Implementation 0.86, eGRPC 0.40, PostConditioning 0.13, Other 0.20)
Clock Runtime: (39%) CTS services      3.64 (RefinePlace 0.23, EarlyGlobalClock 0.28, NanoRoute 2.82, ExtractRC 0.07, TimingAnalysis 0.25)
Clock Runtime: (2%) Other CTS          0.23 (Init 0.10, CongRepair 0.13)
Clock Runtime: (100%) Total            9.23

Synthesizing clock trees with CCOpt done.
**WARN: (IMPSP-9025): No scan chain specified/traced.
Type 'man IMPSP-9025' for more detail.
% End ccopt_design (date=07/08 17:48:07, total cpu=0:00:14.9, real=0:00:10.0, peak res=1627.3M, current mem=1528.4M)
innovus 158> █
```

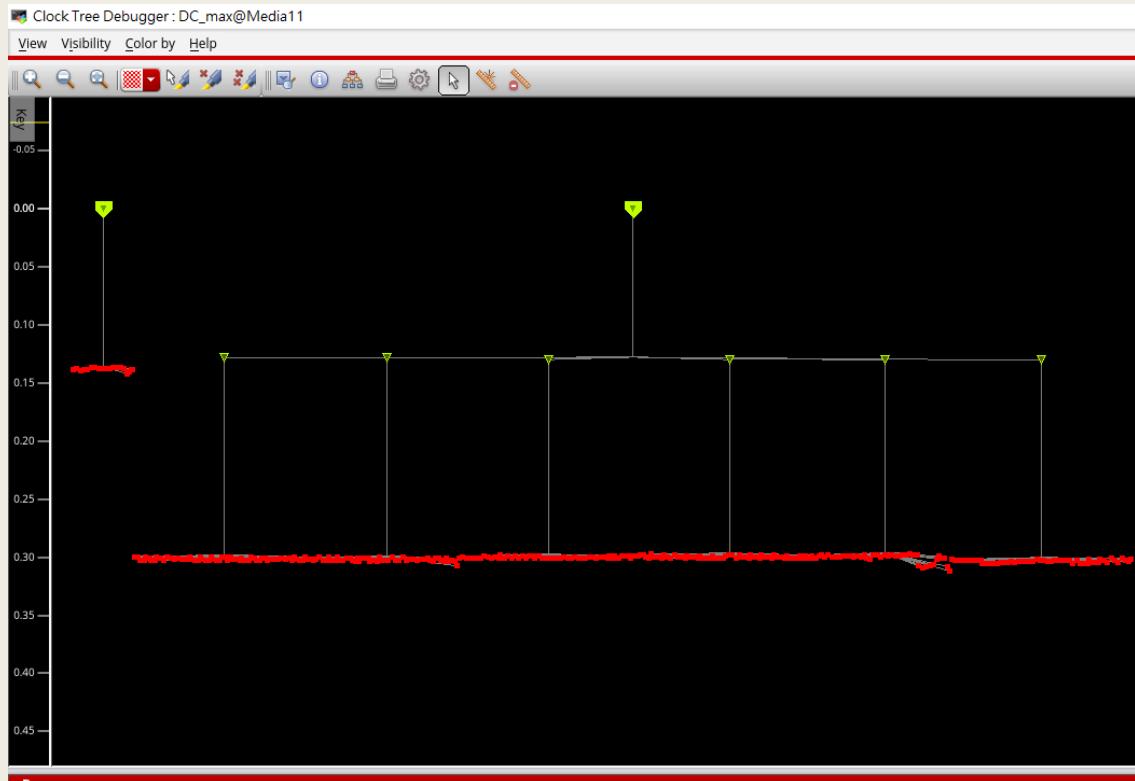
Clock Tree Synthesis

- 4. (Optional) See how well is the CTS result
- Clock → CCOpt Clock Tree Debugger... → OK



Clock Tree Synthesis

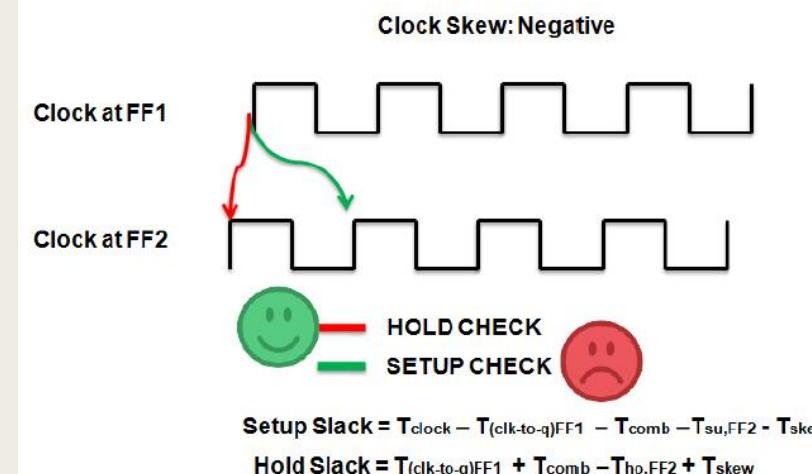
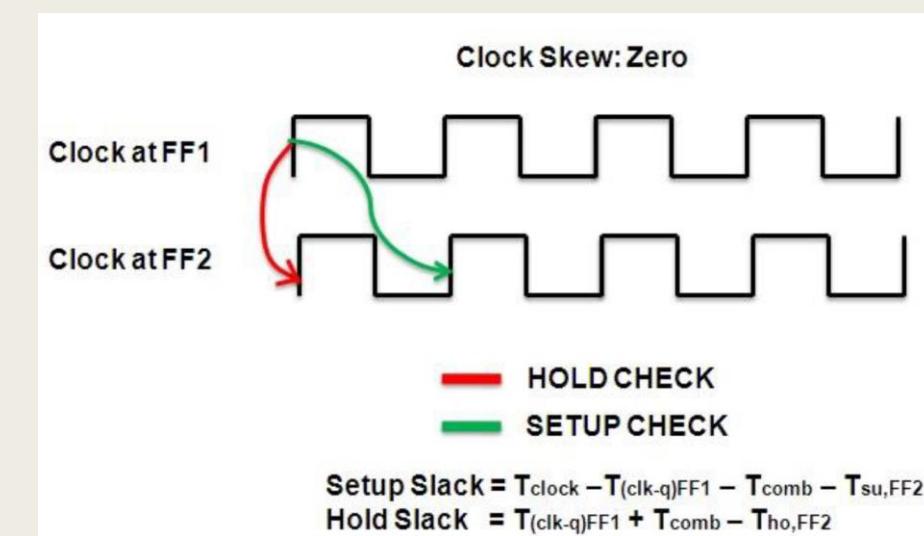
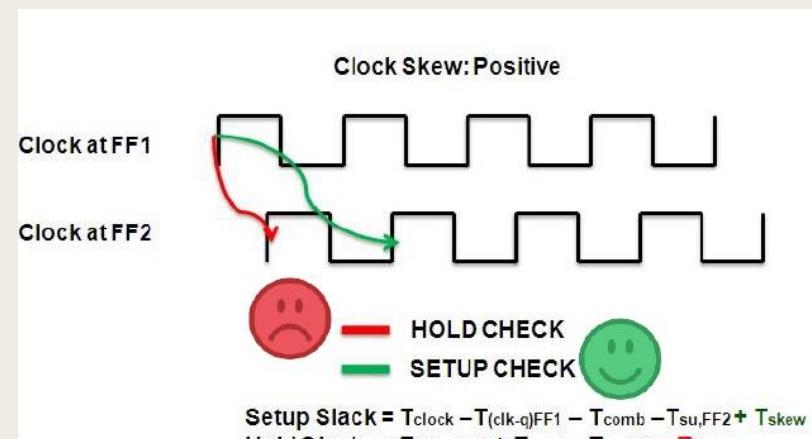
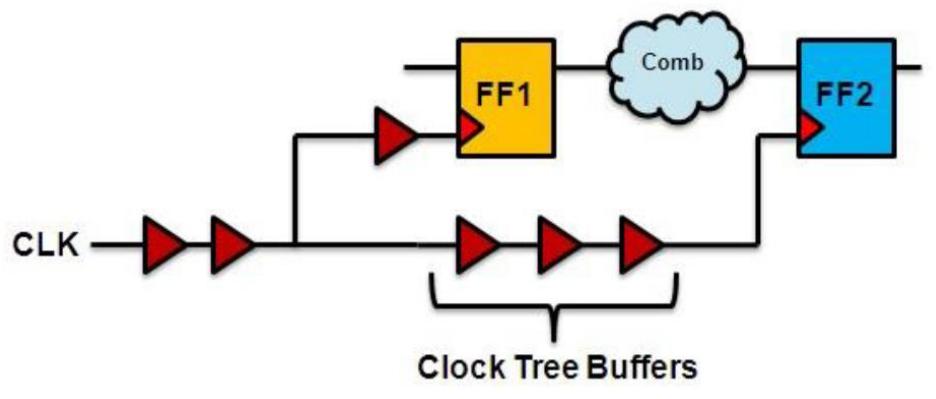
- Let's see our clock.



Analysis View	Skew Group	Skew	Min Delay	Max Delay	Min Pin	MinPath Level	Max Pin	MaxPath Level
DC_max:hold.early	DCK/CM_func	0.006	0.136	0.142	data_reg_5_/CK	3 ...m_256x16/CLKB		
	GCK/CM_func	0.015	0.296	0.311	...reg_15_0_/CK	4 ...m_512x16/CLKA		
DC_max:hold.late	DCK/CM_func	0.006	0.136	0.142	data_reg_5_/CK	3 ...m_256x16/CLKB		
	GCK/CM_func	0.015	0.296	0.311	...reg_15_0_/CK	4 ...m_512x16/CLKA		
DC_max:setup.early	DCK/CM_func	0.006	0.136	0.142	data_reg_5_/CK	3 ...m_256x16/CLKB		
	GCK/CM_func	0.015	0.296	0.311	...reg_15_0_/CK	4 ...m_512x16/CLKA		
DC_max:setup.late	DCK/CM_func	0.006	0.136	0.142	data_reg_5_/CK	3 ...m_256x16/CLKB		
	GCK/CM_func	0.015	0.296	0.311	...reg_15_0_/CK	4 ...m_512x16/CLKA		

Clock Tree Synthesis

- What's clock skew?.



Clock Tree Synthesis

- 5. Save file: File → Save Design... → *Innovus: DBS/cts*
- 6. Check both setup and hold time:
 - Timing → Report Timing → Post-CTS → Setup → OK
 - Timing → Report Timing → Post-CTS → Hold → OK
- If the WNS is negative, use ECO:
 - ECO → Optimize Design... → Post-CTS → Setup → OK
 - ECO → Optimize Design... → Post-CTS → Hold → OK
- You can ECO both at same time.
- 7. Save file: File → Save Design... → *Innovus: DBS/ctsinc*

Outline

- Introduction
- Initial step
- Floor plan
- Power plan
- Power route
- CTS
- Route
 - Post processing
 - Post-layout simulation
 - Reference

Route

- Now, we're going to route our design.
- *Time to verify your bloodline.*

Route

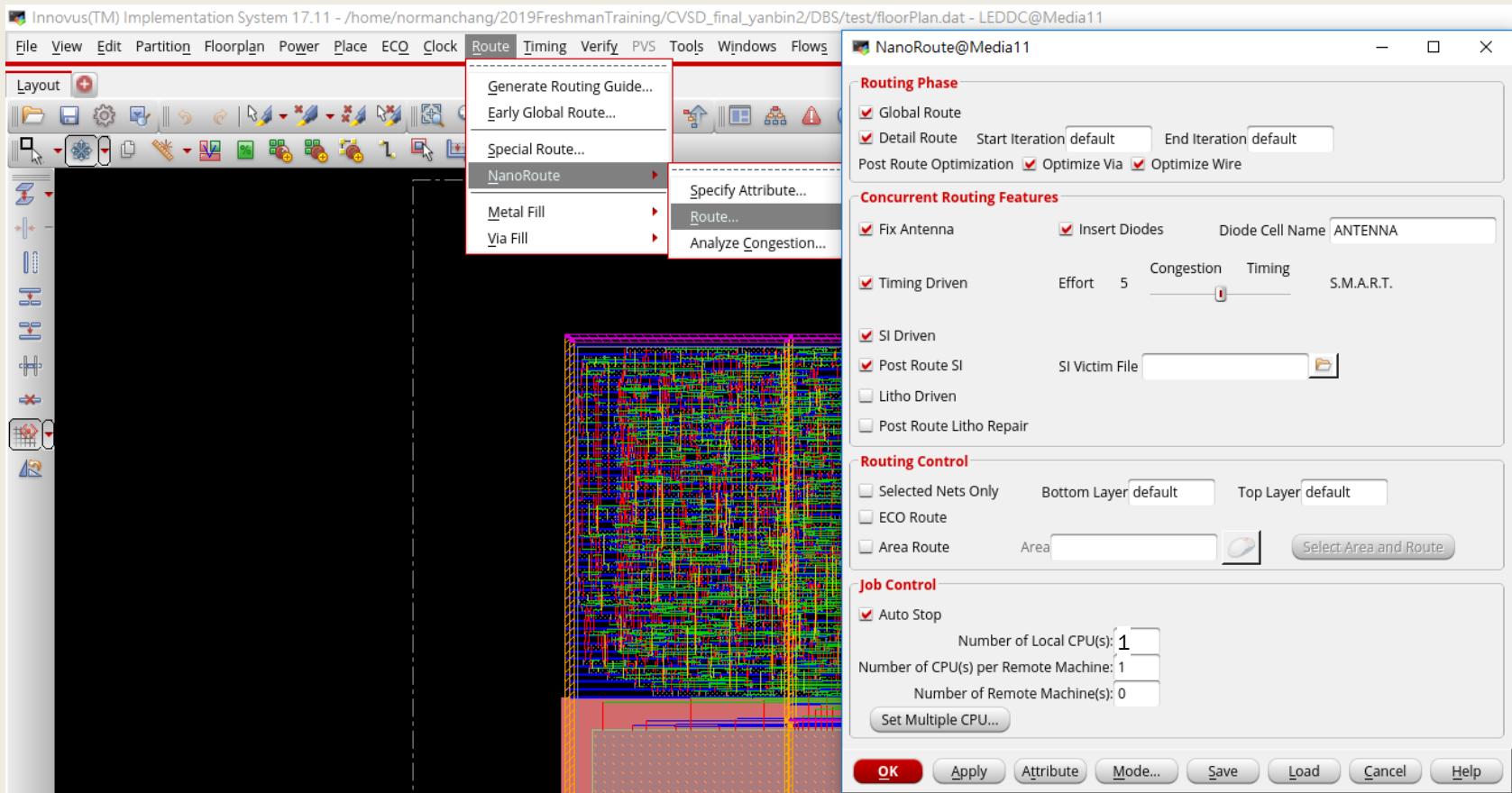
- 1. Add Tie-High Tie-Low:
 - *To connect 1'b0 to VSS and 1'b1 to VDD*
- In innovus command line:
 - Innovus > addTieHiLo -cell {TIEHI TIEL0} -prefix LTIE

```
innovus 164> addTieHiLo -cell {TIEHI TIEL0} -prefix LTIE
Options: No distance constraint, No Fan-out constraint.
Re-routed 18 nets
INFO: Total Number of Tie Cells (TIEHI) placed: 1
INFO: Total Number of Tie Cells (TIEL0) placed: 0
innovus 165> █
```

Route

- 2. Start routing:
- Route → NanoRoute → Route...
 - In Routing Phase, select *Optimize Via & Optimize Wire*
 - In Concurrent Routing Features, select *Insert Diodes* and type ANTENNA at Diode Cell Name
 - Select *Timing Driven, SI Driven, and Post Route SI*
 - Click OK
 - Pray for god.

Route



Route

- Next, be grateful and check timing violation. ~~If God permit, you may not have any violation.~~
- 3. See if there is any white X on the screen. If there is, redo the previous flow again. (Detail order is shown in next page.)
- 4. Check timing
- In Innovus command line:
 - Innovus > setAnalysisMode -analysisType onChipVariation
 - Timing → Report Timing → *Post-route* → *Setup* → OK
 - Timing → Report Timing → *Post-route* → *Hold* → OK
- If the WNS is negative, use ECO:
 - ECO → Optimize Design... → *Post-route* → *Setup* → OK
 - ECO → Optimize Design... → *Post-route* → *Hold* → OK
 - You can choose *Max Fanout* when ECO hold time.

Route

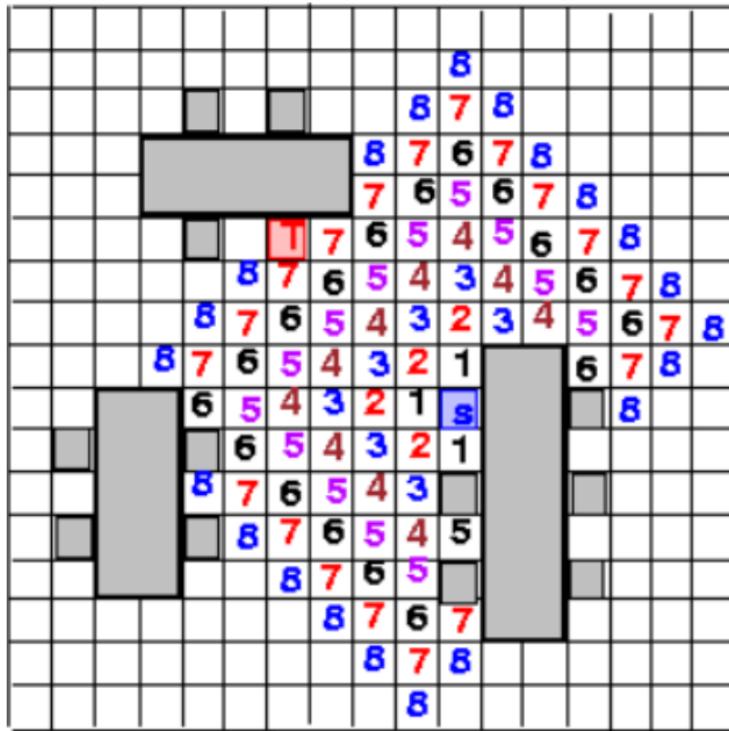
- If you still fail after ECO many times...~~(God discard you)~~
- Load file to re-route → re-place → re-initial → Change RTL
(The order of the file you should load if you always finally fail at routing stage)

Route

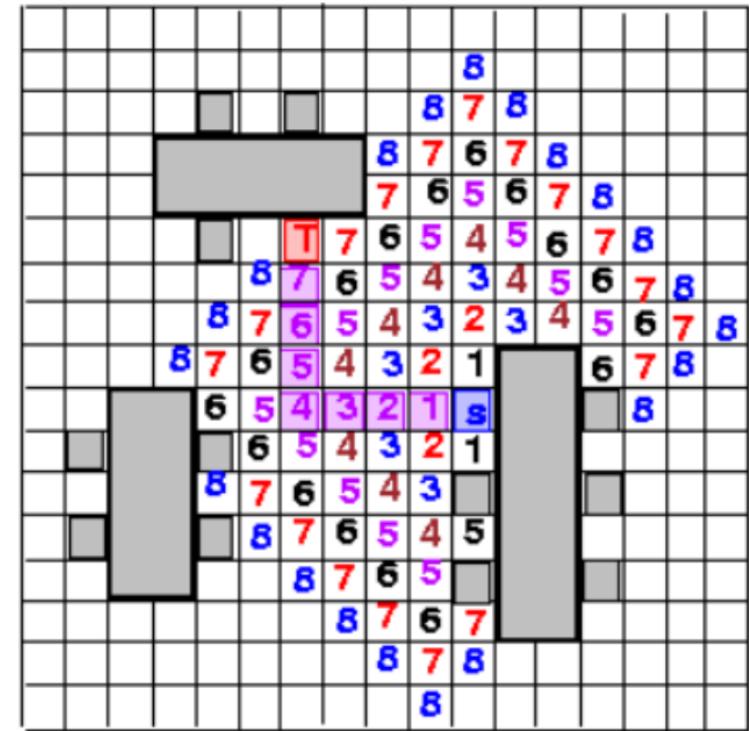
- 5. If timing of your design is fine, save your file first
 - *Save file: File → Save Design... → Innovus: DBS/route*

Route

- Supplementary: How routing work in Innovus?
 - Lee Algorithm



Filling

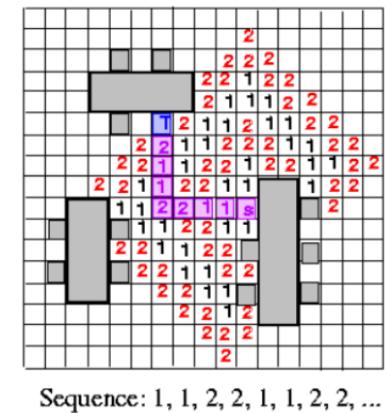
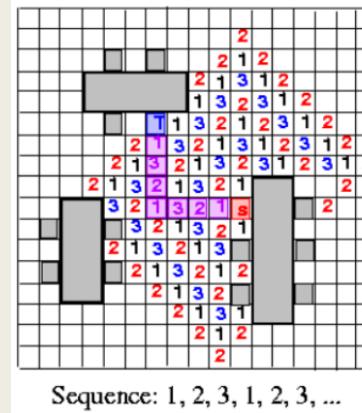


Retrace

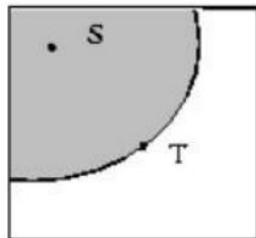
Route

- Disadvantage:
 - *Too slow & Memory consuming*
- Some improve:
 - *Change labeling scheme*

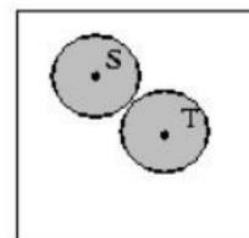
- *Different Searching scheme*



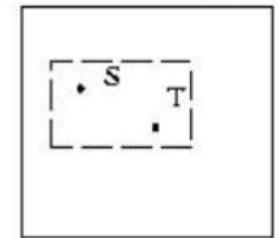
starting point selection



double fan-out



framing



Route

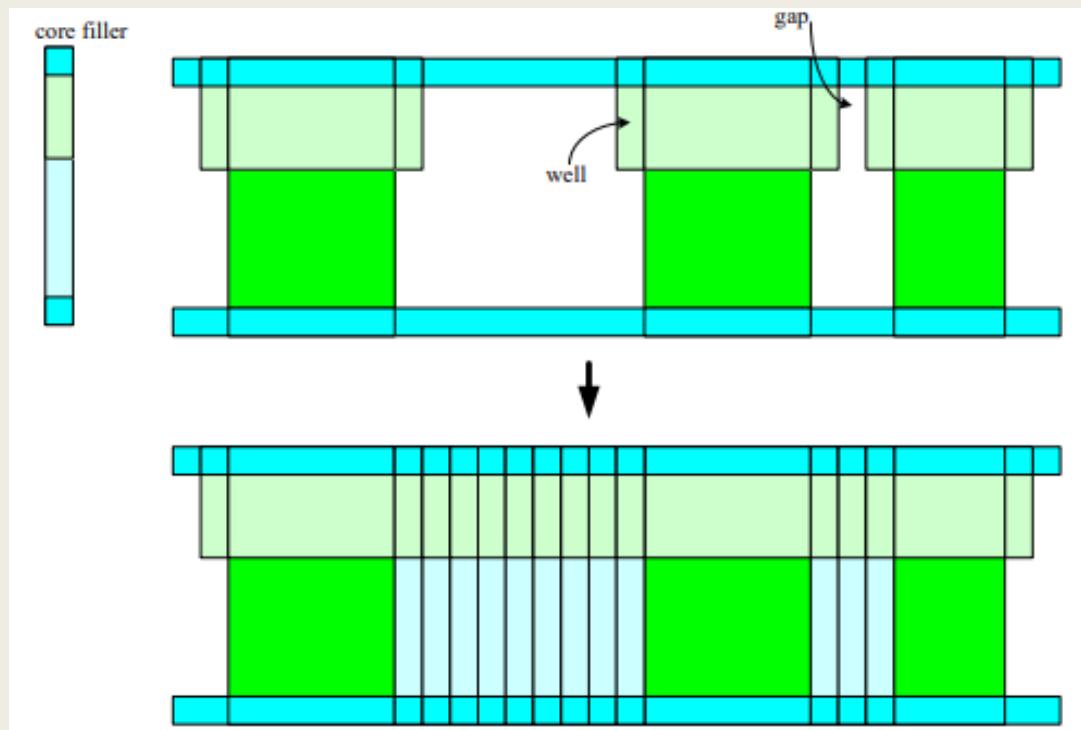
- Other algorithm:
 - *Hadlock, “A shortest path algorithm for grid graphs,” Networks, 1977.*
 - *Soukup, “Fast maze router,” DAC-78.*

Outline

- Introduction
- Initial step
- Floor plan
- Power plan
- Power route
- CTS
- Route
- Post processing**
- Post-layout simulation
- Reference

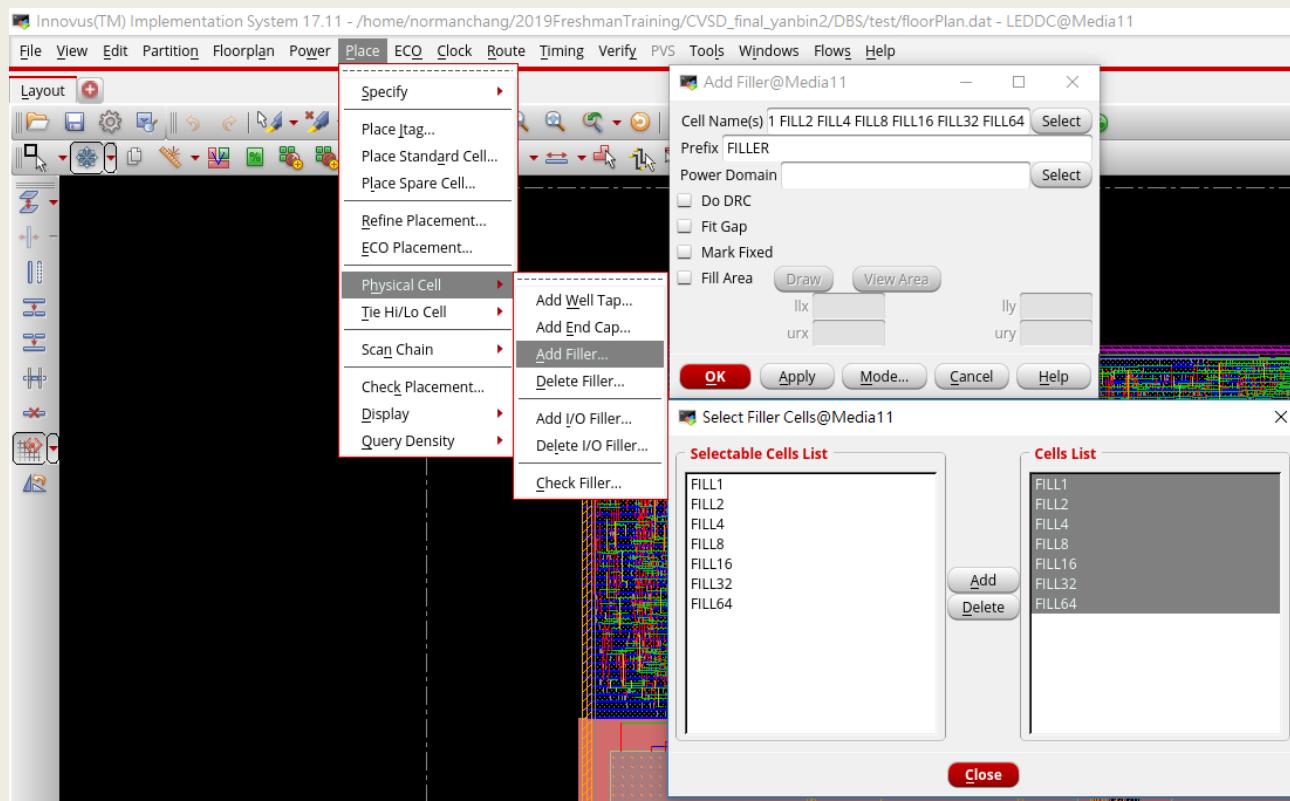
Post Processing

- 1. Add Core Filler
- Why?
 - *To fill the gap between cells.*
 - *Start from wider filler to narrow filler*



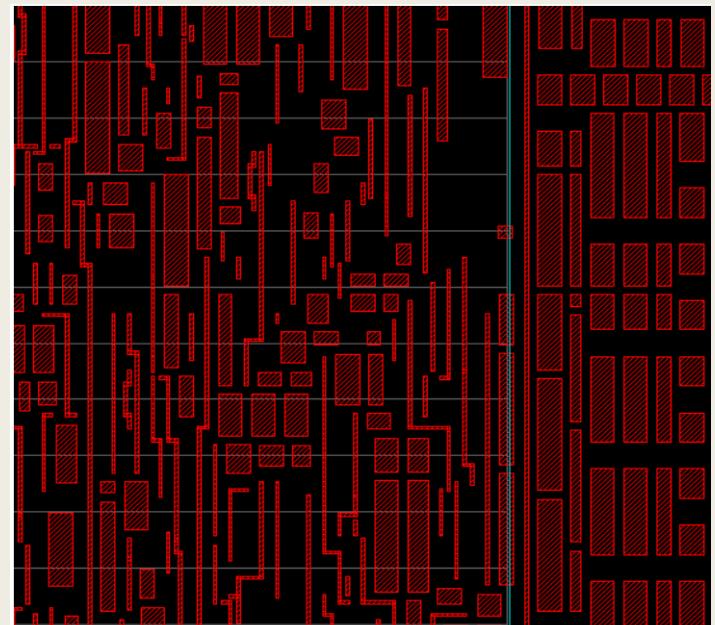
Post Processing

- Place → Physical Cell → Add Filler... →
 - Click Select of Cell Name(s)
 - From Cells List choose all filler and click Add
 - Close Select Filler Cells window and click OK



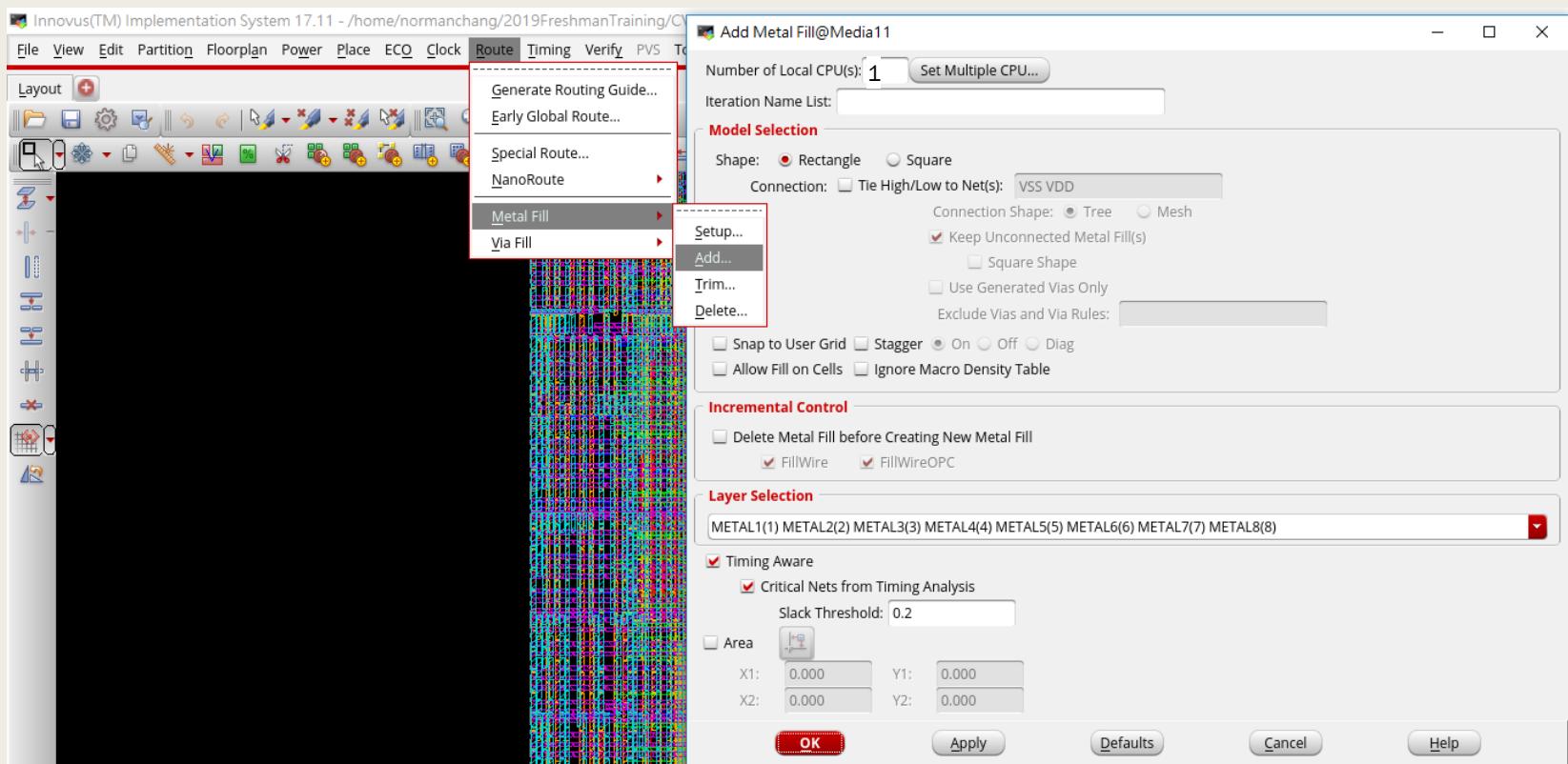
Post Processing

- 2. Add Dummy Metal
- Why?
 - *meet minimize metal density rule – prevent over etching*
 - *prevent sagging in local area*
 - *improve yield*
 - *reduce on chip variation .*
- Better connect dummy metal to VSS.

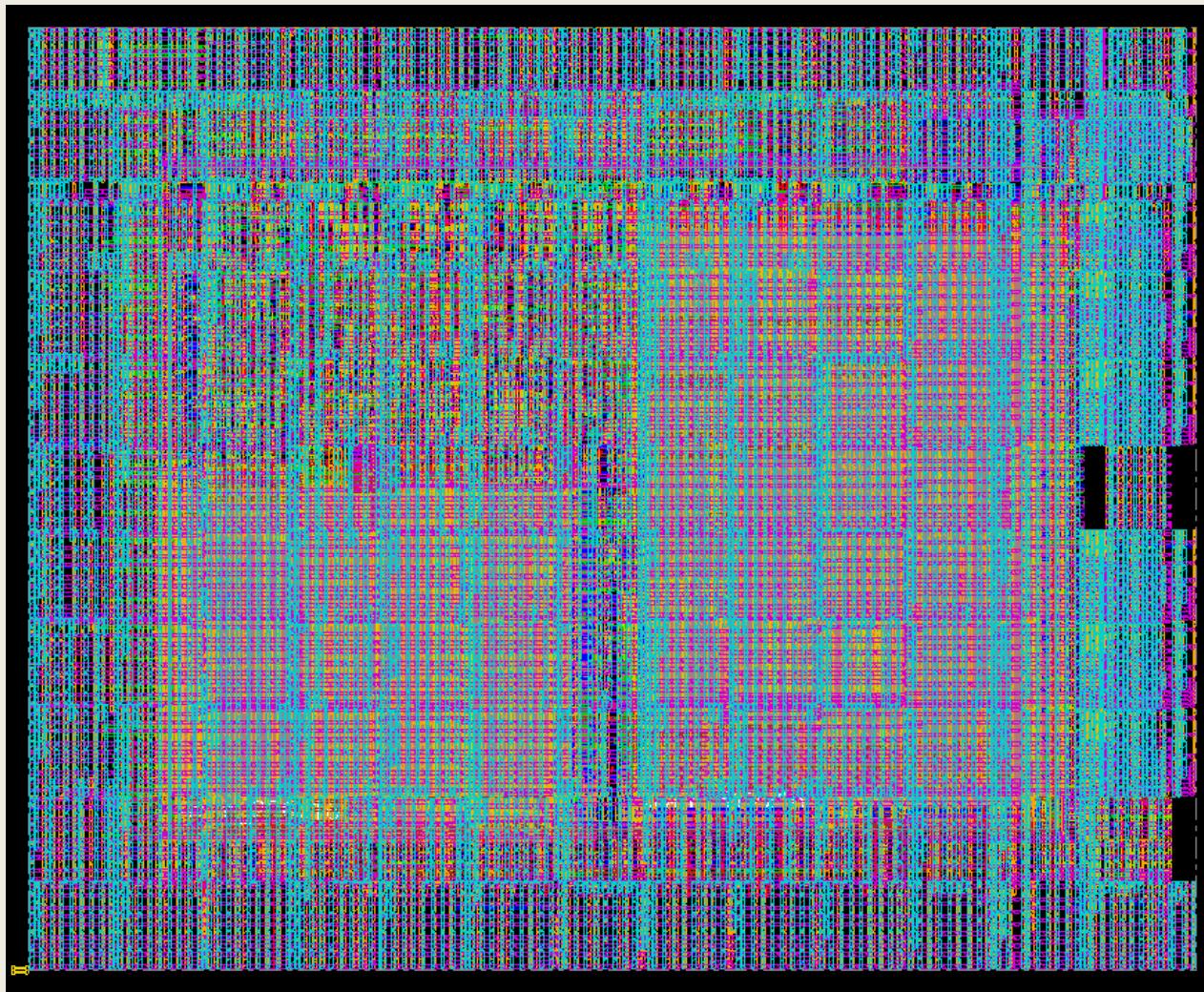


Post Processing

- Route → Metal Fill → Add... →
 - Un-select *Tie High/Low to Net(s)*:
 - Select *Timing Aware* and *Critical Nets from Timing Analysis*
 - Slack Threshold: 0.2



Post Processing



Post Processing

- 3. Verify everything again:
 - Verify → Verify Geometry ... → OK
 - Verify → Verify Process Antenna... → OK
 - Verify → Verify Connectivity... → select *All* → in check, select *Unrouted Net* → OK
- Check if there is any violation
 - If there is any violation → *Cadence Virtuso*
 - If there isn't any violation...

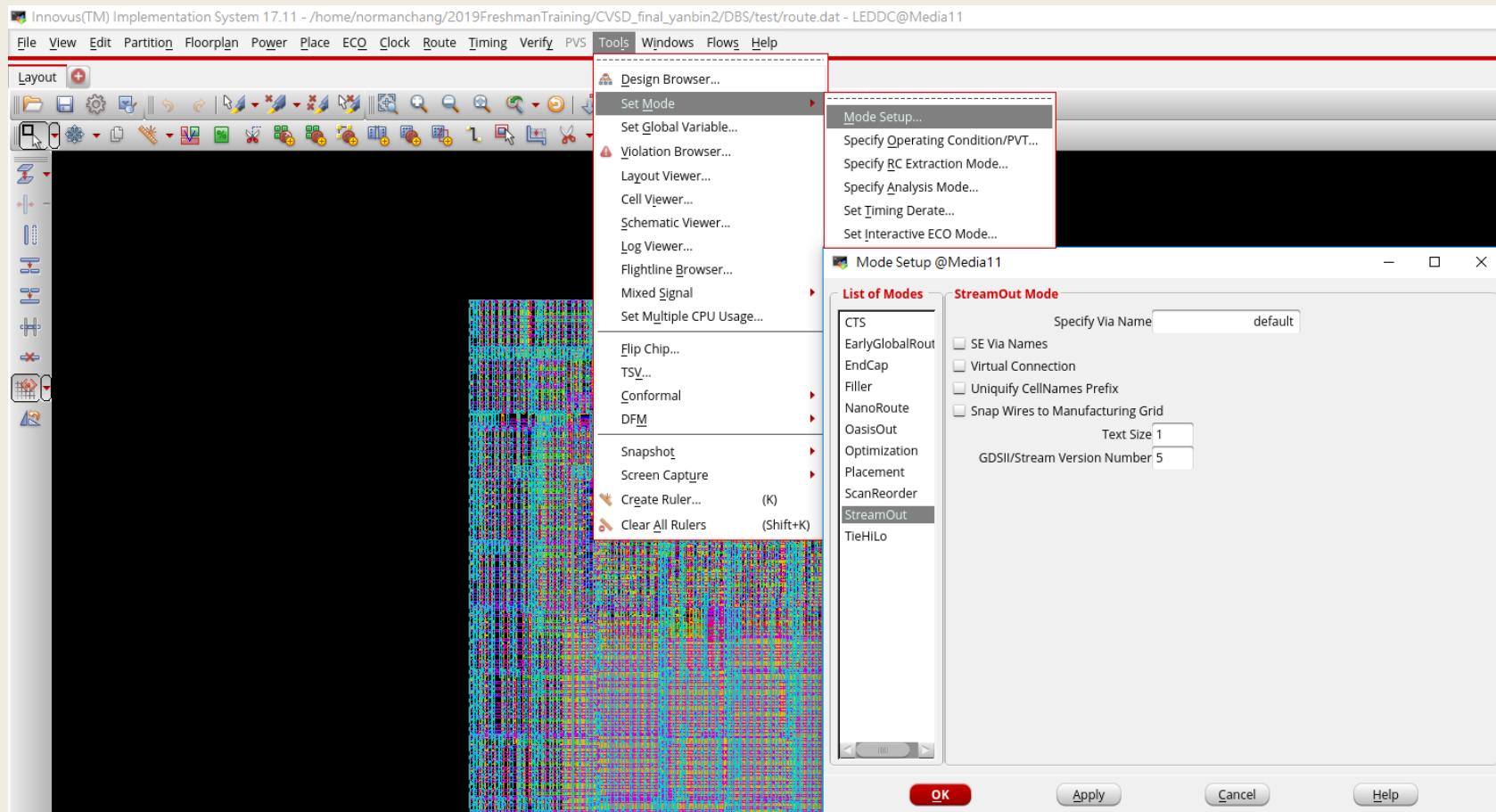
Post Processing

- 4. Save file:
 - Innovus > setAnalysisMode -analysisType bcwc
 - Innovus > write_sdf -max_view AV_func_max -typ_view AV_func_max -edges noedge -splitsetuphold -remashold -splitrecrm -min_period_edges none LEDDC_pr.sdf
 - Innovus > saveNetlist ***your_design_name***_pr.v
- In other course, you may learn this:
 - Timing → Write SDF... → un-select *Ideal Clock* → OK
- However, the output SDF file of this step may not work well.

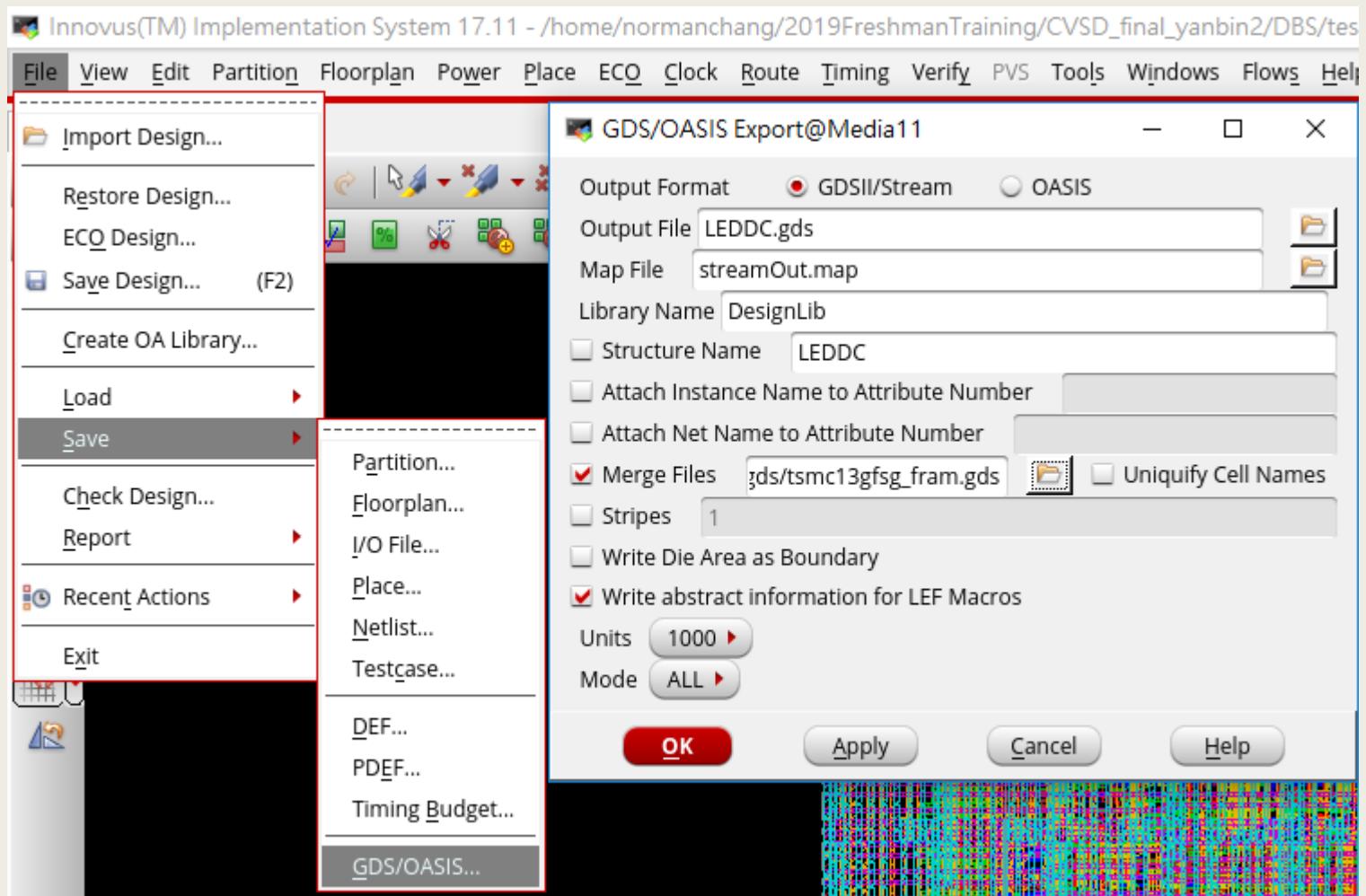
Post Processing

- 4. Streamout GDS:
- Tools → Set Mode → Mode Setup... → StreamOut → Un-select *Virtual Connection*
- File → Save → GDS/OASIS... →
 - Output File: *your_design_name.gds*
 - Select *Merge Files* : find your *tpz013g3_v1.1.gds* and *tsmc13gfsg_fram.gds* (and other gds file like sram) and fill it
 - select *Wire abstract information for LEF Macros*
 - Units: *1000*

Post Processing



Post Processing

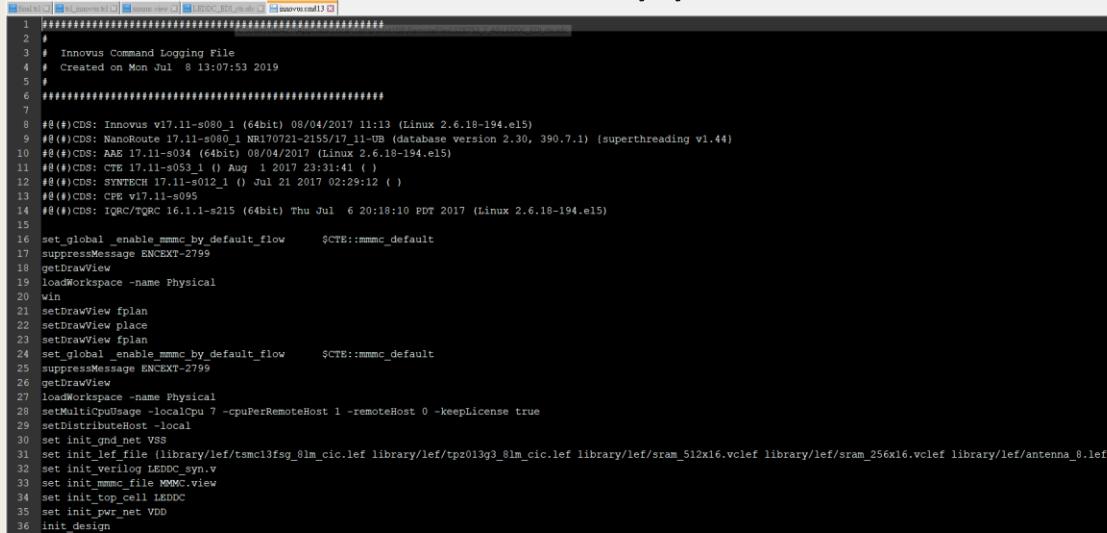


Post Processing

- 5. If you want to see how large is your design:
 - Innovus > analyzeFloorplan

Warning! This step will destroy your design, which means that you are not able to recover your design after this command. Remember to save a copy before you use this.

- 6. Save tcl file:
 - Find the file named innovus.cmdx
 - Store the useful command by yourself



```
1
2 # Innovus Command Logging File
3 # Created on Mon Jul  8 13:07:53 2019
4
5 #####
6
7
8 #(())CDS: Innovus v17.11-s080_1 (64bit) 08/04/2017 11:13 (Linux 2.6.18-194.el5)
9 #(())CDS: NanoRoute 17.11-s00_1 NR170721-2155/17_11-UB (database version 2.30, 390.7.1) {superthreading v1.44}
10 #(())CDS: AAB 17.11-s034 (64bit) 08/04/2017 (Linux 2.6.18-194.el5)
11 #(())CDS: CTD 17.11-s053_1 () Aug 1 2017 23:31:41 ( )
12 #(())CDS: SYNTech 17.11-s012_1 () Jul 21 2017 02:29:12 ( )
13 #(())CDS: CPF v17.11-s095
14 #(())CDS: IQRC/TQRC 16.1.1-s215 (64bit) Thu Jul  6 20:18:10 PDT 2017 (Linux 2.6.18-194.el5)
15
16 set_global _enable_mmmc_by_default_flow      $CTE:mmmc_default
17 suppressMessage ENCEXT-2799
18 gettraview
19 loadWorkspace -name Physical
20 win
21 settraview fplan
22 settraview place
23 settraview fplan
24 set_global _enable_mmmc_by_default_flow      $CTE:mmmc_default
25 suppressMessage ENCEXT-2799
26 gettraview
27 loadWorkspace -name Physical
28 setMultiPcuUsage -localpcu 7 -cpuPerRemoteHost 1 -remoteHost 0 -keepLicense true
29 setDistributeHost -local
30 set init_gm net VSS
31 set init_lef file/tsmc13fsg_8lm_cic.lef library/lef/tpz013g3_8lm_cic.lef library/lef/sram_512x16.vclef library/lef/sram_256x16.vclef library/lef/antenna_8.lef
32 set init_verilog LEDDC_syn.v
33 set init_mmmc_file MMCN.view
34 set init_top_cell LEDDC
35 set init_pwr net VDD
36 init_design
```

Outline

- Introduction
- Initial step
- Floor plan
- Power plan
- Power route
- CTS
- Route
- Post processing
- Post-layout simulation

Post-layout Simulation

- 1. Change the sdf file in your testbench to the sdf output by innovus
- 2. Run:
 - *ncverilog your_testbench.v yor_apr_result.v tsmc13_neg.v +define+SDF*

```
-----  
Congratulations! All data have been generated successfully!  
-----PASS-----  
Simulation complete via $finish(1) at time 83331290 NS + 0  
. ./testfixture_60fps.v:305      $finish;  
ncsim> exit  
# normanchang @ Mediall in ~/2019FreshmanTraining/CVSD_final_yanbin2 [16:41:17]  
$ ncverilog testfixture_60fps.v LEDDC_pr.v tsmc13_neg.v +define+SDF
```

Outline

- Introduction
- Initial step
- Floor plan
- Power plan
- Power route
- CTS
- Route
- Post processing
- Post-layout simulation
- Reference

Reference

- [1] NARLabs Cell-Based IC Physical Design and Verification
 - [https://github.com/mediaic/Crash_Course_for_New_Members
/blob/master/legacy/2018_VLSI_Crash_Course.md](https://github.com/mediaic/Crash_Course_for_New_Members/blob/master/legacy/2018_VLSI_Crash_Course.md)
- [2] 2018 Fall Computer-aided VLSI System Design