Cloch => gives us the signal, which can be:

- active high (semnalul creste)
- active low (semnalul scade)

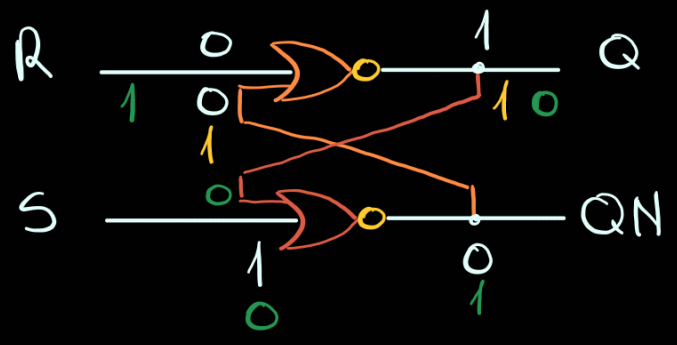
Stare instabila => Oscileaza (Metastability)

⇓

We Don't Want That!

Vrem sa avem o stare stabila!

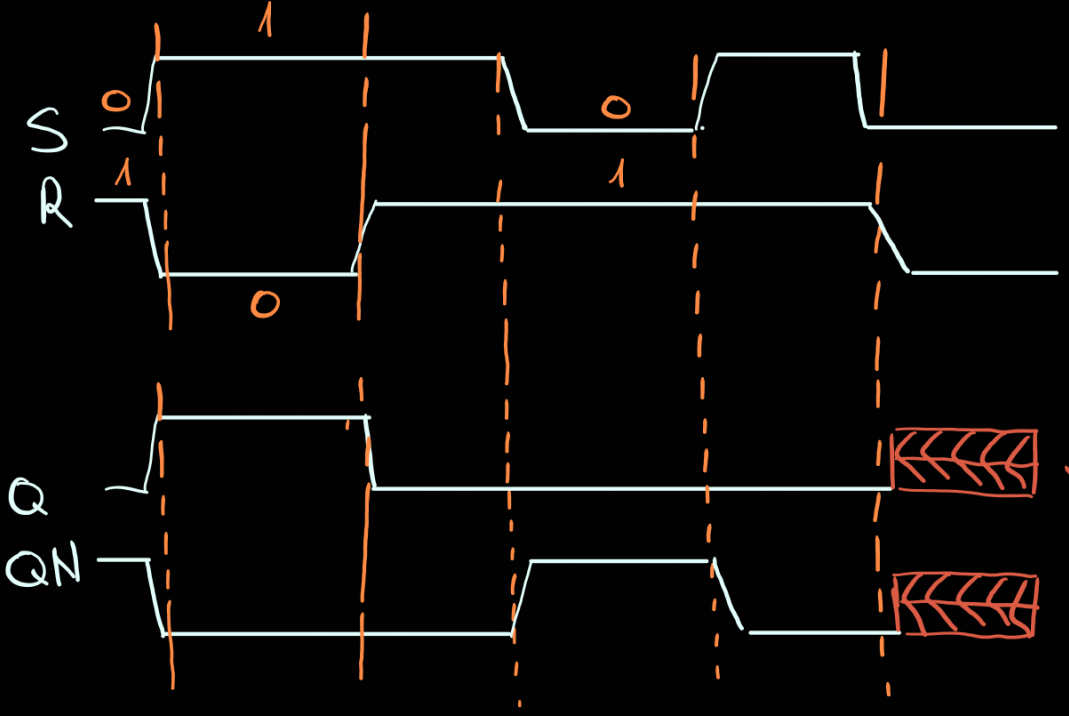
S-R Latch:



S	R	Q	QN
1	0	1	0
1	1	0	0
0	1	0	1
0	0	last Q	last QN

FORBIDDEN COMBINATION

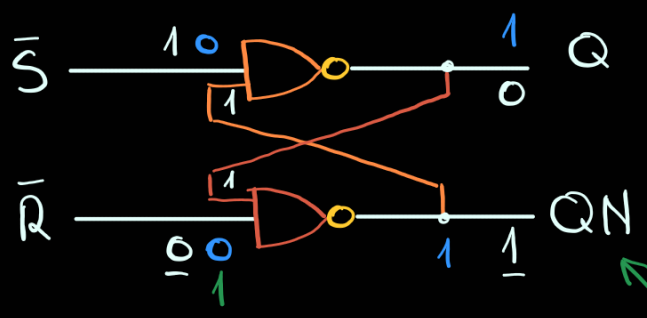
=>



când timpul minim e mai mic decât timpul folosit!

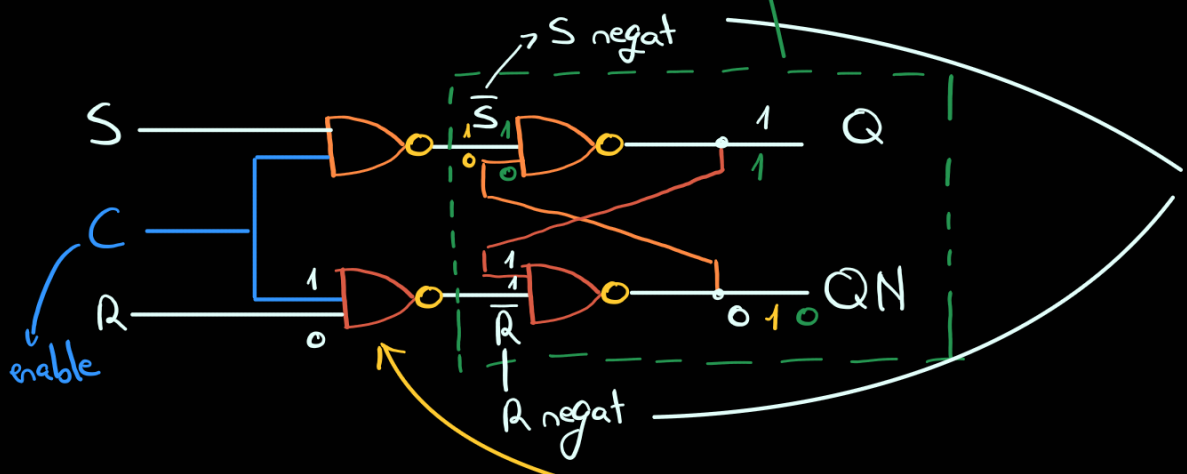
când ambele devin brusc zero => apar oscilații

$\bar{S}$-$\bar{R}$ Latch:



$\bar{S}$	$\bar{R}$	Q	QN
1	0	0	1
1	1	last Q	last QN
0	1	1	0
0	0	1	1

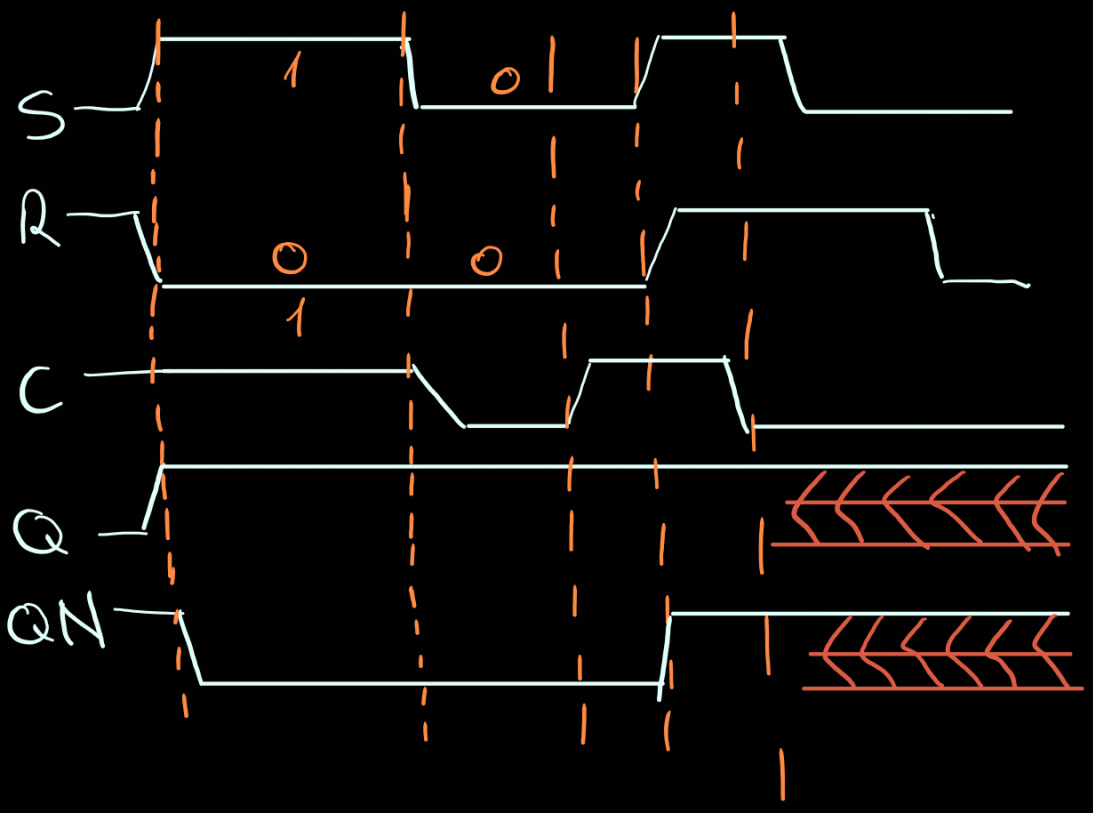
$\bar{S}$-$\bar{R}$ Latch with Enable:



=> din cauza asta folosim D pentru S și R

Pentru NAND Gates, better start with 1 cases

C	S	R	Q	QN
1	1	0	1	0
1	1	1	1	1
1	0	0	last Q	last QN
1	0	1	0	1
0	X	X	last Q	last QN



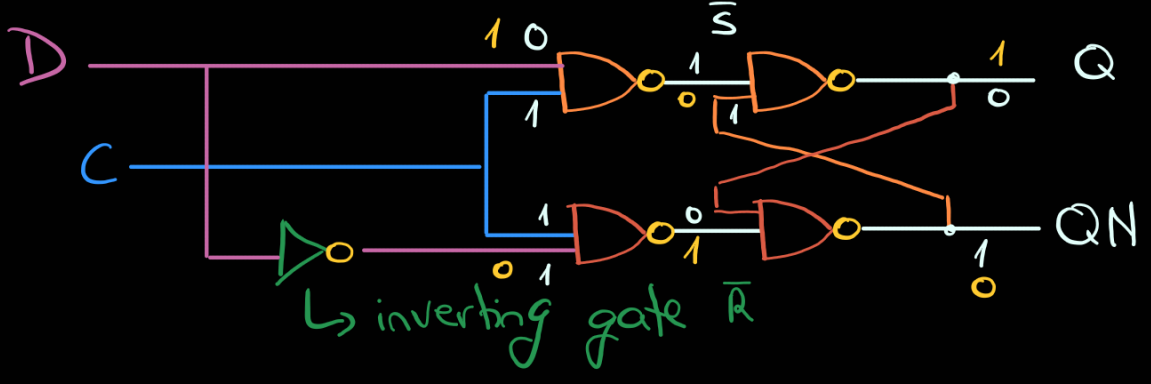
When $C = 1$: behaves normally

$C = 0$: remains in previous state

!! $S = R = 1$, C - changes from 1 to 0 =>

=> METASTABILITY

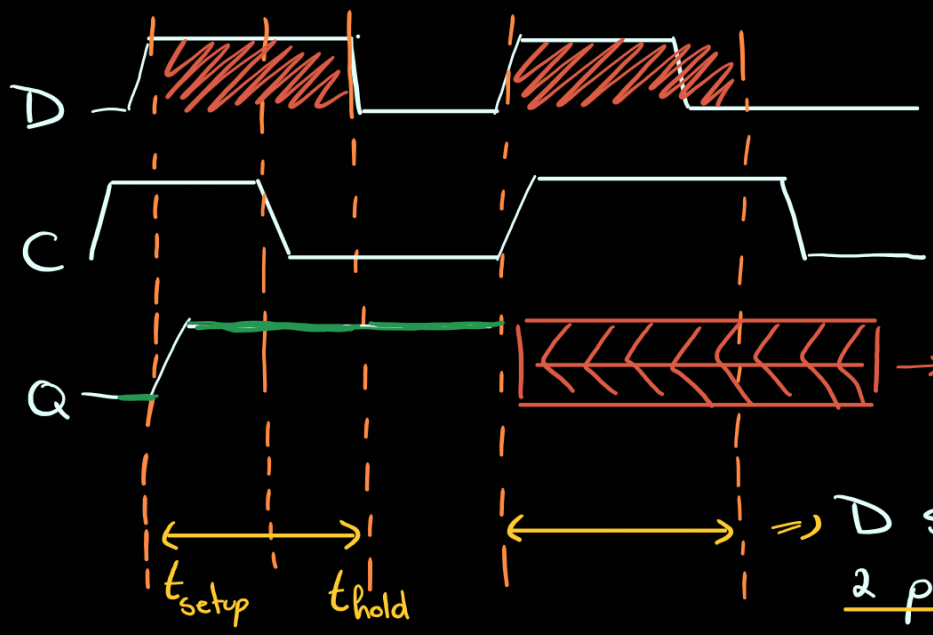
D - Latch:



↳ inverting gate $\bar{R}$

↳ nu tre să se schimbe!! Altfel apar oscilații !!

C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	last Q	last QN



Doamne să ne ajute pe toți!

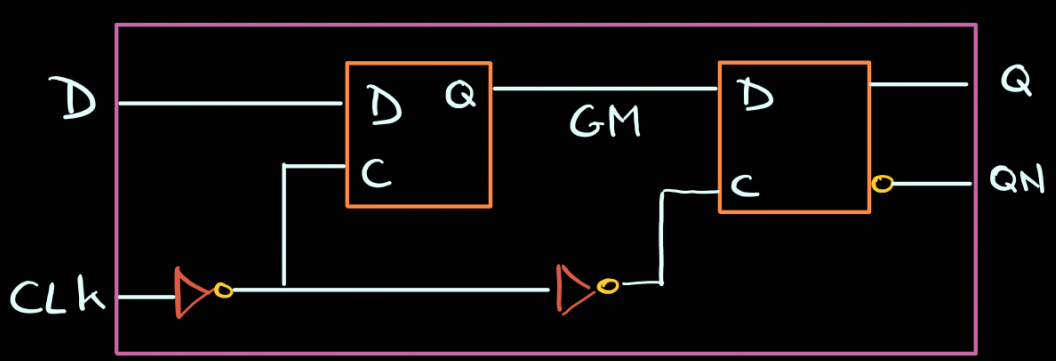
→ aici apar oscilațiile

⇒ D se schimbă în cele 2 perioade de timp!!

Când C e 1 ⇒
- D e 0 ⇒ Q e 0
- D e 1 ⇒ Q e 1

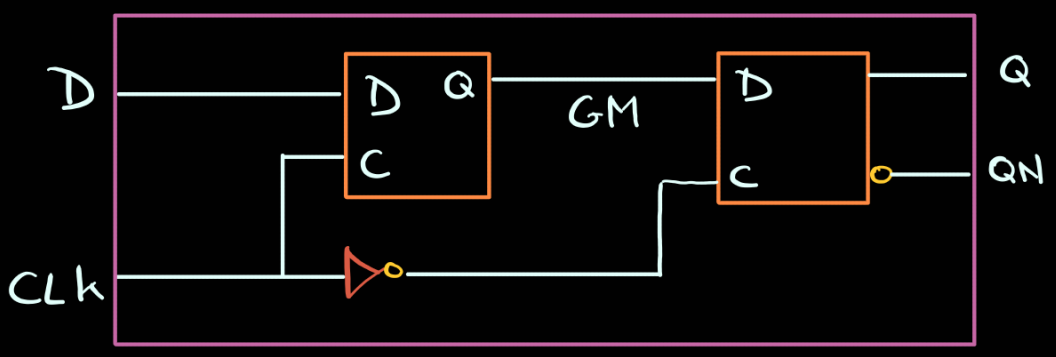
Când C e 0 ⇒ D și Q păstrează valoarea anterioară

Positive Edge Triggered D Ff



D	CLk	Q	QN
1	↑	0	1
1	↑	1	0
X	0	last Q	last QN
X	1	last QN	last Q

Negative Edge D Ff



D	CLK	Q	QN
0	↓	0	1
1	↓	1	0
x	0	last Q	last QN
x	1	last Q	last QN