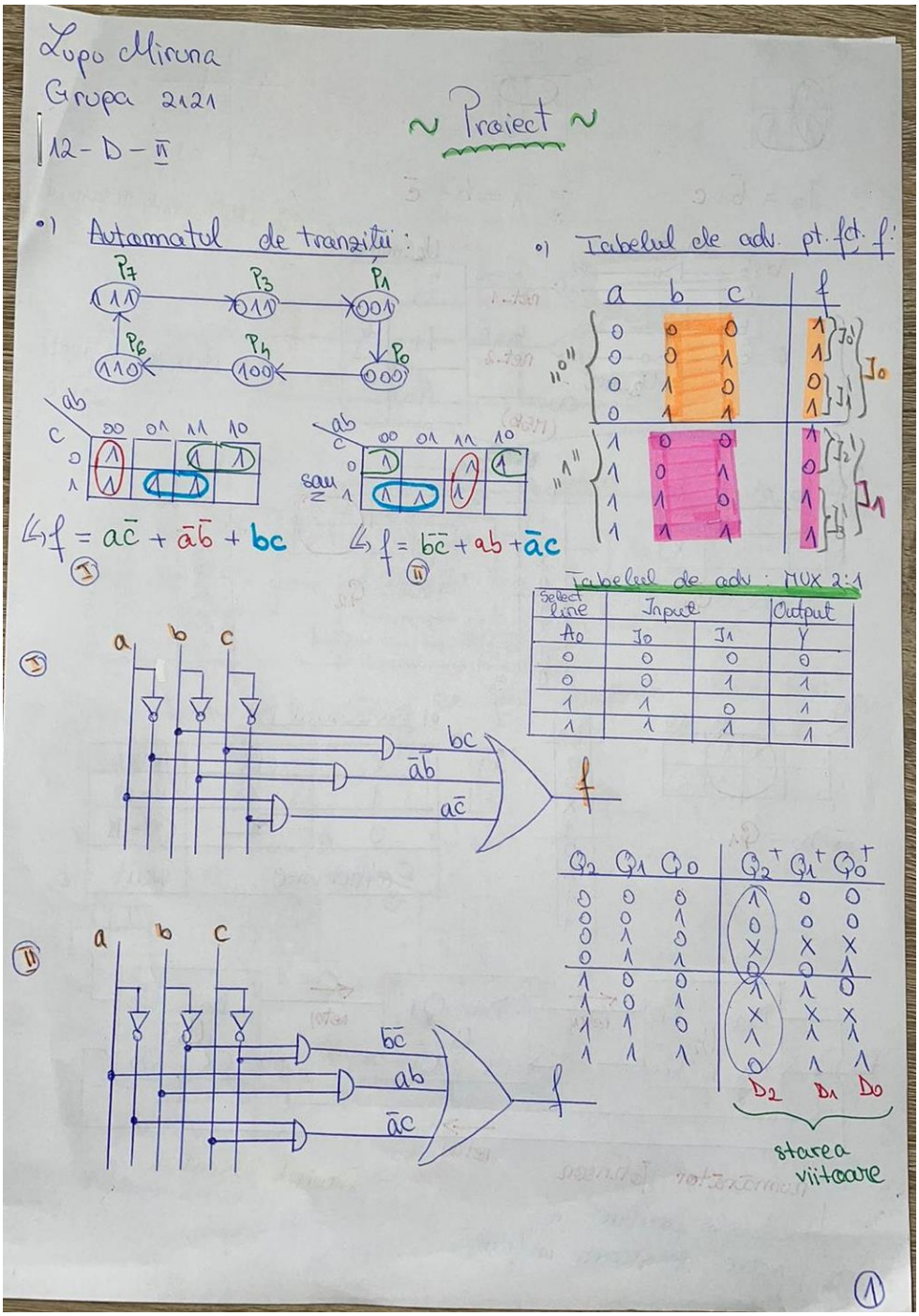
LUPU MIRUNA

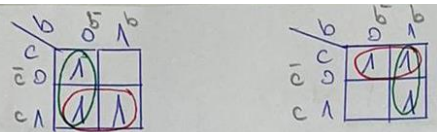
GRUPA 2121

12-D-II

PROIECT CID

- Rezolvarea temei de proiect pe hartie :



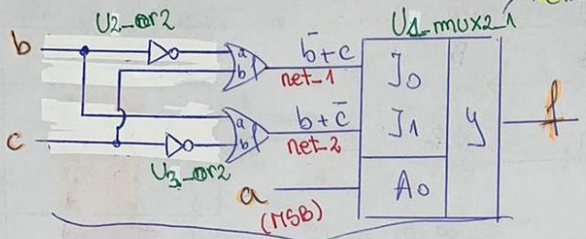


⇒

a	f
0	$\bar{b}+c$
1	$b+\bar{c}$

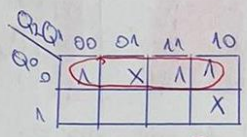
⇒ $J_0 = \bar{b}+c$ ⇒ $J_1 = b+\bar{c}$

→ Circuitul combinațional



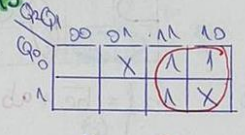
MUX2:1 + porți logice

FVIT3



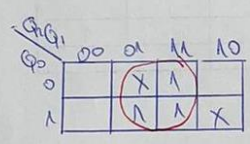
⇒ $D_2 = \bar{Q}_0$

D_2
1
0
X
0
1
X
1
0



⇒ $D_1 = Q_2$

D_1
0
0
X
0
1
X
1
0

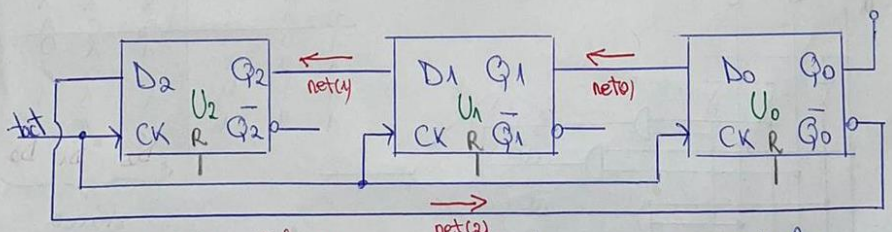


⇒ $D_0 = Q_1$

D_0
0
0
X
1
0
X
1
1

o) Bistabilul D:

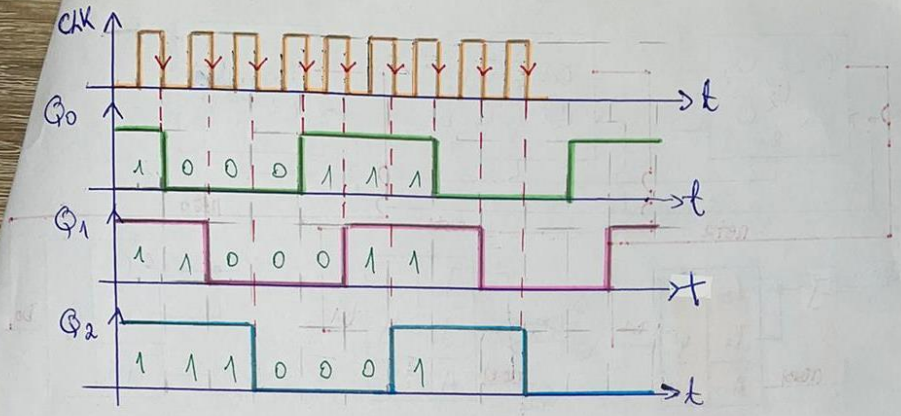
r	clk	Action
1	X	Reset
0	↓	$Q^+ = D$
otherwise		Wait

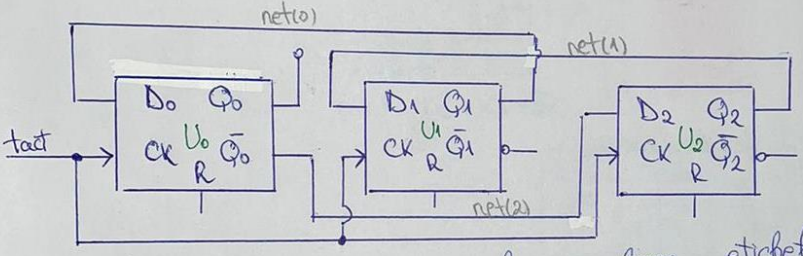


numărător Johnson

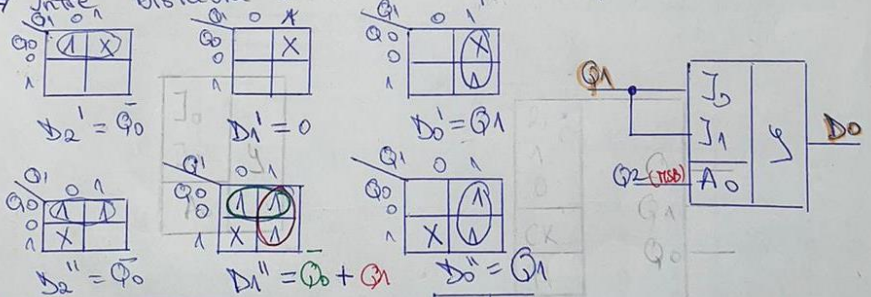
↳ 2 bucle posibile în funcție de starea inițială

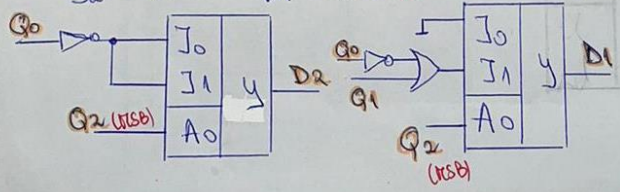
↳ Circuitul secvențial

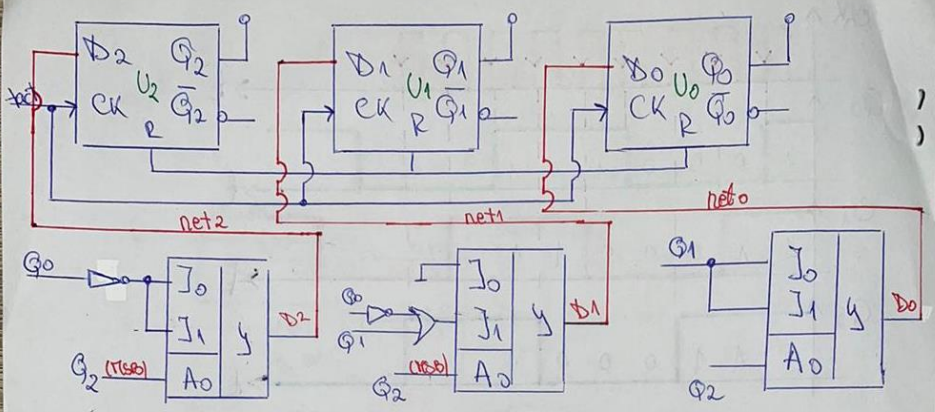




→ Între bistabile și MUX se fac conform „etichetelor".






D2
Q2
U2
CK
R
Q2
D1
Q1
U1
CK
R
Q1
D0
Q0
U0
CK
R
Q0
net2
net1
net0
Q0
J0
J1
A0
y
D2
Q2
(MSB)
Q0
Q1
J0
J1
A0
y
D1
Q2
(MSB)
Q1
J0
J1
A0
y
D0
Q2

- Capturi de ecran :

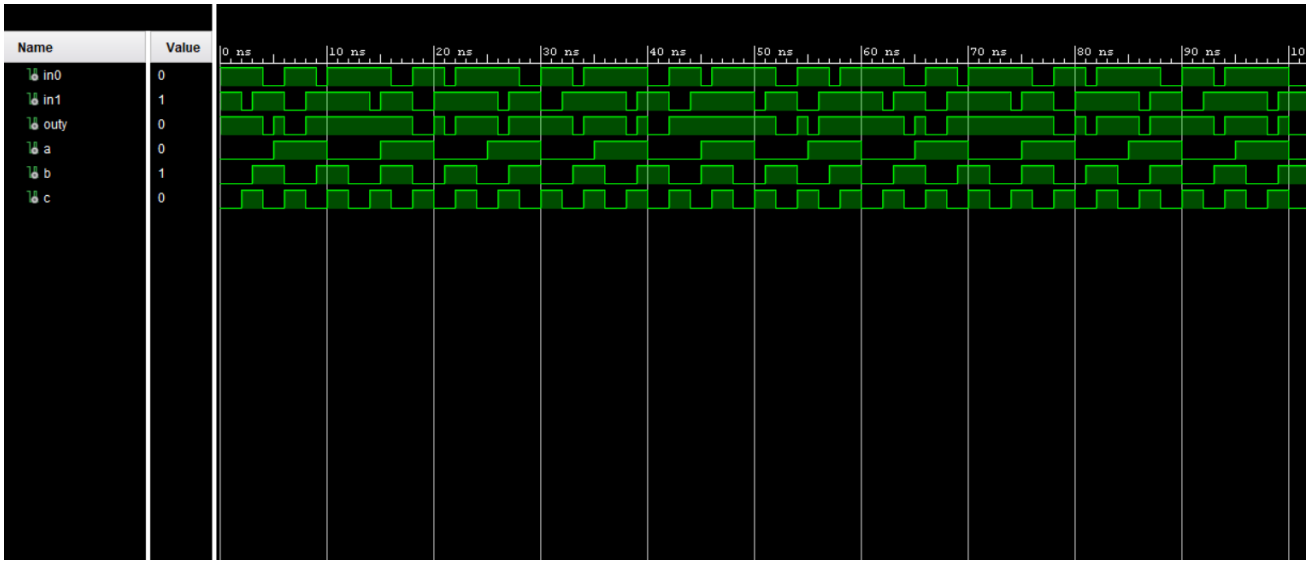
- Circuitul combinational: **MUX2:1**

C:/Miruna/LupuMiruna_2111_Proiect_CID.srcs/sources_1/new/mux2_1.vhd

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.ALL;
3
4
5   entity mux2_1 is
6       Port ( I0 : in STD_LOGIC;
7              I1 : in STD_LOGIC;
8              a : in STD_LOGIC;
9              y : out STD_LOGIC);
10  end mux2_1;
11
12  architecture Behavioral of mux2_1 is
13  begin
14
15  process (I0,I1,a)
16  begin
17      if a='0' then
18          y <= I0;
19      else
20          y <= I1 ;
21      end if;
22  end process;
23
24  end Behavioral;
25
```

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity testmux2_1 is
--  Port ( );
end testmux2_1;

architecture Behavioral of testmux2_1 is

component mux2_1 is
    Port ( I0 : in STD_LOGIC;
           I1 : in STD_LOGIC;
           a : in STD_LOGIC;
           y : out STD_LOGIC);
end component mux2_1;

signal in0, in1, outy, a, b, c: std_logic;

begin

in0 <= (not b) or c;
in1 <= b or (not c);

MUX: mux2_1 port map ( I0 => in0, I1 => in1, a => a, y => outy);

generate_ina: process
begin
a <= '0'; wait for 5 ns;
a <= '1'; wait for 5 ns;
end process;
```

```vhdl
generate_ina: process
begin
a <= '0'; wait for 5 ns;
a <= '1'; wait for 5 ns;
end process;

generate_in0: process
begin
b <= '0'; wait for 3 ns;
b <= '1'; wait for 3 ns;
end process;

generate_in1: process
begin
c <= '0'; wait for 2 ns;
c <= '1'; wait for 2 ns;
end process;


end Behavioral;
```



- Circuitul secvential : Bistabilul D

C:/Miruna/LupuMiruna_2111_Proiect_CID.srcs/sources_1/new/bistabil.vhd

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.ALL;
3
4
5   entity bistabil is
6       Port ( D : in STD_LOGIC;
7              CLK : in STD_LOGIC;
8              R : in STD_LOGIC;
9              Q : out STD_LOGIC);
10  end bistabil;
11
12  architecture Behavioral of bistabil is
13
14  signal qint: std_logic;
15
16  begin
17
18  bistabil: process(R, CLK)
19  begin
20  if (R ='1') then
21       qint<= '1';
22       elsif (CLK'event and falling_edge (CLK)) then
23        qint <= d;
24        else
25        qint <= qint;
26   end if;
27   end process;
28
29   Q <= qint;
30
31  end Behavioral;
```

SIMULAREA:

C:/Miruna/LupuMiruna_2111_Proiect_CID.srcs/sim_1/new/simulation.vhd

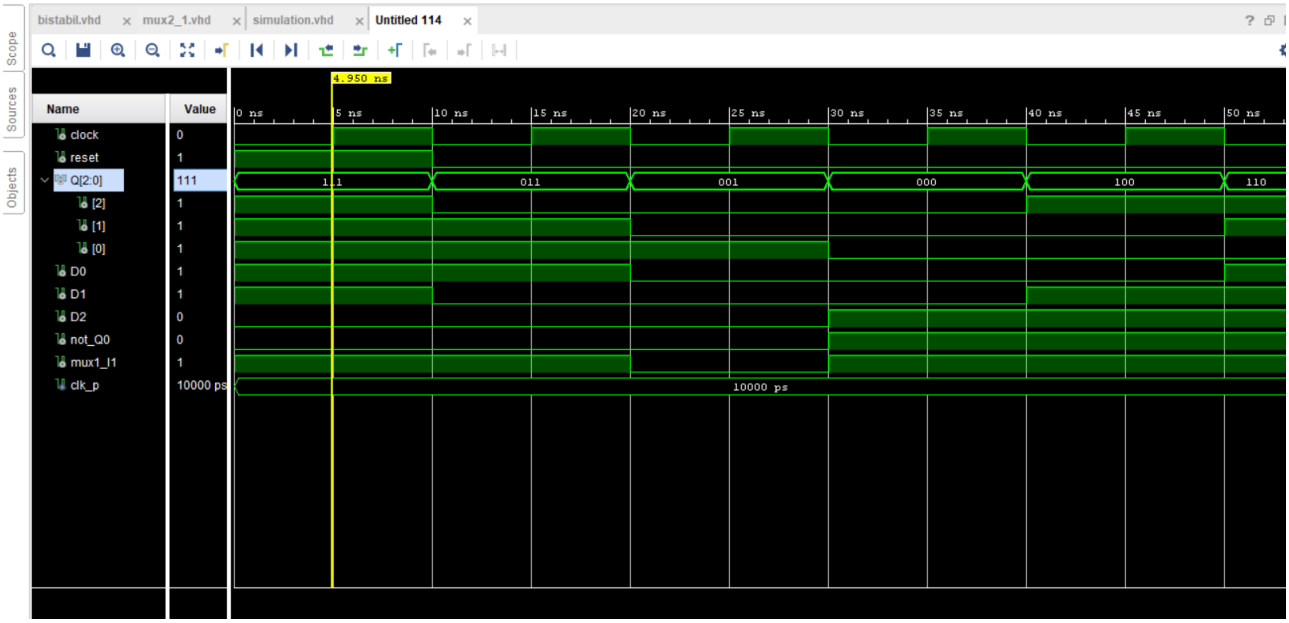
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity testbench_dff is
end testbench_dff;

architecture Behavior of testbench_dff is

    component bistabil is      -- componenta bistabilului
        Port ( D : in STD_LOGIC;
               CLK : in STD_LOGIC;
               R : in STD_LOGIC;
               Q : out STD_LOGIC);
    end component;

    component mux2_1 is        -- componenta mux2:1
        Port ( I0 : in STD_LOGIC;
               I1 : in STD_LOGIC;
               a : in STD_LOGIC;
               y : out STD_LOGIC);
    end component;


     constant clk_p : time := 10 ns;   -- perioada de timp
     signal clock  : STD_LOGIC := '0';
     signal reset  : STD_LOGIC := '0';
     signal Q  : STD_LOGIC_VECTOR (2 downto 0) := "111";  --setam starea initiala ca fiind "111" de la automatul de tranzitii
     signal  D0, D1, D2 : STD_LOGIC := '1';
     signal not_Q0 : STD_LOGIC := '1';  -- poarta Qo negat intrucat o folosim la doar mux-uri
     signal mux1_I1 : STD_LOGIC :='1';  -- poarta or intre Q0 negat si Q1
```

C:/Miruna/LupuMiruna_2111_Proiect_CID.srcs/sim_1/new/simulation.vhd

```vhdl
     signal mux1_I1 : STD_LOGIC :='1';  -- poarta or intre Q0 negat si Q1

begin

    not_Q0 <= not Q(0);
    mux1_I1 <= (not Q(0)) or Q(1);

    BST0: bistabil port map( D => D0, CLK => clock, R => reset, Q => Q(0));  -- 3 bistabile realizate de starea viitoare din tabelul de adevar
    BST1: bistabil port map( D => D1, CLK => clock, R => reset, Q => Q(1));
    BST2: bistabil port map( D => D2, CLK => clock, R => reset, Q => Q(2));

    MUX0: mux2_1 port map(I0 => Q(1), I1 => Q(1), a => Q(2), y => D0);      -- 3 mux-uri realizate de starea viitoare din tabelul de adevar
    MUX1: mux2_1 port map(I0 => '0', I1 => mux1_I1, a => Q(2), y => D1);
    MUX2: mux2_1 port map(I0 => not_Q0, I1 => not_Q0, a => Q(2), y => D2);

    clk: process            -- procesul de clock
    begin
            clock <= '0';
            wait for clk_p/2;
            clock <= '1';
            wait for clk_p/2;

    end process;


    stim: process           -- procesul de reset
    begin
          reset <= '1';
          wait for 10 ns;
          reset <= '0';
          wait;
```

```vhdl

    stim: process           -- procesul de reset
    begin
          reset <= '1';
          wait for 10 ns;
          reset <= '0';
          wait;
    end process;

end;
```

REZULTATUL SIMULARII:


bistabil.vhd
mux2_1.vhd
simulation.vhd
Untitled 114
Scope
Sources
Objects
Name
Value
clock
0
reset
1
Q[2:0]
111
[2]
1
[1]
1
[0]
1
D0
1
D1
1
D2
0
not_Q0
0
mux1_I1
1
clk_p
10000 ps
4.950 ns
0 ns
5 ns
10 ns
15 ns
20 ns
25 ns
30 ns
35 ns
40 ns
45 ns
50 ns
111
011
001
000
100
110
10000 ps