

## Enzo Zhu

### Present Address

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**Interests** My research interests lie at Programming Language and System, Formal Methods and System Verification.

**Education** **University of Science and Technology of China (USTC)**, Hefei, China 2018 - 2022  
Undergraduate  
B.S. in Computer Science  
Performance: Major 3.02/4.3 or 80.43/100

**Awards** Third Prize in National Computer System Contest in Compiler Designing 08/2021  
Second Prize in National Computer System Contest in Chip Designing 08/2020

**Work** Part-time Principles and Techniques of Compiler TA in USTC Sep-Dec 2021  
**Experience** Part-time Computer Programming TA in USTC Sep-Dec 2020

**Project and** **ORMIR** 09/2021 - current

**Research** I worked with Kai Ma to design a automatic verifier which verify Django project and ORM  
**Experience** operations' consistency properties.

**Bazinga Compiler** [https://github.com/misakihanayo/bazinga\\_compiler](https://github.com/misakihanayo/bazinga_compiler) 08/2021  
I worked in a team on a compiler to translate code from sysc language to arm-v8 assembly code. Within this project, I implemented the lexer, the parser, part of the middle IR, several optimization passes, part of the lower IR and the code generator.

**Heterogeneous Isolated Execution in ARM TrustZone (HKU)**, Hong Kong Summer 2021  
Internship  
I designed a trusted accelerator in ARM trustzone with my advisor Heming Cui, including a PCIe device to control the execution zone of a program. This device can distinguish codes from different zone(Trusted or Normal), execute them in different zone of the system, and forbid inaccurate access to data.

**USTC-SYS Reading Group** Fall 2020 - current

I participated in the reading group and went through a bunch of up-to-date, state of the art papers, and gave a report about the paper "Storage Systems are Distributed Systems (So Verify Them That Way!)", OSDI 20.

**Ustc-Nscsc-2020-1** <https://github.com/misakihanayo/ustc-nscsc-2020-1> 08/2020  
I built a 5 stage MIPS Chip in a team. Within this project, I designed the MEM stage, the exception module, the TLB and the instruction and data cache. the chip can run a P-mon system on it, and support VGA video output.

**FPGAOL**

07/2019-12/2019

I worked in a team on a web system to provide online FPGA support for the collage digital circuits labs.