



ATtiny212/412

ATtiny212/412 Silicon Errata and Data Sheet Clarification

Introduction

The ATtiny212/412 devices you have received conform functionally to the current device data sheet (DS40001911B), except for the anomalies described in this document. The erratas described in this document will likely be addressed in future revisions of the ATtiny212/412 devices.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

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1. Silicon Errata

1.1 Errata - ATtiny212/ATtiny412

1.1.1 Die Revision B

1.1.1.1 Device

1 –

The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)

The temperature sensor is not calibrated on parts with date code 727/728 (used on QFN packages) and 1728 (used on SOIC packages).

Fix/Work Around:

If temperature sensor calibration data is required, devices with the affected date code may be returned through the Microchip RMA service. Devices with this date code are no longer shipped by Microchip.

1.1.1.2 ADC

1 –

One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Fix/Work Around:

Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

2 –

ADC Functionality Cannot be Guaranteed with ADCCLK Above 1.5 MHz for All Conditions

The ADC functionality cannot be guaranteed if ADCCLK > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'. The ADC functionality cannot be guaranteed if ADCCLK > 1.5 MHz and VDD < 2.7V.

Fix/Work Around:

If ADC is operated with CLK_ADC > 1.5 MHz and VDD > 2.7V, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle). Do not use ADC at CLK_ADC > 1.5 MHz and VDD < 2.7V.

1.1.1.3 CCL

1 –

Connecting LUTs in Linked Mode Require OUTEN Set to '1'

Connecting the LUTs in linked mode require LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Fix/Work Around:

Use an event channel to link the LUTs or do not use the corresponding I/O pin for other purposes.

2 –

D-latch is Not Functional

The CCL D-latch is not functional.

Fix/Work Around:

None.

1.1.1.4 RTC

1 –

Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the RTC and PIT prescaler.

Fix/Work Around:

None.

2 –

Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Fix/Work Around:

Do not disable the RTC or the PIT if any of the modules are used.

1.1.1.5 TCB

1 –

Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

Fix/Work Around:

Ensure that the high/low period of input events is equal to or longer than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

2 –

The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is only restarted after a TCA OVF.

Fix/Work Around:

None.

1.1.1.6 USART

1 –

TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Fix/Work Around:

There are two possible work-arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

2 –

Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATA before the RxD line goes high.

Fix/Work Around:

Wait for the RxD pin to go high before reading RXDATA, for instance by polling the bit in PORTn.IN where the RxD pin is located.

1.1.2 Die Revision A

1.1.2.1 AC

1 –

AC Interrupt Flag Not Set Unless Interrupt is Enabled

ACn.STATUS.CMP is not set if the ACn.INTCTRL.CMP is not set.

Fix/Work Around:

Enable ACn.INTCTRL.CMP or use ACn.STATUS.STATE for polling.

2 –

False Triggers May Occur Under Certain Conditions.

False triggers may occur on falling input pin:

- For common-mode voltage below 0.5V
- For common-mode voltage above 0.5V if the slew rate is greater than 1 V/μs

Fix/Work Around:

None.

1.1.2.2 ADC

1 –

One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Fix/Work Around:

Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

2 –

Changing ADC Control Bits During Free-Running Mode not Working

If control signals are changed during Free-Running mode, the new configuration is not properly taken into account in the next measurement. This is valid for the ADC.CTRLB, ADC.CTRLA, ADC.SAMPCTRL registers and the ADC.MUXPOS, ADC.WINLT and ADC.WINHT registers.

Fix/Work Around:

Disable ADC Free-Running mode before updating the ADC.CTRLB, ADC.CTRLC, ADC.SAMPCTRL, ADC.MUXPOS, ADC.WINLT or ADC.WINHT registers.

3 –

ADC Wake-Up with WCOMP

When waking up from STANDBY Sleep mode with ADC WCOMP interrupt the ADC is disabled for a few cycles before the device enters ACTIVE mode. A new INITDLY is required before the next conversion.

Fix/Work Around:

Use INITDLY before the next conversion.

4 –

SAMPDLY and ASDV Does Not Work Together with SAMPLEN

Using SAMPCTRL.SAMPLEN at the same time as CTRLD.SAMPDLY or CTRLD.ASDV will cause an unpredictable sampling length.

Fix/Work Around:

When setting SAMPCTRL.SAMPLEN greater than '0' the CTRLD.SAMPDLY and CTRLD.ASDV must be cleared.

5 –

ADC Functionality Cannot be Guaranteed with ADCCLK Above 1.5 MHz for All Conditions

The ADC functionality cannot be guaranteed if ADCCLK > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'. The ADC functionality cannot be guaranteed if ADCCLK > 1.5 MHz and VDD < 2.7V.

Fix/Work Around:

If ADC is operated with CLK_ADC > 1.5 MHz and VDD > 2.7V, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle). Do not use ADC at CLK_ADC > 1.5 MHz and VDD < 2.7V.

1.1.2.3 CCL

1 –

Connecting LUTs in Linked Mode Require OUTEN Set to '1'

Connecting the LUTs in linked mode require LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Fix/Work Around:

Use an event channel to link the LUTs or do not use the corresponding I/O pin for other purposes.

2 –

D-latch is Not Functional

The CCL D-latch is not functional.

Fix/Work Around:

None.

1.1.2.4 RTC

1 –

Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the RTC and PIT prescaler.

Fix/Work Around:

None.

2 –

Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Fix/Work Around:

Do not disable the RTC or the PIT if any of the modules are used.

1.1.2.5 TCB

1 –

Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

Fix/Work Around:

Ensure that the high/low period of input events is equal to or longer than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

2 –

The TCB Interrupt Flag is Cleared When Reading CCMPH

TCBn.INTFLAGS.CAPT is cleared when reading TCBn.CCMPH instead of CCMPL.

Fix/Work Around:

Read both TCBn.CCMPL and TCBn.CCMPH.

3 –

TCB Input Capture Frequency and Pulse-Width Measurement Mode Not Working with Prescaled Clock

The TCB Input Capture Frequency and Pulse-Width Measurement mode may lock to freeze state if CLKSEL in TCB.CTRLA is set to any other value than 0x0.

Fix/Work Around:

Only use CLKSEL equal to 0x0 when using Input Capture Frequency and Pulse-Width Measurement mode.

4 –

The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is only restarted after a TCA OVF.

Fix/Work Around:

None.

1.1.2.6 TWI

1 –

TIMEOUT Bits in the TWI.MCTRLB Register are Not Accessible

The TIMEOUT bits in the TWI.MCTRLB register are not accessible from software.

Fix/Work Around:

When initializing TWI, BUSSTATE in TWI.MSTATUS should be brought into IDLE state by writing 0x1 to it.

2 –

TWI Smart Mode Gives Extra Clock Pulse

TWI Master with Smart mode enabled gives an extra clock pulse on the SCL line after sending NACK.

Fix/Work Around:

None.

3 –

TWI Master Mode Wrongly Detects the Start Bit as a Stop Bit

If TWI is enabled in Master mode followed by an immediate write to the MADDR register the bus monitor recognizes the Start bit as a Stop bit.

Fix/Work Around:

Wait for a minimum of two clock cycles from TWI.MCTRLA.ENABLE until TWI.MADDR is written.

4 –

The TWI Master Enable Quick Command is Not Accessible

TWI.MCTRLA.QCEN is not accessible from software.

Fix/Work Around:

None.

1.1.2.7 USART

1 –

TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Fix/Work Around:

There are two possible work-arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

2 –

Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

Fix/Work Around:

Wait for the RxD pin to go high before reading RXDATA, for instance by polling the bit in PORTn.IN where the RxD pin is located.

2. Data Sheet Clarification

No known issues.

3. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

3.1 Rev. A - 06/2019

Initial release.

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