

Muhammed Mishal

Graduate Electronics Engineer | RTL Design | Verilog | Vivado | Embedded Systems

Contact

Phone

+91 96450 23010

Email

mishalp789@gmail.com

Address

Pallathil House, Deverkovil,
Kuttiady Via, Kozhikode
Kerala-675308

Skills

- Digital Design & Verification: Verilog, RTL Design, Testbenches
- Simulation Tools: Vivado, GTKWave, Icarus Verilog
- Programming: Python, C, C++
- Embedded Systems: Arduino, RFID
- Frontend: HTML, CSS, JavaScript
- Tools: MATLAB, Git

Certifications

- Fundamentals of MATLAB - MATLAB
- Python Fundamentals by Microsoft
- Analog and Digital IC Design by IEEE CASS (micro - course)

Leadership & Roles

- Vice Chair, IEEE Computer Society – GEC Kozhikode (2023–24)
- Program Team Member, IEEE RAS – Kerala Section (2023–24)
- Campus Ambassador, IEEEExtreme 18.0
- Magazine Editor, College Union (2023–24)

Soft Skills

- Team collaboration
- Fast learner
- Communication skills
- Adaptability

Career Objective

Recent Electronics and Communication Engineering graduate with hands-on experience in Verilog RTL design, testbench creation, and waveform simulation. Skilled in embedded systems, hardware-software interfacing, and digital design tools. Seeking a VLSI Design and Verification Engineer role to contribute to real-world SoC and processor verification projects.

Education

- **Government Engineering College, Kozhikode, Kerala**
Bachelor of Technology: Electronics and Communication Engineering (2021-2025)
CGPA - 7.72
- **A J John Memorial Higher Secondary School, Chattanghottunada, Kerala**
Higher Secondary Education (Graduated in 2020)
Percentage – 92.25% (12th Grade)
- **Sirajul Huda English Medium School, Kuttiady, Kerala**
High School (Graduated in 2018)
Percentage – 86.6% (10th Grade)

Projects

- **Major Project: Simulated and implemented a Cosine Modulated Filter Bank (CMFB) for FPGA using Verilog in Vivado.**
Tools: Verilog, Vivado, MATLAB
 - Designed 32-tap FIR filters, each with 460 coefficients, emphasizing RTL design and modular hierarchy.
 - Focused on multirate signal decomposition suitable for real-time applications on FPGA.
 - Verified functionality using self-checking testbenches and waveform analysis in Vivado, showcasing digital design and hardware simulation skills.
- **Mini Project: Smart Library Management System using RFID**
Tools: Arduino, RFID, Python Flask, HTML/CSS/JS
 - Built an embedded system integrating RFID-based book tracking with a Flask web interface.
 - Interfaced Arduino with Python via serial communication for real-time issue/return handling.
 - Developed a responsive frontend and demonstrated hardware-software integration for automation use-cases.
- **GitHub: github.com/mishalp789/smart-library-rfid**
- **Mini CPU Core RTL Design**
Tools: Verilog, Icarus Verilog, GTKWave
 - Developed basic instruction-handling logic (MOV, HALT, registers) in a simple custom CPU core.
 - Verified instruction flow through waveform simulation using GTKWave.
- **GitHub: github.com/mishalp789**