Computer Architecture Homework #3

Verilog Exercise Matrix-Vector Multiplication

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Due 2019/12/3 13:00 Tuesday (CEIBA, no late homework is allowed.)

1. Introduction

In this exercise, you need to design a Verilog program to compute the operation 2*A*x + b. Vectors x and b are directly sent to your circuit and matrix A is stored in a memory. You need to access the memory to acquire the data and then compute the answer y. Here is an example of y = 2*A*x + b, where the dimension of matrix A is 2x2 and the size of vectors x and b is 2x1.

$$2 * \begin{bmatrix} 1 & 2 \\ 3 & 4 \end{bmatrix} * \begin{bmatrix} 3 \\ 2 \end{bmatrix} + \begin{bmatrix} 2 \\ 6 \end{bmatrix} = \begin{bmatrix} 16 \\ 40 \end{bmatrix}$$

In this exercise, the size of matrix A is 16x16 and the size of vectors x and b is 16x1. Each number in the matrix or vectors are represented with 8 bits. The numbers are unsigned. You don't need to consider overflow problem in this exercise, so the numbers of the output vector are also represented in 8 bits.

2. Specification

The input/output pins are defined in Table1:

Tabel1 :I/O pins specification

Signal name	Input / Output	Bit width	Description
CLK	I	1	Clock signal. Positive edge trigger.
RST	I	1	Active high **asynchronous** reset signal.
vector_x	I	128	Input data $\mathbf{x}_{16x1}$. This signal is consistent.
vector_b	I	128	Input data $\mathbf{b}_{16x1}$. This signal is consistent.
vector_y	O	128	Output data $\mathbf{y}_{16x1}$. It'll be checked when finish is 1.
Q	I	128	Input data sent from memory.
A	O	4	The address of the memory.
finish	O	1	Control signal. Set it 1 when all the computation is done; otherwise set it 0.

3. Timing Diagram for Memory

Fig. 1 shows the timing diagram for reading data from a memory. Here CEN is always 0 and WEN is always 1. You just need to control the address A in this exercise. Note that you may need to operate CEN and WEN signals by yourself in the future exercises. Here the memory stores matrix A. The i-th word in the memory represents $A_{i,0:15}$. You can change A to access different words in the memory.

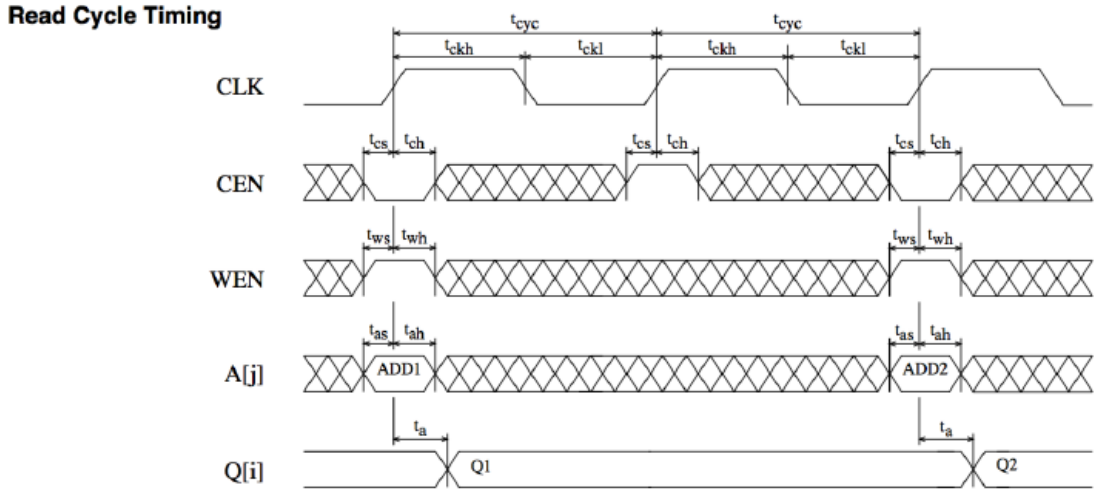

Figure 1: Read data from a memory

4. Simulation Scripts

4.1 Sample Code: findmax

Circuit findmax.v finds the max and argmax value for eight continuous inputs. Visit folder sample/findmax and run the following script.

ncverilog testfixture.v findmax.v +access+r

4.2 Sample Code: matvec2x2

Circuit matvec2x2.v computes matrix-vector multiplication Ax. In this sample, the size of matrix A is 2x2 and the size of vector x is 2x1. Visit folder sample/matvec2x2 and run the following script.

This sample is similar to the exercise. If you're not very familiar with Verilog, please make sure you fully understand this sample code.

ncverilog testfixture.v matvec2x2.v +access+r +define+tb1 +notimingchecks

4.3 RTL Simulation

ncverilog testfixture.v matvecmult.v +access+r +define+tb1 +notimingchecks

You can change between test cases by substituting tb1 to tb2

4.4 Synthesis

Please execute this script in syn folder. Synopsys Design Compiler will automatically

synthesize your RTL code into gate-level netlist following the commands in this script.

dc_shell

Run the code: **source run.tcl**

Please check if there's any error message (you can ignore most warning messages). If any, read the error messages and try to resolve them; if not, enter exit to leave Design Compiler.

4.5 Gate-level Simulation

ncverilog testfixture.v matvecmult_syn.v -v tsmc13.v +access+r +define+tb1+SDF

4.6 Debug

Use program nWave to view the simulated signals. This will be very helpful for this exercise.

nWave&

5. Files

The deadline for this exercise is 13:00, Dec. 3th. Please pack your files in a folder named CA_hw3_yourid, compress it into a HW3.zip file and then submit to CEIBA. There's a 5% penalty for incorrect upload format. No late submission is accepted.

Example:

./CA_hw3_r08943016/

- matvecmult.v (RTL file)
- matvecmult_syn.v (synthesized gate-level netlist)
- matvecmult_syn.ddc (Design database generated by Synopsys Design Compiler)
- matvecmult_syn.sdf (Pre-layout gate-level sdf)
- r08943016.pdf
- area.txt
- timing.txt

6. Grading Criteria

Item	Description
RTL correctness(30%)	Your matvecmult.v should give correct answer.
RTL tb3(hidden) (20%)	Additional test case besides the provided files
Gate level no latch(10%)	There are no latches in your gate level.
Gate-level correctness (20%)	Your matvecmult_syn.v should give correct answer.
Report (20%)	Snapchat: 1. rtl_tb1 2. rtl_tb2 3. gatelevel_tb1 4. gatelevel_tb2

	5. no latch 6. Timing report 7. Area report Please describe how you design this circuit and what difficulties you encountered when working on this exercise. (This exercise might be easy if you had experiences in Verilog. Please write down your Verilog experiences.)

Ref:

No latch

```
Inferred memory devices in process
        in routine matvecmult line 108 in file
                '/home/raid7_2/user08/r08016/TA/matvecmult_ans.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|     finish_reg      | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|    counter_r_reg    | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|        A_reg        | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|    vector_y_reg     | Flip-flop |  128  |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/user08/r08016/TA/matvecmult.db:matvecmult'
Loaded 1 design.
Current design is 'matvecmult'.
Using operating conditions 'slow' found in library 'slow'.
Warning: Setting attribute 'fix_multiple_port_nets' on design 'matvecmult'. (UIO-59)
Information: Checking out the license 'DesignWare'. (SEC-104)
Information: Evaluating DesignWare library utilization. (UISN-27)
```

Gate level:

```
START!!! Simulation Start .....

--------------------------------------------------

SDF File ./matvecmult_syn.sdf were used for this simulation.
================================================

 Congratulations!!! Your answer is correct!
```

Timing Report

```
  add_0_root_add_2_root_add_26_15/B[5] (matvecmult_DW01_add_0)
                                                          0.00       4.31 f
  add_0_root_add_2_root_add_26_15/U1_5/S (ADDFX2)         0.58       4.88 f
  add_0_root_add_2_root_add_26_15/SUM[5] (matvecmult_DW01_add_0)
                                                          0.00       4.88 f
  add_0_root_add_26_15/A[5] (matvecmult_DW01_add_30)      0.00       4.88 f
  add_0_root_add_26_15/U1_5/S (ADDFHX4)                   0.43       5.32 r
  add_0_root_add_26_15/SUM[5] (matvecmult_DW01_add_30)
                                                          0.00       5.32 r
  U236/Y (BUFX8)                                          0.23       5.55 r
  add_44/A_6_ (matvecmult_DW01_add_28)                    0.00       5.55 r
  add_44/U1_6/CO (CMPR32X2)                               0.47       6.02 r
  add_44/U1_7/Y (XOR3X2)                                  0.27       6.29 r
  add_44/SUM[7] (matvecmult_DW01_add_28)                  0.00       6.29 r
  U209/Y (NAND2X1)                                        0.13       6.42 f
  U271/Y (NAND2X2)                                        0.12       6.55 r
  vector_y_reg_15_/D (DFFRX2)                             0.00       6.55 r
  data arrival time                                                  6.55

  clock CLK (rise edge)                                   6.30       6.30
  clock network delay (ideal)                             0.50       6.80
  clock uncertainty                                      -0.10       6.70
  vector_y_reg_15_/CK (DFFRX2)                            0.00       6.70 r
  library setup time                                     -0.15       6.55
  data required time                                                 6.55
  ---------------------------------------------------------------------------
  data required time                                                 6.55
  data arrival time                                                 -6.55
  ---------------------------------------------------------------------------
  slack (MET)                                                        0.00
```

Area Report

```
dc_shell> report_area

****************************************
Report : area
Design : matvecmult
Version: N-2017.09-SP2
Date   : Sat Nov  9 16:23:28 2019
****************************************

Library(s) Used:

    slow (File: /home/raid7_2/course/cvsd/CBDK_IC_Conte

Number of ports:                         1538
Number of nets:                          3553
Number of cells:                         1893
Number of combinational cells:           1676
Number of sequential cells:               170
Number of macros/black boxes:               0
Number of buf/inv:                        225
Number of references:                      86

Combinational area:              26119.591118
Buf/Inv area:                     1573.489776
Noncombinational area:            5163.490818
Macro/Black Box area:                0.000000
Net Interconnect area:          201087.680267

Total cell area:                 31283.081936
Total area:                     232370.762204
1
```