臺灣大學

# IC Design
# HW2 Tutorial

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# Outline

- Connect to workstations
- Flow chart
- Transistor-level Simulation: HSPICE
- Debug tool: nWave

# Connect to Workstations

## MobaXterm

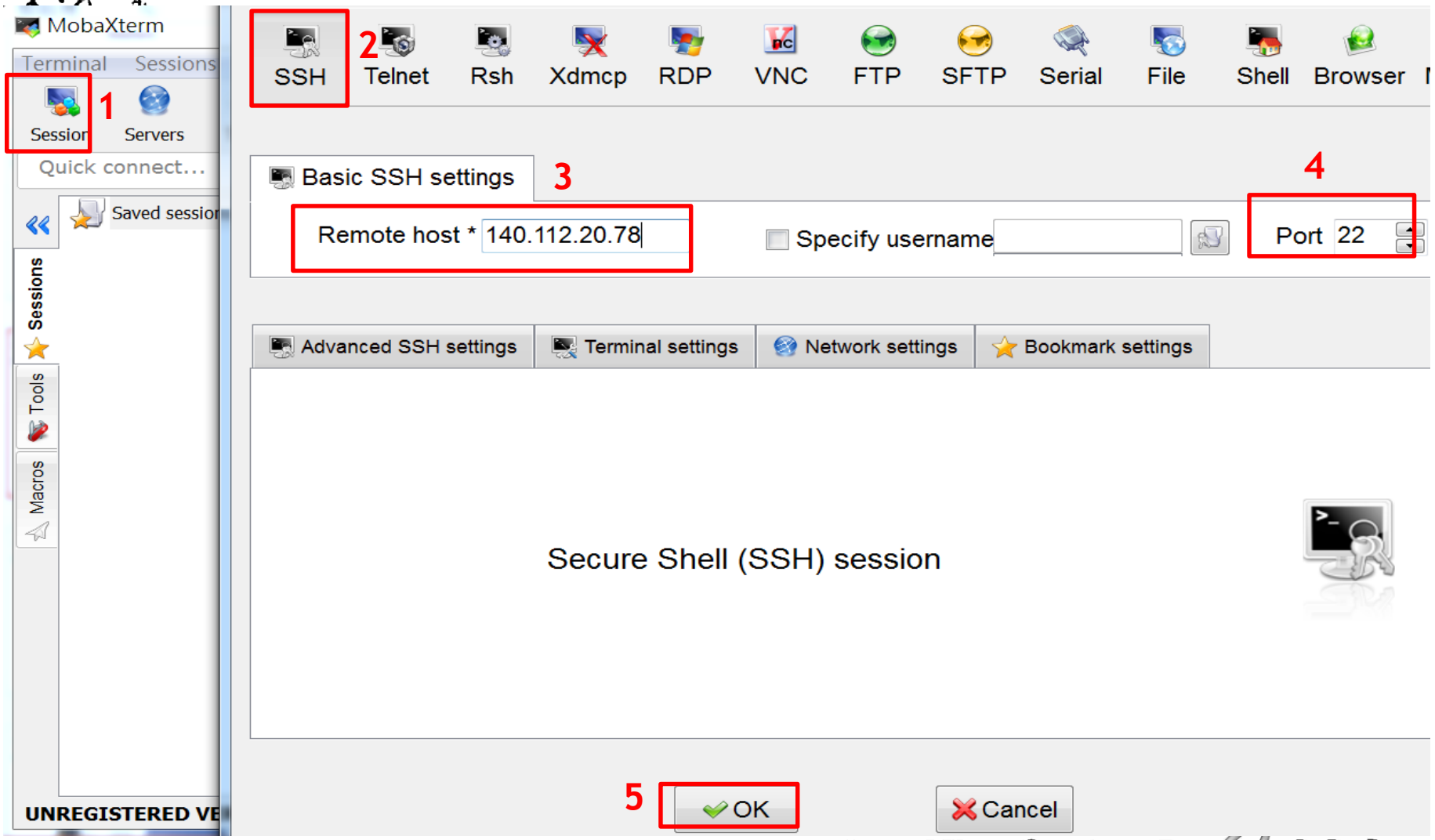
# Preparatory Works

- Download MobaXterm
  - http://mobaxterm.mobatek.net/download-home-edition.html
  - MobaXterm Home Edition v9.4 Portable edition

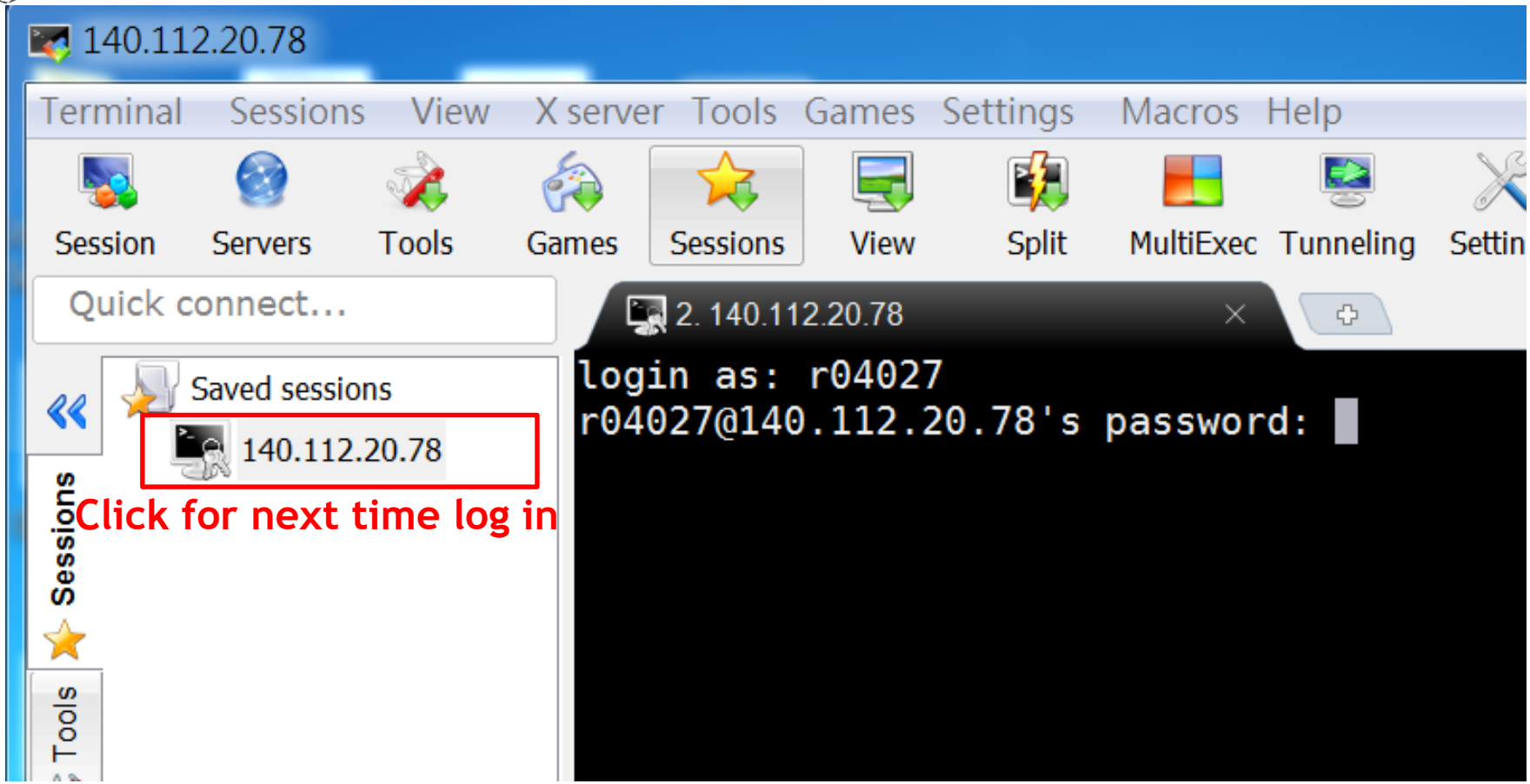
- Choose an Workstation IP
  - http://cad.ee.ntu.edu.tw/wordpress/?p=33
  - Use 140.112.20.72/74/83/84
  - You can try it and find appropriate IP

# Connect Workstation

- MobaXterm→Session→SSH→Remote host:IP Port:22



# Log-In (1/2)


140.112.20.78
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Settin
Quick connect...
Saved sessions
140.112.20.78
Click for next time log in
Sessions
Tools
2. 140.112.20.78
login as: r04027
r04027@140.112.20.78's password:

# Log-In (2/2)

- User Name
  - Ex: For NTUEE(901) and GIEE(943) student, remove 901/943

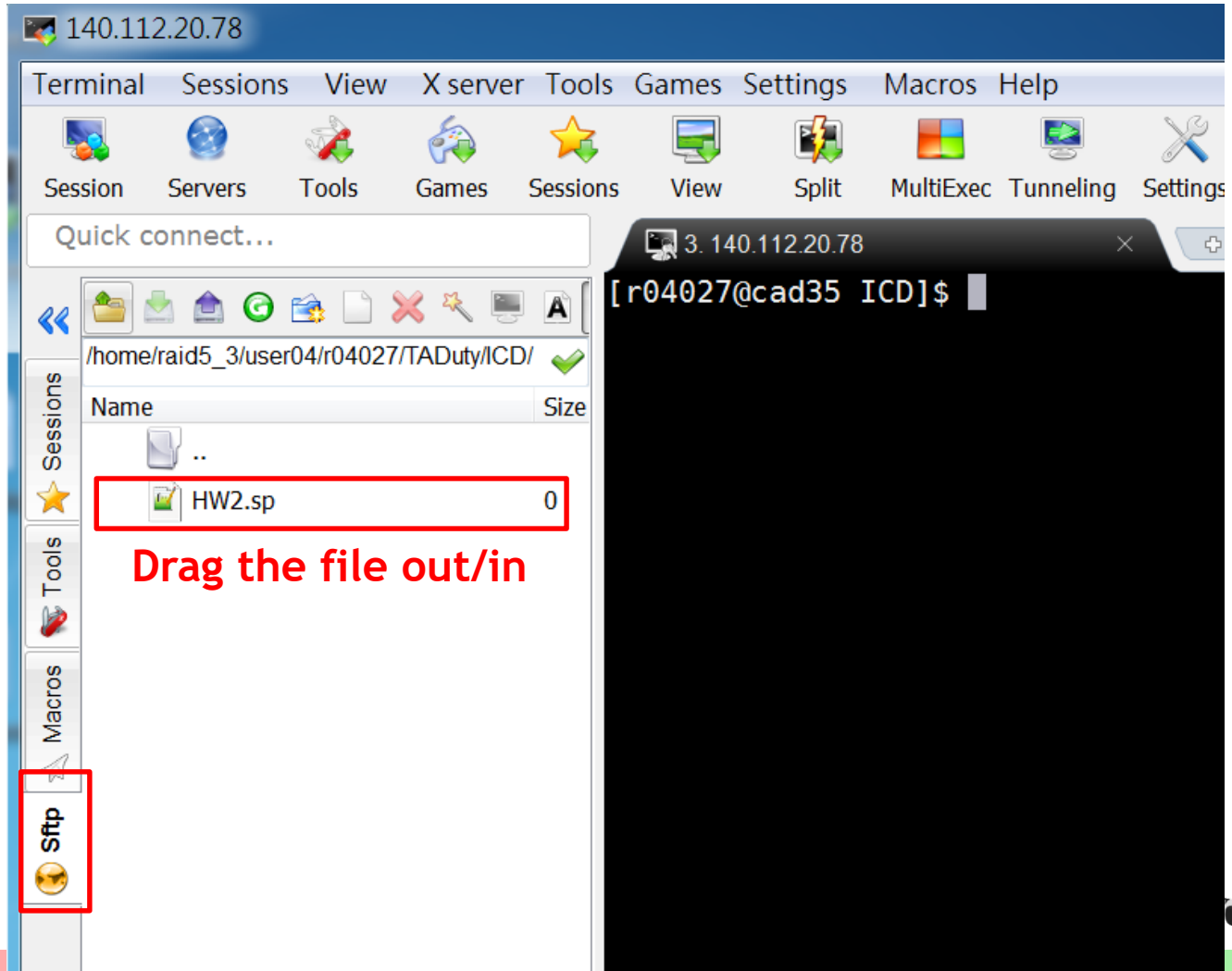
    r04943027 -> r04027

    b01901123 -> b01123
  - Ex: For other NTU student, remove number right after first English character

    b96502040 -> b6502040
- Password
  - What you fill in application form

# Down/Upload File From Workstation

- Just drag the file in/out left hand side file list



# Simple Linux command

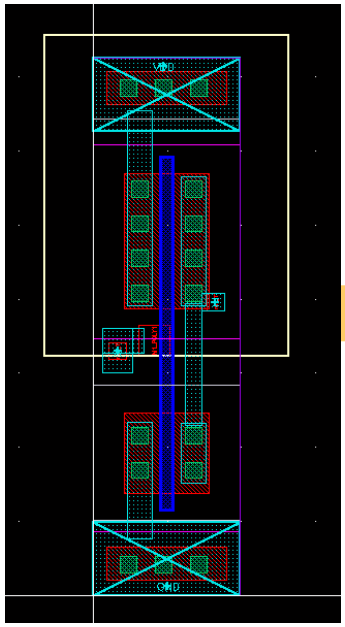
- Source the setting file
  - source
- Document management
  - cd [directory name/..] : Move to other directory
  - cd .. : Move to upper directory
  - ls [-a/-l] : List all files in current directory
  - mkdir [directory name] : Create new directory
  - cp [source] [destination] : Copy file
  - rm [file/directory] : Remove file
  - mv [source] [destination] : Rename file
- Text Editor
  - vim
- More in “鳥哥的Linux 私房菜” http://linux.vbird.org/

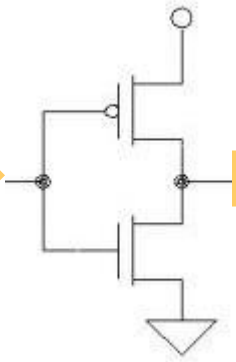
# Source the needed files

- Need to do it every time when you log in
- Cadence tool
  - source /usr/cadence/cshrc
- HSPICE
  - source /usr/cad/synopsys/CIC/hspice.cshrc
- nWave
  - source /usr/spring_soft/CIC/verdi.cshrc

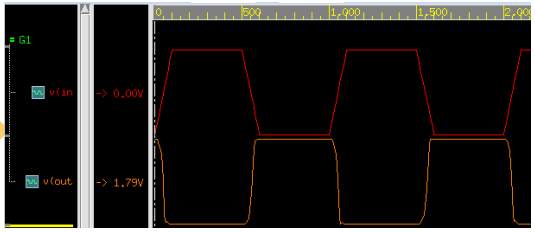
# Flow Chart

Picture → Your job: Write netlist, draw transistor level and give input → *.sp 90nm_bulk.l → Hspice → *.tr0 → nWave



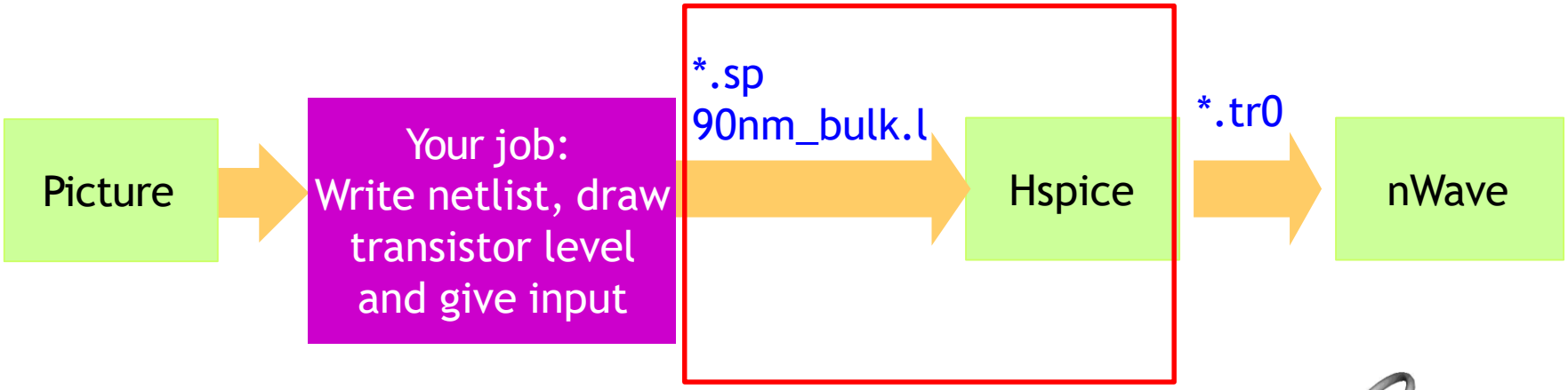


```
.SUBCKT Inv DVDD GND In Out
MM1 Out In GND GND NMOS l=0.1u w=0.25u m=1
MM2 Out In DVDD DVDD PMOS l=0.1u w=0.5u m=1
.ENDS
```



# HSPICE

## Transistor-level Simulation



# Hspice Syntax(1/7)

- Create an Hspice file “*.sp”
- Edit with text editors such as WordPad or Notepad++
- First line must be a comment line or be left blank.
- Comment start with *
- Remember to .inc ’90nm_bulk.l’
- Case sensitive
- “0” means ground
- Transistor name must start with “M”
- Sub-circuit name must start with “x”

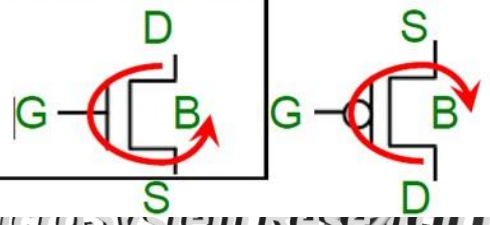
# Hspice Syntax (2/7)

- Hspice codes compose of three parts:

  (1)include lib file (2)define sub-circuit (3)input signal

```
*********************************************************************************
.inc '90nm_bulk.l'                                    <-- (1)source library
.SUBCKT    Inv    DVDD   GND    In   Out
*.PININFO DVDD:I GND:I In:I Out:O
MM1    Out    In     GND      GND      NOMS      l=0.1u      w=0.25u     m=1
MM0    Out    In     DVDD     DVDD     PMOS      l=0.1u      w=0.5u      m=1   <-- (2)transistors
.ENDS  D      G      S        B        Type      L           W
*********************************************************************************
        start  end
        node   node
Vdd    DVDD   0     1.8
Vss    GND    0     0

Vin    In     0     pulse(0 1.8 0 100n 100n 0.4u 1u)   <-- (3)Input a square wave

x1     DVDD   GND    In   Out    Inv                   <-- (2)Include a sub-circuit
            simulation time
.tran 10n 1.1u                                        <-- (3)scan transient
.op
.option post
.end
```

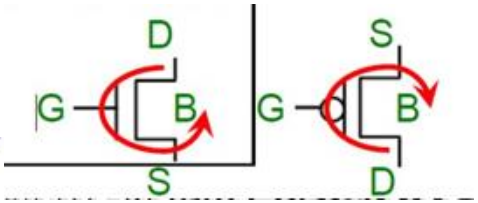
simulation



# Hspice Syntax (3/7)

- Define sub-circuit (Transistor name must start with “M”)
  - Start with .SUBCKT, end with .ENDS

Sub-circuit name  Port name(Input first, Output last)




```
.SUBCKT   Inv     DVDD   GND    In   Out
*.PININFO DVDD:I GND:I In:I Out:O
MM1       Out     In     GND    GND    NOMS    l=0.1u    w=0.25u   m=1
MM0       Out     In     DVDD   DVDD   PMOS    l=0.1u    w=0.5u    m=1
.ENDS     D       G      S      B      Type    L         W
```

Transistor name

- Set VDD GND (DVDD and GND are nodes’ name)

Node name  ground

```
Vdd   DVDD   0   1.8
Vss   GND    0   0
```

Voltage

- Call sub-circuit (Sub-circuit name must start with “x”)

sub-circuit port(Same order as defined)

```
x1   DVDD   GND   In   Out   Inv
```

sub-circuit name  sub-circuit type

# Hspice Syntax(4/7)

- Model input AC signal: pulse

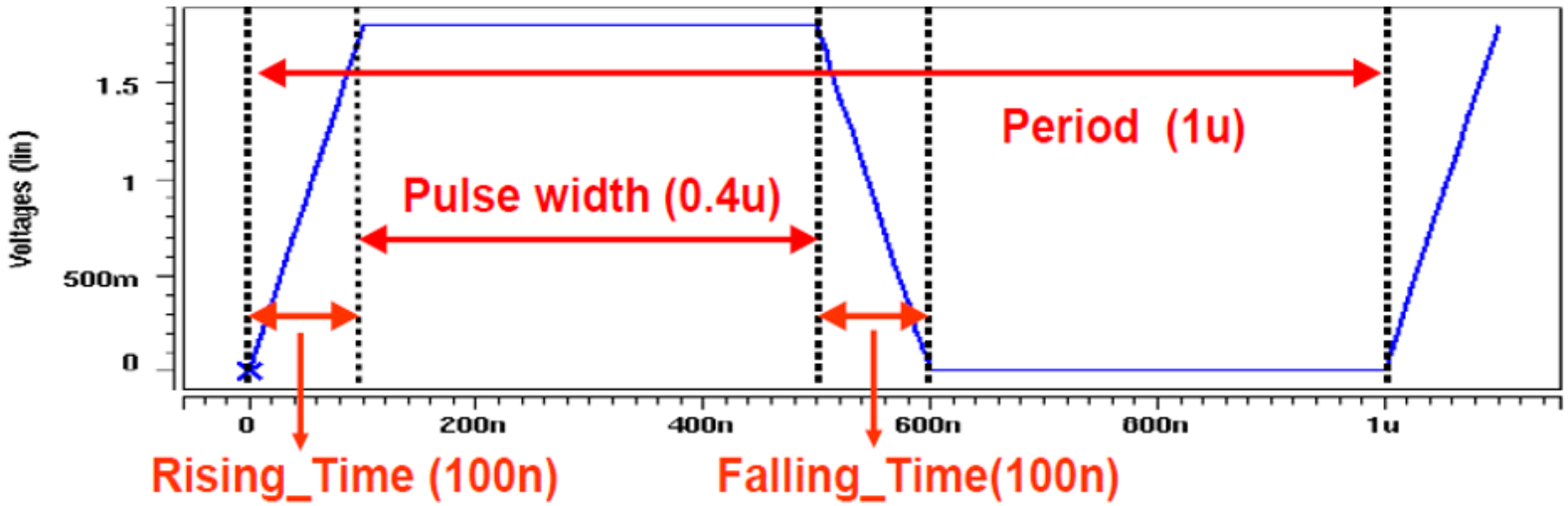
```
Vin    In     0    pulse(0 1.8 0 100n 100n 0.4u 1u)
```

voltage_name node1 node2 pulse( GND VDD delay_time

rising_time falling_time pulse_width period)

Example : Vin In 0 pulse(0 1.8 0 100n 100n 0.4u 1u)

Node name

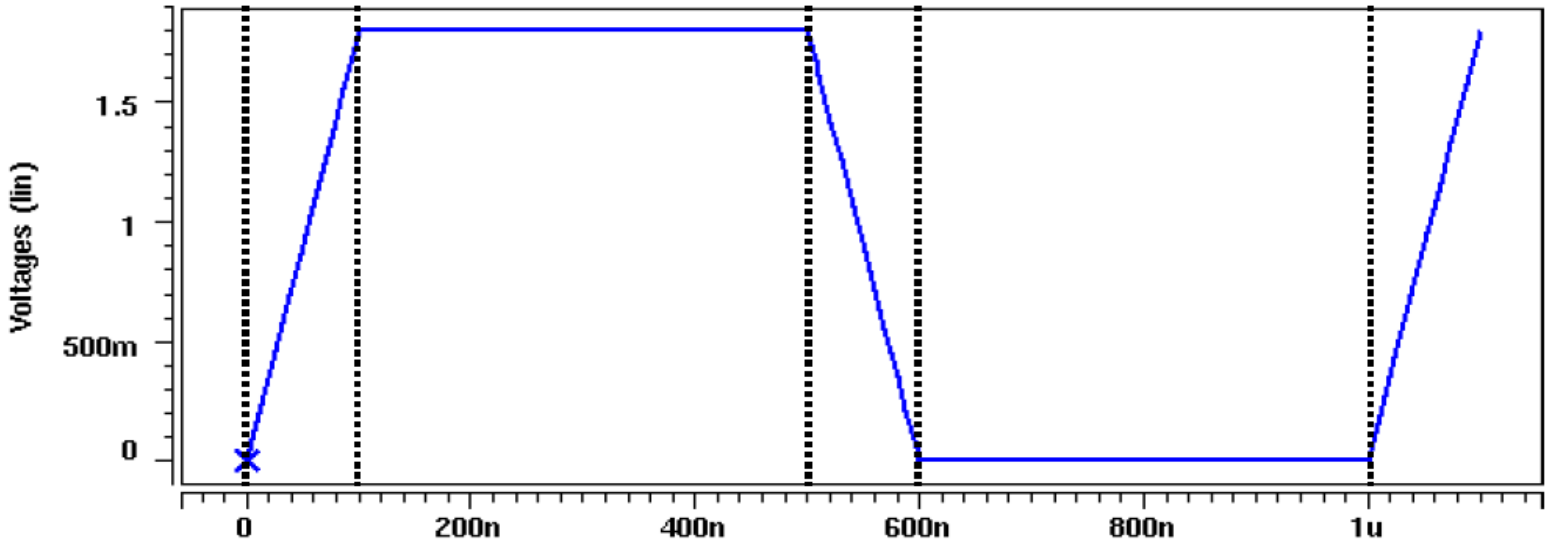


# Hspice Syntax (5/7)

- Another signal waveform: pwl (recommended)

PWL( {time1} {v1} {time2} {v2} ... {time3} {v3} )

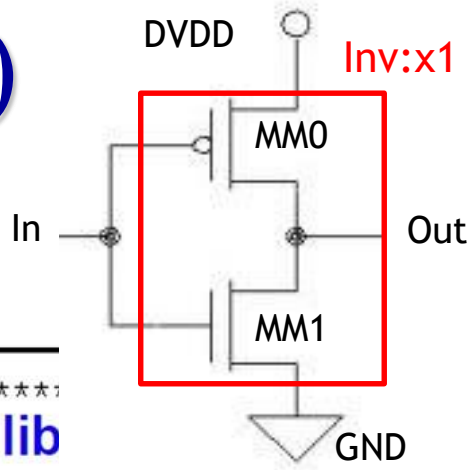
Example : Vin In 0 pwl(0n 0v 100n 1.8v 500n 1.8v 600n 0v ...)



# Hspice Syntax(6/7)

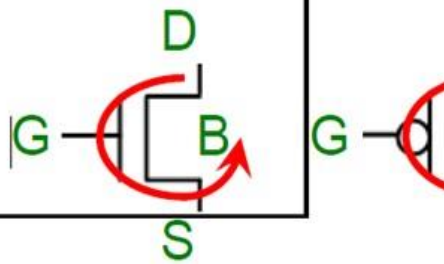
- Define DC voltage source: Vvdd(name) vdd(vddport) gnd 1.8V
- .tran 多久取樣一次 總共模擬多久，可改動，Ex .tran 10n 1u
- .op (計算操作點電壓 operation point ，基本上都要加)
- .option post (轉出檔案(ex: .tr0 file…)給scope用 ，基本上都要加)
- .end

# Hspice Syntax(7/7)




- It an inverter circuit

```
*********************************************************************
.inc '90nm_bulk.l'                                  <-- (1)source lib
.SUBCKT    Inv    DVDD   GND    In   Out
*.PININFO DVDD:I GND:I In:I Out:O
MM1    Out    In     GND      GND      NOMS      l=0.1u      w=0.25u    m=1
MM0    Out    In     DVDD     DVDD     PMOS      l=0.1u      w=0.5u     m=1   <-- (2)transist
.ENDS  D      G      S        B        Type      L           W

*********************************************************************


Vdd    DVDD   0    1.8
Vss    GND    0    0

Vin    In     0    pulse(0 1.8 0 100n 100n 0.4u 1u)   <-- (3)Input a square wave

x1     DVDD   GND    In   Out    Inv                  <-- (2)Include a sub-circuit

.tran 10n 1.1u                                      <-- (3)scan transient
.op
.option post
.end
```



# Hspice Simulation (1/2)

- SPICE is generally a circuit analysis tool for simulation of electrical circuits in steady-state, transient, and frequency domains
- Source your environment setting file
  - source /usr/cad/synopsys/CIC/hspice.cshrc
- Upload .sp file and 90nm_bulk.l to workstation by dragging into MobaXterm

# Hspice Simulation (2/2)

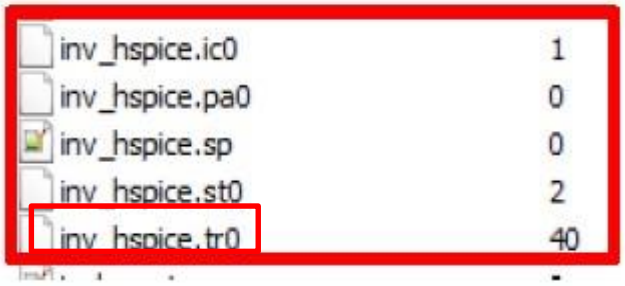
- Save Hspice file and run simulation
  - hspice [hspice file]，Ex. hspice hw2.sp
- Error

```
                ***** job aborted
>info:          ***** hspice job aborted
 lic: Release hspice token(s)
```

- Successful

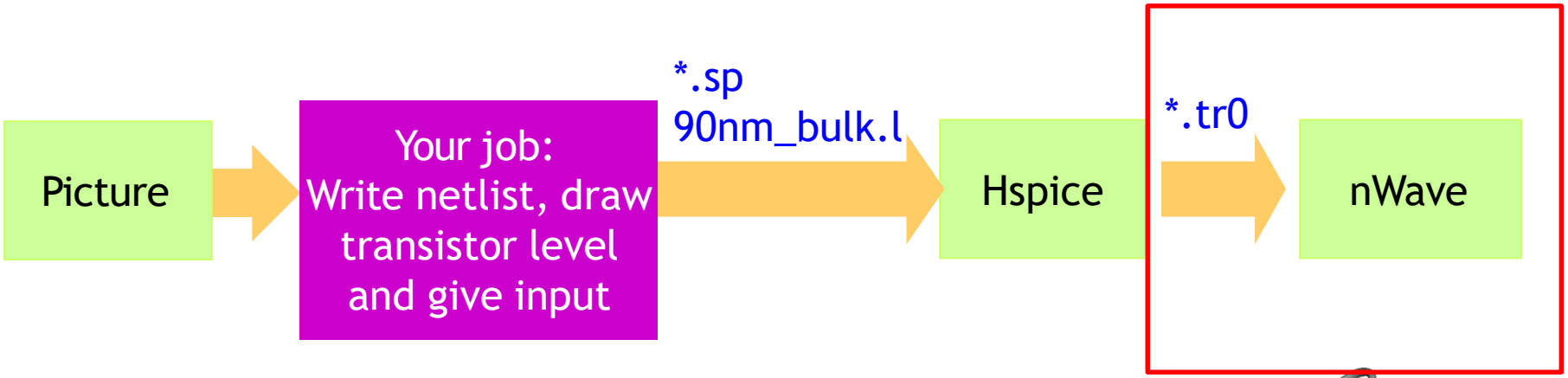
```
>info:          ***** hspice job concluded
 lic: Release hspice token(s)
real 0.56
```

- Output wave file(.tr0)



# Debug tool

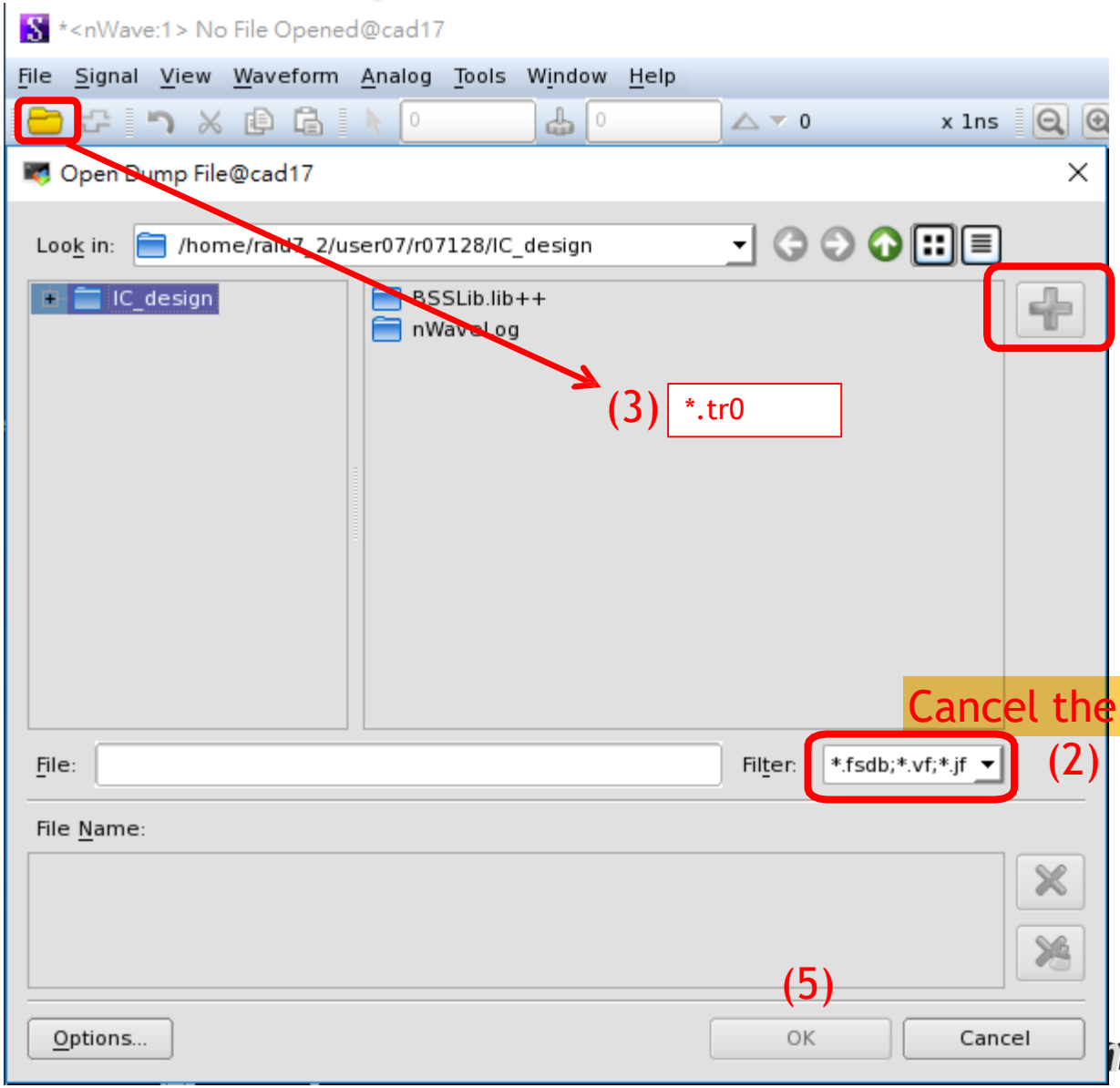
## nWave



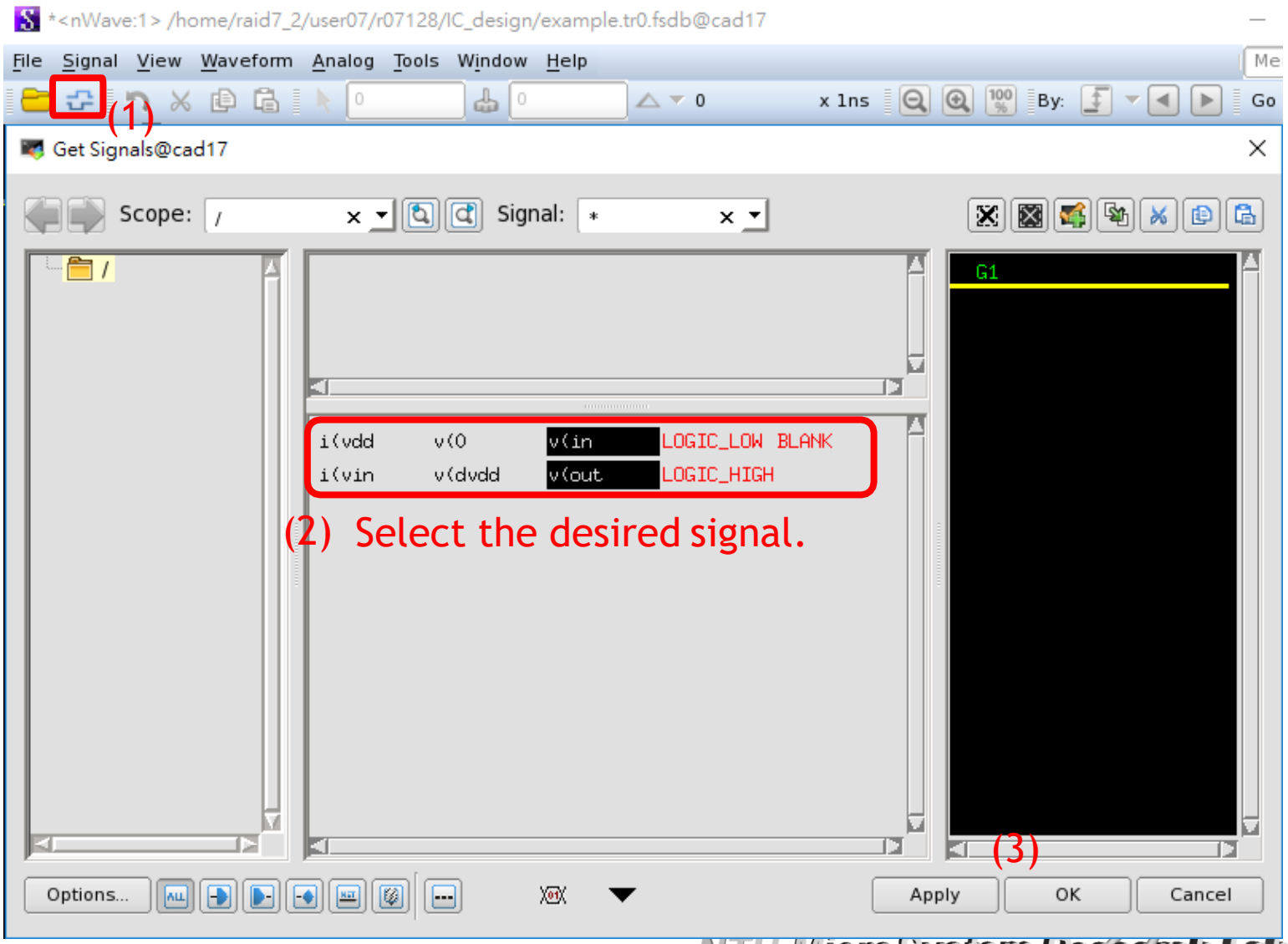
# nWave: Source File and Execute

- Source
  - source /usr/spring_soft/CIC/verdi.cshrc
- Execute nWave
  - nWave &

# Select Output File Generated by Hspice

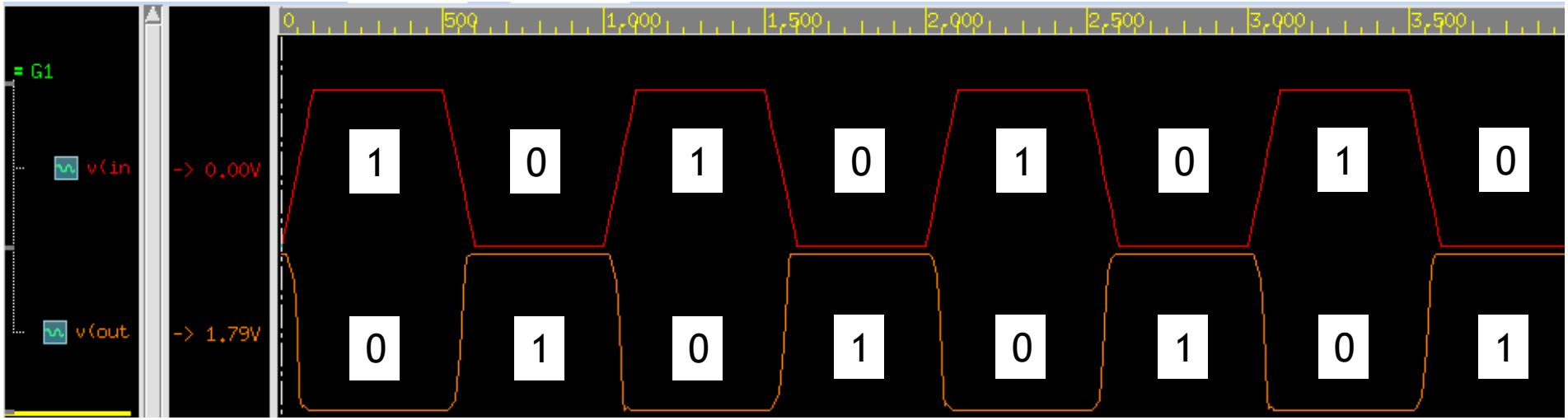


# Select Desired Signal



# Check Waveform

- Remember to check all possible input
- Record the waveform into your report
- Ex: Inverter



# Reminder

- Be patient and careful about each step!
- References
  - [1] “SPICE,” CIC handout, 2001
  - [2] “鳥哥的Linux 私房菜” http://linux.vbird.org/
- If there’s any workstation account/password problem, please directly contact workstation administrator
  - 邱茂菱，d01943010@ntu.edu.tw
- If you have any questions, please contact TA
  - 王鈺凱，EE2-329，r06943124@ntu.edu.tw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# Thanks for your attention!

Q & A