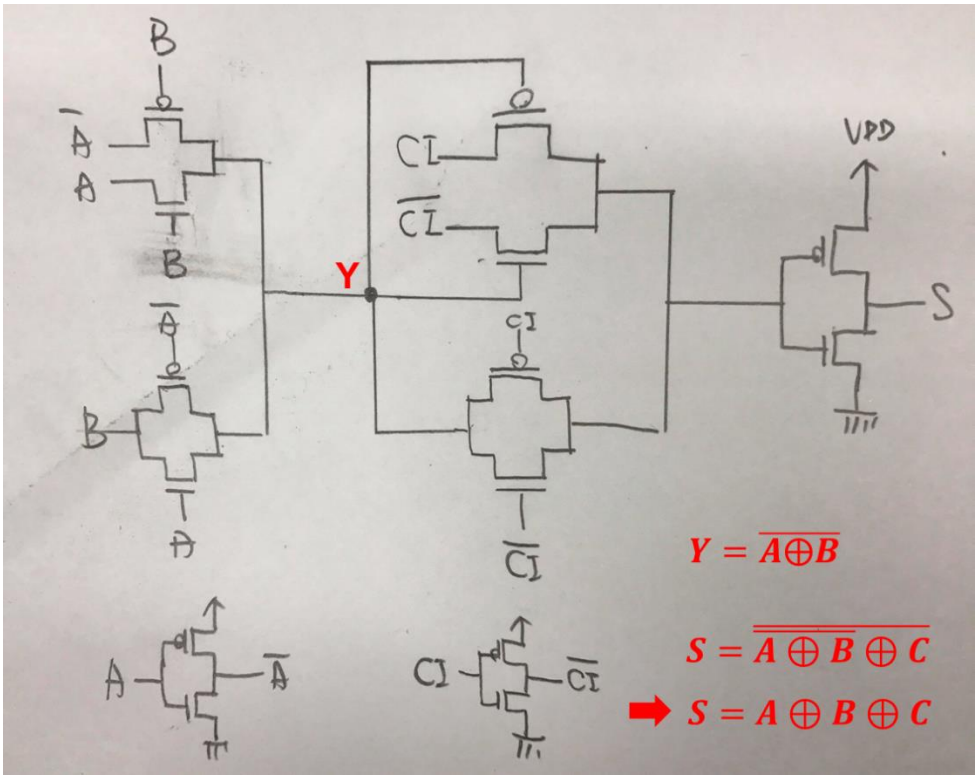
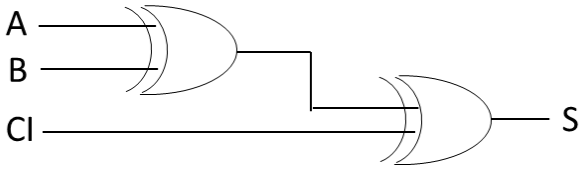
# HW2 參考解答

**1.(70%, each for 35%) 這邊舉 FA1 圖的右半部為例(Sum)**

Transistor-level (10%)




Gate-level circuit (1%)




Truth table (5%)

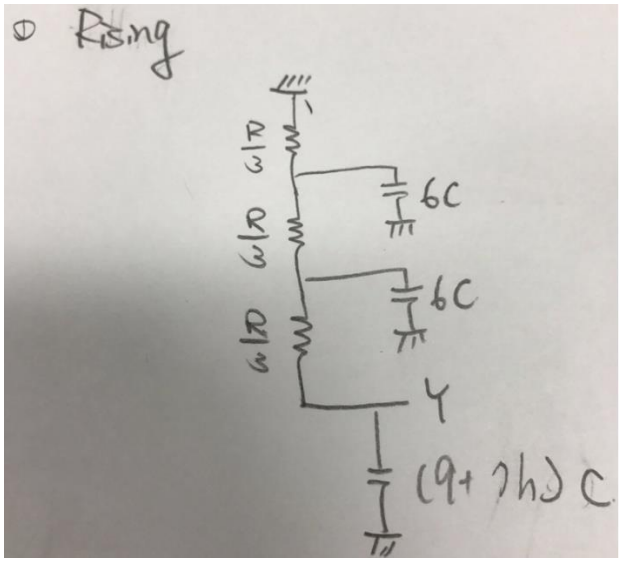
| A | B | CI | S |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

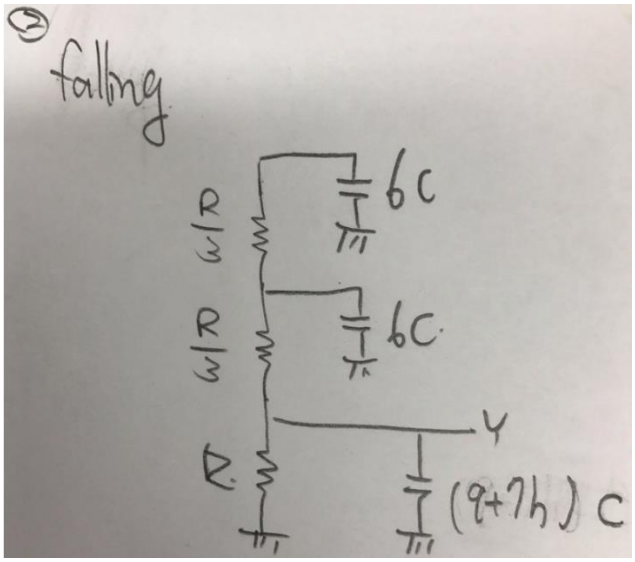
Waveform (10%) Code (4%) Discuss problems you have encountered. (5%)

**2. (20%)**

Rising delay (10%) Falling delay (10%)

等效電路圖如下，使用 Elmore delay model 來求出 rising & falling delay




**3. (10%)**

Dynamic power (5%,reason for 4%)

Static power (5%, reason for 4%)

$V_{DD}$ ↓ ， Due to $P_{sw} = \alpha C V_{DD}^2 f$ ， Dynamic power ↓

To maintain clock speed , we will to reduce $V_t$ , but the leakage current will increase .

So the $P_{static}$ will ↑