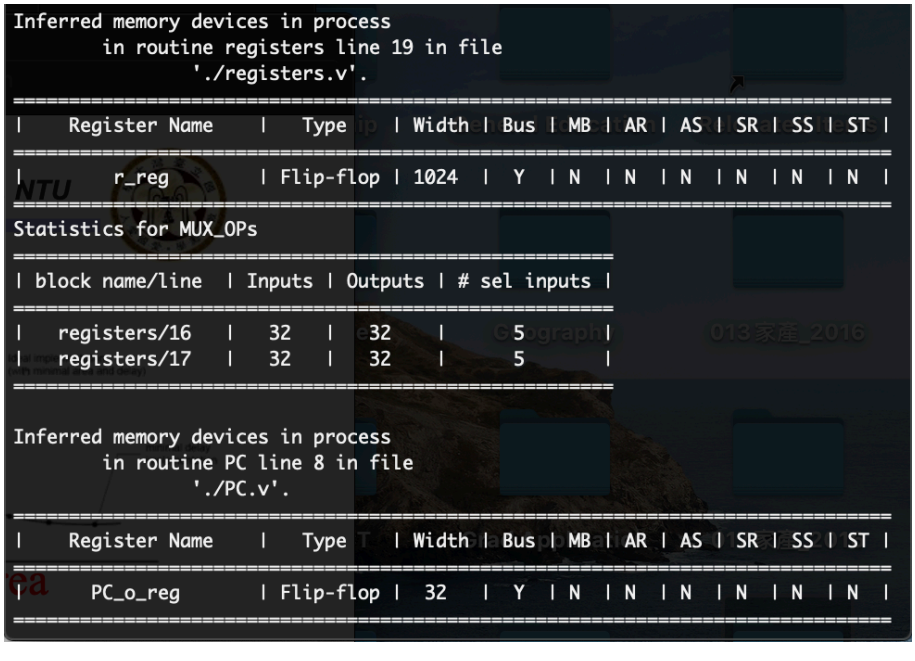
MIPS (files for RTL simulation: ALU.v/control.v/registers.v/ PC.v/sign_extend.v/add.v)

1. Simulated timing (ns): 5.5
2. Area (um^2):

dc_shell> report_area

```
****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Mon May  4 15:16:11 2020
****************************************
Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                          277
Number of nets:                          6365
Number of cells:                         6186
Number of combinational cells:           5161
Number of sequential cells:              1024
Number of macros/black boxes:               0
Number of buf/inv:                       1491
Number of references:                      76

Combinational area:          40053.548695
Buf/Inv area:                 7692.616757
Noncombinational area:       27835.662176
Macro/Black Box area:            0.000000
Net Interconnect area:      748817.081665

Total cell area:             67889.210871
Total area:                 816706.292536
```

3. Cost (A*T): 373390.6597905
4. Screenshot:



```
Inferred memory devices in process
        in routine registers line 19 in file
                './registers.v'.
===========================================================================
|    Register Name    |   Type   | Width | Bus | MB | AR | AS | SR | SS | ST |
===========================================================================
|      r_reg          | Flip-flop | 1024  |  Y  | N  | N  | N  | N  | N  | N  |
===========================================================================
Statistics for MUX_OPs
=============================================
| block name/line  | Inputs | Outputs | # sel inputs |
=============================================
|   registers/16   |   32   |   32    |      5       |
|   registers/17   |   32   |   32    |      5       |
=============================================

Inferred memory devices in process
        in routine PC line 8 in file
                './PC.v'.
===========================================================================
|    Register Name    |   Type   | Width | Bus | MB | AR | AS | SR | SS | ST |
===========================================================================
|      PC_o_reg       | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
===========================================================================
```

RISCV (files for RTL simulation: ALU.v/control.v/registers.v/ PC.v/ImmGen.v/add.v)

1. Simulated timing (ns): 6.5
2. Area (um^2):

dc_shell> report_area

```
****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Sat Apr 25 18:48:16 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/
typical.db)

Number of ports:                  163
Number of nets:                  6231
Number of cells:                 5367
Number of combinational cells:           4343
Number of sequential cells:              1024
Number of macros/black boxes:               0
Number of buf/inv:                       749
Number of references:                     97

Combinational area:          39953.401327
Buf/Inv area:                 5204.228406
Noncombinational area:       27818.688173
Macro/Black Box area:            0.000000
Net Interconnect area:      709663.559052

Total cell area:             67772.089500
Total area:                 777435.648552
```

3. Cost (A*T): 440518.58175
4. Screenshot:

```
Inferred memory devices in process
        in routine PC line 8 in file
                './PC.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      PC_o_reg       | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================
Warning:  ./control.v:21: DEFAULT branch of CASE statement cannot be reached. (ELAB-311)

Statistics for case statements in always block at line 16 in file
        './control.v'
============================================
|           Line           |  full/ parallel  |
============================================
|            17            |    auto/auto     |
|            19            |    auto/auto     |
|            21            |    auto/auto     |
============================================
Warning:  ./registers.v:26: DEFAULT branch of CASE statement cannot be reached. (ELAB-311)

Statistics for case statements in always block at line 19 in file
        './registers.v'
============================================
|           Line           |  full/ parallel  |
============================================
|            26            |    auto/auto     |
============================================

Inferred memory devices in process
        in routine registers line 19 in file
                './registers.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       r_reg         | Flip-flop | 1024  |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================
```

RISCV_RV32IC (files for RTL simulation: ALU.v/control.v/ registers.v/PC.v/ImmGen.v/add.v/decompressor.v)

1. Simulated timing (ns): 8.5
2. Area (um^2):

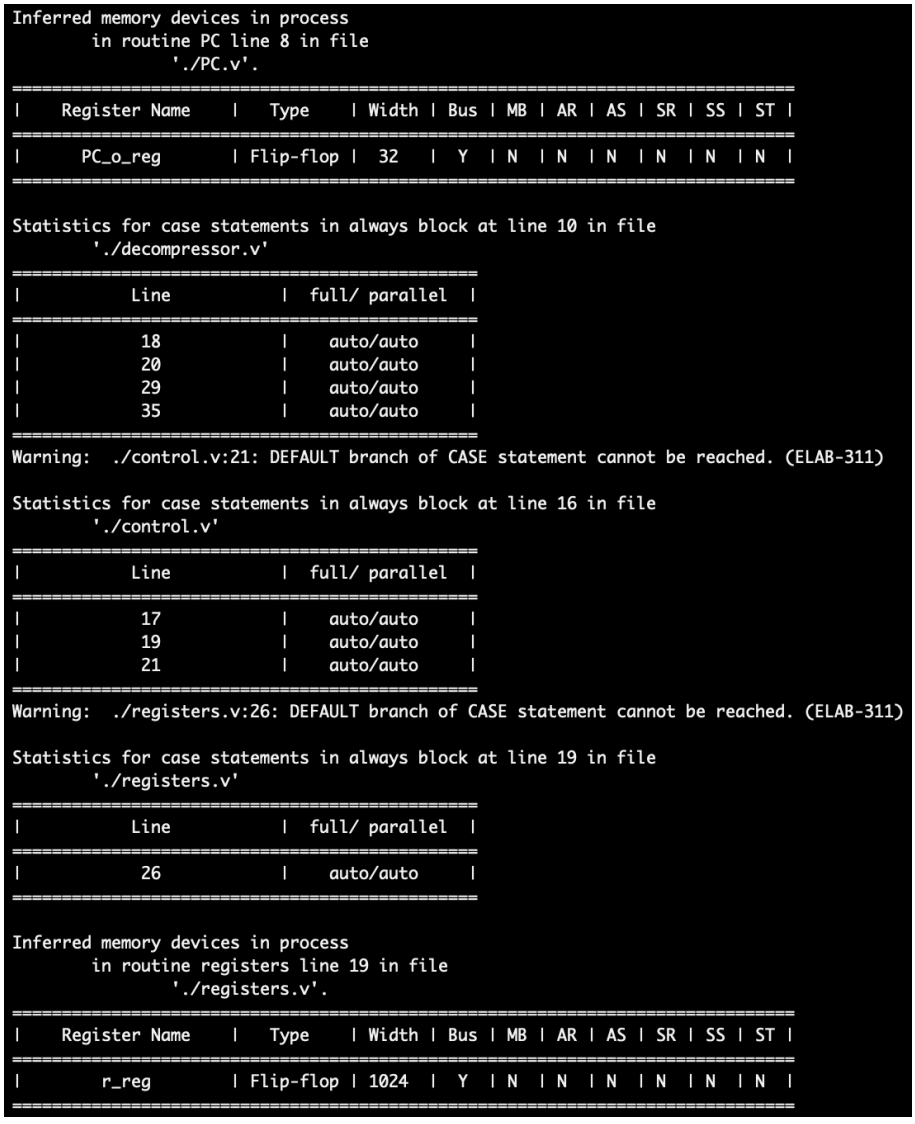
dc_shell> report_area

```
****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Thu Apr 30 16:32:02 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                  163
Number of nets:                  6568
Number of cells:                 5574
Number of combinational cells:           4550
Number of sequential cells:              1024
Number of macros/black boxes:               0
Number of buf/inv:                       638
Number of references:                    101
```

Combinational area: 40174.063345
Buf/Inv area: 4235.012983
Noncombinational area: 27810.201172
Macro/Black Box area: 0.000000
Net Interconnect area: 727490.314301

Total cell area: 67984.264517
Total area: 795474.578818

3. Cost (A*T): 577866.2483945
4. Screenshot:



```
Inferred memory devices in process
        in routine PC line 8 in file
                './PC.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      PC_o_reg       | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================

Statistics for case statements in always block at line 10 in file
        './decompressor.v'
===============================================
|           Line           |  full/ parallel  |
===============================================
|            18            |    auto/auto     |
|            20            |    auto/auto     |
|            29            |    auto/auto     |
|            35            |    auto/auto     |
===============================================
Warning:  ./control.v:21: DEFAULT branch of CASE statement cannot be reached. (ELAB-311)

Statistics for case statements in always block at line 16 in file
        './control.v'
===============================================
|           Line           |  full/ parallel  |
===============================================
|            17            |    auto/auto     |
|            19            |    auto/auto     |
|            21            |    auto/auto     |
===============================================
Warning:  ./registers.v:26: DEFAULT branch of CASE statement cannot be reached. (ELAB-311)

Statistics for case statements in always block at line 19 in file
        './registers.v'
===============================================
|           Line           |  full/ parallel  |
===============================================
|            26            |    auto/auto     |
===============================================

Inferred memory devices in process
        in routine registers line 19 in file
                './registers.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|        r_reg        | Flip-flop | 1024  |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================
```