cache_dm.v

(1) Cycle time: 10 (ns)

(2) General spec:

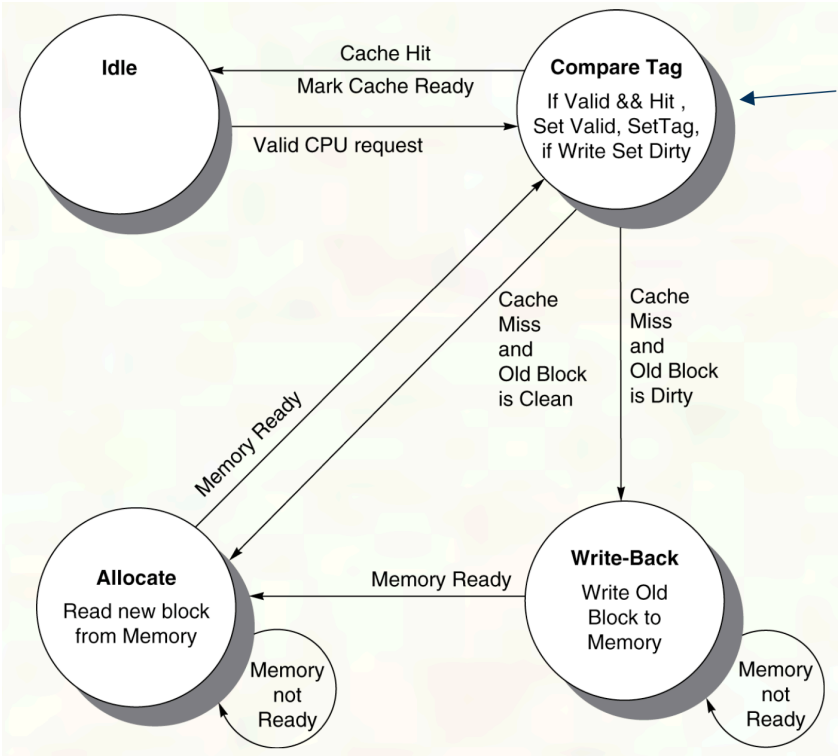
- Number of words: 32 words (8 blocks x 4 words)

Block	Tag (25 bits)	Data (4 words)
0		
1		
2		
3		
4		
5		
6		
7		

- Placement policy: directed mapped
- Address format:
  - Tag: 25 bits
  - Index: 3 bits
  - Offset: 2 bits
- Block details:
  - Total: 155 bits per block
  - Valid: 1 bit
  - Dirty: 1 bit
  - Tag: 25 bits
  - Data: 128 bits (4 words)

(3) Read/write policy: write-back, write allocate

(4) FSM:



- IDLE: No operation.
- COMPARE_TAG: 讀取由processor傳來的proc_read或是proc_write的訊號，再執行讀或寫等動作。若block_hit為high，則直接讀取或是寫入cache block，再回到idle state。若block_hit為low，則視block是否為dirty再決定要不要先write back或是直接進行write allocate。
- WRITE_BACK: 若block_hit為low且block為dirty，則把該block的data寫回memory（更新memory）。Write back成功後進入allocate stage。
- ALLOCATE: 若block_hit為low且block為clean，表示cache block data和memory data一致，所以直接把目標memory address的data直接寫入，再進到compare tag stage。

(5) Performance evaluation:

- No latch:

```
Inferred memory devices in process
      in routine cache line 192 in file
            '/home/raid7_2/userb05/b05013/DSD_HW4/cache_dm.v'.
==========================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
==========================================================================
|   mem_addr_r_reg    | Flip-flop |  28   |  Y  | N  | N  | N  | N  | N  | N  |
|   mem_wdata_r_reg   | Flip-flop |  128  |  Y  | N  | N  | N  | N  | N  | N  |
|  current_state_reg  | Flip-flop |   2   |  Y  | N  | N  | N  | N  | N  | N  |
|      block_reg      | Flip-flop | 1240  |  Y  | N  | N  | N  | N  | N  | N  |
|  proc_rdata_r_reg   | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
|  proc_stall_r_reg   | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
==========================================================================
```

- report_area:

```
****************************************
Report : area
Design : cache
Version: N-2017.09-SP2
Date   : Tue May 26 16:24:10 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/
typical.db)

Number of ports:                          386
Number of nets:                          5698
Number of cells:                         5471
Number of combinational cells:           4040
Number of sequential cells:              1431
Number of macros/black boxes:               0
Number of buf/inv:                       1517
Number of references:                      66

Combinational area:              38700.719633
Buf/Inv area:                     8790.834643
Noncombinational area:           38868.762001
Macro/Black Box area:                0.000000
Net Interconnect area:          774764.137756

Total cell area:                 77569.481634
Total area:                     852333.619391
```

- report_timing:

```
****************************************
```

```
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : cache
Version: N-2017.09-SP2
Date   : Tue May 26 16:24:17 2020
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: proc_addr[4]
              (input port clocked by CLK)
  Endpoint: block_reg[0][0]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  cache              tsmc13_wl10           slow

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.50       0.50
  input external delay                     0.30       0.80 f
  proc_addr[4] (in)                        0.01       0.81 f
  U4338/Y (CLKINVX1)                       0.20       1.01 r
  U4373/Y (CLKINVX2)                       0.30       1.31 f
  U5305/Y (NAND3X1)                        0.36       1.67 r
  U5034/Y (INVX4)                          0.33       2.00 f
  U4752/Y (BUFX20)                         0.34       2.34 f
  U5004/Y (AO22X1)                         0.29       2.63 f
  U6256/Y (NOR4X1)                         0.40       3.03 r
  U6257/Y (OAI22XL)                        0.19       3.21 f
  U5444/Y (AOI221XL)                       0.35       3.56 r
  U4340/Y (NAND4XL)                        0.18       3.75 f
  U4329/Y (NOR3XL)                         0.42       4.17 r
  U4326/Y (NAND3X2)                        0.29       4.46 f
  U4325/Y (OAI21XL)                        0.40       4.86 r
  U4324/Y (NAND2X2)                        0.32       5.19 f
  U4323/Y (NOR2X1)                         0.61       5.80 r
  U4374/Y (NOR2XL)                         0.27       6.07 f
  U6718/Y (BUFX4)                          0.36       6.43 f
  U6719/Y (NOR2X1)                         0.65       7.08 r
  U4315/Y (BUFX20)                         0.46       7.54 r
  U7350/Y (OAI222XL)                       0.21       7.76 f
  block_reg[0][0]/D (DFFQX2)               0.00       7.76 f
  data arrival time                                   7.76

  clock CLK (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.50      10.50
  clock uncertainty                       -0.10      10.40
  block_reg[0][0]/CK (DFFQX2)              0.00      10.40 r
  library setup time                      -0.20      10.20
  data required time                                 10.20
  -----------------------------------------------------------
  data required time                                 10.20
  data arrival time                                  -7.76
  -----------------------------------------------------------
  slack (MET)                                         2.44
```

- miss rate, execution cycles, stalled cycles:

```
Processor: Read initial data from memory.
    Done correctly so far! ^_^

        >>>> Read session 1:      3588 cycles

        >>>> hit:   1278

        >>>> miss:  1279

        >>>> miss rate: 50.02%

Processor: Write new data to memory.
    Finish writing!

        >>>> Write session:       5072 cycles

        >>>> write hit:   1279

        >>>> write miss:  1280

        >>>> miss rate: 50.02%

Processor: Read new data from memory.
    Done correctly so far! ^_^

        >>>> Read session 2:      8240 cycles

        >>>> hit:   3326

        >>>> miss:  3327

        >>>> miss rate: 50.01%

        >>>> access:  3072

        >>>> stall cycles: 13823 (81.79% total cycles)

        >>>> execution cycles:  3076 (18.20% total cycles)

        >>>> total cycles: 16900

==== CONGRATULATIONS! Pass cache read-write-read test. ====
```

cache_2way.v

(1) Cycle time: 10 (ns)

(2) General spec:

- Number of words: 32 words (4 sets x 2 ways x 4 words)

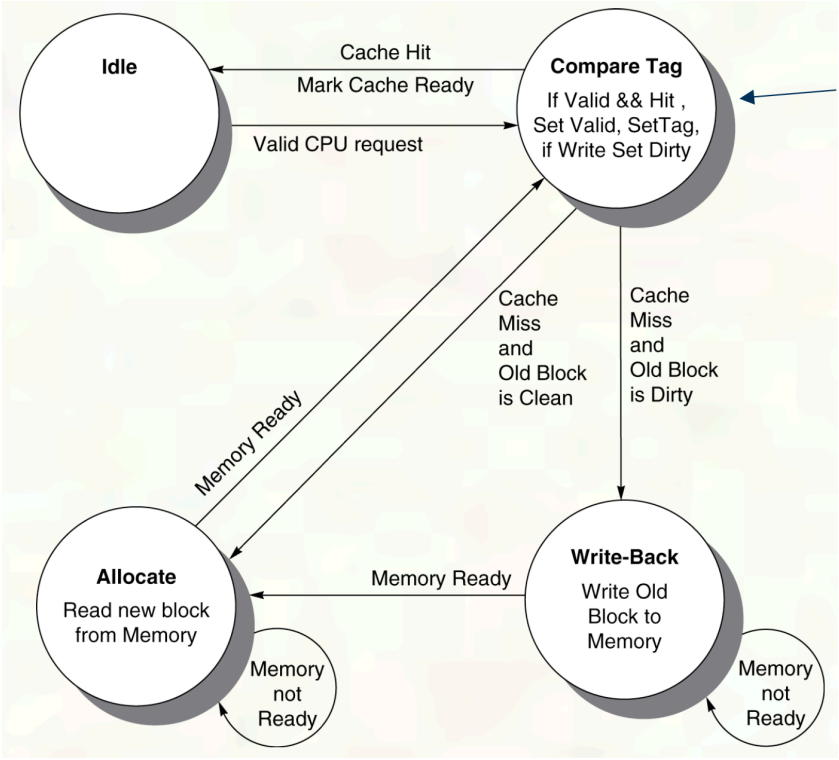
Set0	Tag (26 bits)	Data (4 words)	Set1	Tag (26 bits)	Data (4 words)
0			0		
1			1		
2			2		
3			3		

- Placement policy: 2-way set associative
- Address format:
  - Tag: 26 bits

  - Index: 2 bits
  - Offset: 2 bits
- Block detail:
  - Total: 156 bits per block
  - Valid: 1 bit
  - Dirty: 1 bit
  - Tag: 26 bits
  - Data: 128 bits (4 words)

(3) Read/write policy: write-back, write allocate, LRU

(4) FSM (same design architecture of cache_dm.v):



- IDLE: No operation.
- COMPARE_TAG: 讀取由processor傳來的proc_read或是proc_write的訊號，再執行讀或寫等動作。若block_hit為high，則直接讀取或是寫入cache block，再回到idle state，least recently used(LRU)指標也會改變指向另一個block。若block_hit為low，則視block是否為dirty再決定要不要先write back或是直接進行write allocate。
- WRITE_BACK: 若block_hit為low且block為dirty，則把該block的data寫回memory（更新memory）。Write back成功後進入allocate stage。
- ALLOCATE: 若block_hit為low且block為clean，表示cache block data和memory data一致，所以直接把目標memory address的data直接寫入，再進到compare tag stage。此階段的LRU指標會改變指向另一個block。

(5) Performance evaluation:

- No latch:

```
Inferred memory devices in process
     in routine cache line 232 in file
          '/home/raid7_2/userb05/b05013/DSD_HW4/cache_2way.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
```

```
============================================================================
|  proc_stall_r_reg   | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
|   mem_addr_r_reg    | Flip-flop |  28   |  Y  | N  | N  | N  | N  | N  | N  |
|   mem_wdata_r_reg   | Flip-flop |  128  |  Y  | N  | N  | N  | N  | N  | N  |
|  current_state_reg  | Flip-flop |   2   |  Y  | N  | N  | N  | N  | N  | N  |
|       lru_reg       | Flip-flop |   4   |  Y  | N  | N  | N  | N  | N  | N  |
|      block_reg      | Flip-flop | 1248  |  Y  | N  | N  | N  | N  | N  | N  |
|  proc_rdata_r_reg   | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
============================================================================
```

- report_area:

```
****************************************
Report : area
Design : cache
Version: N-2017.09-SP2
Date   : Thu May 28 21:35:47 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/
typical.db)

Number of ports:                          386
Number of nets:                          7086
Number of cells:                         6891
Number of combinational cells:           5448
Number of sequential cells:              1443
Number of macros/black boxes:               0
Number of buf/inv:                        636
Number of references:                      80

Combinational area:              49567.474653
Buf/Inv area:                     6261.708745
Noncombinational area:           39189.570597
Macro/Black Box area:                0.000000
Net Interconnect area:          956765.075287

Total cell area:                 88757.045250
Total area:                    1045522.120537
```

- report_timing:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : cache
Version: N-2017.09-SP2
Date   : Thu May 28 21:36:38 2020
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: proc_addr[2]
              (input port clocked by CLK)
  Endpoint: block_reg[1][1][26]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
```

```
  ------------------------------------------------
  cache              tsmc13_wl10           slow

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.50       0.50
  input external delay                     0.30       0.80 f
  proc_addr[2] (in)                        0.05       0.85 f
  U5580/Y (INVX1)                          0.17       1.02 r
  U5579/Y (NAND2X2)                        0.24       1.27 f
  U5576/Y (INVX8)                          0.47       1.74 r
  U6058/Y (AO22X1)                         0.23       1.97 r
  U10481/Y (AOI211X1)                      0.15       2.12 f
  U10482/Y (OAI22XL)                       0.35       2.47 r
  U10211/Y (AOI221XL)                      0.15       2.61 f
  U5584/Y (NAND4XL)                        0.27       2.88 r
  U6970/Y (NOR4X1)                         0.15       3.03 f
  U5566/Y (NAND3X2)                        0.31       3.34 r
  U5565/Y (CLKINVX1)                       0.30       3.64 f
  U5601/Y (NOR2X1)                         0.47       4.12 r
  U5626/Y (CLKINVX1)                       0.33       4.45 f
  U5563/Y (AO21X2)                         0.24       4.68 f
  U5561/Y (OAI22X1)                        0.25       4.93 r
  U9682/Y (AOI211X4)                       0.28       5.21 f
  U10550/Y (OAI21X1)                       0.39       5.60 r
  U6909/Y (NOR2X4)                         0.41       6.01 f
  U6877/Y (NAND3X1)                        0.34       6.35 r
  U6861/Y (NOR2X1)                         0.18       6.54 f
  U5998/Y (INVX4)                          0.39       6.93 r
  U5846/Y (BUFX16)                         0.47       7.40 r
  U10939/Y (OAI22XL)                       0.19       7.59 f
  U7686/Y (AOI21XL)                        0.28       7.87 r
  U10940/Y (OAI21XL)                       0.15       8.02 f
  block_reg[1][1][26]/D (DFFQX2)           0.00       8.02 f
  data arrival time                                   8.02

  clock CLK (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.50      10.50
  clock uncertainty                       -0.10      10.40
  block_reg[1][1][26]/CK (DFFQX2)          0.00      10.40 r
  library setup time                      -0.19      10.21
  data required time                                 10.21
  -----------------------------------------------------------
  data required time                                 10.21
  data arrival time                                  -8.02
  -----------------------------------------------------------
  slack (MET)                                         2.19
```

- miss rate, execution/stall cycle:

```
Processor: Read initial data from memory.
    Done correctly so far! ^_^

        >>>> Read session 1:      3588 cycles

        >>>> hit:   1278

        >>>> miss:  1279

        >>>> miss rate: 50.02%

Processor: Write new data to memory.
    Finish writing!

        >>>> Write session:       5072 cycles
```

```
        >>>> write hit:   1279

        >>>> write miss:  1280

        >>>> miss rate: 50.02%

Processor: Read new data from memory.
    Done correctly so far! ^_^

        >>>> Read session 2:      3632 cycles

        >>>> hit:   2558

        >>>> miss:  2559

        >>>> miss rate: 50.01%

        >>>> access:  3072

        >>>> stall cycles:  9215 (74.97% total cycles)

        >>>> execution cycles:  3076 (25.02% total cycles)

        >>>> total cycles: 12292

==== CONGRATULATIONS! Pass cache read-write-read test. ====
```

Comparison:

這次分別實作direct mapping cache和2-way associative cache，前兩階段模擬的成果差異不大。我推測是由於使用的testbench只有非常規則的循序讀和寫(依序讀memory -> 依序寫memory -> 依序讀memory)，所以不能顯著表現出direct-mapping和2-way associative set之間的效能差異。不過2-way associative cache比起direct mapping cache在第三階段的讀取出乎意料地少了約4700個stall cycles，這階段的效率就有很明顯的進步。兩種cache的miss penalty差不多，如果block是dirty那需要等兩個state transition(WRITE_BACK -> ALLOCATE)，如果是clean那只需要等一個state transition(ALLOCATE)，詳情請見FSM。

	miss rate	accesses	stall cycles	execution cycles	total cycles
cache_dm.v	50.01%	3072	13823	3076	16900
cache_2way.v	50.01%	3072	9215	3076	12292