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DSD Final Project Scores (MIPS)

1. Baseline

(1) Area: 249159.647325 (um2)

截圖:

```
****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Sun Jun 28 01:07:58 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         1525
Number of nets:                         20212
Number of cells:                        19102
Number of combinational cells:          15159
Number of sequential cells:              3940
Number of macros/black boxes:               0
Number of buf/inv:                       3129
Number of references:                     150

Combinational area:             140100.001422
Buf/Inv area:                    21107.169114
Noncombinational area:          109059.645903
Macro/Black Box area:                0.000000
Net Interconnect area:         2342585.313324

Total cell area:                249159.647325
Total area:                    2591744.960649
```

(2) Total Simulation Time of given hasHazard testbench: 8369.94 (ns)

截圖:

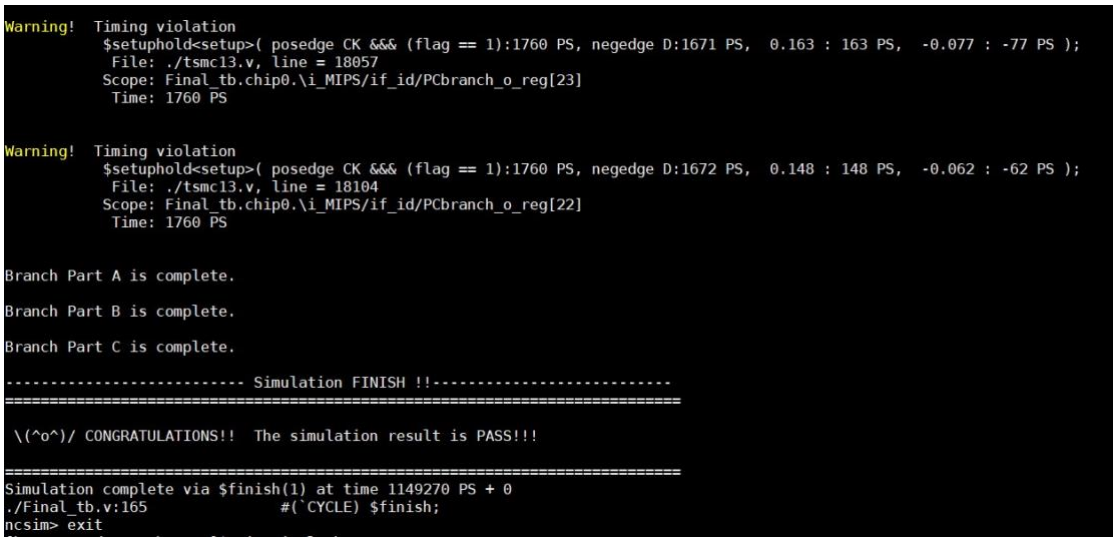
```
Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):2290 PS, negedge D:2113 PS,  0.187 : 187 PS,  -0.106 : -106 PS );
           File: ./tsmc13.v, line = 18057
          Scope: Final_tb.chip0.I_cache.\block_data_reg[1][20]
           Time: 2290 PS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):2290 PS, negedge D:2113 PS,  0.191 : 191 PS,  -0.111 : -111 PS );
           File: ./tsmc13.v, line = 18057
          Scope: Final_tb.chip0.I_cache.\block_tag_reg[1][9]
           Time: 2290 PS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):2290 PS, negedge D:2114 PS,  0.191 : 191 PS,  -0.111 : -111 PS );
           File: ./tsmc13.v, line = 18057
          Scope: Final_tb.chip0.I_cache.\block_tag_reg[3][19]
           Time: 2290 PS

addr =    0, data =         0, answer =         0
addr =    1, data =         1, answer =         1
addr =    2, data =         1, answer =         1
addr =    3, data =         2, answer =         2
addr =    4, data =         3, answer =         3
addr =    5, data =         5, answer =         5
addr =    6, data =         8, answer =         8
addr =    7, data =        13, answer =        13
addr =    8, data =        21, answer =        21
addr =    9, data =        34, answer =        34
addr =   10, data =        55, answer =        55
addr =   11, data =        89, answer =        89
addr =   12, data =       144, answer =       144
addr =   13, data =       233, answer =       233
addr =   14, data =       377, answer =       377
addr =   15, data =       610, answer =       610
addr =   16, data =       610, answer =       610
addr =   17, data =       377, answer =       377
addr =   18, data =       233, answer =       233
addr =   19, data =       144, answer =       144
addr =   20, data =        89, answer =        89
addr =   21, data =        55, answer =        55
addr =   22, data =        34, answer =        34
addr =   23, data =        21, answer =        21
addr =   24, data =        13, answer =        13
addr =   25, data =         8, answer =         8
addr =   26, data =         5, answer =         5
addr =   27, data =         3, answer =         3
addr =   28, data =         2, answer =         2
addr =   29, data =         1, answer =         1
addr =   30, data =         1, answer =         1
addr =   31, data =         0, answer =         0
addr =   32, data =      3421, answer =      3421
------------------------- Simulation FINISH !!----------------------------
==============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

==============================================================================
Simulation complete via $finish(1) at time 8369940 PS + 0
```

(3) Area*Total Simulation Time:
249159.647325 * 8369.94 ≈ 2085451298.5314105 (um^2 * ns)
(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)
Sdc: 3
Tb: 4.57

2. BrPred

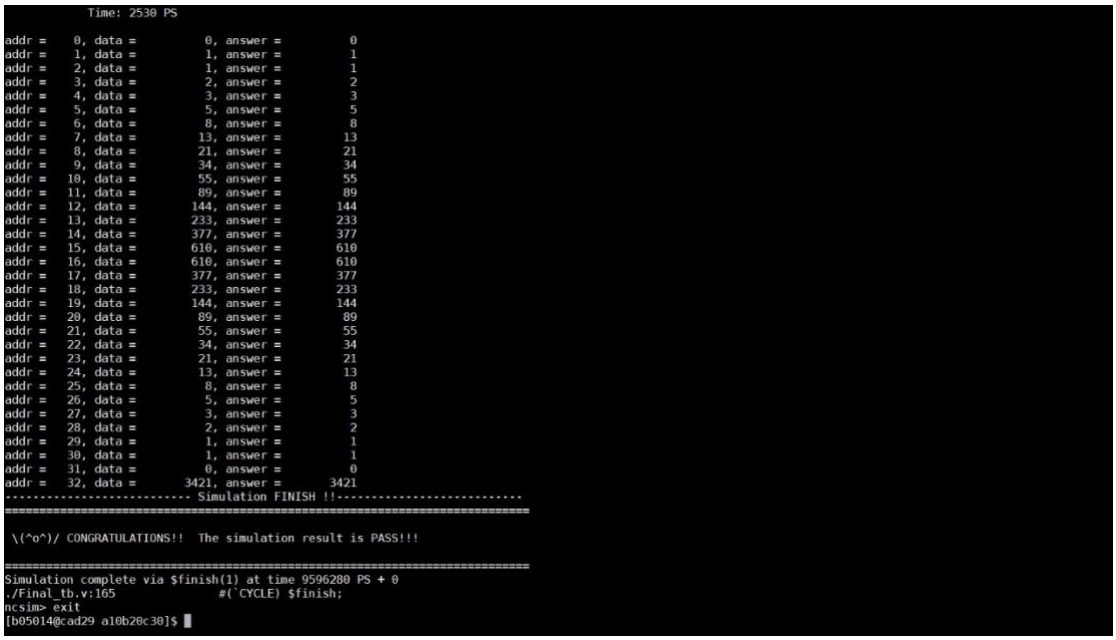
(1) Total execution cycles of given I_mem_BrPred: 1149(ns)

截圖:



(2) Total execution cycles of given I_mem_hasHazard: 9596(ns)

截圖:



(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): 267800-249159=18641(um2)

```
****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Tue Jun 23 22:41:07 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         1491
Number of nets:                         20912
Number of cells:                        19481
Number of combinational cells:          15502
Number of sequential cells:              3976
Number of macros/black boxes:               0
Number of buf/inv:                       3508
Number of references:                     164

Combinational area:             157275.991928
Buf/Inv area:                    25983.799279
Noncombinational area:          110524.502142
Macro/Black Box area:                0.000000
Net Interconnect area:         2401338.937622

Total cell area:                267800.494070
Total area:                    2669139.431692

Hierarchical area distribution
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                               Global cell area             Local cell area
                               -------------------  ------------------------------
Hierarchical cell              Absolute     Percent  Combi-       Noncombi-    Black-
                               Total        Total    national     national     boxes   Design
------------------------------ -----------  -------  -----------  -----------  ------  ---------
CHIP                           267800.4941    100.0   65448.3492   16183.0116  0.0000  CHIP
D_cache                         68717.5406     25.7   34862.8981   33854.6425  0.0000  cache_1
I_cache                         64346.7357     24.0   30801.0201   33545.7157  0.0000  cache_0
i_MIPS_register                 53104.8570     19.8   26163.7246   26941.1324  0.0000  registers
------------------------------ -----------  -------  -----------  -----------  ------  ---------
Total                                                157275.9919  110524.5021  0.0000
                                                                                      1,1           Top
```

3. L2 Cache

(1) Average memory access time: 6.263(ns)

HT1+MR1*(HT2+MR2*MP2) = 5.71*(1+0.085*(1+0.028*5)) = 6.263

(2) Total execution time of given I_mem_L2Cache: (ns)

截圖:

```
Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):2860 PS, negedge D:2797 PS,  0.093 : 93 PS,  -0.050 : -50 PS );
           File: ./tsmc13.v, line = 23104
          Scope: Final_tb.chip0.\i_MIPS/pc/PC_o_reg[18]
           Time: 2860 PS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):2860 PS, negedge D:2802 PS,  0.092 : 92 PS,  -0.049 : -49 PS );
           File: ./tsmc13.v, line = 23104
          Scope: Final_tb.chip0.\i_MIPS/pc/PC_o_reg[10]
           Time: 2860 PS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):2860 PS, negedge D:2803 PS,  0.092 : 92 PS,  -0.045 : -45 PS );
           File: ./tsmc13.v, line = 23151
          Scope: Final_tb.chip0.\i_MIPS/pc/PC_o_reg[6]
           Time: 2860 PS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):2860 PS, negedge D:2778 PS,  0.096 : 96 PS,  -0.049 : -49 PS );
           File: ./tsmc13.v, line = 23151
          Scope: Final_tb.chip0.\i_MIPS/pc/PC_o_reg[5]
           Time: 2860 PS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):2860 PS, negedge D:2741 PS,  0.148 : 148 PS,  -0.061 : -61 PS );
           File: ./tsmc13.v, line = 18104
          Scope: Final_tb.chip0.\i_MIPS/pc/PC_o_reg[31]
           Time: 2860 PS

------------------------- Simulation FINISH !!--------------------------
==============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

==============================================================================
Simulation complete via $finish(1) at time 205636850 PS + 0
./Final_tb.v:211              #(`CYCLE) $finish;
ncsim> exit
[b05014@cad29 nb20incre3]$
```

4. MultDiv

(1) Area of MultDiv (Total area of MultDiv minus baseline design, two design clock cycle need to be same): 284726.9667 – 249159.647325 = 35567.3194(um^2)

```
****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Mon Jun 22 16:40:57 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         1525
Number of nets:                         23514
Number of cells:                        22371
Number of combinational cells:          18083
Number of sequential cells:              4285
Number of macros/black boxes:               0
Number of buf/inv:                       3908
Number of references:                     163

Combinational area:             165645.871266
Buf/Inv area:                    24439.165263
Noncombinational area:          119081.095434
Macro/Black Box area:                0.000000
Net Interconnect area:         2711953.833313

Total cell area:                284726.966700
Total area:                    2996680.800013
```

(2) Total execution time of given I_mem_MultDiv: 1917.98(ns)

```
addr = 0, data =      40320, answer =      40320
addr = 1, data =          1, answer =          1
addr = 2, data =       3421, answer =       3421
-------------------------- Simulation FINISH !!--------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 1917980 PS + 0
```

(3) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

Sdc: 3

Tb: 4.21