1082 DSD Final Project - Pipelined MIPS Design

Checkpoint Proposal

B05901013 張景皓/B05901014 吳靖平, 06/11/2020

Current Results

Baseline Passed

Spent the majority of time on debugging the forwarding unit.
TBD: cache performance optimization(?)

Extension Topics Plan

To Do

(will complete as many functions as possible)

- Branch Prediction mechanism
- Two-level caches (L1 + L2)
- Multiplication/Division instruction set

Collaboration

吳靖平	張景皓
Cache	Other modules
Connecting modules (i_MIPS)	Logic Synthesis
Troubleshooting	Troubleshooting
Extension Topics (TBD)	