ECE 153A/253, CS 153A - Homework 1 Solutions

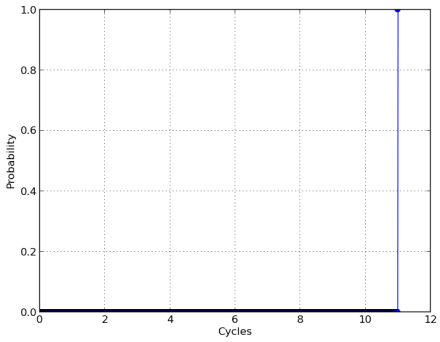
1. Problem 1:

   (a) Given random reads of the 16-bit memory space,
   Expected access time with cache disabled: ≈ 11 cycles (5 points)
   Expected access time with cache enabled: ≈ 16.5 cycles (5 points)

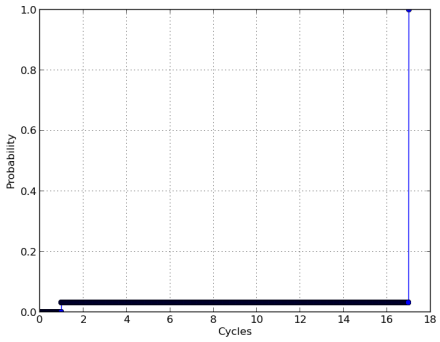
   (b) Assuming that:
   s=0.6 is the probability that the next address follows the current one,
   p=0.35 is the probability that the next address is not sequential but is within 40 words (either direction) of the current one,
   thus 0.05 is the probability of a random far address,
   Expected access time with cache disabled: ≈ 6.5 cycles (10 points)
   Expected access time with cache enabled: ≈ 6 cycles (10 points)
   These values were computed with the assumption that address values wrap, i.e., if $+1$ or $+-40$ results in an address < 0 or $> 2^{16}-1$, the accessed addresses are $(address+2^{16})$ and $(address-2^{16})$ respectively.

   (c) The worst case memory access times are 11 cycles and 17 cycles with the cache disabled and enabled respectively. (5 points)

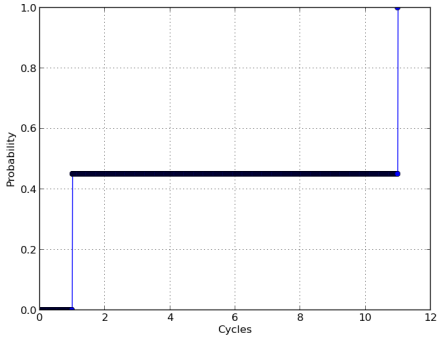
   (d) The CDFs are shown below:



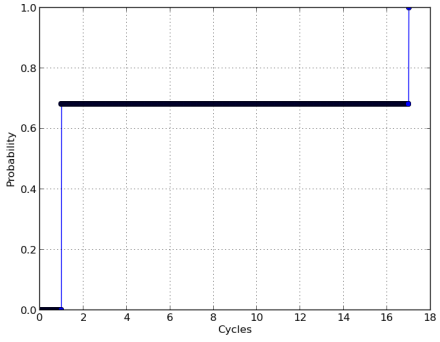
(a) CDF for part(a) Uncached Access



(b) CDF for part(a) Cached Access



(c) CDF for part(b) Uncached Access



(d) CDF for part(b) Cached Access

Figure 1: CDFs (5 points each)

The following confidence limits can be read from the CDFs:

i. For random uncached memory accesses, the probability of the access time being less than the worst case (11 cycles) is 0.00007.

ii. For random cached memory accesses, the probability of the access time being less than the worst case (17 cycles) is 0.031.

iii. For non-random uncached memory accesses, the probability of the access time being less than the worst case (11 cycles) is 0.45.

iv. For non-random cached memory accesses, the probability of the access time being less than the worst case (17 cycles) is 0.681

Worst case bounds are hard to estimate in a real system as the data gathered hardly meets Gaussian (normal) statistics. The values obtained are highly dependent on the state of the system, and it is not possible to exhaustively simulate test cases for all possible states of the system. (5 points)

2. Problem 2:

Task	Description	Time to Run	Deadline
Ctrl	Control Calculations	9 ms	24 ms
Torq	Torque Check	3 ms	18 ms
Temp	Temperature Check	3 ms	30 ms
UI	User Interface	5 ms	30 ms

(a) Utility (U) $= \sum_{i=1}^{n} \frac{T_i}{P_i}$, where T_i is the time to run task i and P_i is the period of task i. Since the period of each task has to be less than its deadline (D) for a schedule to be feasible, let us assume $P_i = D_i$
$\Rightarrow U = \frac{9}{24} + \frac{3}{18} + \frac{3}{30} + \frac{5}{30} = 0.808\bar{3}$ (5 points)

(b) The schedule is shown below: (10 points)

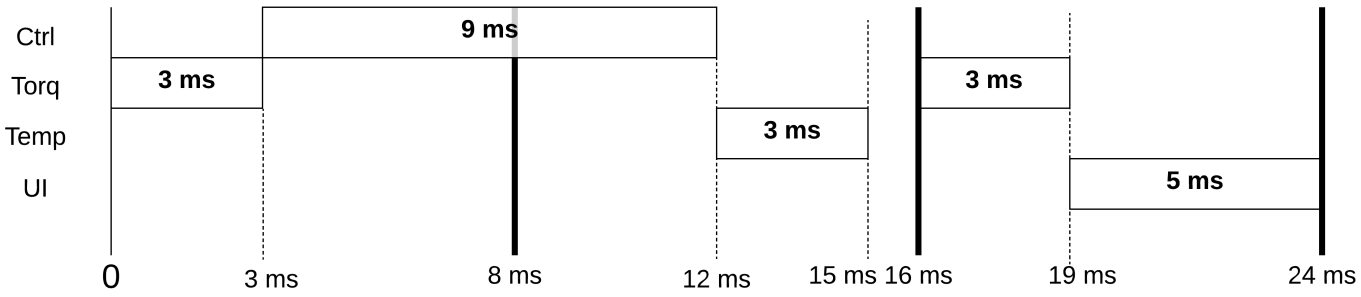


Figure 2: Schedule with 8 ms loop time

The period for Ctrl, Temp and UI is 24 ms. Torq operates with a non-uniform period that alternates between 16 ms and 8 ms.

(c) Utility of the above schedule, $U = \frac{9}{24}(Ctrl) + \frac{6}{24}(Torq) + \frac{3}{24}(Temp) + \frac{5}{24}(UI) = \frac{23}{24} = 0.958\bar{3}$
Utility of a valid schedule is the fraction of time the processor is doing something useful.
(5 points)

(d) $U_e = \sum_{i=1}^{n} \frac{T_i}{L\left\lfloor \frac{P_i}{L} \right\rfloor}$

For a loop time (L) of 10 ms, assuming that the period for each task is equal to its deadline,

$$U_e = \frac{9}{10*2} + \frac{3}{10*1} + \frac{3}{10*3} + \frac{5}{10*3} = \frac{61}{60} > 1$$

Since $U_e > 1$, no schedule is feasible! (5 points)

(e) The schedule is shown below (10 points):

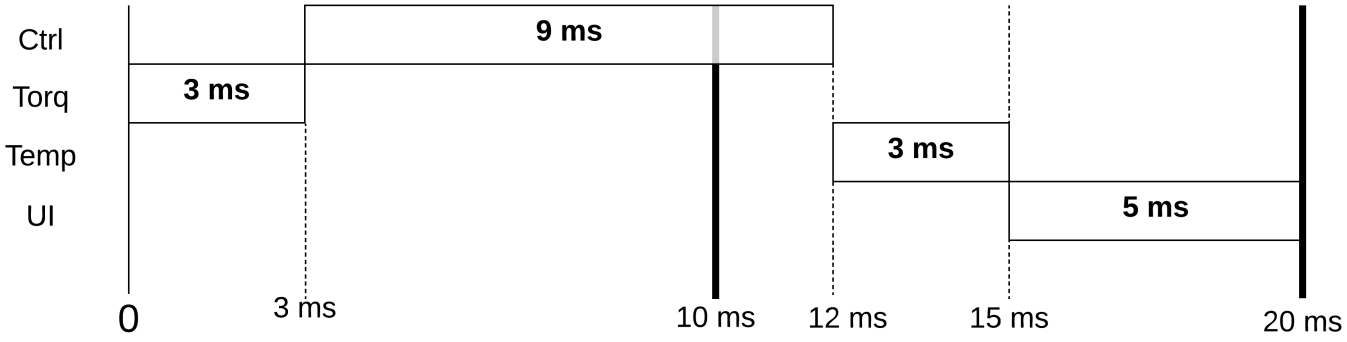


Figure 3: Schedule with 10 ms loop time

(f) Utility of the above schedule, $U = \frac{9}{20}(Ctrl) + \frac{3}{20}(Torq) + \frac{3}{20}(Temp) + \frac{5}{20}(UI) = 1$

This schedule has a higher utility than the schedule in part (b) (5 points)