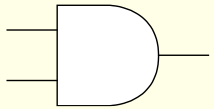
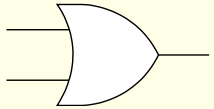
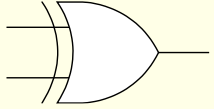
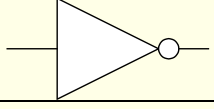


# Boolean Logic KO

Define problems using Boolean logic

AND		$\wedge$	$A \wedge B$ A AND B
OR		$\vee$	$A \vee B$ A OR B
XOR		$\underline{\vee}$	$A \underline{\vee} B$ A XOR B
NOT		$\neg$	$\neg A$ NOT A
The same as		$\equiv$	$A \equiv B$ A is the same as B

Truth tables:

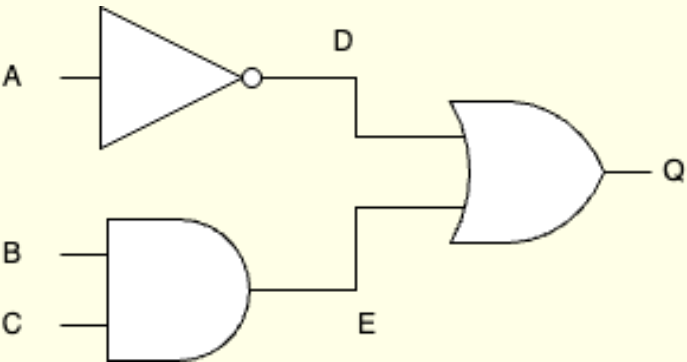
<table><tr><th colspan="3">AND <math>\wedge</math></th></tr><tr><td>A</td><td>B</td><td>Output</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	AND $\wedge$			A	B	Output	0	0	0	0	1	0	1	0	0	1	1	1	<table><tr><th colspan="3">OR <math>\vee</math></th></tr><tr><td>A</td><td>B</td><td>Output</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	OR $\vee$			A	B	Output	0	0	0	0	1	1	1	0	1	1	1	1	<table><tr><th colspan="2">NOT <math>\neg</math></th></tr><tr><td>A</td><td>Output</td></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	NOT $\neg$		A	Output	0	1	1	0
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<p>The XOR gate produces a 1 output if either, but not both of the inputs are 1.</p> <table><tr><th colspan="3">XOR <math>\underline{\vee}</math></th></tr><tr><td>A</td><td>B</td><td>Output</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	XOR $\underline{\vee}$			A	B	Output	0	0	0	0	1	1	1	0	1	1	1	0	<table><tr><th colspan="3">NAND</th></tr><tr><td>A</td><td>B</td><td>Output</td></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	NAND			A	B	Output	0	0	1	0	1	1	1	0	1	1	1	0									
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1	1	0																																												

Multiple logic gates can be connected to produce an output based on multiple inputs.

This circuit can be represented by the expression

$$Q = \neg A \vee (B \wedge C)$$

or alternatively as  $Q = (\text{NOT } A) \text{ OR } (B \text{ AND } C)$

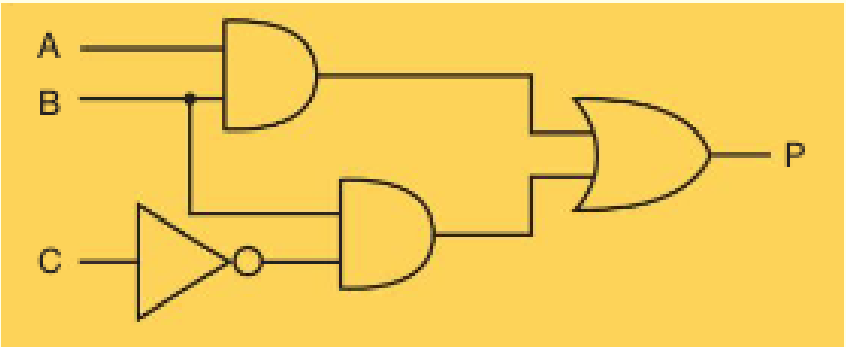


Evaluate the brackets first

Input A	Input B	Input C	$D = \neg A$	$E = B \wedge C$	Output $Q = D \vee E$
0	0	0	1	0	1
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	1	1

How to write Boolean expression represented in a logic diagram:

Write the Boolean expression represented by the logic diagram below, using AND, OR and NOT instead of symbols. Then write the same expression using symbols.



First write  $(A \text{ AND } B)$ .

Then write  $(B \text{ AND NOT } C)$

These are the inputs to the OR gate

so the expression is:

$$P = (A \text{ AND } B) \text{ OR } (B \text{ AND NOT } C)$$

$$P = (A \wedge B) \vee (B \wedge \neg C)$$

### Defining problems with Boolean logic

A boiler has two sensors, a pressure sensor and a temperature sensor. If either the temperature (T) or the pressure (P) is too high, a valve (V) will close.

This can be expressed as  $V = T \vee P$  or alternatively as  $V = T \text{ OR } P$

The table representing these conditions could be drawn as follows:

Input	Binary value	Condition
T	1	Temperature too high
	0	Temperature not too high
P	1	Pressure too high
	0	Pressure not too high

### Worked Example

A chemical process has a sensor to detect a dangerous situation, in which case it sounds an alarm (A). The alarm is sounded if:

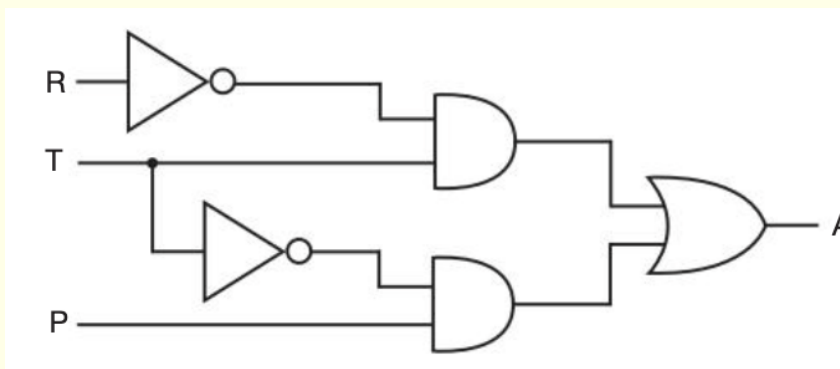
either temperature  $\geq 100^\circ\text{C}$  AND rotator is OFF

or

PH  $> 6$  AND temperature  $< 100^\circ\text{C}$

A table can be drawn to represent these conditions as Boolean values.

Input	Binary value	Condition
T	1	Temperature $\geq 100^\circ\text{C}$
	0	Temperature $< 100^\circ\text{C}$
R	1	Rotator ON
	0	Rotator OFF
P	1	PH $> 6$
	0	PH $\leq 6$



The conditions can be written as

$$A = (T \wedge \neg R) \vee (P \wedge \neg T) \text{ or alternatively as } A = (T \text{ AND NOT } R) \text{ OR } (P \text{ AND NOT } T)$$

Input R	Input T	Input P	$X = T \wedge \neg R$	$Y = P \wedge \neg T$	$A = X \vee Y$
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	0	0
1	1	1	0	0	0

## Karnaugh maps (K Maps)

### The four-variable problem

- A K Map is a tool that is used for **simplifying Boolean algebra expressions**
- A **visual method** of **grouping together expressions** with **common factors**
- The format of the map makes it **easy to identify** and **eliminate redundant terms**
- They are used in digital logic design, such as simplifying the logic of digital circuits

#### 1. Grouping the 1's

- Make rectangular groups
- Make groups that are as large as possible
- Make groups that contain either 8,4,2 or 1 ones
- Groups can overlap (i.e. some ones can be in multiple groups)
- The Karnaugh map 'grid' wraps round in all directions so the groups can wrap round

#### 2. Write a term for each group by finding the variables that **stay the same** in that group. If a variable is 0 in the group → use **NOT** of it.

#### 3. **OR** the group terms together to form the simplified expression. (Use $\vee$ )

**Example: Give a simplified version of the expression using the Karnaugh map.**

		AB			
		00	01	11	10
CD	00	1	1	1	1
	01	1	1	1	1
	11	0	1	1	0
	10	0	1	1	0

**You must show your working [3]**

Looking at the group of 8 in the middle of the map, for all the cells in the group the variable B is always a 1

The 3 other variables change across the group (i.e. for some cells they are 0 and for others they are 1)  
So this group is B

Looking at the other group of 8, for all the cells in this group, C is always 0 but the other 3 variables can be 1 or 0 in this group So this group simplifies to  $\neg C$

**$B \vee \neg C$**

**Example 2: Wrap around**

		AB			
		00	01	11	10
CD	00	1	0	0	1
	01	1	0	0	1
	11	1	0	0	1
	10	1	0	0	1

**Simplified  $\neg B$**

## Simplifying Boolean Expressions

### Boolean Simplification Rules

Rule name	Original expression	Simplified form
<b>AND</b>	X AND 1	X
	X AND 0	0
	X AND X	X
	NOT X AND X	0
<b>OR</b>	X OR 0	X
	X OR 1	1
	X OR X	X
	NOT X OR X	1

Rule name	Original expression	Simplified form
<b>De Morgan's Law</b>  Flip AND ↔ OR, move NOT inside	$\neg(A \wedge B)$	$\neg A \vee \neg B$
	$\neg(A \vee B)$	$\neg A \wedge \neg B$
<b>Distribution</b>  Expanding brackets	$A \wedge (B \vee C)$	$(A \wedge B) \vee (A \wedge C)$
	$A \vee (B \wedge C)$	$(A \vee B) \wedge (A \vee C)$
<b>Reverse distribution (factoring)</b>  Factor out common term	$(A \wedge B) \vee (A \wedge C)$	$A \wedge (B \vee C)$
	$(A \vee B) \wedge (A \vee C)$	$A \vee (B \wedge C)$
<b>Association</b> Brackets removable	$(A \wedge B) \wedge C$	$A \wedge B \wedge C$
	$(A \vee B) \vee C$	$A \vee B \vee C$
<b>Commutation</b>  Order doesn't matter	$A \vee B$	$B \vee A$
	$A \wedge B$	$B \wedge A$
<b>Double negation</b>  Two NOTs cancel	$\neg\neg A$	A
<b>Absorption</b>  If A is true, result is true	$A \wedge (A \vee B)$	A
	$A \vee (A \wedge B)$	A

### Worked Example: Boolean Simplification

Step	Explanation	Expression
<b>Original</b>	Given expression	$(\neg C \wedge \neg D) \vee (C \wedge \neg D)$
<b>Step 1</b>	Identify the repeated term in both brackets	Common term: $\neg D$
<b>Step 2</b>	Factor out the common term (reverse distribution / factoring)	$\neg D \wedge (\neg C \vee C)$
<b>Step 3</b>	Apply General OR rule: NOT X OR X = 1	$\neg D \wedge 1$
<b>Final</b>	Simplified expression	<b><math>\neg D</math></b>

More simplified versions of the following Boolean expressions and the rule applied:

Original expression	Simplified expression	Rule(s) applied
$\neg\neg A$	A	Double negation
$\neg A \wedge \neg B$	$\neg(A \vee B)$	De Morgan's Law
$A \vee (A \wedge B) \vee \neg A$	1	Absorption, Complement

## Adders and Flip Flops

### Half Adder

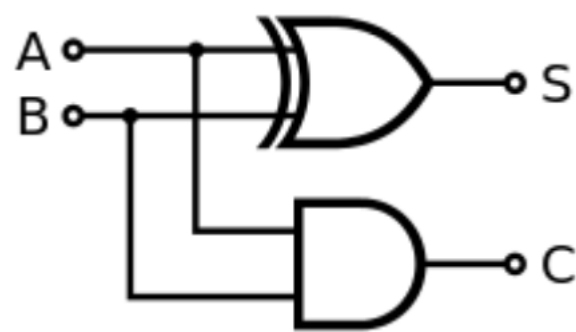
A half adder has two inputs, A and B, and two outputs, Sum and Carry. The circuit is formed from just two logic gates: AND and XOR.

S = SUM

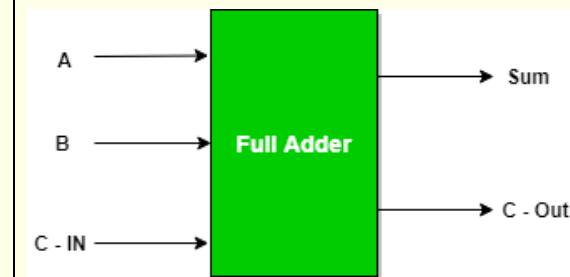
C – Carry

0+0 = 0      SUM 0 No Carry 0  
 1+0 = 1      SUM 1 No Carry 0  
 1+1 = 1 0    SUM 0 Carry 1  
 1+1+1=11    SUM 1 Carry 1

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



**Full Adder** A full adder is similar to a half adder, but has an additional input, allowing for carry in to be represented.



A	B	C <sub>in</sub>	C <sub>out</sub>	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

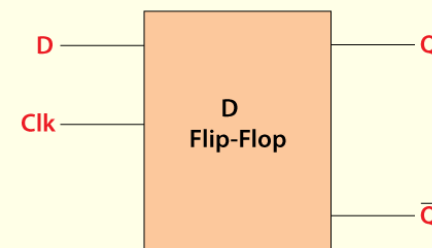
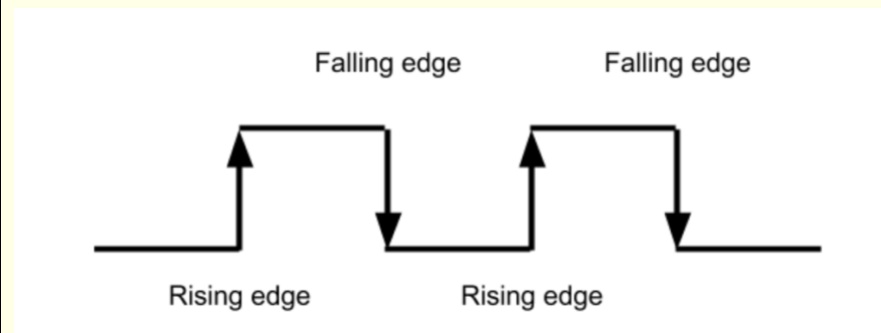
Cover the Cout and SUM columns in the Truth Table and fill in the table yourself

## D Type Flip Flops

A flop flop is a type of logic circuit which can store the value of one bit.

A flip flop has two inputs, a control signal and a clock input.

Clock Pulse



A D-type flip flop can only change at a rising edge, the start of a clock tick.

D – INPUT

Q – OUTPUT

