

| arithmetic_operations | |
|-----------------------|------------------|
| 1 | addi x1 x0 52 |
| 2 | addi x2 x0 21 |
| 3 | ori x3 x0 4 |
| 4 | add x4 x1 x2 |
| 5 | sub x5 x1 x2 |
| 6 | sll x6 x1 x3 |
| 7 | srli x7 x2 1 |
| 8 | sub x8 x0 x7 |
| 9 | slt x9 x8 x7 |
| 10 | sltu x10 x8 x7 |
| 11 | xor x11 x7 x8 |
| 12 | slti x12 x1 -1 |
| 13 | sltiu x13 x1 -1 |
| 14 | slli x14 x1 8 |
| 15 | andi x15 x8 -25 |
| 16 | xori x16 x8 -122 |
| 17 | lui x17 12345 |
| 18 | addi x18 x0 678 |
| 19 | or x17 x17 x18 |
| 20 | addi x18 x0 122 |
| 21 | |

Figure 1: Arithmetic Operations in RISC-V

| Control and Status | | |
|--------------------|--------|----------------|
| Registers | | Floating Point |
| Name | Number | Value |
| zero | 0 | 0x00000000 |
| ra | 1 | 0x00000034 |
| sp | 2 | 0x00000015 |
| gp | 3 | 0x00000004 |
| tp | 4 | 0x00000049 |
| t0 | 5 | 0x0000001f |
| t1 | 6 | 0x00000340 |
| t2 | 7 | 0x0000000a |
| s0 | 8 | 0xffffffff6 |
| s1 | 9 | 0x00000001 |
| a0 | 10 | 0x00000000 |
| a1 | 11 | 0xffffffffc |
| a2 | 12 | 0x00000000 |
| a3 | 13 | 0x00000001 |
| a4 | 14 | 0x00003400 |
| a5 | 15 | 0xffffffffe6 |
| a6 | 16 | 0x00000070 |
| a7 | 17 | 0x030392a6 |
| s2 | 18 | 0x0000007a |
| s3 | 19 | 0x00000000 |
| s4 | 20 | 0x00000000 |
| s5 | 21 | 0x00000000 |
| s6 | 22 | 0x00000000 |
| s7 | 23 | 0x00000000 |
| s8 | 24 | 0x00000000 |
| s9 | 25 | 0x00000000 |
| s10 | 26 | 0x00000000 |
| s11 | 27 | 0x00000000 |
| t3 | 28 | 0x00000000 |
| t4 | 29 | 0x00000000 |
| t5 | 30 | 0x00000000 |
| t6 | 31 | 0x00000000 |
| pc | | 0x00400054 |

Figure 2: Expected Results

| | |
|----|-------------|
| 0 | 00000000 |
| 1 | 00000034 |
| 2 | 00000015 |
| 3 | 00000004 |
| 4 | 00000049 |
| 5 | 0000001f |
| 6 | 00000340 |
| 7 | 0000000a |
| 8 | ffffffff6 |
| 9 | 00000001 |
| 10 | 00000000 |
| 11 | ffffffffffc |
| 12 | 00000000 |
| 13 | 00000001 |
| 14 | 00003400 |
| 15 | ffffffe6 |
| 16 | 00000070 |
| 17 | 030392a6 |
| 18 | 0000007a |
| 19 | 00000000 |
| 20 | 00000000 |
| 21 | 00000000 |
| 22 | 00000000 |
| 23 | 00000000 |
| 24 | 00000000 |
| 25 | 00000000 |
| 26 | 00000000 |
| 27 | 00000000 |
| 28 | 00000000 |
| 29 | 00000000 |
| 30 | 00000000 |
| 31 | 00000000 |

Figure 3: Actual Results

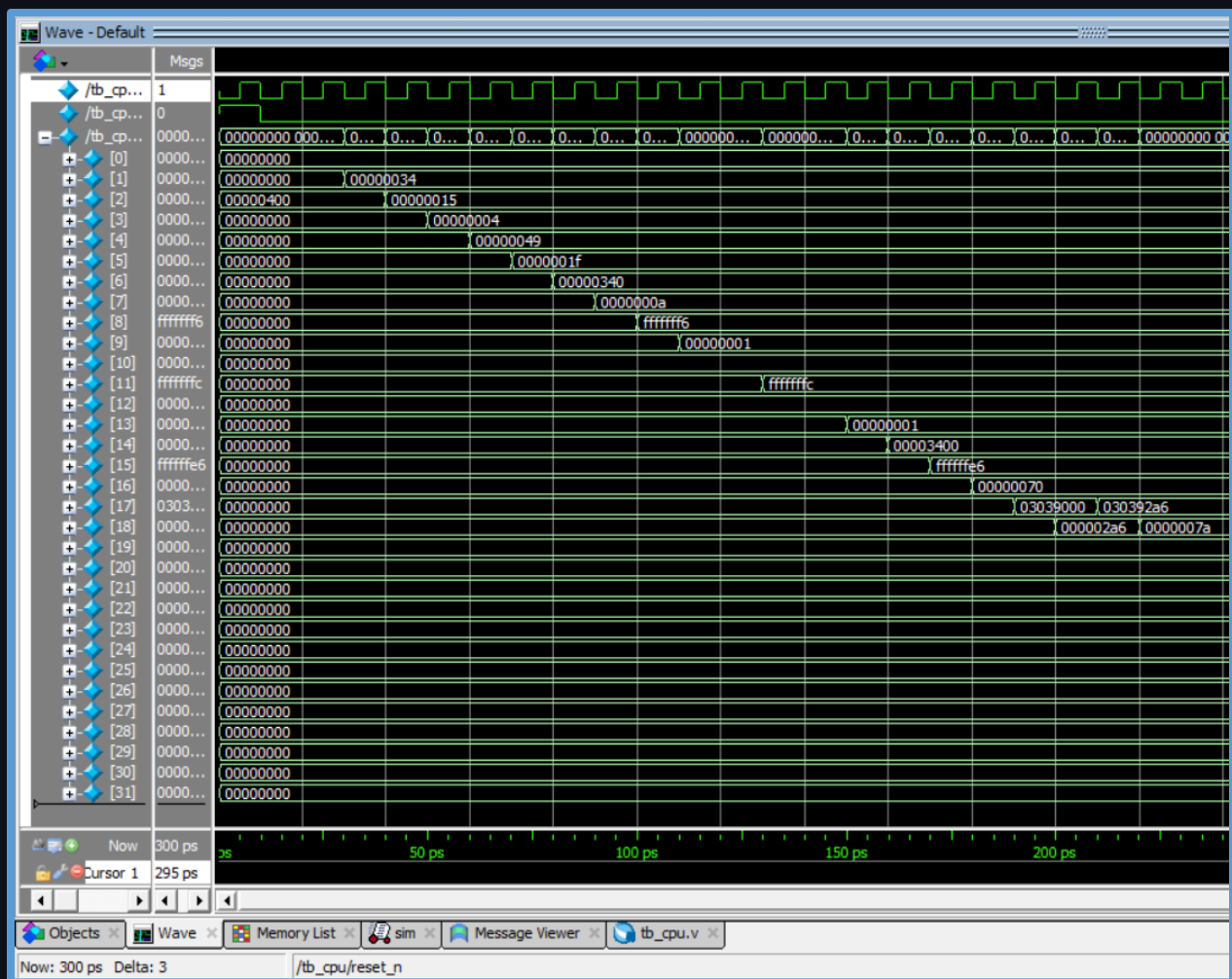


Figure 4: Register File

| | | | | |
|----|----|----|----|----|
| 0 | 13 | d0 | 00 | 08 |
| 4 | 13 | 54 | 00 | 10 |
| 8 | 13 | 13 | 00 | 18 |
| 12 | 33 | 00 | 44 | 20 |
| 16 | 33 | 00 | 45 | 28 |
| 20 | b3 | 00 | 46 | 30 |
| 24 | 93 | 06 | 80 | 38 |
| 28 | 33 | 00 | 0f | 40 |
| 32 | 33 | 01 | 0e | 4a |
| 36 | b3 | 01 | 0e | 52 |
| 40 | 33 | 02 | d0 | 59 |
| 44 | 13 | fd | 7f | 60 |
| 48 | 93 | fd | 7f | 68 |
| 52 | 93 | 20 | 40 | 70 |
| 56 | 93 | 9f | 3f | 7a |
| 60 | 13 | 1a | 3e | 82 |
| 64 | b7 | 1c | 18 | 88 |
| 68 | 13 | 98 | 0a | 90 |
| 72 | 33 | 03 | 64 | 8c |
| 76 | 13 | e8 | 01 | 90 |

Figure 5: Instruction Memory