



# **Circuit Simulation Project**

https://esim.fossee.in/circuit-simulation-project

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Title of the circuit: Illustration of 2:1 MUX using logic gates

#### **Theory/ Description:**

Multiplexing means sharing. A multiplexer (MUX) is a logic circuit that accepts several data inputs and allows only one of them at a time to get through the output. The routing of the desired data input to the output is controlled by SELECT lines/ inputs. The fig.1 shows the functional block diagram of the MUX.

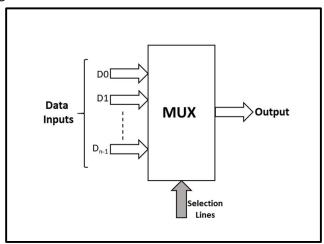


Fig. 1 – Functional Block Diagram of MUX

The multiplexer acts like a digitally controlled multi-position switch. The digital code applied to the select inputs determines which data lines will be switched to the output. We can say that a multiplexer selects 1-out-of-N input data sources and transmits the selected data to a single output channel. This is called multiplexing. The **truth table** for 2:1 MUX is:

Table 1: Truth Table of 2:1 MUX

S	D0	D1	Υ
0	0	X	0
0	1	X	1
1	X	0	0
1	Х	1	1

where S = selection line; D0 and D1 are the data input lines; and Y = output.

Hence depending on the value of the selection line S(Sin), the inputs i.e., D0, D1 are produced at outputs. The output is D0 when select value is S = 0; and output D1 when select value is S = 1.

Expression of a typical 2:1 MUX is as follows:

$$Y = \overline{S}D0 + SD1$$

The circuit diagram of 2:1 MUX is shown in fig. 2. The logic gates from the above expression which are used are AND, and OR gates and a invertor (NOT) gate.

Multiplexers find numerous and varied applications in digital of all types. These applications include data selections, data routing, operation sequencing, parallel-to-serial conversion, waveform generation, and logic function generation.

#### Circuit Diagram(s):

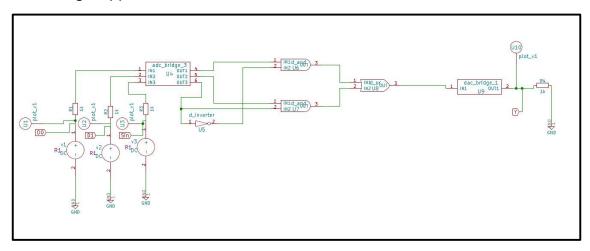
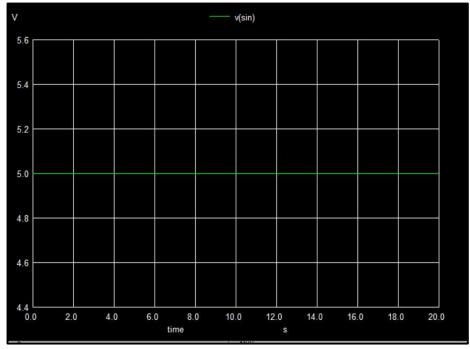


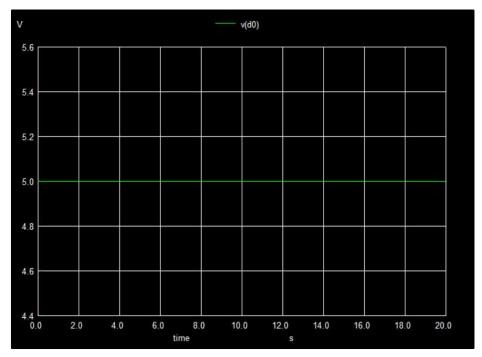
Fig. 2 – Circuit diagram of 2:1 MUX using Logic Gates

## Results (Input, Output waveforms and/or Multimeter readings):

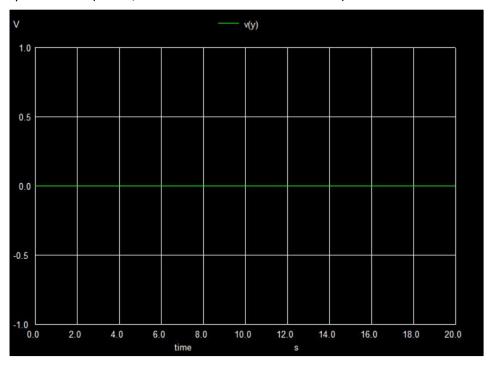
1. Selection line  $-S_{in}$ 



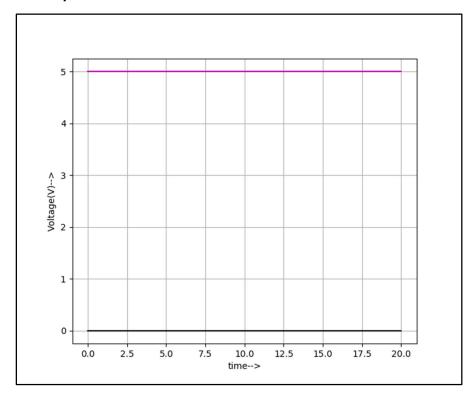
2. Data inputs –  $D_0$  = 5V (DC) and  $D_1$  = 0V



3. Output – Y = 0V ( $S_{in}$  = 1; Y = D1 = 0V Case 3 of Truth Table)



## **Python Plot:**



Transient Analysis	
List of Nodes:	
✓ d0	y <del></del>
✓ d1	
netr1-pad2_	
netr2-pad2_	
netr3-pad2_	
✓ sin	
✓ y	

## Source/Reference(s):

- $\textbf{1.} \quad \underline{\text{https://www.electronicshub.org/multiplexerandmultiplexing/\#2-to-1\_Multiplexer}\\$
- 2. Digital Circuits by Anand Kumar book.
- 3. Digital logic o& computer design by M Morris Mano book.