RENESAS

Home Products Optoelectronics Technical Description

Explanation of Solid State Relay (optical-coupled MOS FET) Specifications

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The specifications of semiconductor devices are usually prescribed on an ambient temperature(T_A: Air temperature around the device) or package surface temperature (T_C) of 25 degree Centigrade.
Actual usage environments vary greatly, but in the case of characteristics or a tolerance range other than 25 degree Centigrade, the user must perform calculations according to the usage environment for the device the user designs, using characteristics curves, etc.
General specification items are described below.

Absolute Maximum Ratings **Electrical Characteristics**

Absolute Maximum Ratings

Each item is basically specified for direct current.
Therefore, if switching alternating current, think of the ratings on the output side as half-wave peak values (half of amplitude in the case of a sine wave).

Isolation Voltage: BV(Vr.m.s.)
Allowable maximum alternating current voltage that can be applied between the input pins and output pins is expressed as a root mean square (r.m.s.) value.
This value guarantees a certain insulation resistance.
Normally, this value is guaranteed not for an unlimited period, but for a limited test time, of 1 minute, for example.

Operating Ambient Temperature: T_A (degree Centigrade)
Allowable temperature range in which power application is possible.
Usually when the actual ambient temperature rises, the power dissipation (P_D) declines.
Moreover, power application is inhibited when the actual ambient temperature is out of this range.
In the case of OCMOS FETs, the temperature at which power can be applied is not described as the "package surface temperature", but instead as the "ambient temperature (air temperature around the device)".

Storage Temperature: T_{stg} (degree Centigrade)
Allowable temperature range when power is not applied (stored state).

Light Emitting Diode: Forward Current: I_F (mA)
Allowable maximum current at which destruction does not occur, within the allowable power dissipation (P_D) range of the LED (light emitting diode) on the input side when the ambient temperature is 25 degree Centigrade.
In the case of OCMOS FETs, the forward current affects the response time, but has almost no influence on the static characteristics of output.
However, since response time does not change so much depends on the forward current larger than optimum value, excessively raising

the forward current is not significant.
Mainly design circuits so that the maximum value of the forward current remains within this range, even if the forward current is subject to variations or fluctuations.

Light Emitting Diode: Reverse Voltage: V_R (V)

Note that the reverse withstand voltage of the LED (Light Emitting Diode) on the light-emitting side is low.
When the reverse withstand voltage is exceeded, a reverse current suddenly flows. (In this case, the LED does not emit light.)
Moreover, when a reverse current flows, the subsequent light emitting efficiency is lowered.
Therefore, when a reverse voltage exceeding this value is applied even momentarily, destruction or non-recoverable degradation may occur.

Light Emitting Diode: Power Dissipation: P_D (mW)

Allowable power dissipation of LED on input side at ambient temperature of 25 degree Centigrade.
As described in the "Light Emitting Diode: Forward Current (I_F)" section, in the case of OCMOS FETs, excessively raising the forward current is not significant.

MOS FET: Power Dissipation: P_D (mW)

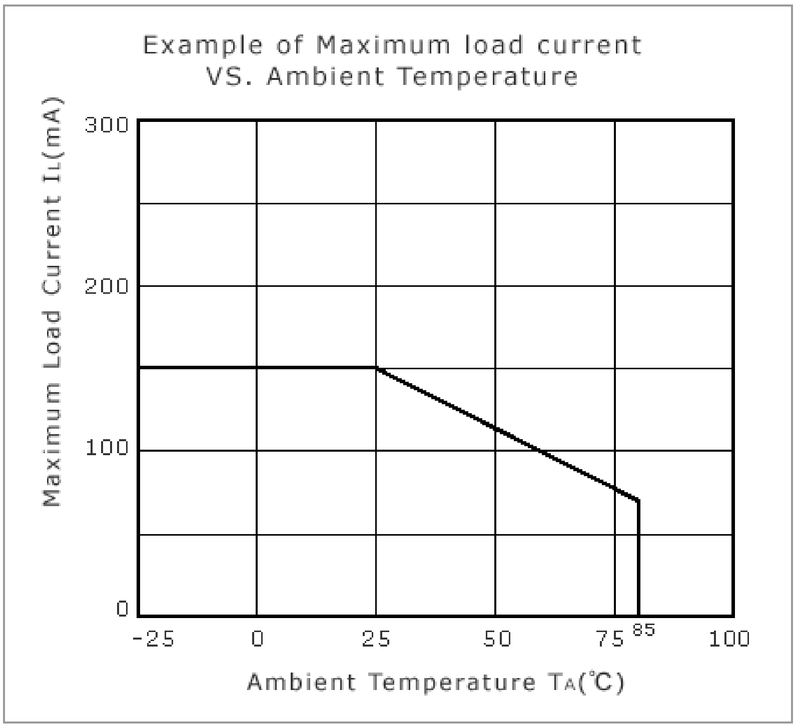
Allowable power dissipation of MOS FET on output side for ambient temperature of 25 degree Centigrade.
In the case of OCMOS FETs, the output resistance are almost constant against the change of the load current in the "ON" state, so internal loss on the output side is almost obtained from the load current value.

MOS FET: Breakdown Voltage/Load Voltage: V_L (V)

Allowable maximum voltage that can be applied between drains (and also between drain and source) when the MOS FETs on the output side are "OFF" state.
If using the two MOS FETs on the output side with their opposite polarities connected in series, the half-wave peak values (Half of amplitude in the case of sine wave) of the AC signal must not exceed this value.

MOS FET: Continuous Load Current: I_L (mA)

Allowable maximum value of the load current that can flow through the output MOS FET in the "ON" state.
Whether DC or AC, keep the peak value (Half of amplitude in the case of a sine wave) within this range.
Because of temperature dependency of allowable power dissipation, when the ambient temperature rises, this range declines as shown in the figure below.



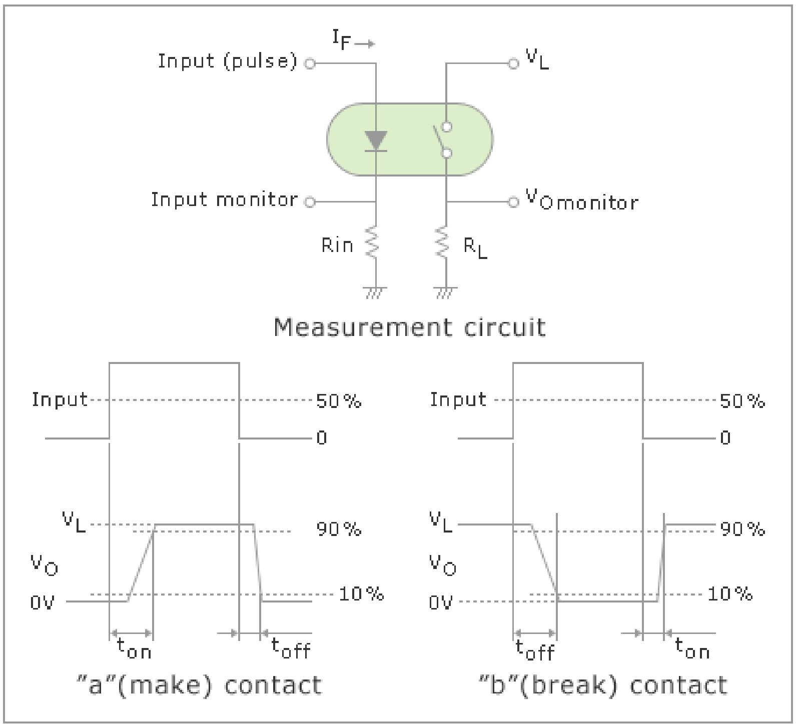
MOS FET: Pulse Load Current: I_{LP} (mA)

Allowable maximum DC load current that can be flow through the output MOS FET for a prescribed short time only.
This value is acceptable as long as it remains within the prescribed allowable range, including time limitations, such as pulse current generated by inductive load or charge and discharge peak current of capacitive load.
Basically, cyclic application is not allowed.

Electrical Characteristics

Turn-on Time/Turn-off Time: t_{on}, t_{off} (ms)

Delay time from the change of the forward current(I_F) to the change of the output when a forward current flows through a LED on the input side as a pulse.



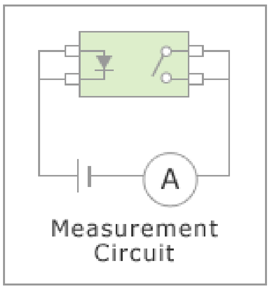
In certain case, the shorter the input pulse width as stated in the data sheet, the longer the time (t_{off} & t_{on} as below mentioned) than either the value specified in the specification or the "Typical characteristic" curve.

"a"(make) contact : turn-off time(t_{off})
"b"(break) contact : turn-on time(t_{on})

Please ensure that Input Pulse Width is operated within specified range.

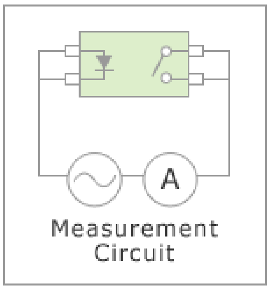
Isolation Resistance: R_{I-O} (Ω)

Initial insulation resistance when a high direct-current voltage is applied between the input and output pins.
Since the isolation resistance can decline depending on the usage environment, such as the humidity, or the application time of the voltage, perform design and testing taking into consideration actual usage conditions.



Isolation Capacitance: C_{I-O} (pF)

Capacitance when a high-frequency signal is applied between input and output pins.
The larger this value, the more likelihood of noise getting output due to sudden fluctuations in electric potential difference between input and output pins.
Since this value may increase due to wiring conditions, etc., perform design and verification taking into consideration these factors.



Light Emitting Diode: "ON" state Current: I_{Fon} (mA)

Minimum forward current(I_F) required for turning-on the output of the "a" contact ("Make" contact: Normally open: Non-conducting when no input) type OCMOS FET.
Input a forward current(I_F) greater than this value, referring to the "turn-on time vs. forward current" curve and "turn-off time vs. forward current" curve, according to the required response time.

Light Emitting Diode: "OFF" state Current: I_{Foff} (mA)

Minimum forward current(I_F) required for cutting off the output of the "b" contact ("Break" contact: Normally closed: Conducting when no input) type OCMOS FET.
Input a forward current(I_F) greater than this value, referring to the "turn-on time vs. forward current" curve and "turn-off time vs. forward current" curve, according to the required response time.

Light Emitting Diode: Forward Voltage: V_F(V)

This is the inter-pin voltage when a forward current flows through a LED on the input side.
The product of this value and the forward current value expresses the internal loss of the input side.
Generally, the increasing of the forward current or the falling of the ambient temperature causes rising of this voltage.

Light Emitting Diode: Reverse Current: I_R (μA)

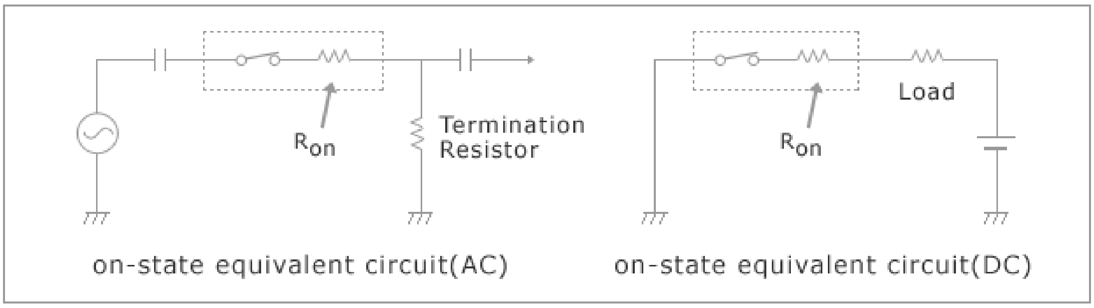
This current flows when a prescribed reverse voltage is applied within the maximum rating range to the LED on the input side.
Generally, the increasing of the reverse voltage or the rising of the ambient temperature causes increasing of this current.
In the case of circuits in which a reverse voltage is applied to the LED, design the drive circuit taking into consideration that this value is affected by usage conditions.

MOS FET: "OFF" state Leakage Current: I_{Loff} (μA)

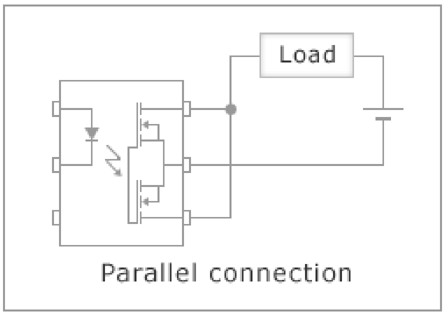
Drain leakage current when the MOS FET on the output side is non-conducting.
Generally it is proportional to the signal voltage which is switched, and the rising of the ambient temperature causes increasing of this current.
Perform design the load resistor (or termination resistor) value taking into consideration that this current tends to be affected by the temperature.

MOS FET: "ON" state Resistance: R_{on} (Ω)

Without specified otherwise, this is the resistance between drains when the MOS FETs on the output side are conducting.
The load resistor (or termination resistor) value should be generally set to a value much greater than this value.



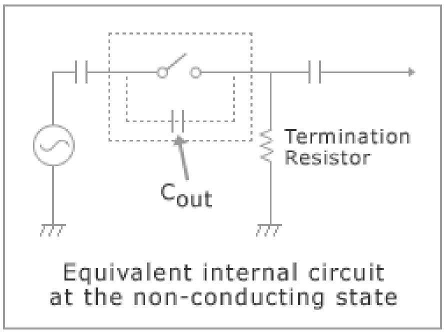
In the case of products which provide source pins, the "ON" state resistance between the drain and source of each MOS FET is approximately half of this rated value. Furthermore, by using of MOS FETs connected together in parallel as shown in the figure below, the "ON" state resistance approximately quarter of this rated value is expected (not guaranteed).



The "ON" state resistance is not influenced by the value of the forward current(I_F) of the input side, but the rising of the ambient temperature causes increasing of this resistance.
Moreover, in the case of products of the high conduction resistance type, the "ON" state resistance tends to decline with the large load current, and the specifications are provided on both of the small current area and the large current area.
When use a large conduction resistance type product between the drain and source, apply the "ON" state resistance prescribed on the small current area.

MOS FET: Output Capacitance: C_{out} (pF)

Capacitance between the output pins (between drain and drain) in relation to high-frequency signals, when the MOS FET on the output side is "OFF" state.
The smaller the voltage between the output pins, the larger this value.
Since AC signals leak through this capacitance on the "OFF" state, a fully "OFF" state cannot be obtained unless termination with a sufficiently small resistance for the higher frequency signal.


Termination
Resistor
Cout
Equivalent internal circuit
at the non-conducting state