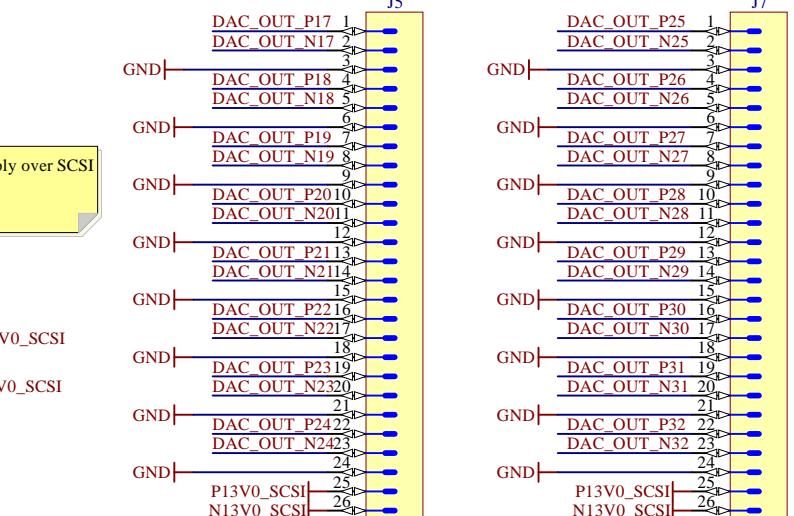
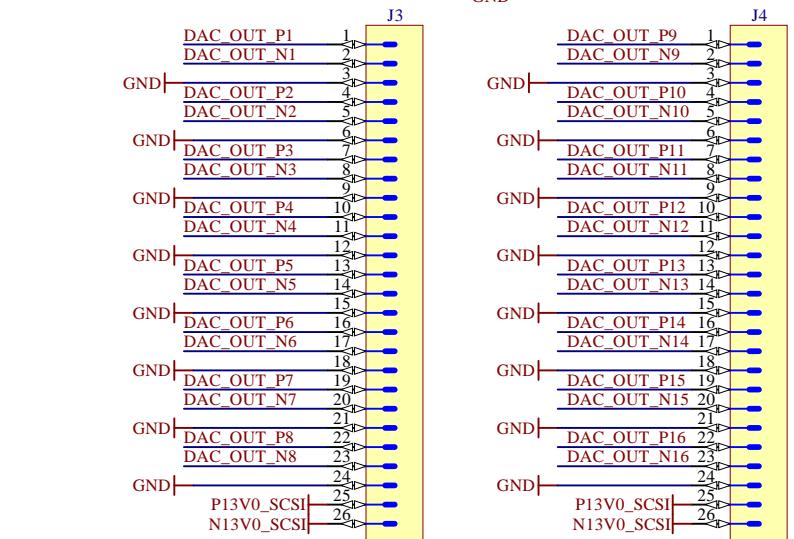
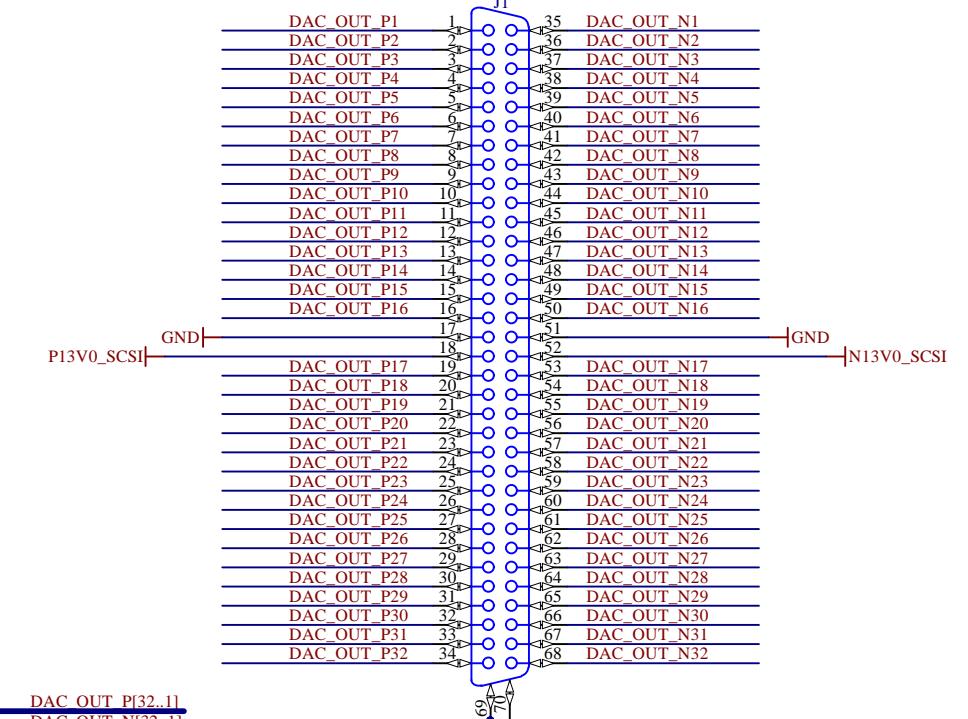
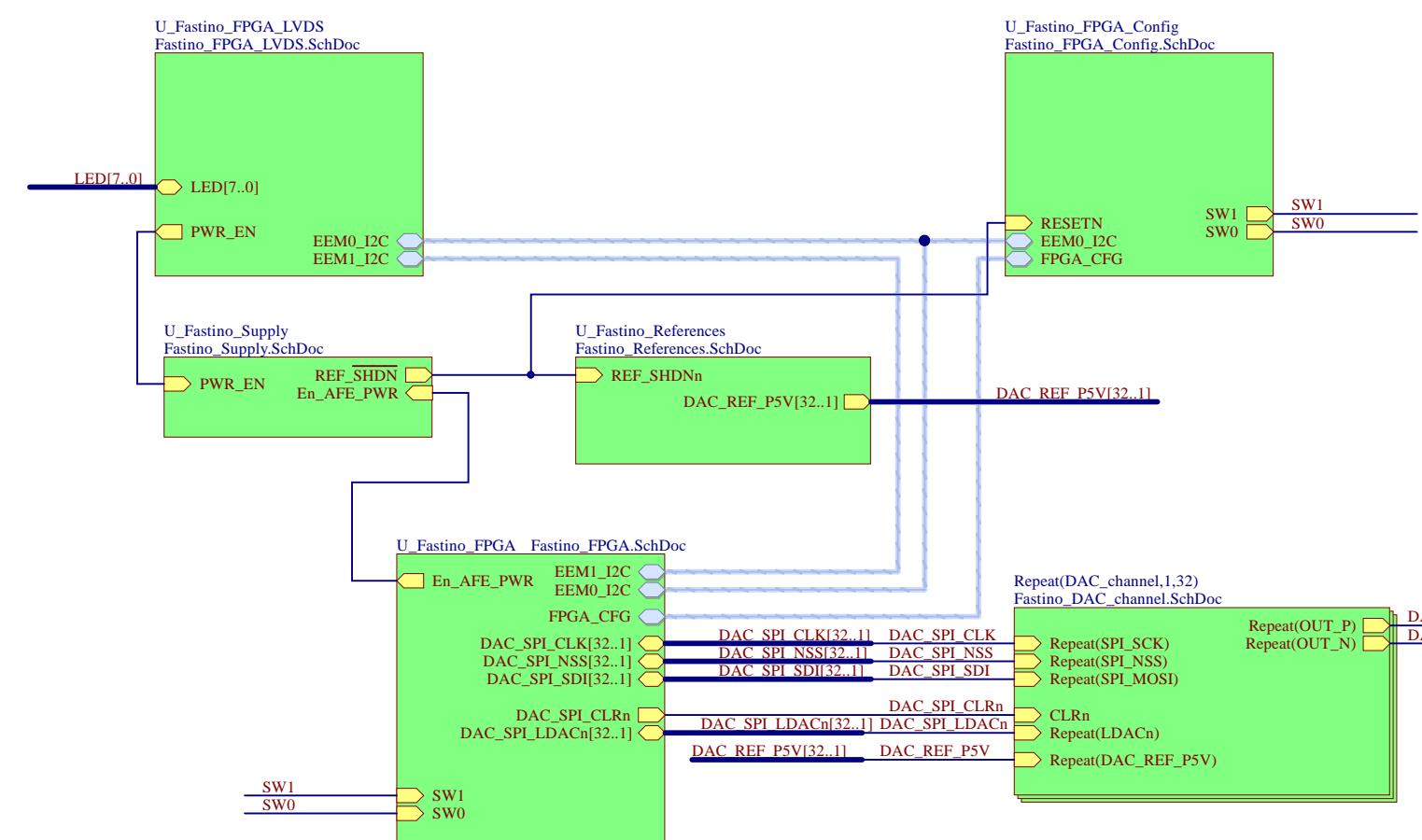
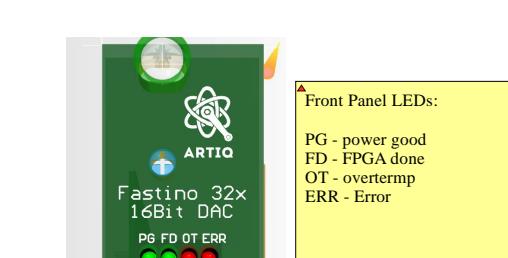


SCREW1  
2 -56 UNC

SCREW2  
2 -56 UNC



## Front panel grounding



Front Panel LEDs:  
PG - power good  
FD - FPGA done  
OT - overtemp  
ERR - Error

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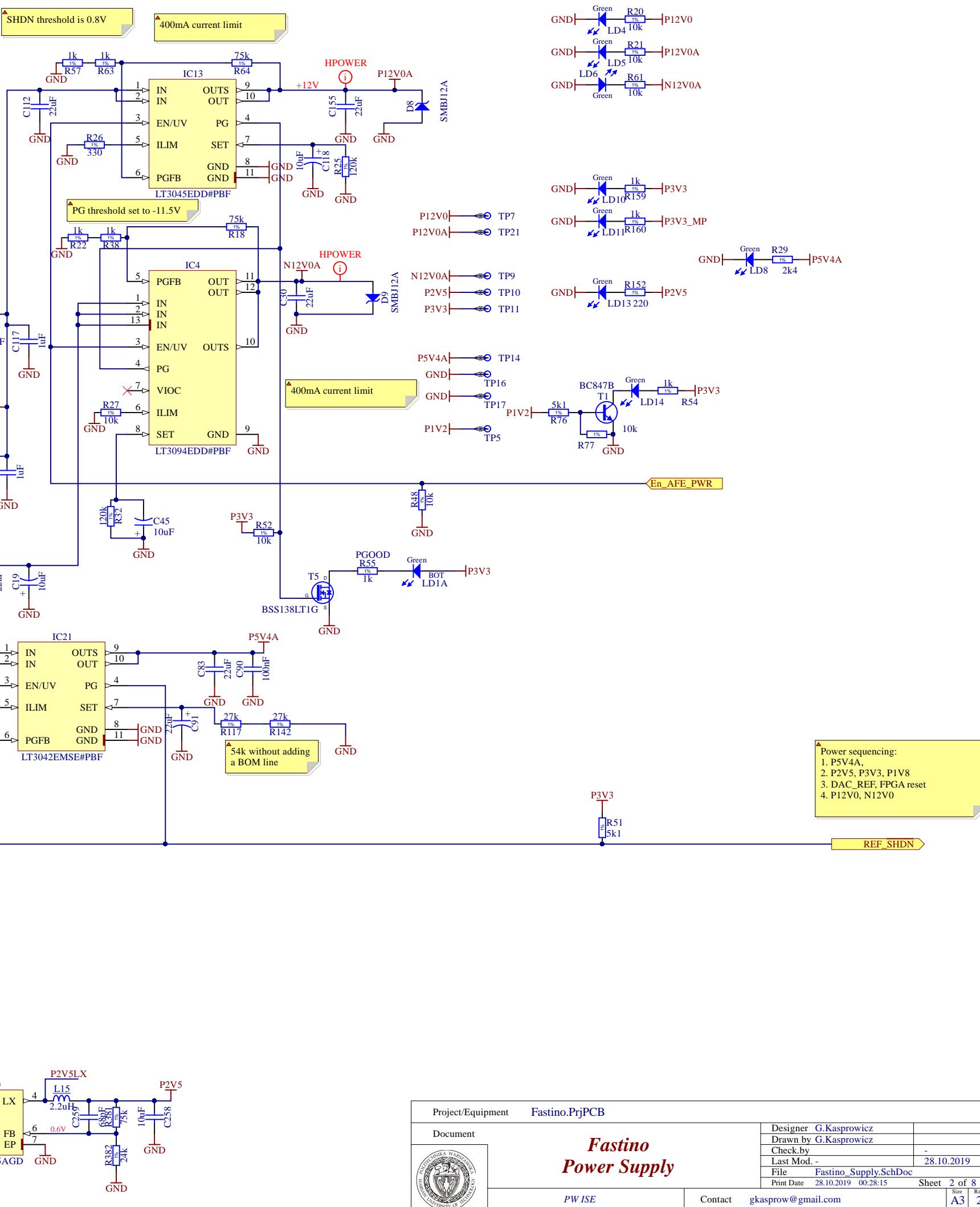
Project/Equipment	Fastino.PrjPCB	Designer	G.Kasprowicz
Document		Drawn by	G.Kasprowicz
		Check by	-
		Last Mod.	-
		File	Fastino.schdoc
		Print Date	28.10.2019 00:28:14
		Sheet	1 of 8
		Size	A3
		Rev	2

Fastino v1  
Top

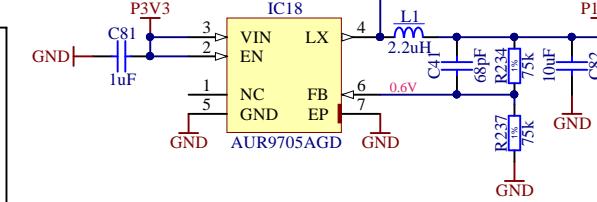
PW ISE Contact gkasprow@gmail.com

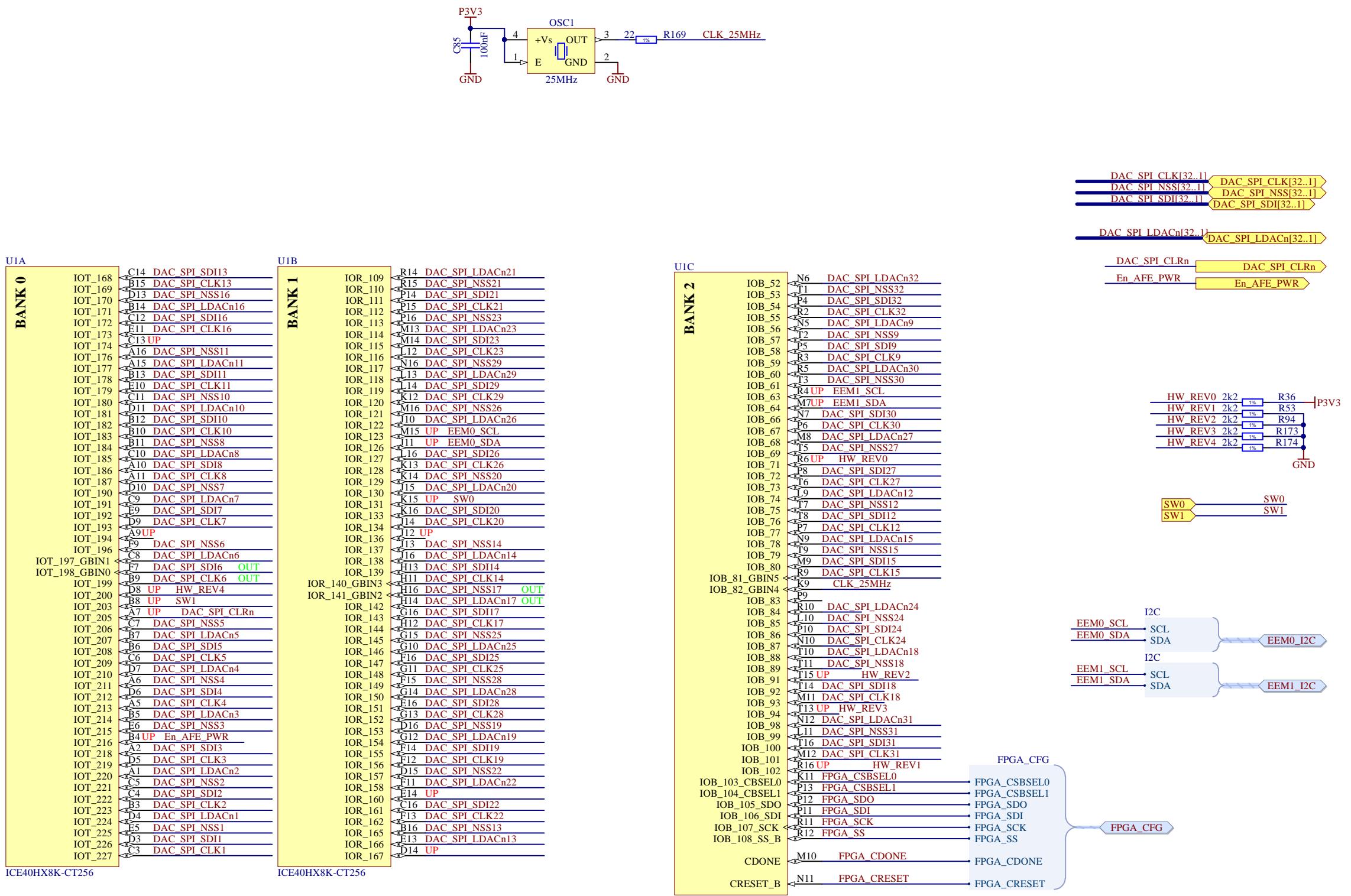
Power Budget (ext Excel file). It assumes 10mA symmetrical load on every output channel

Rail	P12V0	P1V2	P1V8	P2V5	P3V3	P5V4A	P6V0A	P7V0A	P12V0A	P12V0A	P3V3MP	P13V0	N13V0
Part													
LT3042 GND current													
LT3042 load													
AD5542 VDD													
OPA2197 DAC opamp													
OPA2197 load (10mA)													
LM75													
ADA4528													
LTC6655													
LED													
FP LEDs													
Ref load 1kx4													
LDOS:													
LT3045 (P12V0A)													
LT3094 (N12V0A)													
2xLT3042 (P5V4)													
Iq:													
NCP3170 (3V3)													
CC10-1212DF-E													
TPS62175													
AUR9705(1V2)													
AUR9705(2V5)													
FPGA													
AT25SF081-SHD-T													
2AA02E048													
rail current	52,1	500	0	302	346,1	83,6	20	9,5	396	386	3	0,03	0,03
rail current from dep.						164,7273			83,6	9,5			
rail current with dep.	52,1	500	0	302	510,8273	83,6	103,6	9,5	405,5	386	3	396,03	386,03
rail power	625,2	500	0	755	1685,73	451,44	621,6	66,5	4866	4632	9,9	5148,39	5018,39
rail converter efficiency	1	0,75	0,9	0,9	0,9	0,9	0,85	0,538462	0,8	0,8	0,9	0,923846	0,923846 total losses
rail converter losses	0	125	0	75,5	168,573	45,144	93,24	30,69231	973,2	926,4	9,9	392,0697	382,1697
													3221,888708



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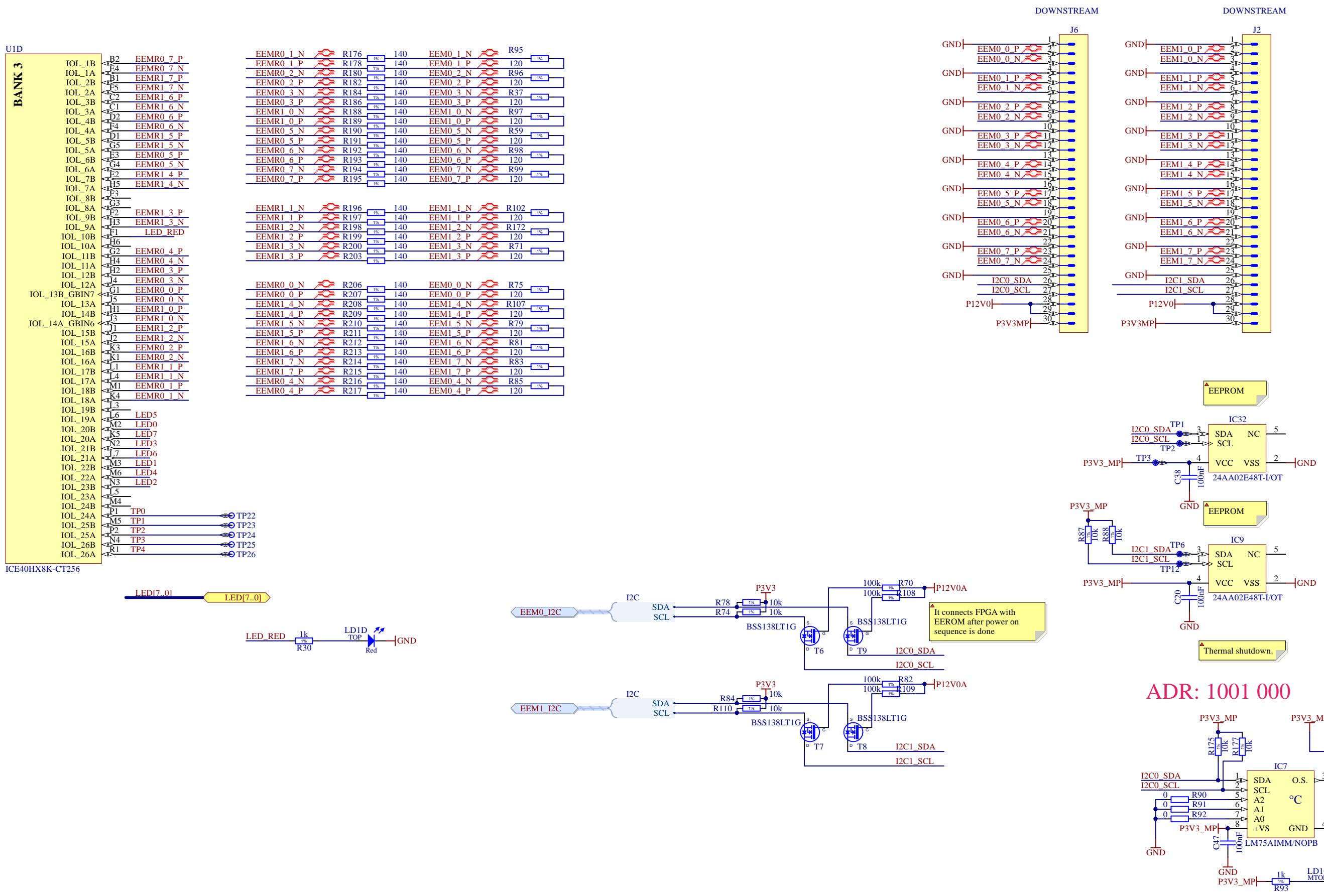




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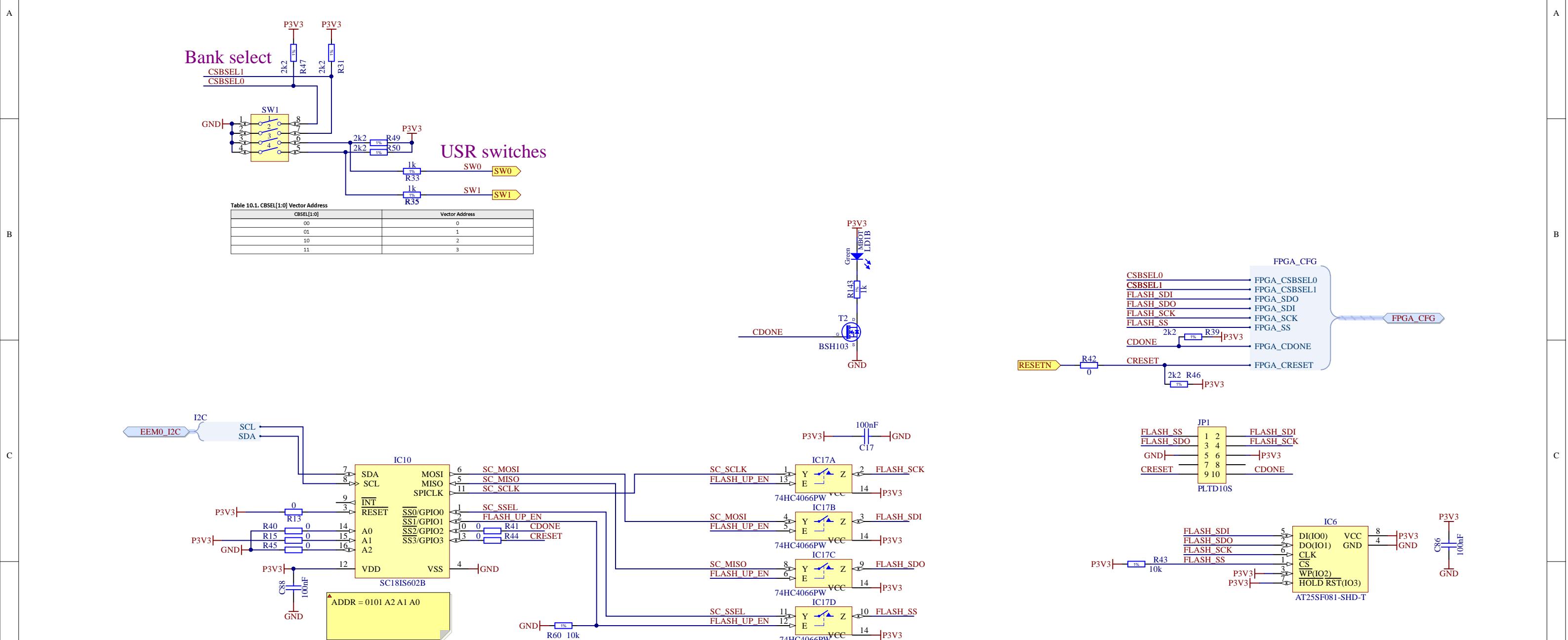
Designer	G.Kasprowicz
Drawn by	G.Kasprowicz
Check by	-
Last Mod.	27.10.2019
File	Fastino_FPGA.SchDoc
Print Date	28.10.2019 00:28:16
Sheet	3 of 8
Size	A3
Rev	2

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Project/Equipment	Fastino.PrjPCB			
Document	<b><i>Fastino</i></b> <b><i>FPGA EEM connections</i></b>	Designer	G.Kasprowicz	
		Drawn by	G.Kasprowicz	
		Check by	-	
		Last Mod.	-	27.10.2019
		File	Fastino_FPGA_LVDS.SchDoc	
		Print Date	28.10.2019 00:28:16	Sheet 4 of 8
	PW ISE	Contact	gkasprow@gmail.com	Size A3 Rev 2



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Project/Equipment: **Fastino.PrjPCB**  
Document:   
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FPGA Configuration**

Designer: G.Kasprowicz
Drawn by: G.Kasprowicz
Check by: -
Last Mod.: 27.10.2019
File: Fastino_FPGA_Config.SchDoc
Print Date: 28.10.2019 00:28:17
Sheet: 5 of 8

Size: A3 Rev: 2

PW ISE Contact: gkasprow@gmail.com

A

A

B

B

C

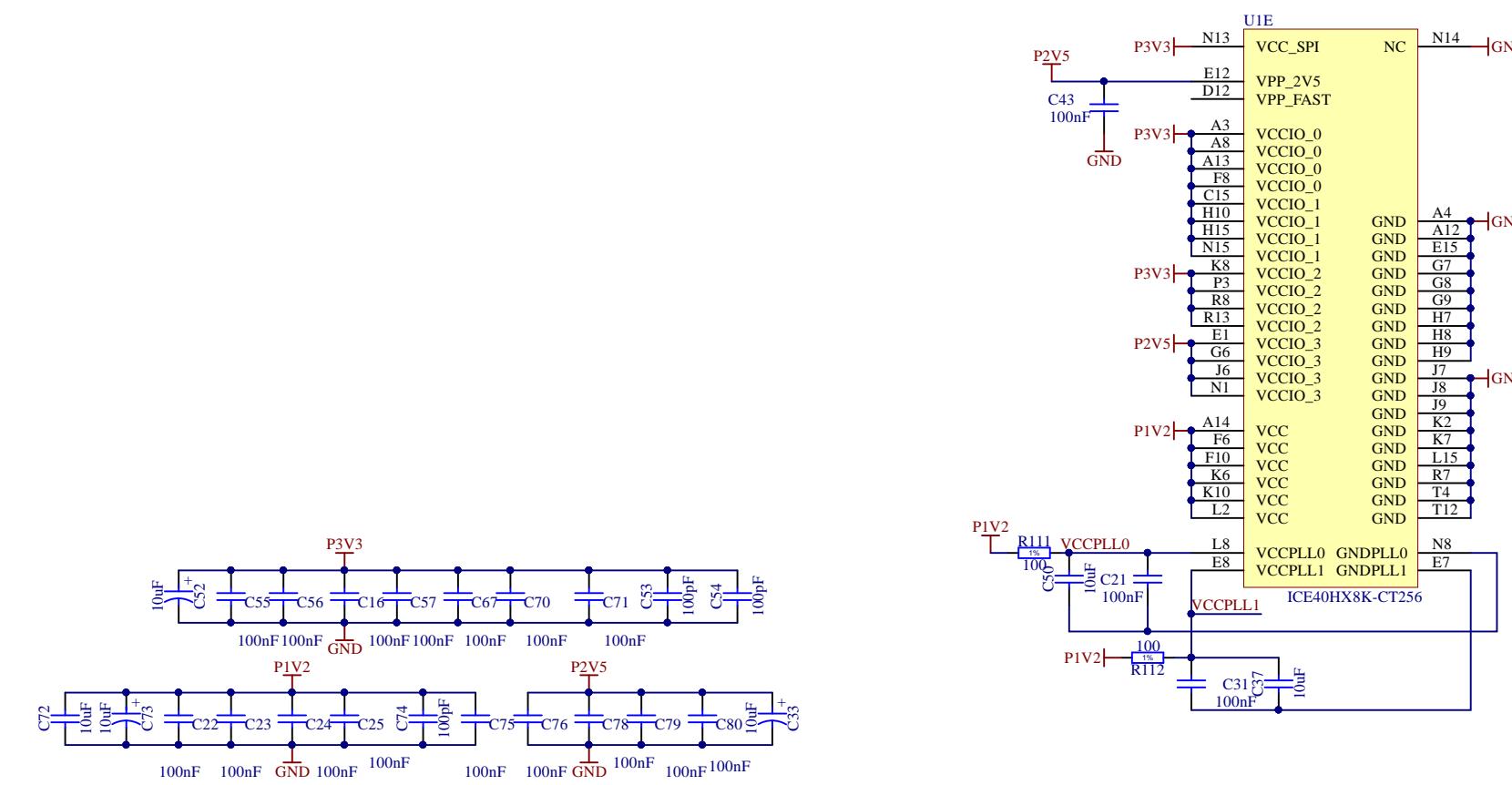
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D

D

E

E



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Project/Equipment Fastino.PrjPCB

Document

**Fastino****FPGA supply**

Designer: G.Kasprowicz

Drawn by: G.Kasprowicz

Check by:

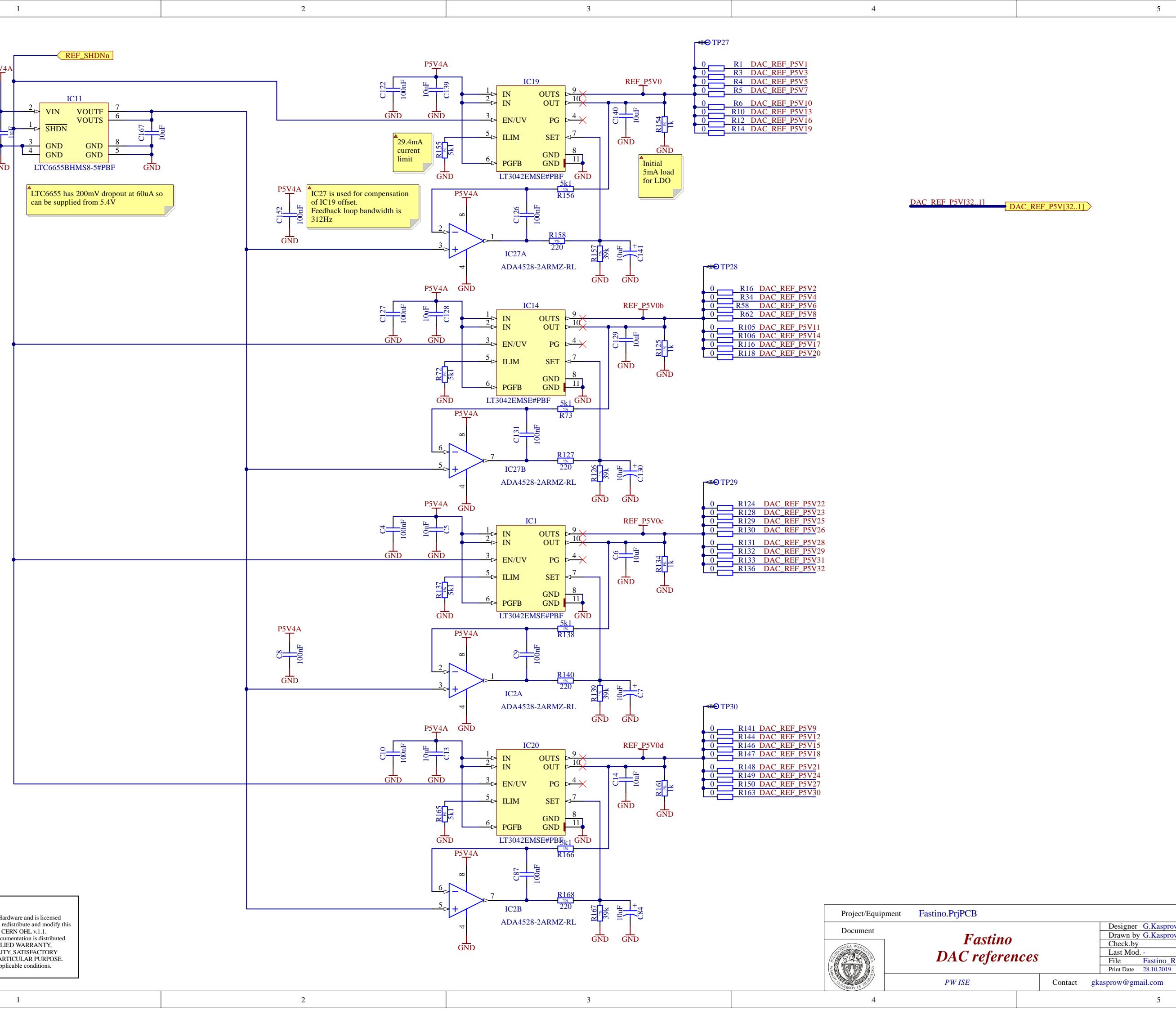
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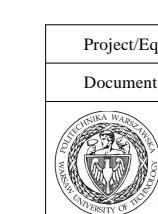
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Project/Equipment: Fastino.PrjPCB

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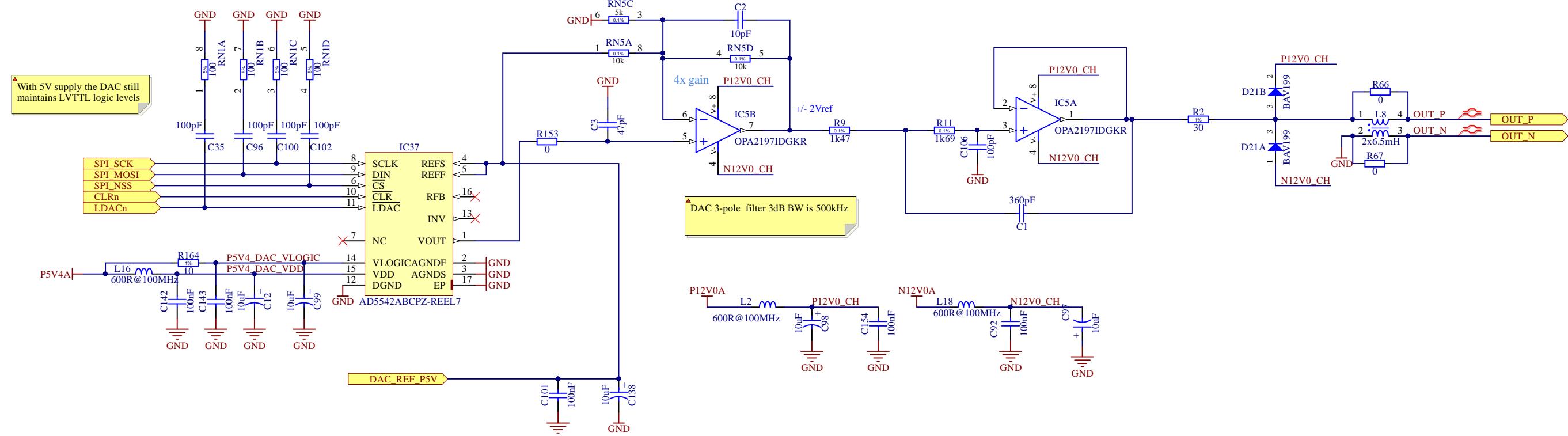
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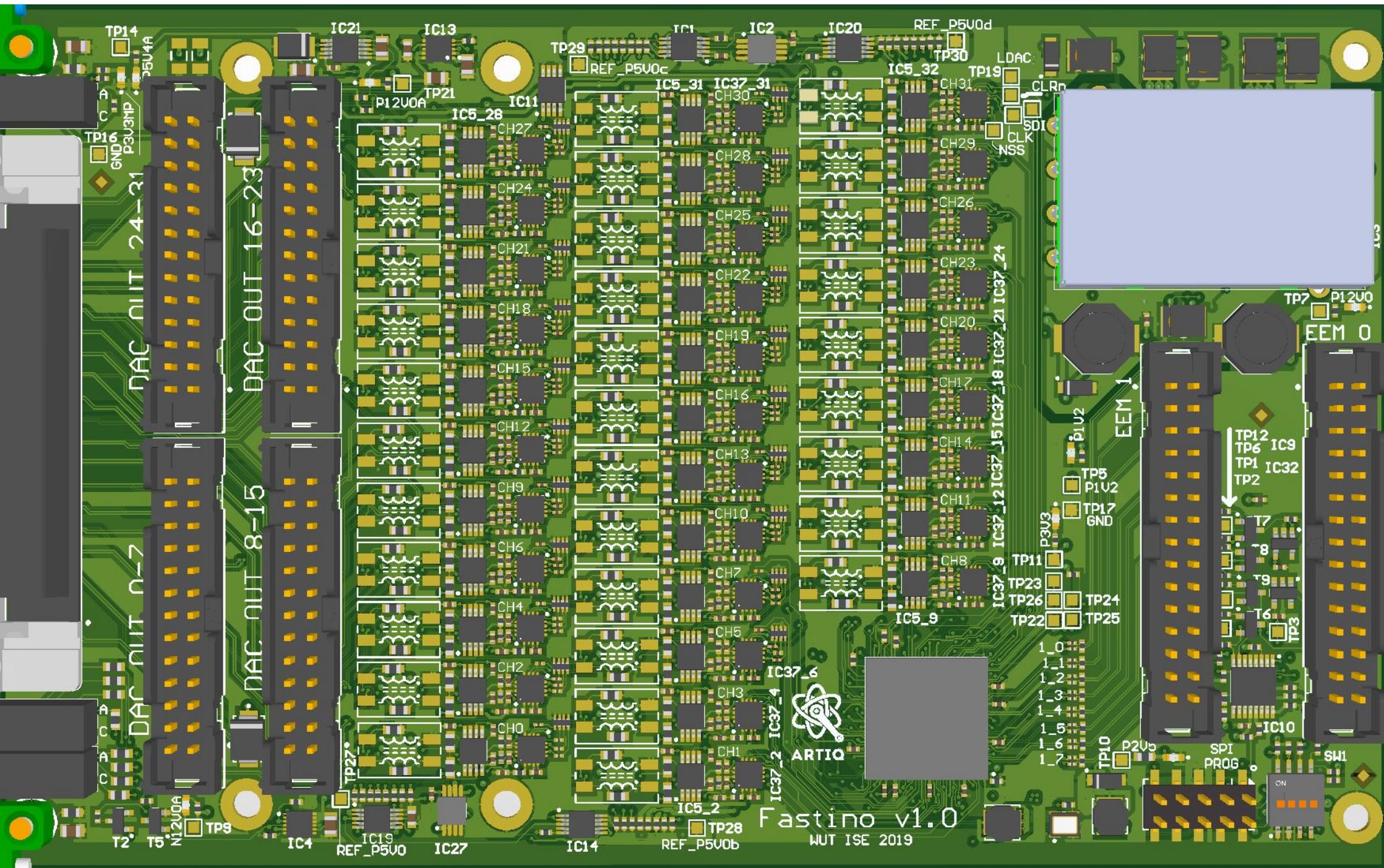
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PW ISE		Contact gkasprow@gmail.com	



Fastino v1.0



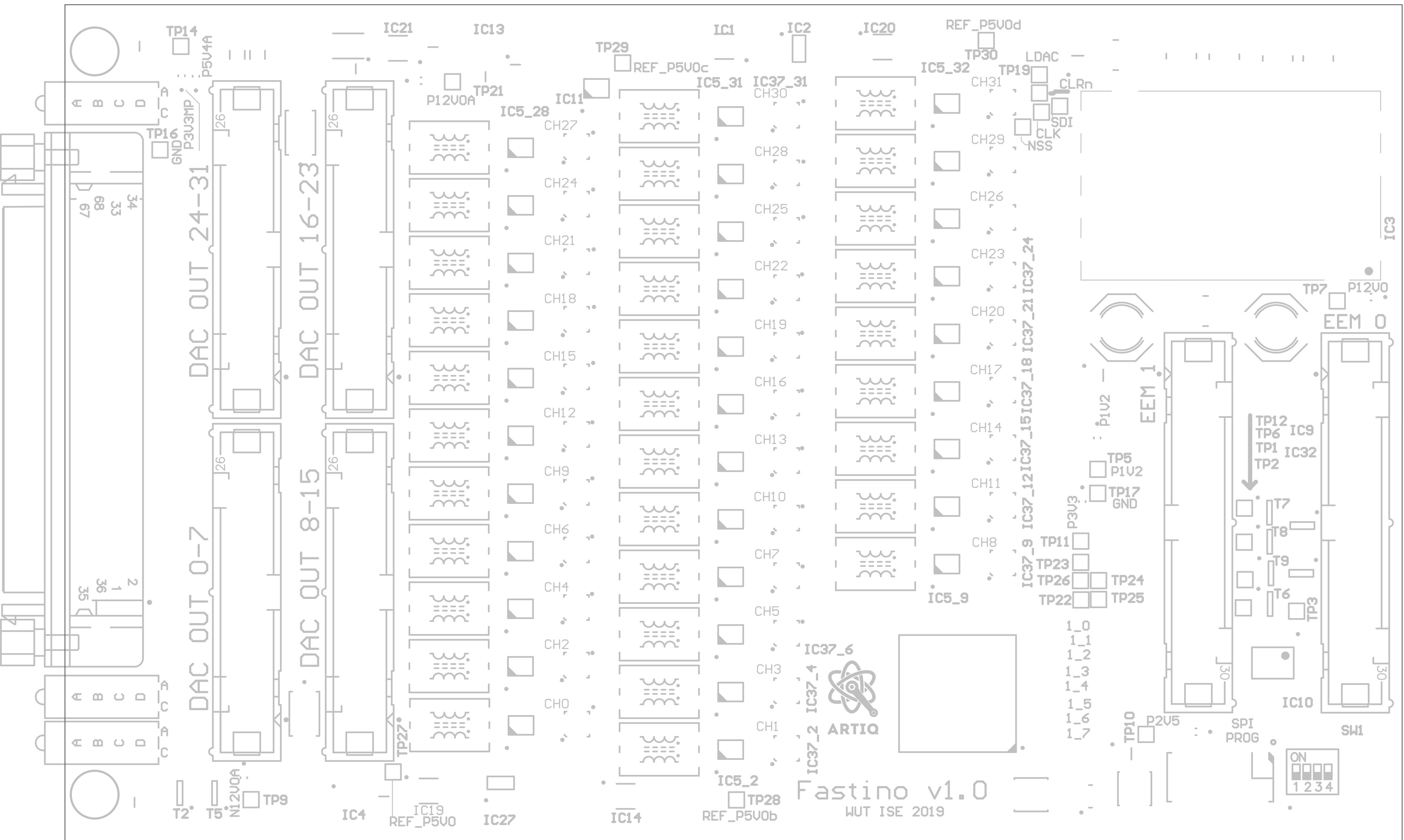
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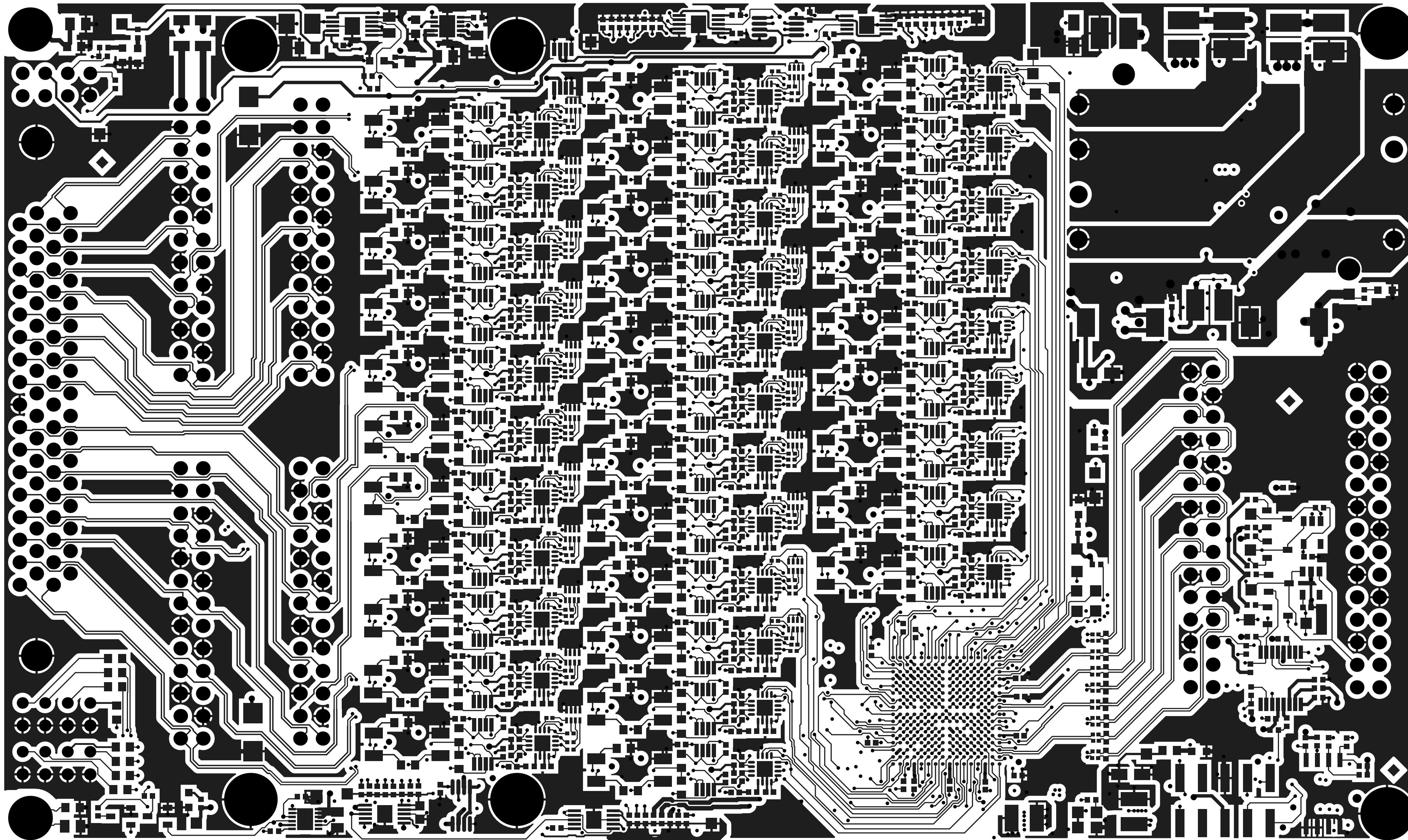
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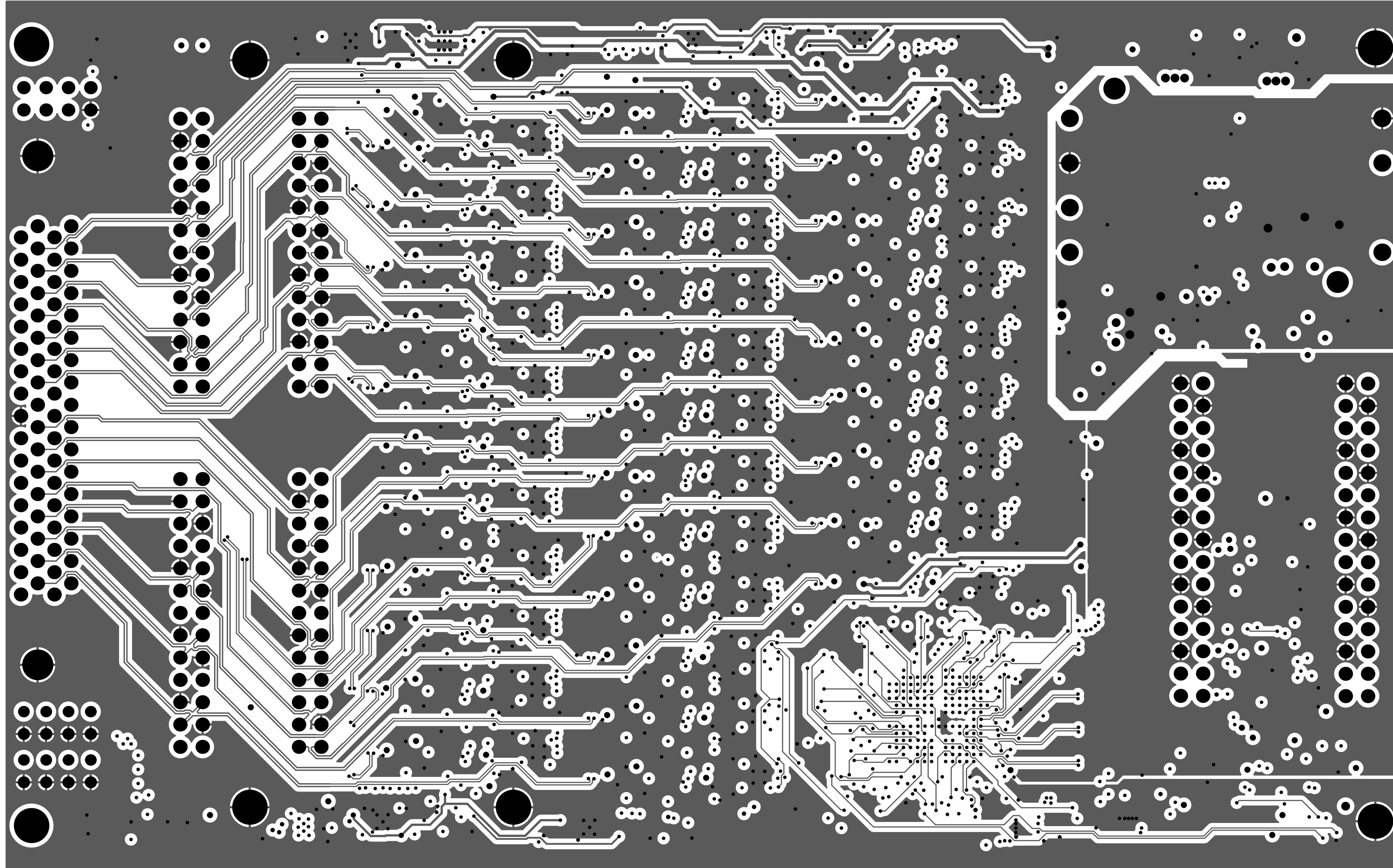
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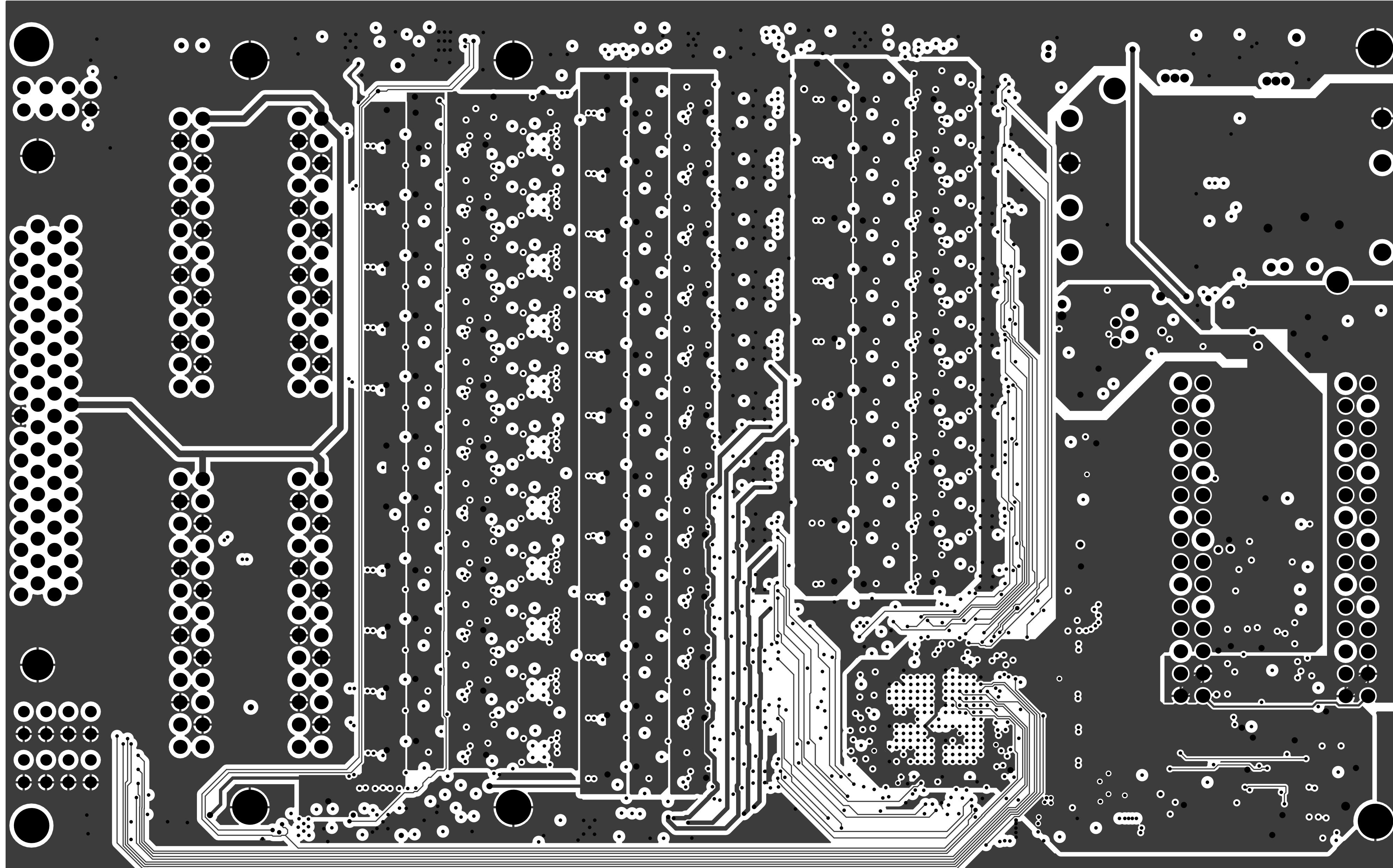
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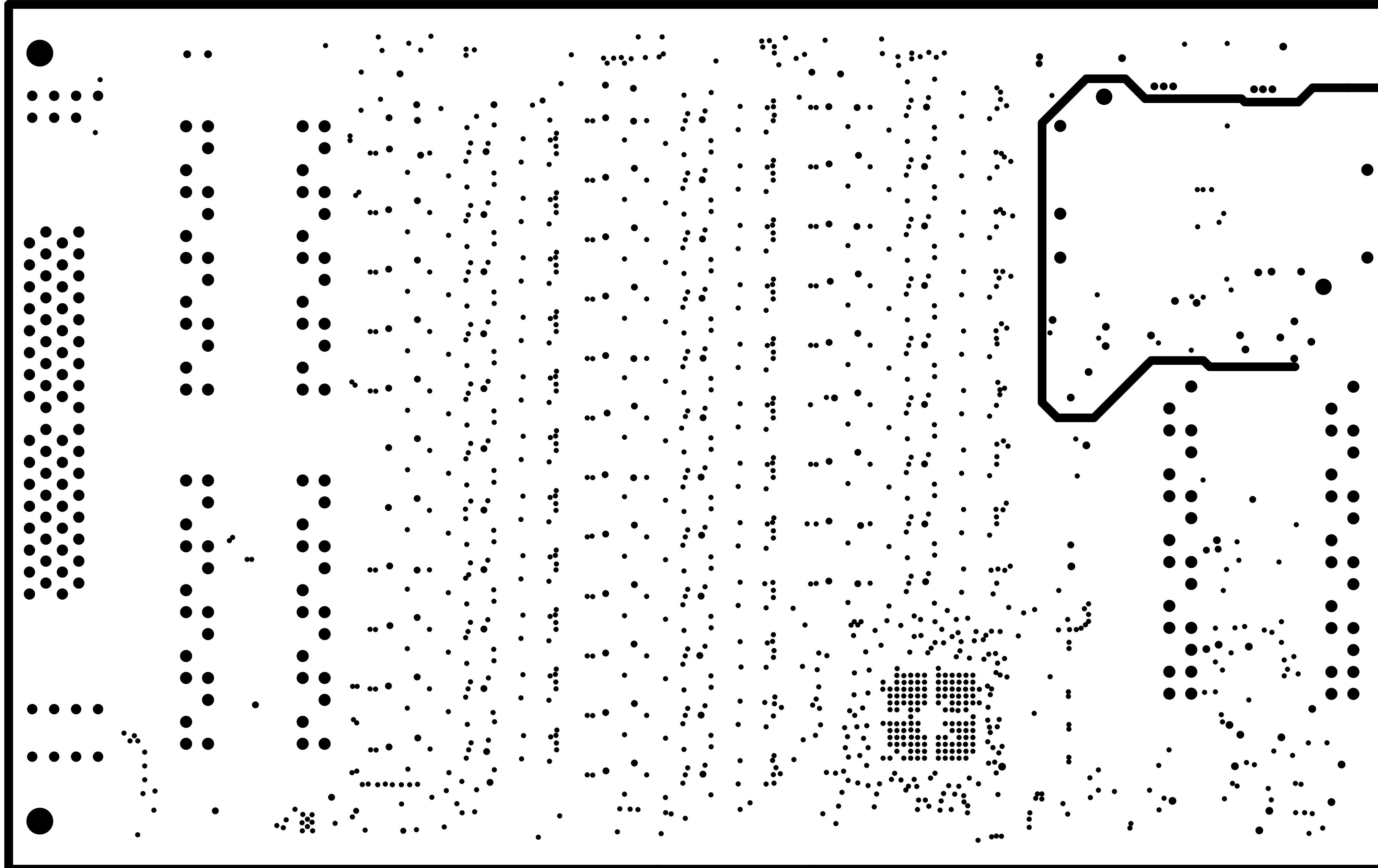
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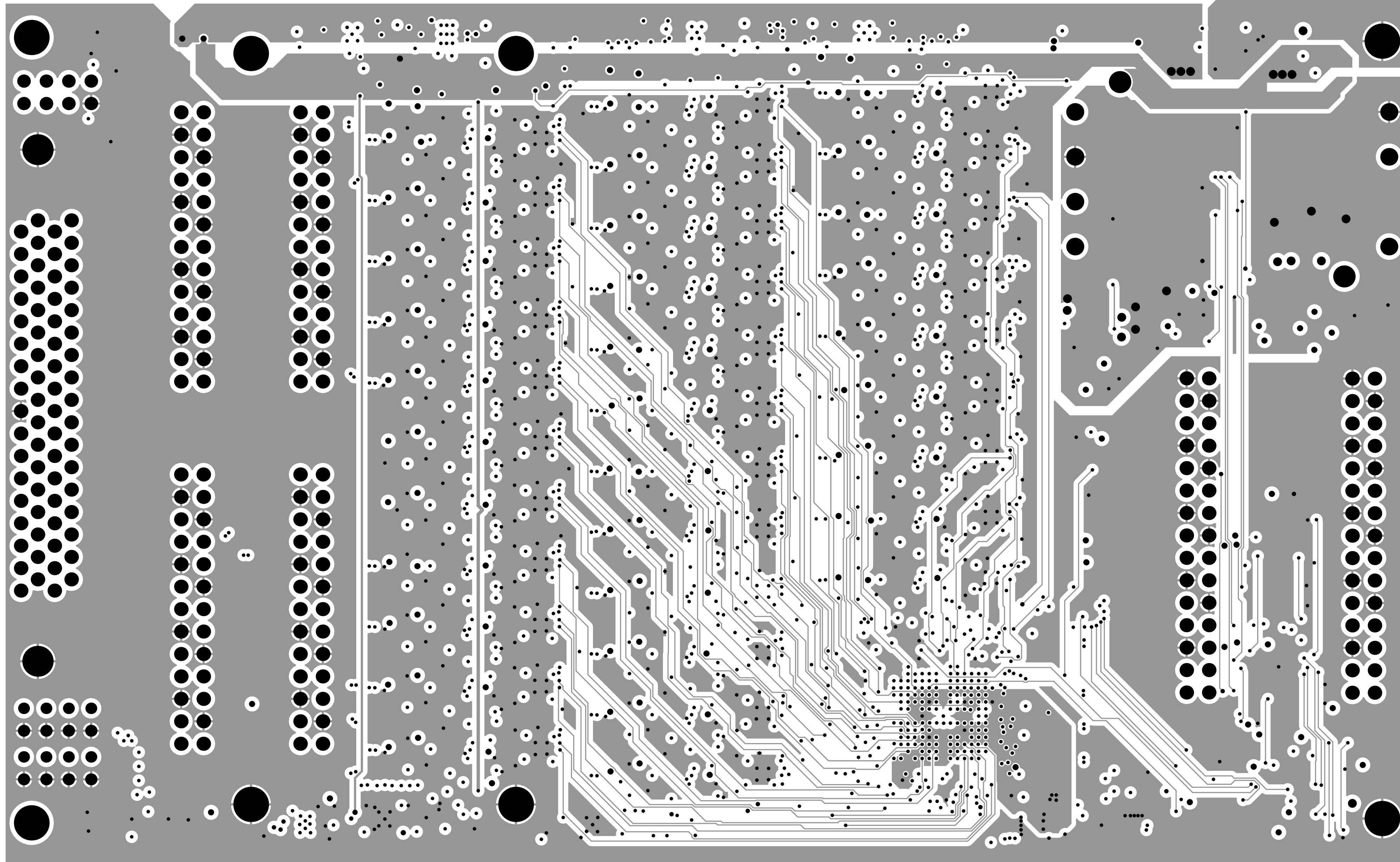


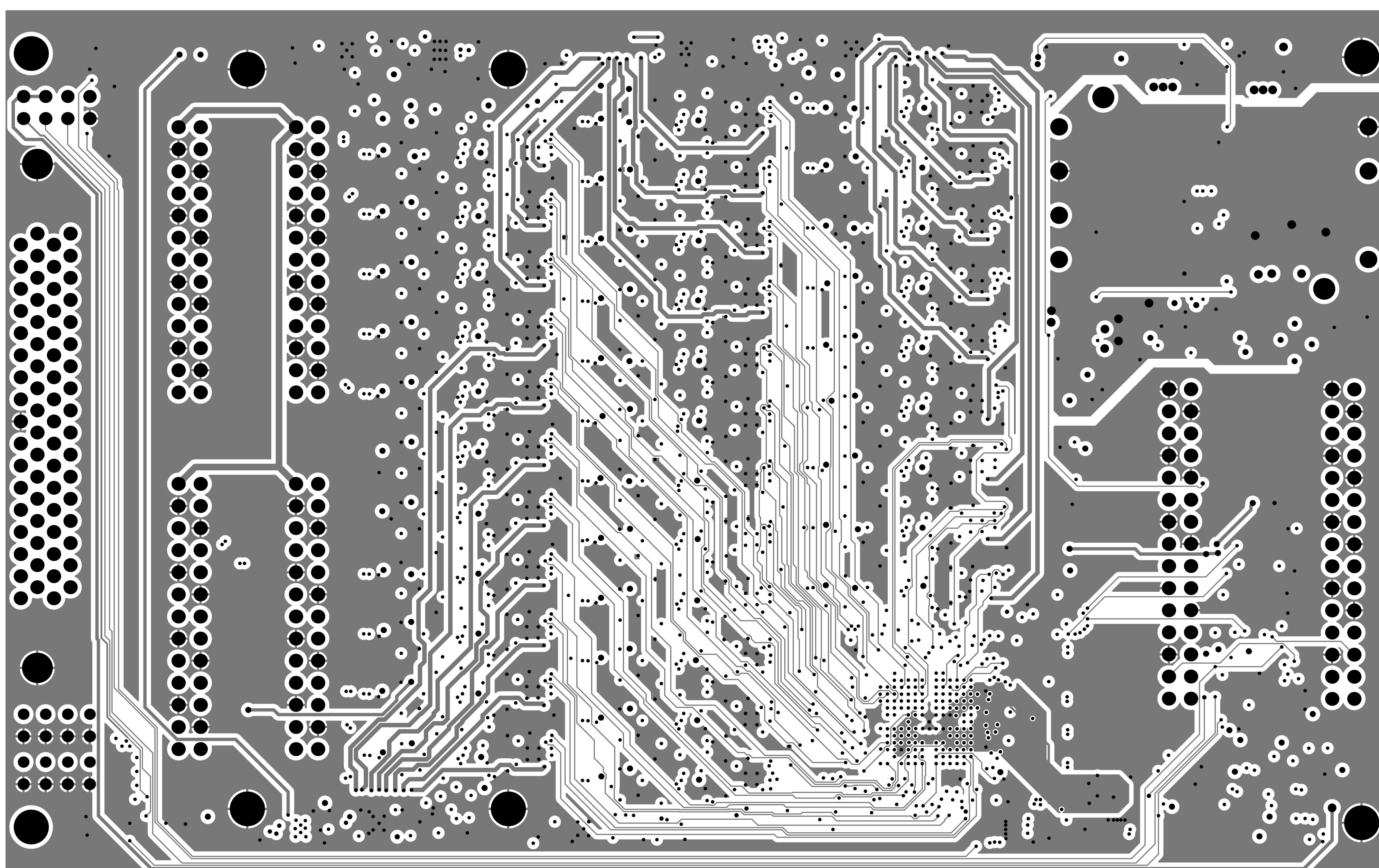


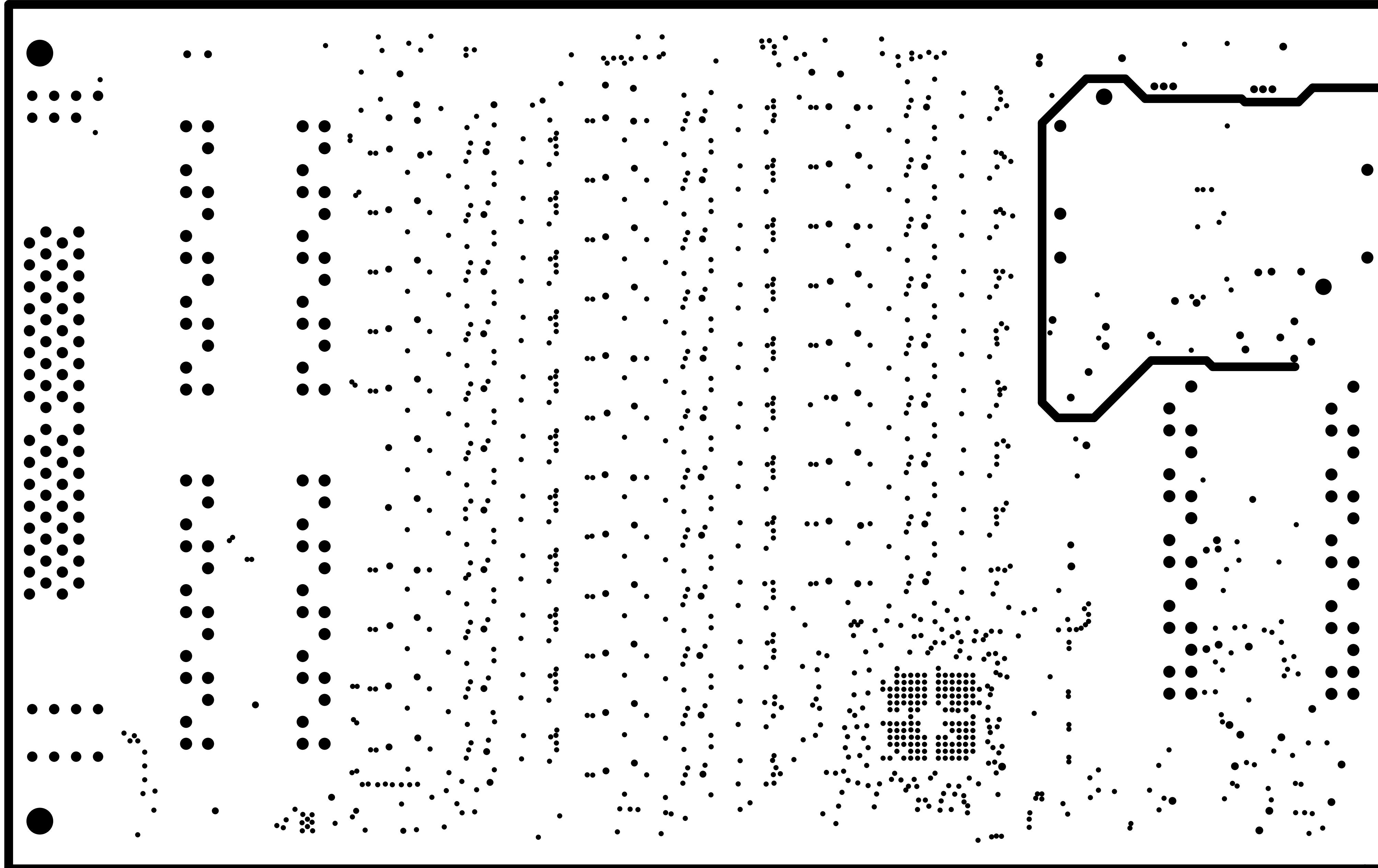


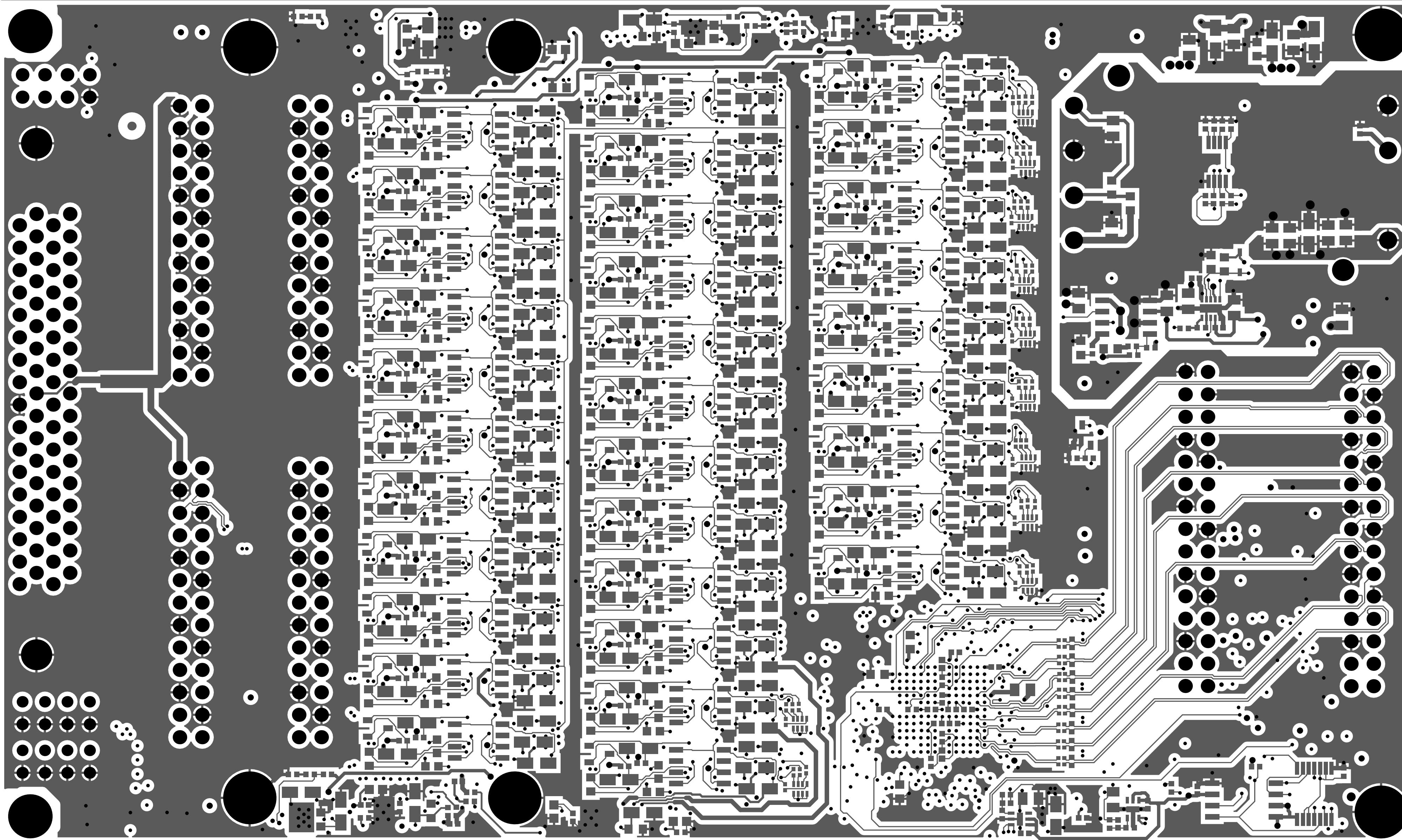






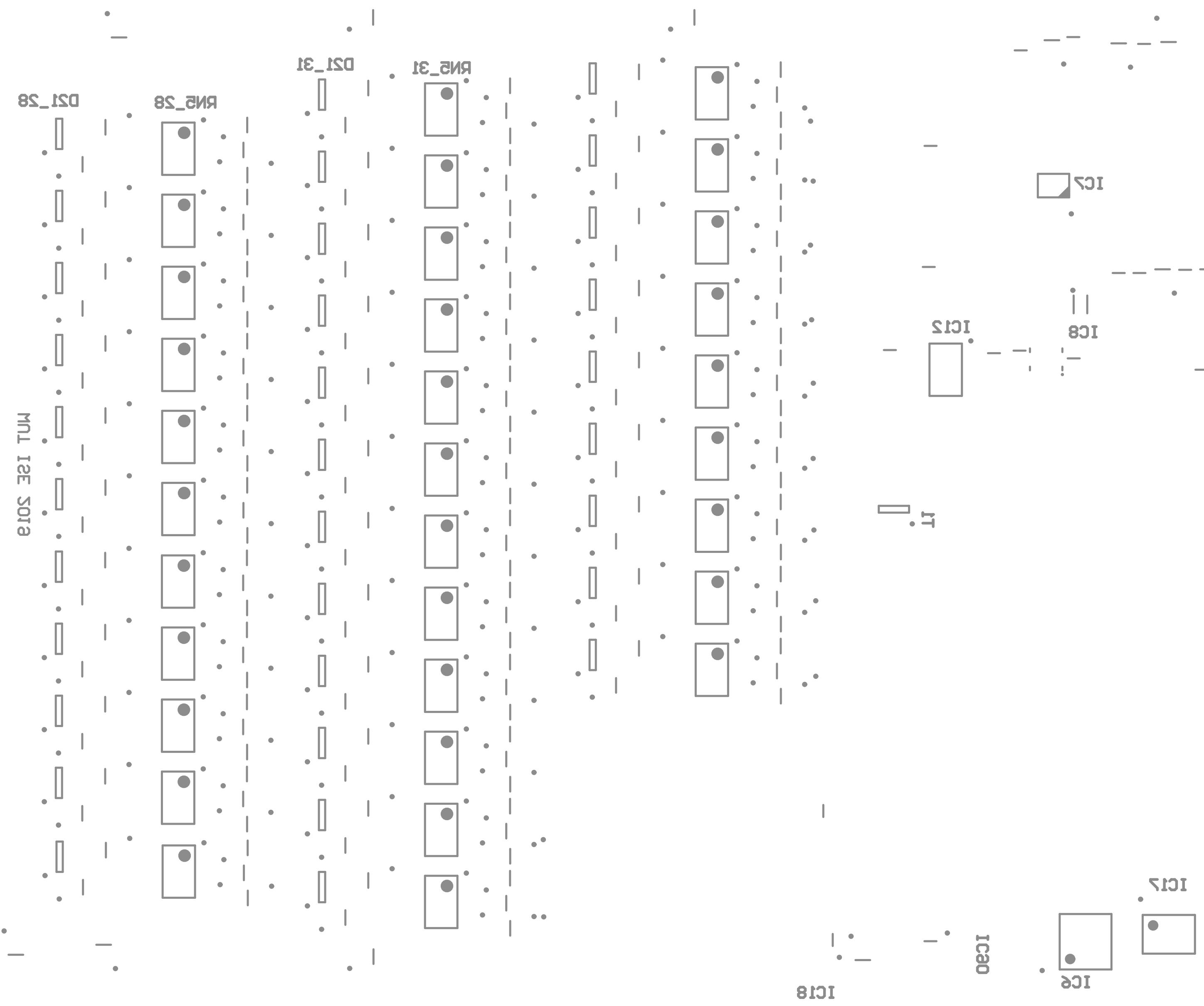








Digitized by srujanika@gmail.com



# Board Stack Report

Stack Up		Layer Stack				
Layer	Board Layer Stack	Name	Material	Thickness	Constant	
1		TopPaste				
2		Top Overlay				
3		Top Solder	Solder Resist	1,34mil	3,5	
4		L1	Copper	1,38mil		
5		Dielectric1	FR4	7,09mil	4,2	
6		L2	Copper	0,71mil		
7		Dielectric 9	Core-009	4,00mil	4,5	
8		L3	Copper	0,71mil		
9		Dielectric 1	FR4	18,11mil	4,2	
10		P4	Copper	0,71mil		
11		Dielectric 2	Core-009	4,00mil	4,5	
12		L5	Copper	0,71mil		
13		Dielectric 8	FR4	18,11mil	4,2	
14		L6	Copper	0,71mil		
15		Dielectric4	FR4	7,09mil	4,2	
16		P7	Copper	0,71mil		
17		Dielectric3	PP-006	2,80mil	4,1	
18		L8	Copper	1,40mil		
19		Bottom Solder	Solder Resist	1,34mil	3,5	
20		Bottom Overlay				
21		BottomPaste				
	Height : 70,90mil					