altera
An Intel Company

MAX® 10 FPGA Device Overview

Online Version
Send Feedback

683658
M10-OVERVIEW
2025.03.10

Contents

683658 | 2025.03.10

Send Feedback

MAX® 10 FPGA Device Overview

MAX® 10 devices are single-chip, non-volatile low-cost programmable logic devices (PLDs) to integrate the optimal set of system components.

The highlights of the MAX 10 devices include:

- Internally stored dual configuration flash
- User flash memory
- Instant on support
- Integrated analog-to-digital converters (ADCs)
- Single-chip Nios® II soft core processor support

MAX 10 devices are the ideal solution for system management, I/O expansion, communication control planes, industrial, automotive, and consumer applications.

Altera expands the MAX 10 device family with the new high I/O density packages with smaller form factor—up to 485 I/Os in 19 mm × 19 mm Variable Pitch BGA (VPBGA) packages. The VPBGA packaging is compatible with Type III PCBs that use the design rules equivalent to 0.8 mm ball pitch and standard plated through hole (PTH) vias. The VPBGA ball pitch is variable and it helps to ease signal routing. For more information, refer to the *MAX 10 FPGA Signal Integrity Design Guidelines*.

Related Information

- MAX 10 FPGA Device Datasheet
- MAX 10 FPGA Signal Integrity Design Guidelines

Key Advantages of MAX 10 Devices

Table 1. Key Advantages of MAX 10 Devices

Advantage	Supporting Feature
Simple and fast configuration	Secure on-die flash memory enables device configuration in less than 10 ms
Flexibility and integration	• Single device integrating PLD logic, RAM, flash memory, digital signal processing (DSP), ADC, phase-locked loop (PLL), and I/Os • Small packages available from 3 mm × 3 mm
Low power	• Sleep mode—significant standby power reduction and resumption in less than 1 ms • Longer battery life—resumption from full power-off in less than 10 ms
20-year-estimated life cycle	Built on TSMC's 55 nm embedded flash process technology
High productivity design tools	• Quartus® Prime Lite edition (no cost license) • Platform Designer (Standard) system integration tool • DSP Builder for Intel® FPGAs • Nios II Embedded Design Suite (EDS)

Summary of MAX 10 Device Features

Table 2. Summary of Features for MAX 10 Devices

Feature	Description
Technology	55 nm TSMC Embedded Flash (Flash + SRAM) process technology
Packaging	• Low cost, small form factor packages—support multiple packaging technologies and pin pitches • Multiple device densities with compatible package footprints for seamless migration between different device densities • RoHS6-compliant
Core architecture	• 4-input look-up table (LUT) and single register logic element (LE) • LEs arranged in logic array block (LAB) • Embedded RAM and user flash memory • Clocks and PLLs • Embedded multiplier blocks • General purpose I/Os
Internal memory blocks	• M9K—9 kilobits (Kb) memory blocks • Cascadable blocks to create RAM, dual port, and FIFO functions
User flash memory (UFM)	• User accessible non-volatile storage • High speed operating frequency • Large memory size • High data retention • Multiple interface option
Embedded multiplier blocks	• One 18 × 18 or two 9 × 9 multiplier modes • Cascadable blocks enabling creation of filters, arithmetic functions, and image processing pipelines
ADC	• 12-bit successive approximation register (SAR) type • Up to 17 analog inputs • Cumulative speed up to 1 million samples per second (MSPS) • Integrated temperature sensing capability
Clock networks	• Global clocks support • High speed frequency in clock network
Internal oscillator	Built-in internal ring oscillator
PLLs	• Analog-based • Low jitter • High precision clock synthesis • Clock delay compensation • Zero delay buffering • Multiple output taps
General-purpose I/Os (GPIOs)	• Multiple I/O standards support • On-chip termination (OCT) • Up to 720 megabits per second (Mbps) LVDS receiver and transmitter
External memory interface (EMIF) (1)	Supports up to 600 Mbps external memory interfaces: • DDR3, DDR3L, DDR2, LPDDR2 (on 10M16, 10M25, 10M40, and 10M50.) • SRAM (Hardware support only)

continued...

(1) EMIF is only supported in selected MAX 10 device density and package combinations. Refer to the *MAX 10 External Memory Interface User Guide* for more information.

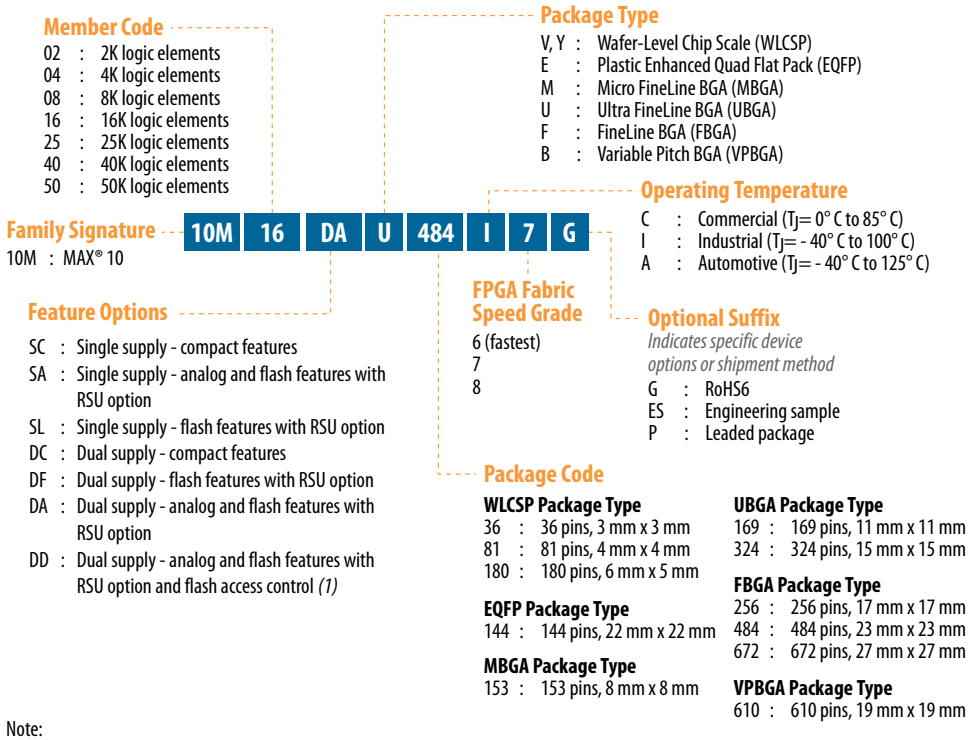
Feature	Description
	Note: For 600 Mbps performance, –6 device speed grade is required. Performance varies according to device grade (commercial, industrial, or automotive) and device speed grade (–6 or –7). Refer to the *MAX 10 FPGA Device Datasheet* or *External Memory Interface Spec Estimator* for more details.
Configuration	• Internal configuration • JTAG • Advanced Encryption Standard (AES) 128-bit encryption and compression options • Flash memory data retention of 20 years at 85 °C
Flexible power supply schemes	• Single- and dual-supply device options • Dynamically controlled input buffer power down • Sleep mode for dynamic power reduction

Related Information

- MAX 10 FPGA Device Datasheet
- MAX 10 External Memory Interface User Guide
- External Memory Interface (EMIF) Spec Estimator
  Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in Altera® FPGAs.

MAX 10 Device Ordering Information

Figure 1. Sample Ordering Code and Available Options for MAX 10 Devices



Note:
(1) DD OPN available only on 10M40 and 10M50 devices with F256, F484, F672, and B610 packages.

Note: The –A6 speed grade of the MAX 10 FPGA devices is not available by default in the Quartus Prime software. Contact your local Altera sales representatives for support.

Related Information

Altera® FPGA Product Selector
Provides the latest information about MAX 10 FPGAs.

MAX 10 Device Feature Options

Table 3. Feature Options for MAX 10 Devices

Option	Feature
Compact	Devices with core architecture featuring single configuration image with self-configuration capability
Flash	Devices with core architecture featuring: • Dual configuration image with self-configuration capability • Remote system upgrade capability • Memory initialization
Analog	Devices with core architecture featuring: • Dual configuration image with self-configuration capability • Remote system upgrade capability • Memory initialization • Integrated ADC

MAX 10 Device Maximum Resources

Table 4. Maximum Resource Counts for MAX 10 Devices

Resource		Device						
		10M02	10M04	10M08	10M16	10M25	10M40	10M50
Logic Elements (LE) (K)		2	4	8	16	25	40	50
M9K Memory (Kb)		108	189	378	549	675	1,260	1,638
User Flash Memory (Kb) (2)		96	1,248	1,376	2,368	3,200	5,888	5,888
18 × 18 Multiplier		16	20	24	45	55	125	144
PLL		2	2	2	4	4	4	4
GPIO		246	246	250	320	360	500	500
LVDS	Dedicated Transmitter	15	15	15	22	24	30	30
	Emulated Transmitter	114	114	116	151	171	241	241
	Dedicated Receiver	114	114	116	151	171	241	241
Internal Configuration Image		1	2	2	2	2	2	2
ADC		—	1	1	1	2	2	2

(2) The maximum possible value including user flash memory and configuration flash memory. For more information, refer to MAX 10 User Flash Memory User Guide.

MAX 10 Devices I/O Resources Per Package

Table 5. Package Plan for MAX 10 Single Power Supply Devices

Device	Package							
	Type	V81 81-pin WLCSP	Y180 180-pin WLCSP	M153 153-pin MBGA	U169 169-pin UBGA	U324 324-pin UBGA	B610 610-pin VPBGA(3)	E144 144-pin EQFP
	Size	4 mm × 4 mm	6 mm × 5 mm	8 mm × 8 mm	11 mm × 11 mm	15 mm × 15 mm	19 mm × 19 mm	22 mm × 22 mm
	Ball Pitch	0.4 mm	0.35 mm	0.5 mm	0.8 mm	0.8 mm	Variable(4)	0.5 mm
10M02		—	—	112	130	246	—	101
10M04		—	—	112	130	246	—	101
10M08		58	—	112	130	246	—	101
10M16		—	125	—	130	246	—	101
10M25		—	—	—	—	—	—	101
10M40		—	—	—	—	—	485	101
10M50		—	—	—	—	—	485	101

Table 6. Package Plan for MAX 10 Dual Power Supply Devices

Device	Package							
	Type	V36 36-pin WLCSP (5)	V81 81-pin WLCSP (5)	U324 324-pin UBGA	F256 256-pin FBGA	B610 610-pin VPBGA(3)	F484 484-pin FBGA	F672 672-pin FBGA
	Size	3 mm × 3 mm	4 mm × 4 mm	15 mm × 15 mm	17 mm × 17 mm	19 mm × 19 mm	23 mm × 23 mm	27 mm × 27 mm
	Ball Pitch	0.4 mm	0.4 mm	0.8 mm	1.0 mm	Variable(4)	1.0 mm	1.0 mm
10M02		27	—	160	—	—	—	—
10M04		—	—	246	178	—	—	—
10M08		—	56	246	178	—	250	—
10M16		—	—	246	178	—	320	—

continued...

(3) I/O placement restriction applies. For more information, refer to the MAX 10 FPGA Signal Integrity Design Guidelines.

(4) The Variable Pitch BGA (VPBGA) packaging is compatible with Type III PCBs that use the design rules equivalent to 0.8 mm ball pitch and standard plated through hole (PTH) vias. The VPBGA ball pitch is variable and it helps to ease signal routing. For more information, refer to the *MAX 10 FPGA Signal Integrity Design Guidelines*.

(5) For the performance specifications of the V36 and V81 packages of MAX 10 dual power supply devices, follow the data sheet specifications for single supply devices.

Device	Package							
	Type	V36 36-pin WLCSP (5)	V81 81-pin WLCSP (5)	U324 324-pin UBGA	F256 256-pin FBGA	B610 610-pin VPBGA(3)	F484 484-pin FBGA	F672 672-pin FBGA
	Size	3 mm × 3 mm	4 mm × 4 mm	15 mm × 15 mm	17 mm × 17 mm	19 mm × 19 mm	23 mm × 23 mm	27 mm × 27 mm
	Ball Pitch	0.4 mm	0.4 mm	0.8 mm	1.0 mm	Variable(4)	1.0 mm	1.0 mm
10M25		—	—	—	178	—	360	—
10M40		—	—	—	178	485	360	500
10M50		—	—	—	178	485	360	500

Related Information

- MAX 10 FPGA Signal Integrity Design Guidelines
- MAX 10 General Purpose I/O User Guide
- MAX 10 High-Speed LVDS I/O User Guide
- MAX 10 External Memory Interface User Guide

(5) For the performance specifications of the V36 and V81 packages of MAX 10 dual power supply devices, follow the data sheet specifications for single supply devices.

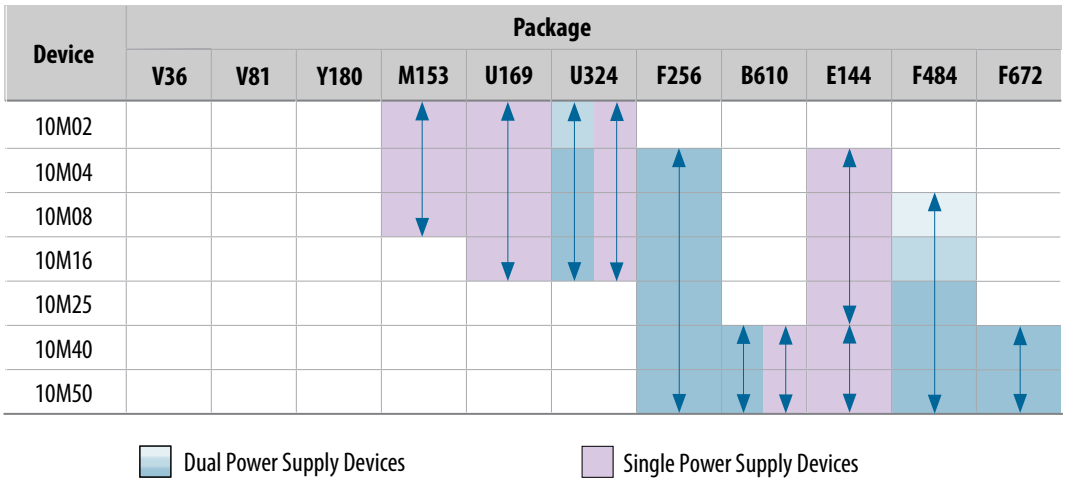
MAX 10 Vertical Migration Support

Vertical migration supports the migration of your design to other MAX 10 devices of different densities in the same package with similar I/O and ADC resources.

MAX 10 I/O Vertical Migration Support

Figure 2. Migration Capability Across MAX 10 Devices

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Non-migratable devices are omitted. Some packages have several migration paths. Devices with lesser I/O resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os usage to match the product line with the lowest I/O count.



Note: Before starting migration work, Intel recommends that you verify the pin migration compatibility through the **Pin Migration View** window in the Quartus Prime software Pin Planner. For example, not all MAX 10 devices support 1.0 V I/O.

MAX 10 ADC Vertical Migration Support

Figure 3. ADC Vertical Migration Across MAX 10 Devices

The arrows indicate the ADC migration paths. The devices included in each vertical migration path are shaded.

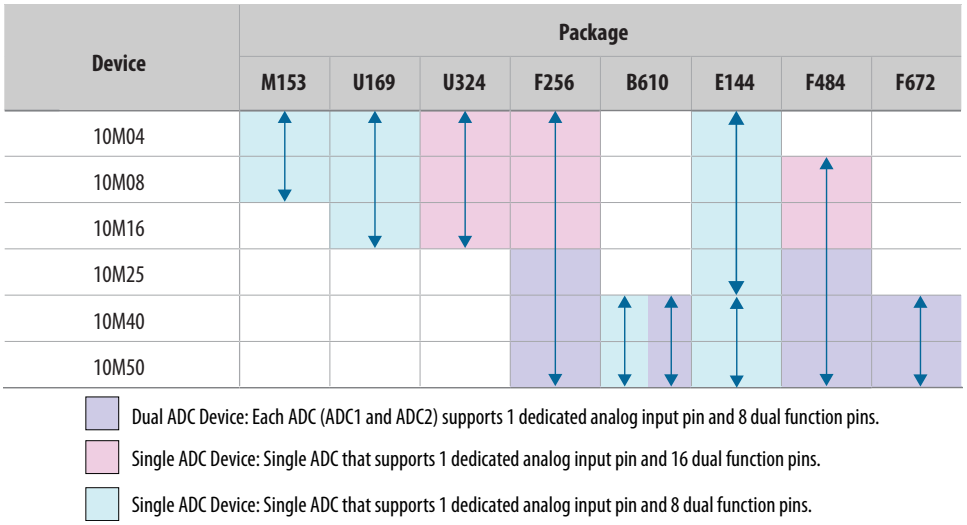


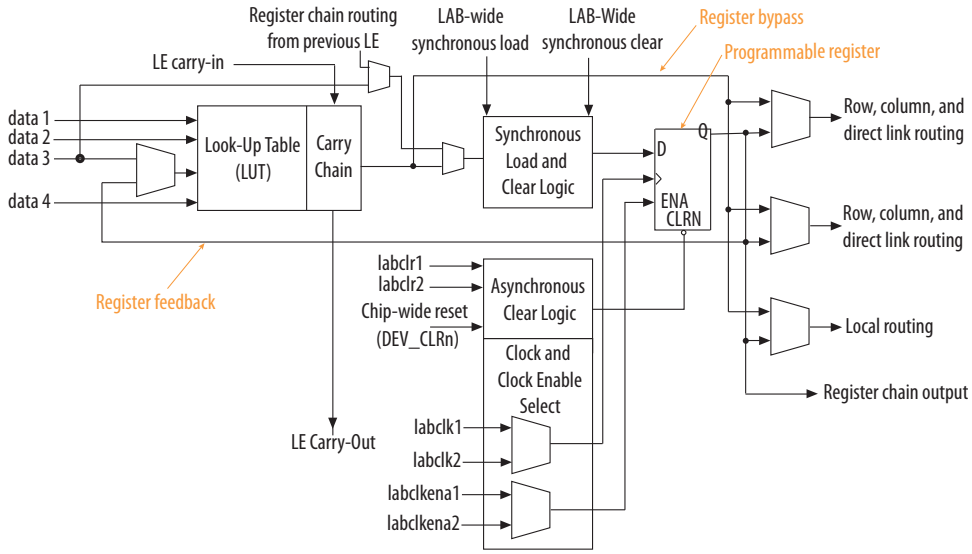
Table 7. Pin Migration Conditions for ADC Migration

Source	Target	Migratable Pins
Single ADC device	Single ADC device	You can migrate all ADC input pins
Dual ADC device	Dual ADC device	
Single ADC device	Dual ADC device	• One dedicated analog input pin. • Eight dual function pins from the ADC1 block of the source device to the ADC1 block of the target device.
Dual ADC device	Single ADC device	

Logic Elements and Logic Array Blocks

The LAB consists of 16 logic elements (LE) and a LAB-wide control block. An LE is the smallest unit of logic in the MAX 10 device architecture. Each LE has four inputs, a four-input look-up table (LUT), a register, and output logic. The four-input LUT is a function generator that can implement any function with four variables.

Figure 4. MAX 10 Device Family LEs



Analog-to-Digital Converter

MAX 10 devices feature up to two ADCs. You can use the ADCs to monitor many different signals, including on-chip temperature.

Table 8. ADC Features

Feature	Description
12-bit resolution	• Translates analog signal to digital data for information processing, computing, data transmission, and control systems • Provides a 12-bit digital representation of the observed analog signal
Up to 1 MSPS sampling rate	Monitors single-ended external inputs with a cumulative sampling rate of 25 kilosamples per second to 1 MSPS in normal mode
Up to 17 single-ended external inputs for single ADC devices	One dedicated analog and 16 dual function input pins
Up to 18 single-ended external inputs for dual ADC devices	• One dedicated analog and eight dual-function input pins in each ADC block • Simultaneous measurement capability for dual ADC devices
On-chip temperature sensor	Monitors external temperature data input with a sampling rate of up to 50 kilosamples per second

User Flash Memory

The user flash memory (UFM) block in MAX 10 devices stores non-volatile information.

UFM provides an ideal storage solution that you can access using Avalon Memory-Mapped (Avalon-MM) slave interface protocol.

Table 9. UFM Features

Features	Capacity
Endurance	Counts to at least 10,000 program/erase cycles
Data retention	• 20 years at 85 ºC • 10 years at 100 ºC
Operating frequency	Maximum 116 MHz for parallel interface and 7.25 MHz for serial interface
Data length	Stores data up to 32 bits length in parallel

Embedded Multipliers and Digital Signal Processing Support

MAX 10 devices support up to 144 embedded multiplier blocks. Each block supports one individual 18 × 18-bit multiplier or two individual 9 × 9-bit multipliers.

With the combination of on-chip resources and external interfaces in MAX 10 devices, you can build DSP systems with high performance, low system cost, and low power consumption.

You can use the MAX 10 device on its own or as a DSP device co-processor to improve price-to-performance ratios of DSP systems.

You can control the operation of the embedded multiplier blocks using the following options:

- Parameterize the relevant IP cores with the Quartus Prime parameter editor
- Infer the multipliers directly with VHDL or Verilog HDL

System design features provided for MAX 10 devices:

- DSP IP cores:
  - Common DSP processing functions such as finite impulse response (FIR), fast Fourier transform (FFT), and numerically controlled oscillator (NCO) functions
  - Suites of common video and image processing functions
- Complete reference designs for end-market applications
- DSP Builder for Intel FPGAs interface tool between the Quartus Prime software and the MathWorks Simulink and MATLAB design environments
- DSP development kits

Embedded Memory Blocks

The embedded memory structure consists of M9K memory blocks columns. Each M9K memory block of a MAX 10 device provides 9 Kb of on-chip memory capable of operating at up to 284 MHz.

You can configure the M9K memory blocks as RAM, FIFO buffers, or ROM.

The MAX 10 device memory blocks are optimized for applications such as high throughput packet processing, embedded processor program, and embedded data storage.

Table 10. M9K Operation Modes and Port Widths

Operation Modes	Port Widths
Single port	×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36
Simple dual port	×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36
True dual port	×1, ×2, ×4, ×8, ×9, ×16, and ×18

Clocking and PLL

MAX 10 devices offer the following resources: global clock (GCLK) networks and phase-locked loops (PLLs) with a 116-MHz built-in oscillator.

MAX 10 devices support up to 20 global clock (GCLK) networks with operating frequency up to 450 MHz. The GCLK networks have high drive strength and low skew.

The PLLs provide robust clock management and synthesis for device clock management, external system clock management, and I/O interface clocking. The high precision and low jitter PLLs offers the following features:

- Reduction in the number of oscillators required on the board
- Reduction in the device clock pins through multiple clock frequency synthesis from a single reference clock source
- Frequency synthesis
- On-chip clock de-skew
- Jitter attenuation
- Dynamic phase-shift
- Zero delay buffer
- Counter reconfiguration
- Bandwidth reconfiguration
- Programmable output duty cycle
- PLL cascading
- Reference clock switchover
- Driving of the ADC block

FPGA General Purpose I/O

The MAX 10 I/O buffers support a range of programmable features.

These features increase the flexibility of I/O utilization and provide an alternative to reduce the usage of external discrete components such as a pull-up resistor and a PCI clamp diode.

MultiVolt I/O Interface

The MultiVolt I/O interface feature of MAX 10 devices maximizes pin utilization per I/O bank. You can connect input signals of different voltages to the same I/O bank.

Examples:

- I/O banks with 3.3 V V_{CCIO}—you can connect 3.3 V, 3.0 V, and 2.5 V input signals
- I/O banks with 3.0 V V_{CCIO}—you can connect 3.3 V, 3.0 V, and 2.5 V input signals

Table 11. MultiVolt I/O Support in MAX 10 Devices

I/O Bank V_{CCIO} (V)	Supported Input Signal
3.3	3.3 V, 3.0 V, 2.5 V LVCMOS/LVTTL
3.0	3.3 V, 3.0 V, 3.0 V PCI, 2.5 V LVCMOS/LVTTL
2.5	3.3 V, 3.0 V, 2.5 V LVCMOS/LVTTL, SSTL-2, 2.5 V LVDS
1.8	1.8 V LVCMOS, SSTL-18, HSTL-18, 1.8 V LVDS, 1.5 V LVCMOS
1.5	1.8 V LVCMOS, 1.5 V LVCMOS, SSTL-15, HSTL-15
1.35	SSTL-135
1.2	1.2 V LVCMOS, HSTL-12, HSUL-12
1.0	1.0 V LVCMOS

For the detailed requirements, refer to the *MAX 10 General-Purpose I/O User Guide*.

Related Information

MAX 10 General Purpose I/O User Guide

LVDS Tunneling Protocol and Interface

The MAX 10 devices support LVDS Tunneling Protocol and Interface (LTPI) soft IP in the Quartus Prime software, specifically targeting data center applications.

The Datacenter - Secure Control Module (DC-SCM) 2.0 specification introduces LTPI and offers higher bandwidth and better scalability compared to the serial general purpose I/O (SGPIO) interface. The LTPI interface is designed to tunnel various low-speed signals (such as GPIO, I2C, UART, data, and OEM) between the Host Processor Module (HPM) and Secure Control Module (SCM). The LTPI protocol operates over the low voltage differential signaling (LVDS) electrical interfaces.

Figure 5. High-level Block Diagram of LTPI

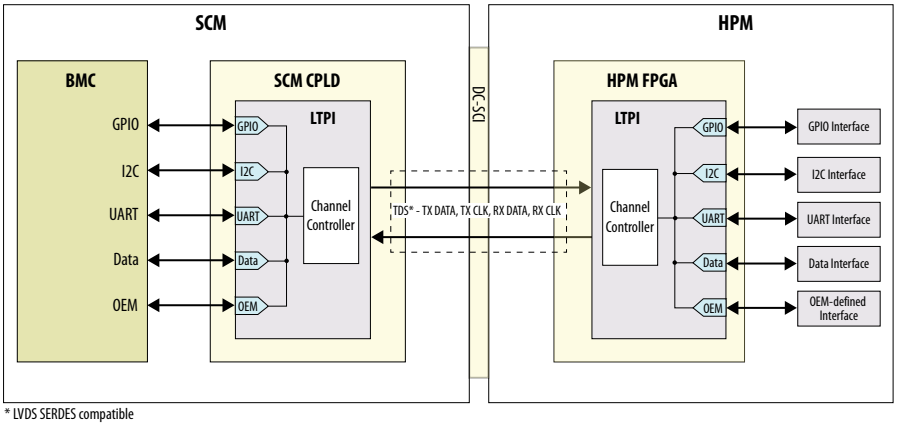


Table 12. Supported LTPI Features

Feature	Description
Specification	Compliant with OCP DC-SCM 2.0 LTPI 1.0.
Speed Grade	Supports all speed grade configuration for the MAX 10 devices.
Channel	• Supports up to five channels of aggregation and disaggregation. • Supports GPIO, I2C, UART, OEM, and data channel.
Link Training	Supports link training for reliable link operation.
Speed	Supports up to 400 Mbps data rate for all speed grade configuration in the MAX 10 devices.

Note: The LTPI IP is currently under development.

External Memory Interface

Dual-supply MAX 10 devices feature external memory interfaces solution that uses the I/O elements on the right side of the devices together with the UniPHY IP.

With this solution, you can create external memory interfaces to 16-bit SDRAM components with error correction coding (ECC).

Note: The external memory interface feature is available only for dual-supply MAX 10 devices.

Table 13. External Memory Interface Performance

External Memory Interface[6]	I/O Standard	Maximum Width	Maximum Frequency (MHz)
DDR3 SDRAM	SSTL-15	16 bit + 8 bit ECC	303
DDR3L SDRAM	SSTL-135	16 bit + 8 bit ECC	303
DDR2 SDRAM	SSTL-18	16 bit + 8 bit ECC	200
LPDDR2 SDRAM	HSUL-12	16 bit without ECC	200[7]

(6) The device hardware supports SRAM. Use your own design to interface with SRAM devices.

Related Information

- MAX 10 External Memory Interface User Guide
- External Memory Interface (EMIF) Spec Estimator
  Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in Altera® FPGAs.

Configuration

Table 14. Configuration Features

Feature	Description
Dual configuration	• Stores two configuration images in the configuration flash memory (CFM) • Selects the first configuration image to load using the CONFIG_SEL pin
Design security	• Supports 128-bit key with non-volatile key programming • Limits access of the JTAG instruction during power-up in the JTAG secure mode • Unique device ID for each MAX 10 device
SEU Mitigation	• Auto-detects cyclic redundancy check (CRC) errors during configuration • Provides optional CRC error detection and identification in user mode
Dual-purpose configuration pin	• Functions as configuration pins prior to user mode • Provides options to be used as configuration pin or user I/O pin in user mode
Configuration data compression	• Decompresses the compressed configuration bitstream data in real-time during configuration • Reduces the size of configuration image stored in the CFM
Instant-on	Provides the fastest power-up mode for MAX 10 devices.

Table 15. Configuration Schemes for MAX 10 Devices

Configuration Scheme	Compression	Encryption	Dual Image Configuration	Data Width
Internal Configuration	Yes	Yes	Yes	—
JTAG	—	—	—	1

Remote System Update

The MAX 10 devices support remote system updates where you can deploy a new image to a MAX 10 FPGA in the field over a network.

The remote update process stores the new image on the flash memory, protects the system during reconfiguration, and reconfigures the FPGA to load the new image:

- Allows flash image update through the On-Chip Flash IP during user mode
- Stores two images on the flash memory:
  - CFM0—the factory golden image
  - CFM1 and CFM2—the application image
- Falls back to the factory golden image if the reconfiguration fails

(7) To achieve the specified performance, constrain the memory device I/O and core power supply variation to within ±3%. By default, the frequency is 167 MHz.

Related Information

Remote Update Intel FPGA IP User Guide

Hitless Update

The hitless update feature avoids glitches on the I/Os during reconfiguration to keep the operation of downstream devices unaffected.

The MAX 10 devices support the following hitless update modes:

- JTAG mode—requires access to external JTAG pins
- Non-JTAG mode—does not require access to external JTAG pins and accessible through the internal JTAG interface and FPGA fabric (e.g., I2C soft IP)

The hitless update feature freezes the I/Os during reconfiguration and reconfigures the new image with the pre-defined I/O states. You can perform the hitless update through a series of instructions using JTAG (internal or external) and the Dual Configuration Intel FPGA IP for non-JTAG mode respectively. For more information refer to *AN 904: MAX 10 Hitless Update Implementation Guidelines* and *AN 963: MAX 10 Hitless Update Implementation Guidelines Using Internal JTAG Interface*.

Related Information

- AN 904: MAX 10 Hitless Update Implementation Guidelines
- AN 963: MAX 10 Hitless Update Implementation Guidelines Using Internal JTAG Interface

Power Management

Table 16. Power Options

Power Options	Advantage
Single-supply device	Saves board space and costs.
Dual-supply device	• Consumes less power • Offers higher performance
Power management controller scheme	• Reduces dynamic power consumption when certain applications are in standby mode • Provides a fast wake-up time of less than 1 ms.

Revision History for the MAX 10 FPGA Device Overview

Document Version	Changes
2025.03.10	• Added the B610 package information to the following tables: — Table: *Package Plan for MAX 10 Single Power Supply Devices* — Table: *Package Plan for MAX 10 Dual Power Supply Devices* • Added the B610 package to the following figures: — Figure: *Migration Capability Across MAX 10 Devices* — Figure: *ADC Vertical Migration Across MAX 10 Devices* • Added new topics under the *FPGA General Purpose I/O* section: — *MultiVolt I/O Interface* — *LVDS Tunneling Protocol and Interface* • Added new topics under the *Configuration* section: — *Remote System Update* — *Hitless Update*
2022.06.14	Updated the LVDS receiver and transmitter speeds from 830 Mbps and 800 Mbps, respectively, to 720 Mbps.
2021.11.01	• Updated the *Sample Ordering Code and Available Options for MAX 10 Devices* diagram. — Added SL and DD feature options, Y package type, and 180 package code. — Removed –I6 speed grade from contact information. All OPNs for –I6 speed grade are available in the Quartus Prime Standard Edition software version 21.1 onwards. • Added V81 and Y180 packages in the *Package Plan for MAX 10 Single Power Supply Devices* table. • Added Y180 package in the *Migration Capability Across MAX 10 Devices* diagram.

Date	Version	Changes
December 2017	2017.12.15	• Added the U324 package for the MAX 10 single power supply devices. • Updated the 10M02 GPIO and LVDS count in the *Maximum Resource Counts for MAX 10 Devices* table. • Updated the I/O vertical migration figure.
February 2017	2017.02.21	• Rebranded as Intel.
December 2016	2016.12.20	• Updated EMIF information in the *Summary of Features for MAX 10 Devices* table. EMIF is only supported in selected MAX 10 device density and package combinations, and for 600 Mbps performance, –6 device speed grade is required. • Updated the device ordering information to include P for leaded package.
May 2016	2016.05.02	• Removed all preliminary marks. • Update the ADC sampling rate description. The ADC feature monitors single-ended external inputs with a cumulative sampling rate of 25 kilosamples per second to 1 MSPS in normal mode.
November 2015	2015.11.02	• Removed SF feature from the device ordering information figure. • Changed instances of *Quartus II* to *Quartus Prime*.
May 2015	2015.05.04	• Added clearer descriptions for the feature options listed in the device ordering information figure. • Updated the maximum dedicated LVDS transmitter count of 10M02 device from 10 to 9. • Removed the F672 package of the MAX 10 10M25 device : — Updated the devices I/O resources per package. — Updated the I/O vertical migration support. — Updated the ADC vertical migration support.

continued...

Date	Version	Changes
		• Updated the maximum resources for 10M25 device: — Maximum GPIO from 380 to 360. — Maximum dedicated LVDS transmitter from 26 to 24. — Maximum emulated LVDS transmitter from 181 to 171. — Maximum dedicated LVDS receiver from 181 to 171. • Added ADC information for the E144 package of the 10M04 device. • Updated the ADC vertical migration diagram to clarify that there are single ADC devices with eight and 16 dual function pins. • Removed the note about contacting Altera for DDR3, DDR3L, DDR2, and LPDDR2 external memory interface support. The Quartus Prime software supports these external memory interfaces from version 15.0.
December 2014	2014.12.15	• Changed terms: — "dual image" to "dual configuration image" — "dual-image configuration" to dual configuration" • Added memory initialization feature for Flash and Analog devices. • Added maximum data retention capacity of up to 20 years for UFM feature. • Added maximum operating frequency of 7.25 MHz for serial interface for UFM feature.
September 2014	2014.09.22	Initial release.