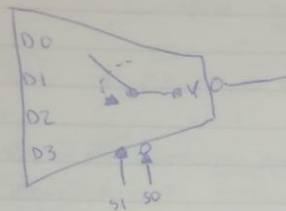


PINS:

D0 = 1  
D1 = 2  
D2 = 3  
D3 = 4  
S1 = 7  
S0 = 8

$$\cancel{51\bar{S}0D0} + \cancel{51\bar{S}0D1} + \cancel{51\bar{S}0D2} + \cancel{51\bar{S}0D3} \xrightarrow{29} \xrightarrow{32} \xrightarrow{42}$$

Lab 3 Pre-lab



High: D0, D1, D2, D3, S1

Low: S0, Y

logic table

S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

logic equation:

$$\bar{S}1\bar{S}0D0 + \bar{S}1S0D1 + S1\bar{S}0D2 + S1S0D3 = Y$$

Truth Table

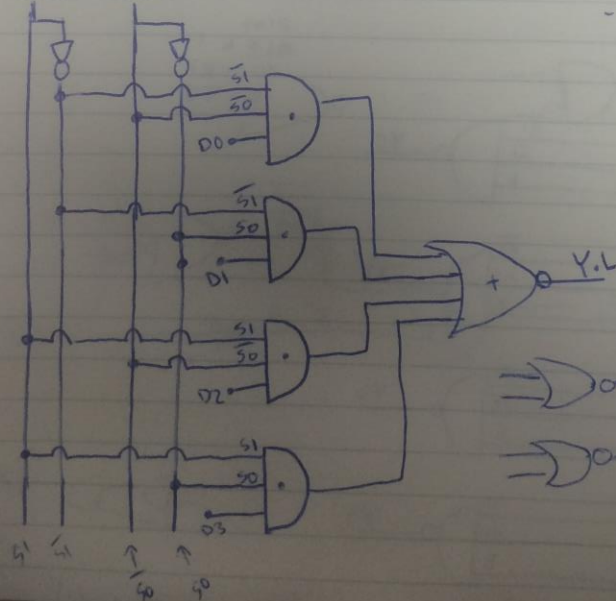
D0	D1	D2	D3	S1	S0	Y
0	-	-	-	0	0	0
1	-	-	-	0	1	1
-	0	-	-	1	0	0
-	1	-	-	1	1	1
-	-	0	-	-	0	0
-	-	1	-	-	1	1
-	-	-	0	-	0	0
-	-	-	1	-	1	1

Voltage Table

D0	D1	D2	D3	S1	S0	Y
L	-	-	-	L	H	H
H	-	-	-	L	H	L
-	L	-	-	L	L	H
-	H	-	-	L	L	L
-	-	L	-	H	H	H
-	-	H	-	H	H	L
-	-	-	L	H	L	H
-	-	-	H	H	L	L

~~51S0D0~~

S1.H S0.L



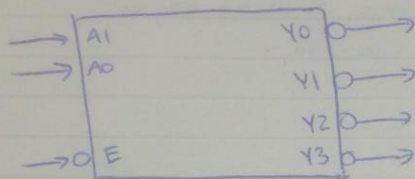
D0	D1	D2	D3	S1	S0	Y
H	-	-	-	L	H	L
-	H	-	-	L	L	L
-	-	H	-	H	H	L
-	-	-	H	H	L	L

Part 2

2:4 Decoder

$A_1, A_0$  High

$Y_0, Y_1, Y_2, Y_3, E$  Low



logic equation:  $\bar{A}_1 \bar{A}_0 \bar{E} = Y_0$   
 $\bar{A}_1 A_0 \bar{E} = Y_1$   
 $A_1 \bar{A}_0 \bar{E} = Y_2$   
 $A_1 A_0 \bar{E} = Y_3$

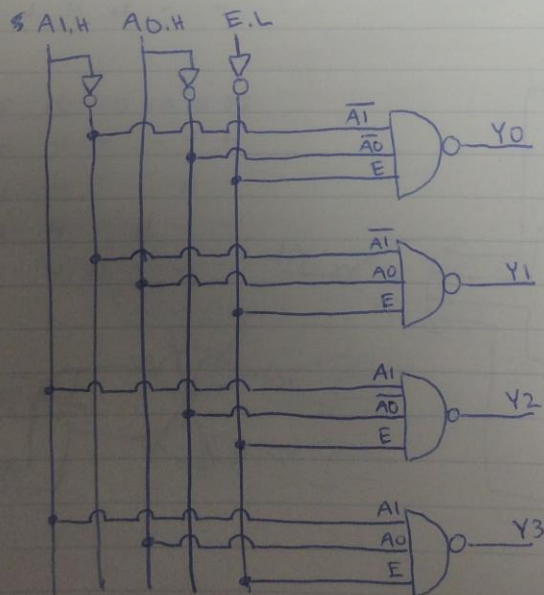
Logic Table

$A_1$	$A_0$	$E$	$Y_0$	$Y_1$	$Y_2$	$Y_3$
-	-	0	0	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

Voltage Table

$A_1$	$A_0$	$E$	$Y_0$	$Y_1$	$Y_2$	$Y_3$
-	-	H	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
H	L	L	H	H	L	H
H	H	L	H	H	H	L

Circuit Diagram:



$\bar{A}_1 \bar{A}_0 \bar{E}$   $\bar{A}_1 A_0 \bar{E}$   $A_1 \bar{A}_0 \bar{E}$   $A_1 A_0 \bar{E}$

PINS  
 $A_1 = 1$   
 $A_0 = 2$   
 $E = 3$

