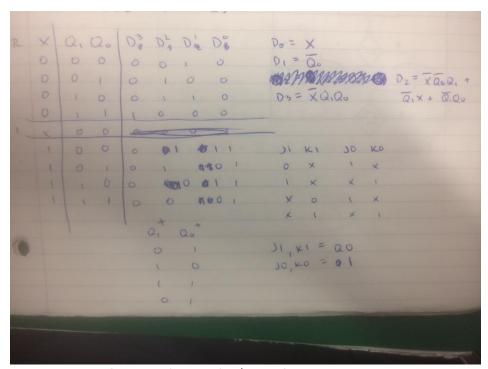
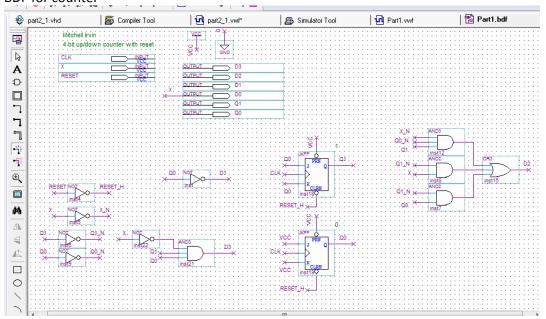
Lab 7 Summary Irvin, Mitchell Section 7441 3/18/16

PART 1

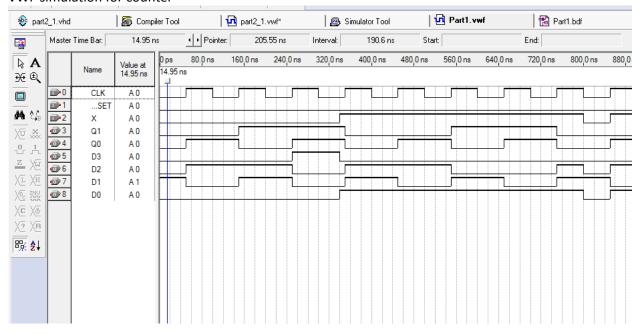


Next state table for part 1 (counter) w/ simplified equations

BDF for counter

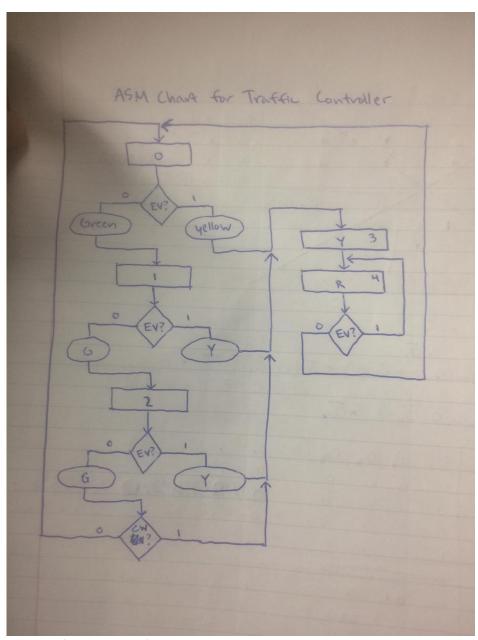


VWF simulation for counter



G=Q2Q,Q5EV+Q2Q,Q6EV+Q2Q,Q6EV
Y = 0,0,0,EV + 0,0,0,EV + 0,0,0,EV + 0,0,0,EV
4 - 050'00'EA + O50'00'EA + O5
R = Ozā, āc MWWWITHINAD araide even
Next State Table + Graveo
LOW TRUE DZ DI DO
LW EV Q2 Q, Q0 Q2 Q1 Q1 G1 G1 GYR
x 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
X 1 0 0 40 0 0 0 0 000
× 0 0 10 01 0 0 0 000
× 1 0 0 1 0 D D OO
0000000000
0 1 0 0 0 0 0 0 00
100000000000000000000000000000000000000
X X 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
X 80 10 00 000
x 1 1 0 0000 0 0 1000
X X II O II X X X X X X X
X X I I O X X X X X X
X X I I I I X X X X X X X
$Q_2^{\dagger} = \overline{Q_2}Q_1Q_0 + \overline{Q_2}Q_1Q_0 EV$
$Q_2 = Q_2 Q_1 Q_0 + Q_2 Q_1 Q_0 EV$ $Q_1^* = \overline{Q_2} \overline{Q_1} \overline{Q_0} EV + \overline{Q_2} \overline{Q_1} \overline{Q_1} \overline{Q_1} \overline{Q_1} \overline{Q_1} EV + \overline{Q_2} \overline{Q_1} \overline{Q_1} \overline{Q_1} \overline{Q_1} \overline{Q_1} EV + \overline{Q_2} \overline{Q_1} \overline{Q_1} \overline{Q_1} EV + \overline{Q_2} \overline{Q_1} \overline{Q_1} \overline{Q_1} \overline{Q_1} EV + \overline{Q_2} \overline{Q_1} \overline{Q_1} \overline{Q_1} \overline{Q_1} \overline{Q_1} \overline{Q_1} \overline{Q_1} + \overline{Q_1} $
$Q_{*}^{+} = \overline{Q_{2}}\overline{Q_{1}}\overline{Q_{0}}\overline{EV} + \overline{Q_{2}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}\overline{Q_{1}}$
00 (1 EV + 0 EV + 0 EV) + 0.0.0. (EV CTV + EV CW + EV CW)
$Q_{+}^{+} = \overline{Q_{2}}\overline{Q_{1}}(\overline{Q_{0}}EV + Q_{0}\overline{EV} + Q_{0}\overline{EV}) + \overline{Q_{2}}\overline{Q_{1}}\overline{Q_{0}}(EV\overline{CW} + EVCW)$ $CW(\Delta + \overline{A})$ $Q_{+}^{+} = \overline{Q_{2}}\overline{Q_{1}}(EV + Q_{0}) + \overline{Q_{2}}\overline{Q_{1}}\overline{Q_{0}}(EV + CW)$ $(EV + CW)$ $(EV + CW)$
(EV + CW) (EV + CW) + Q2Q, Q0 (EV + CW)
Qo+ = QzQ,Qo + QzQ,QoEV + QzQ,Qo(CW+EV)

next state table and simplified equations

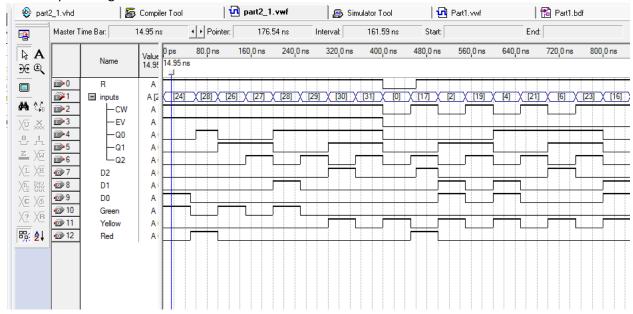


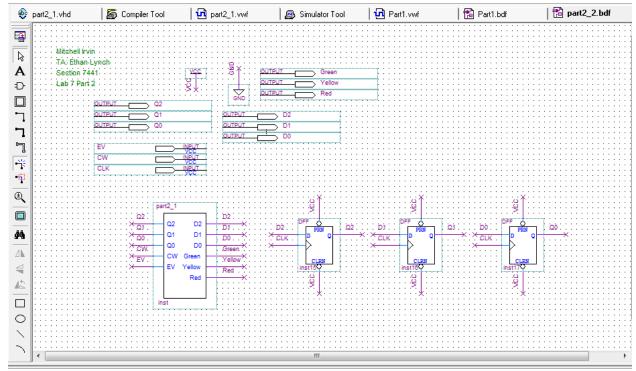
the ASM for the logic of part 2

VHD for part 2 logic

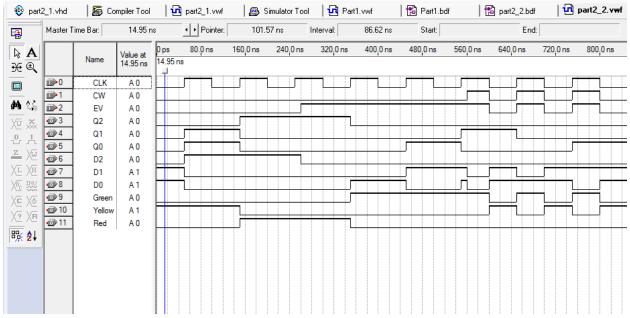
```
part2_1.vhd*
                   Compiler Tool
                                       part2_1.vwf*
                                                           Simulator Tool
                                                                               Part1.vwf
                                                                                                  Part1.bdf
           ■entity part2_1 is port (
Q2, Q1, Q0, CW, EV, R: in bit;
4
        5
ďΑ
        6
                 D2, D1, D0: out bit;
                 Green, Yellow, Red: out bit
۸.,
        8
                 );
            end part2_1;
        9
{}
       10
+
       11
          architecture logic OF part2_1 IS
       12
賃
       13
           ■ D2 <= (((not Q2) and Q1 and Q0) or
1
       14
      15
            (Q2 and (not Q1) and (not Q0) and (not EV))) and R;
%
      16
%
       17
           ■D1 <= (((not Q2) and (not Q1) and ((not EV) or Q0)) or
           ((not Q2) and Q1 and (not Q0) and ((not EV) or (not CW)))) and R;
      18
×
       19
0
           \blacksquare D0 <= (((not Q2) and (not Q1) and (not Q0)) or
      20
       21
            ((not Q2) and (not Q1) and Q0 and (not EV)) or
Z
       22
             (((not Q2) and Q1 and (not Q0)) and ((not CW) or (not EV)))) and R;
€2
       23
       24
           ■Green <= (((not Q2) and (not Q1) and (not Q0) and EV) or
267
268
            ((not Q2) and (not Q1) and Q0 and EV) or
       25
       26
            ((not Q2) and Q1 and (not Q0) and EV));
ab/
       27
           ■ Yellow <= (((not Q2) and (not Q1) and (not Q0) and (not EV)) or
       29
            ((not Q2) and (not Q1) and Q0 and (not EV)) or
....
             ((not Q2) and Q1 and (not Q0) and (not EV)) or
       30
=
       31
            ((not Q2) and Q1 and Q0));
       32
2
       33
             Red <= (Q2 and (not Q1) and (not Q0));
             III
```

VWF for part 2 logic





Part 2 implementation bdf



Part 2 implementation VWF

Memory table w/ addresses and Data bits

						36		
				Δ	Λ	A	HEX D3 D4 D3 D2 D, D0 DATA	
							PZ D, Po GYR 0	
							19800110000	
							112901010014	
							1 8A 0 0 0 1 0 0 0 4	
							186 10001022	
		1					1000000101	
						1	(80	
			1	1		0	186	
	0	1	1	(1	1	1 0 5	
		1	0	0	0	0	1000110000	
	0	1	0	0	0	1	1 1 0 1 0 1 0 0 1 4	
			0	6	1	0	13201110011	
	0	1	0	0	-	1	193100010 22	_
	0	1	0	1	0	0	13400000101	
	0	1	0	1	0	1	1 45	
		1					(4 6	
	0	1	6			1	17	
	0			0		0	08011010 IA	
	0	0	1	0	0	1	09011010 IA	
ACCUSED NO.		0	1	0	1	0	OAOIIOIOIA	
	0						08100010 22	
229000			01				0 (1 0 0 0 0 1 21	
						1		
1120000	0			1			OE	
			0				O F	
		0		0	0	0	00011010 1A	
			0	0	0		01010 1A	
		0	0	0	1			
0		_	0	1			3100010 A	
			0	*			14/10000	_
0				1			5	
0			0	1	1	10	7	
						. 0		