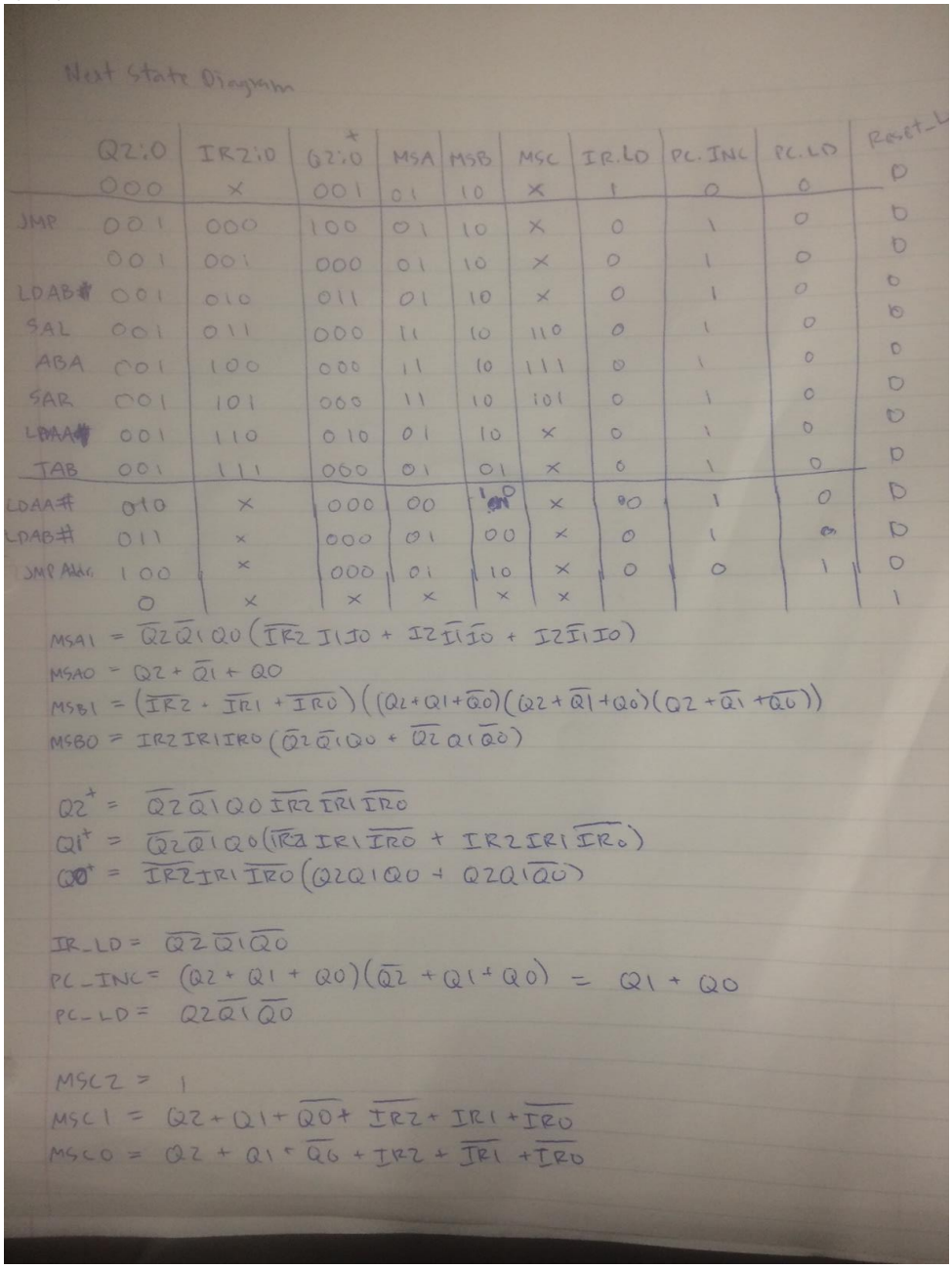
Lab 9 Summary
Irvin, Mitchell
Section 7441
4/15/16



Next State Diagram

	Q2:0	IR2:0	Q2:0+	MSA	MSB	MSC	IR.LD	PC.INC	PC.LD	Reset_L
	000	x	001	01	10	x	1	0	0	0
JMP	001	000	100	01	10	x	0	1	0	0
	001	001	000	01	10	x	0	1	0	0
LDAB#	001	010	011	01	10	x	0	1	0	0
SAL	001	011	000	11	10	110	0	1	0	0
ABA	001	100	000	11	10	111	0	1	0	0
SAR	001	101	000	11	10	101	0	1	0	0
LDAA#	001	110	010	01	10	x	0	1	0	0
TAB	001	111	000	01	01	x	0	1	0	0
LDAA#	010	x	000	00	10	x	0	1	0	0
LDAB#	011	x	000	01	00	x	0	1	0	0
JMP ADD	100	x	000	01	10	x	0	0	1	0
	0	x	x	x	x	x				1

$MSA1 = \overline{Q2}\,\overline{Q1}\,Q0(\overline{IR2}\,I1\,I0 + I2\,\overline{I1}\,\overline{I0} + I2\,\overline{I1}\,I0)$

$MSA0 = Q2 + \overline{Q1} + Q0$

$MSB1 = (\overline{IR2} + \overline{IR1} + \overline{IR0})((Q2+Q1+\overline{Q0})(Q2+\overline{Q1}+Q0)(Q2+\overline{Q1}+\overline{Q0}))$

$MSB0 = IR2\,IR1\,IR0(\overline{Q2}\,\overline{Q1}\,Q0 + \overline{Q2}\,Q1\,\overline{Q0})$

$Q2^{+} = \overline{Q2}\,\overline{Q1}\,Q0\,\overline{IR2}\,\overline{IR1}\,\overline{IR0}$

$Q1^{+} = \overline{Q2}\,\overline{Q1}\,Q0(\overline{IR2}\,IR1\,\overline{IR0} + IR2\,IR1\,\overline{IR0})$

$Q0^{+} = \overline{IR2}\,IR1\,\overline{IR0}(Q2\,Q1\,Q0 + Q2\,Q1\,\overline{Q0})$

$IR\_LD = \overline{Q2}\,\overline{Q1}\,\overline{Q0}$

$PC\_INC = (Q2 + Q1 + Q0)(\overline{Q2} + Q1 + Q0) = Q1 + Q0$

$PC\_LD = Q2\,\overline{Q1}\,\overline{Q0}$

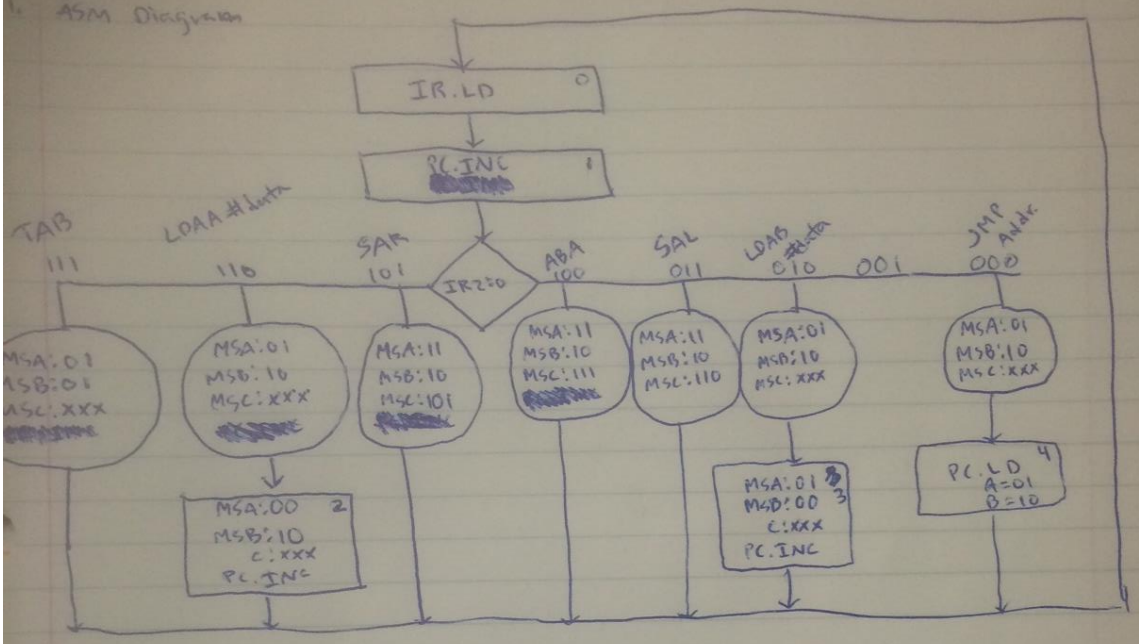
$MSC2 = 1$

$MSC1 = Q2 + Q1 + \overline{Q0} + \overline{IR2} + IR1 + \overline{IR0}$

$MSC0 = Q2 + Q1 + \overline{Q0} + IR2 + \overline{IR1} + \overline{IR0}$

Lab 9

1. ASM Diagram



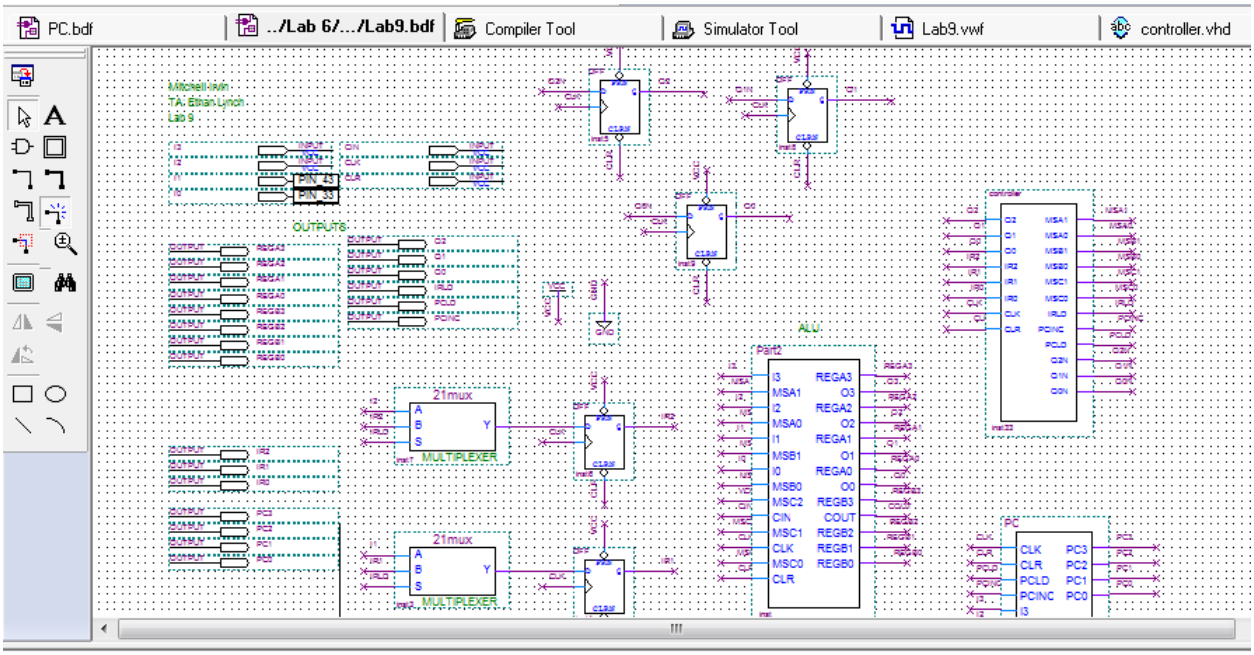
Cy	State	Addr.	Data	PC	IR	A	B
1	0	0	2	0	X	X	X
2	01	0	2	0	2	X	X
3	1	1	5	1	2	X	X
4	0	2	6	2	2	X	5
5	1	2	6	2	6	X	5
6	22	3	4	3	6	X	5
7	0	4	5	4	6	4	5
8	1	4	5	4	5	4	5
9	0	5	4	5	5	2	5
10	1	5	4	5	4	2	5
11	0	6	7	6	4	7	5
12	1	6	7	6	7	7	5
13	0	7	3	7	7	7	7
14	1	7	3	7	3	7	7
15	0	8	0	8	3	E	7
16	1	8	0	8	0	E	7
17	4	9	2	9	0	E	7
18	0	2	6	2	0	E	7

Addr	Data	
200	2	(1)
1	5	
2	6	(2)
3	4	
4	5	(3)
5	4	(4)
6	7	(5)
7	3	(6)
8	0	(7)
9	2	

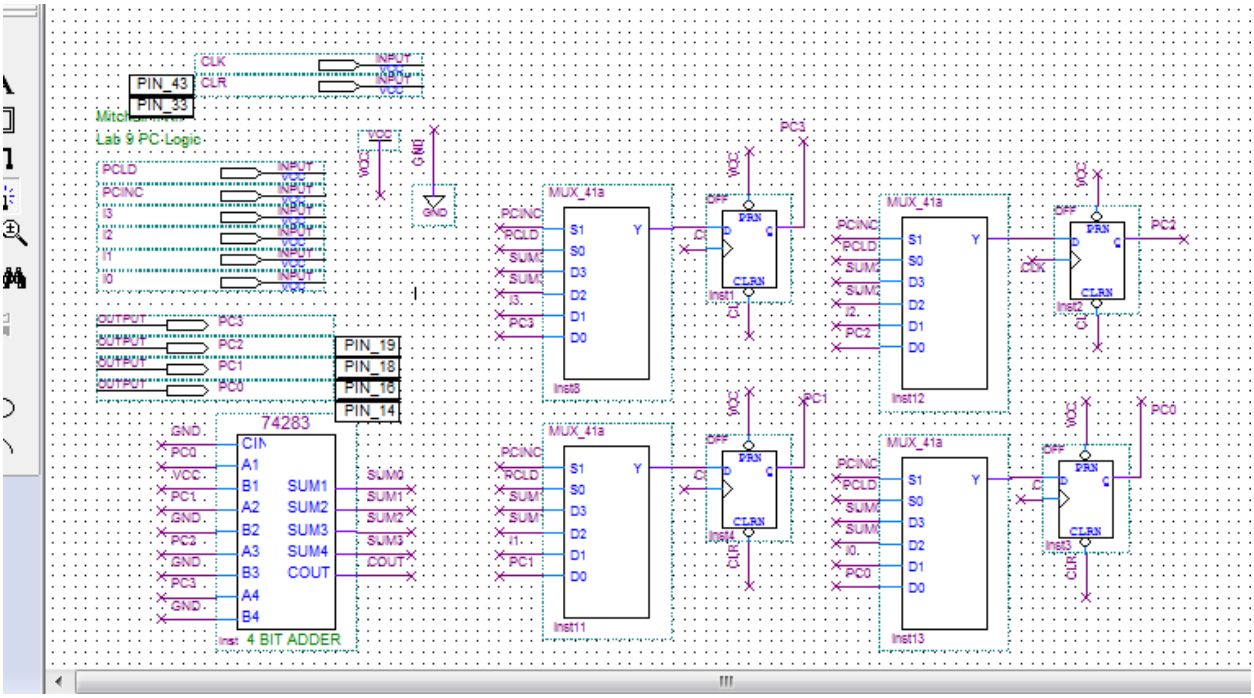
LDB #5 (1)
LDA #4 (2)
SAR (3)
ABA (4)
TAB (5)
SAL (6)
JUMP 2 (7)

BDF files

Lab 9 bdf



PC bdf



```
library ieee;
use ieee.std_logic_1164.all;

entity controller is port (
	Q2, Q1, Q0, IR2, IR1, IR0, CLK, CLR: in bit;
	MSA1, MSA0, MSB1, MSB0, MSC1, MSC0, IRLD, PCINC, PCLD: out bit;
	Q2N, Q1N, Q0N: out bit
	);
end controller;

architecture logic OF controller IS
begin


MSA1 <= ((not Q2) and (not Q1) and Q0) and (
((not IR2) and IR1 and IR0) or
(IR2 and (not IR1) and (not IR0)) or
(IR2 and (not IR1) and IR0) );

MSA0 <= (Q2 or (not Q1) or Q0);

MSB1 <= (Q2 or Q1 or (not Q0) or (not IR2) or (not IR1) or (not IR0)) and
(Q2 or (not Q1) or (not Q0));

MSB0 <= ( (IR2 and IR1 and IR0) and
((not Q2) and (not Q1) and Q0) );

MSC1 <= (Q2 or Q1 or (not Q0) or (not IR2) or IR1 or (not IR0));

MSC0 <= (Q2 or Q1 or (not Q0) or (not IR1) or IR2 or (not IR0));

IRLD <= ((not Q2) and (not Q1) and (not Q0));

PCINC <= (Q1 or Q0);

PCLD <= (Q2 and (not Q1) and (not Q0));

Q2N <= ((not Q2) and (not Q1) and Q0 and (not IR2) and (not IR1) and (not IR0));

Q1N <= ((not Q2) and (not Q1) and Q0) and (
((not IR2) and IR1 and (not IR0)) or
(IR2 and IR1 and (not IR0)) );

Q0N <= ((not Q2) and (not Q1) and (not Q0)) or
(((not Q2) and (not Q1) and Q0) and
((not IR2) and IR1 and (not IR0)));

end logic;
```

VWF Simulation of the correct instructions