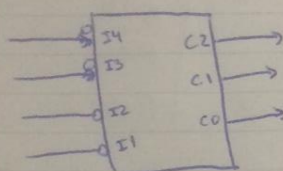


# Lab 4

Mitchell Irvin  
 EEL3701C  
 Section: 7441  
 TA: Ethan Lynch

Part 1

1.



Voltage +  
 Truth Table

I4	I3	I2	I1	C2	C1	C0
1 <sub>H</sub>	x	x	x	1 <sub>H</sub>	0 <sub>L</sub>	0 <sub>L</sub>
0 <sub>H</sub>	1 <sub>H</sub>	x	x	0 <sub>L</sub>	1 <sub>H</sub>	1 <sub>H</sub>
0 <sub>H</sub>	0 <sub>H</sub>	1 <sub>H</sub>	x	0 <sub>L</sub>	1 <sub>H</sub>	0 <sub>L</sub>
0 <sub>H</sub>	0 <sub>H</sub>	0 <sub>H</sub>	1 <sub>H</sub>	0 <sub>L</sub>	0 <sub>L</sub>	1 <sub>H</sub>
0 <sub>H</sub>	0 <sub>H</sub>	0 <sub>H</sub>	0 <sub>H</sub>	0 <sub>L</sub>	0 <sub>L</sub>	0 <sub>L</sub>

~~Wavy line~~

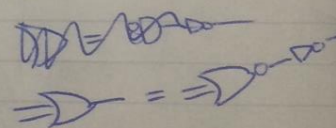
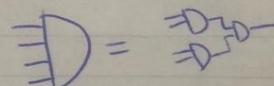
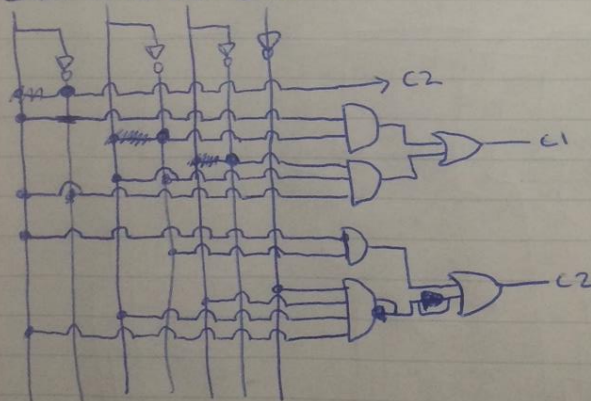
~~128~~

$$C2 = I4 +$$

$$C1 = \overline{I4} I3 + I2 \overline{I3} I4$$

$$C0 = \overline{I4} I3 + \overline{I1} I2 \overline{I3} I4$$

I4.L I3.L I2.L I1.L



PINS

$$C0 = 11$$

$$C1 = 12$$

$$C2 = 14$$

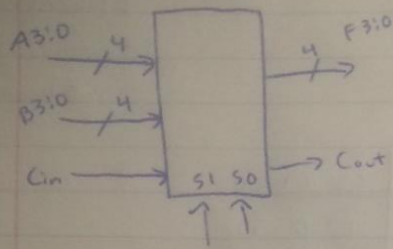
$$I1 = 18$$

$$I2 = 19$$

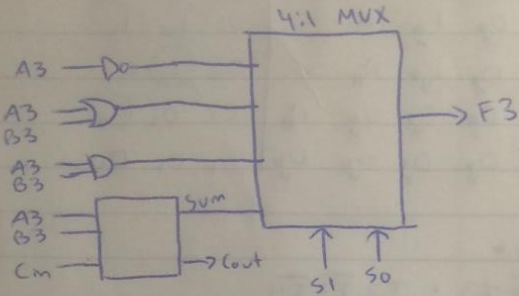
$$I3 = 20$$

$$I4 = 21$$

# ALU

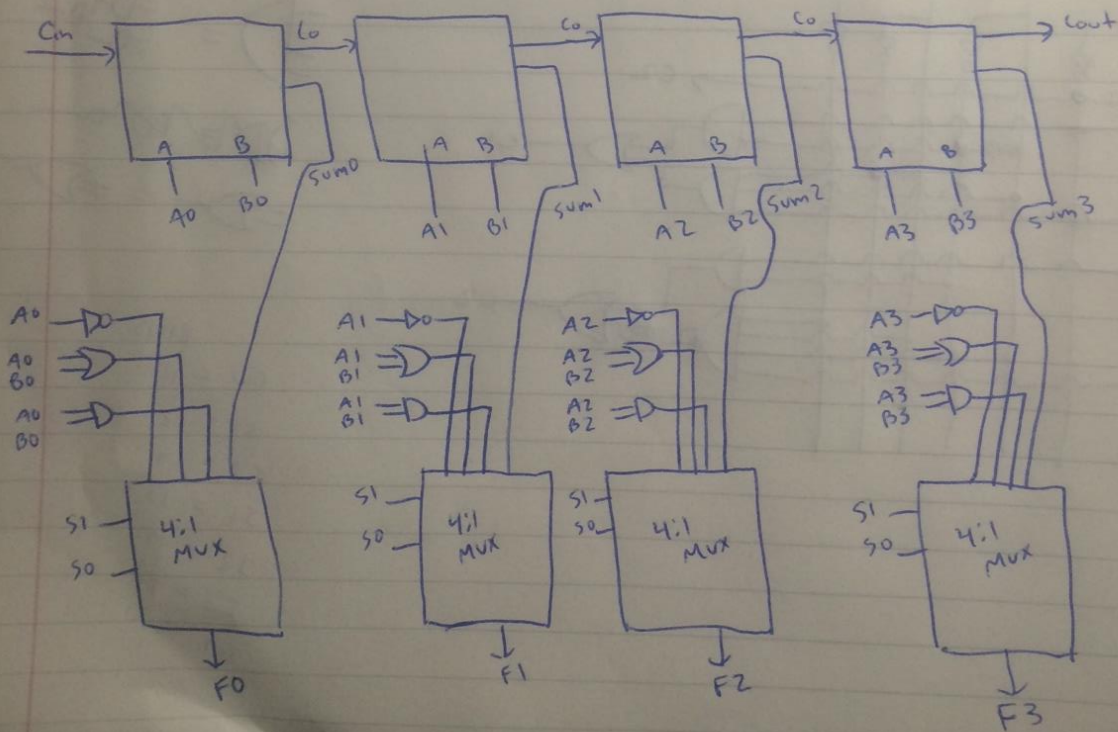


S1	S0	F
0	0	$\bar{A}$
0	1	$A \vee B$
1	0	$A \wedge B$
1	1	$A \text{ sum } B$

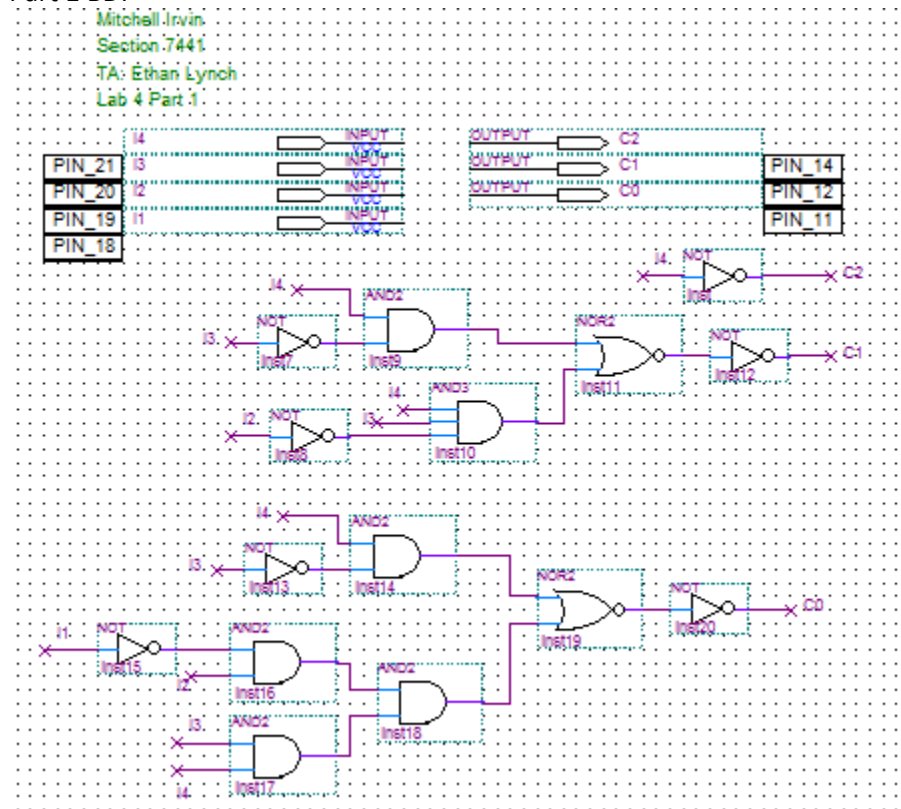


Repeat for  $A2:0$ ,  $B2:0$ , and  $F2:0$

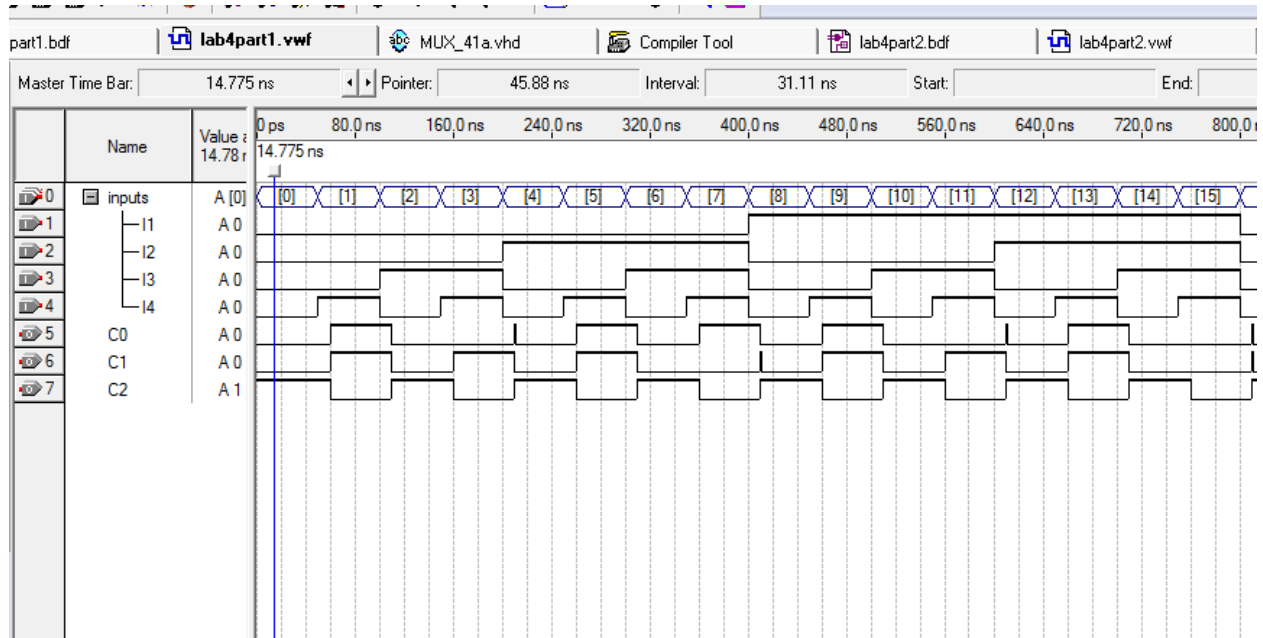
for sums:



Part 1 BDF



## Part 1 VWF



Mitchell Irvin  
Section 7441  
TA: Ethan Lynch  
Lab 4 Part 2

The image shows a logic simulator interface with a grid background. On the left, there are input and output ports. The inputs are labeled A3, A2, A1, A0, B3, B2, B1, B0, Cin, S1, and S0. The outputs are labeled F3, F2, F1, F0, and Cout. In the center, there is a 74283 4-bit adder block (inst) with inputs A0-A3, B0-B3, and Cin, and outputs SUM1, SUM2, SUM3, SUM4, and COUT. To the right, there are four MUX\_41a blocks (inst1, inst2, inst3, inst4) with inputs S0, S1, D0, D1, D2, D3, and outputs Y, F0, F1, F2, F3. The circuit is connected to implement a 4-bit ripple-carry adder.

The screenshot shows the Logic Analyzer tool interface. The top bar displays the file names: lab4part1.bdf, lab4part1.vwf, MUX\_41a.vhd, Compiler Tool, lab4part2.bdf, lab4part2.vwf, and Simulator Tool. The Master Time Bar shows a time of 16.274 ns. The Pointer is at 324.71 ns, and the Interval is 308.44 ns. The Start and End times are also indicated. The main display area shows a timing diagram for various signals. The signals are listed on the left: A0, A1, A2, A3, B0, B1, B2, B3, Cin, S0, S1, Cout, F0, F1, F2, and F3. The signals A0 through A16 are shown as digital waveforms. The signals B0 through B3 are shown as digital waveforms. The signals Cin, S0, S1, Cout, F0, F1, F2, and F3 are shown as digital waveforms. The time scale ranges from 0 ps to 960 ns. A specific time point of 16.274 ns is highlighted, showing the state of the signals at that moment.

#### 4:1 MUX VHDL file

part1.bdf | lab4part1.vwf | MUX\_41a.vhd | Compile

```
1  library ieee; use ieee.std_logic_1164.all;
2  entity MUX_41a is port (
3      S1, S0: in bit;
4      D3, D2, D1, D0: in bit;
5      Y: out bit
6  );
7  end MUX_41a;
8  architecture logic OF MUX_41a IS
9  begin
10     Y <= (D0 and (not S1) and (not S0)) or
11         (D1 and (not S1) and S0 ) or
12         (D2 and S1 and (not S0)) or
13         (D3 and S1 and S0 ) ;
14 end logic;
```