Lab 4 Summary
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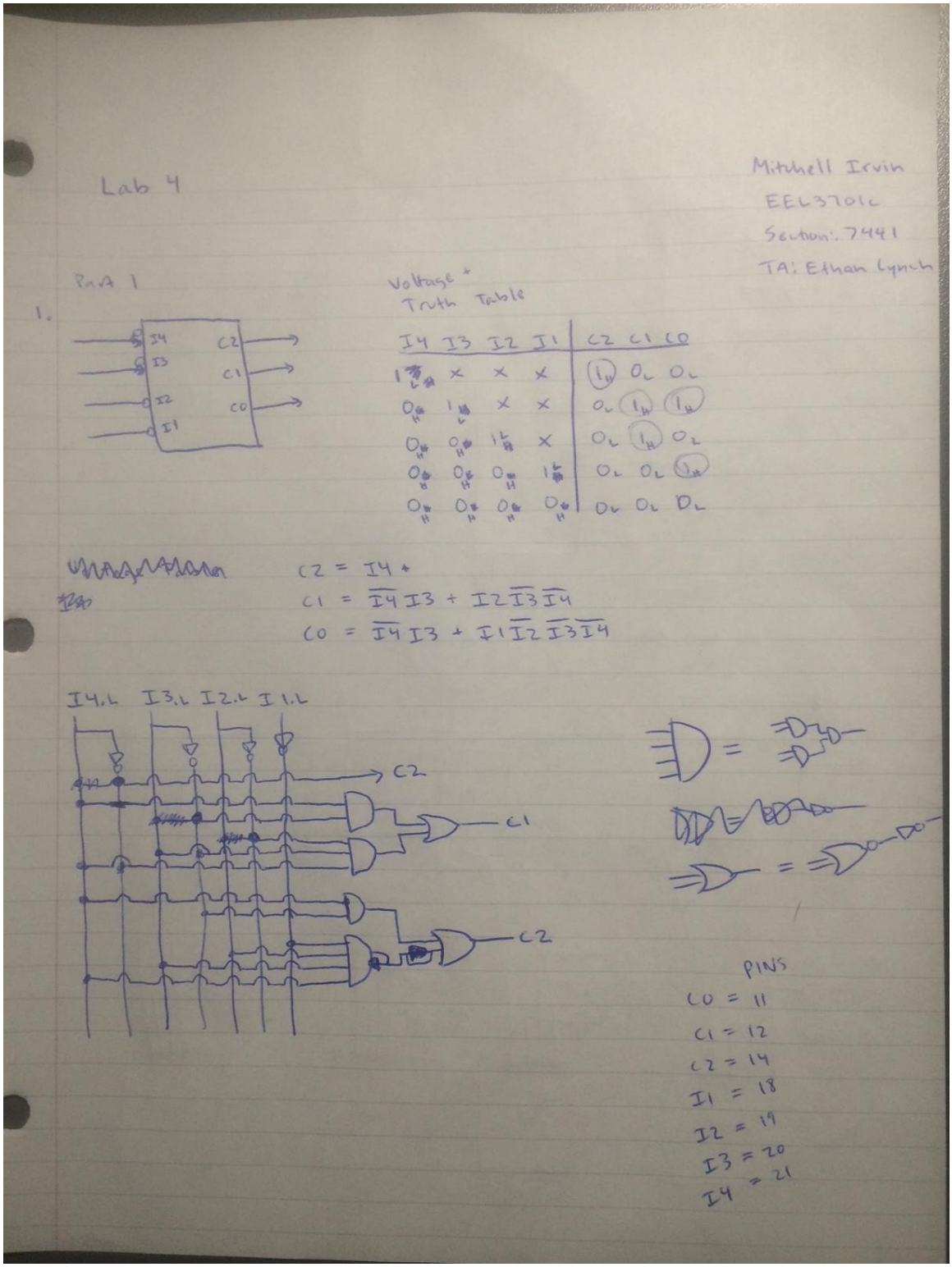
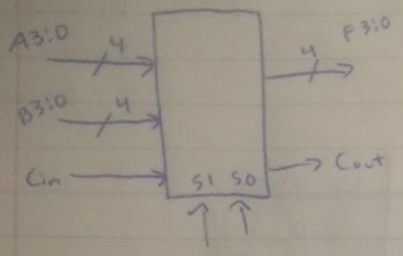
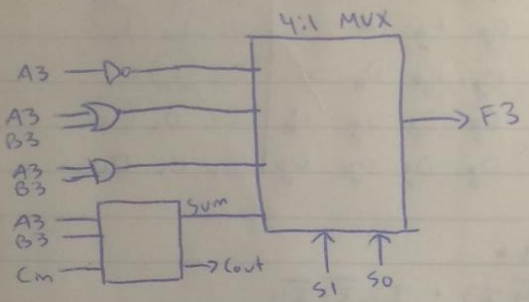
Section 7441
02/05/16



ALU

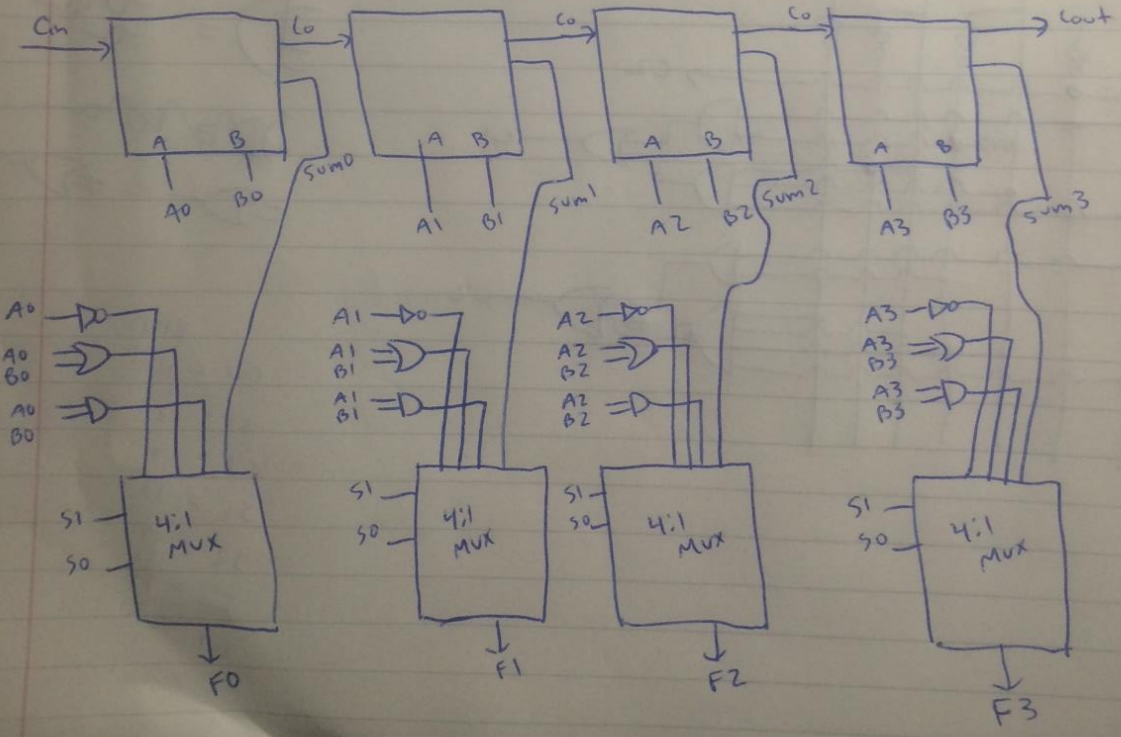


S1	S0	F
0	0	$\bar{A}$
0	1	A ∨ B
1	0	A ∧ B
1	1	A sum B

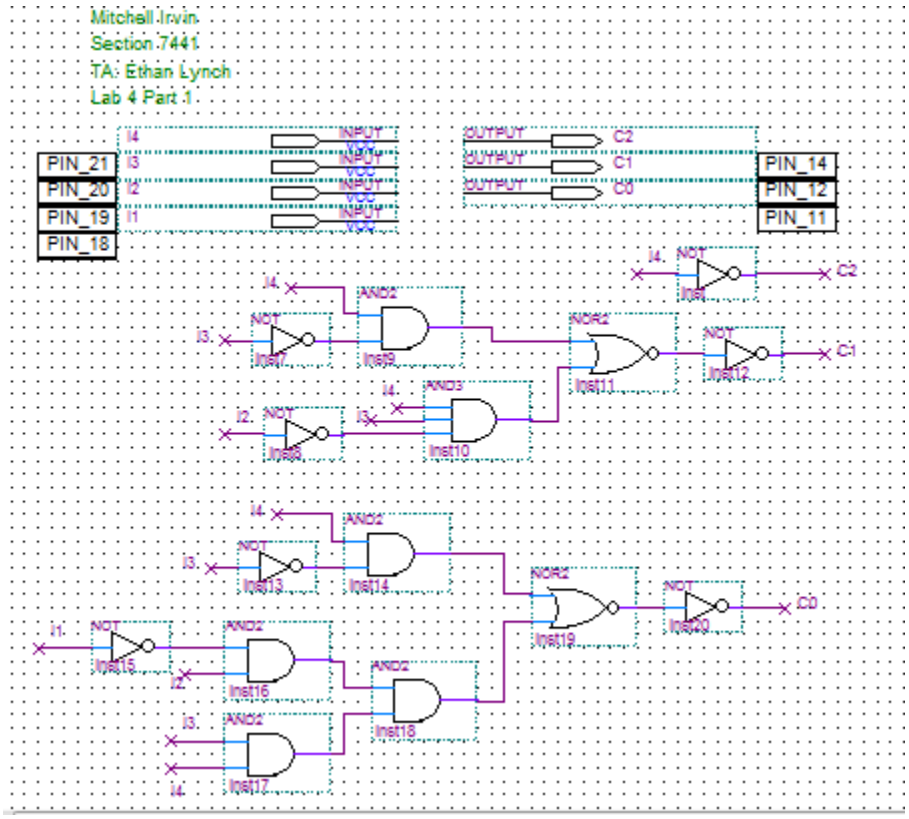


Repeat for A2:0, B2:0, and F2:0

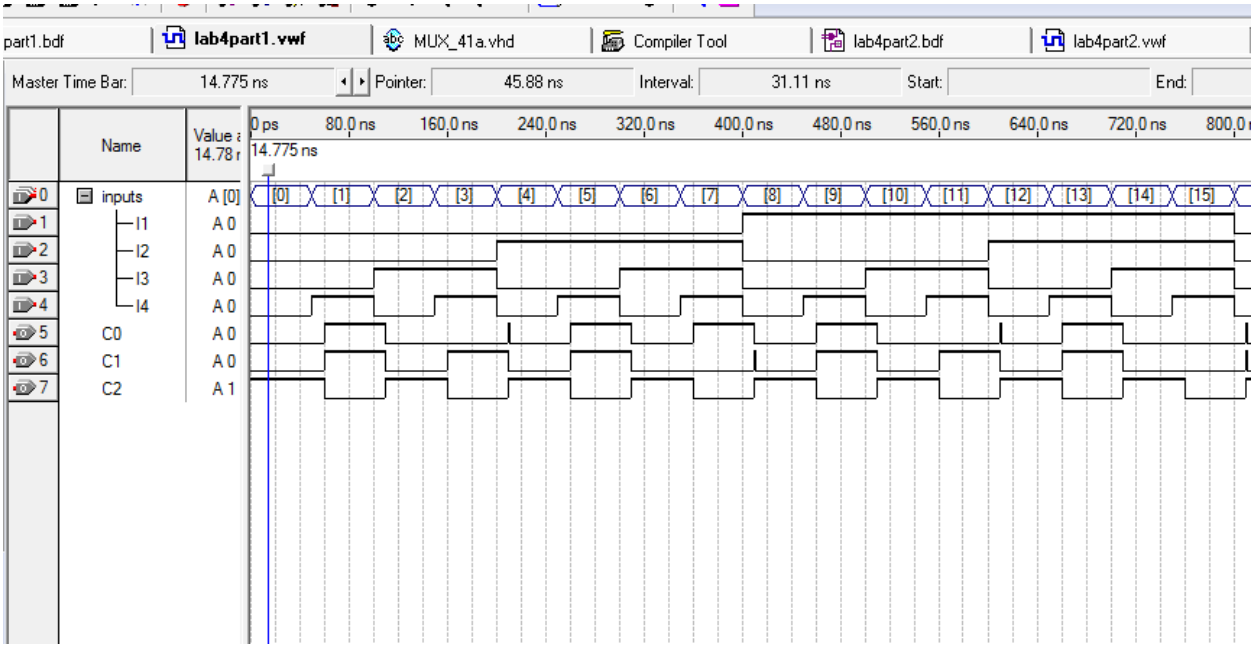
for sums:



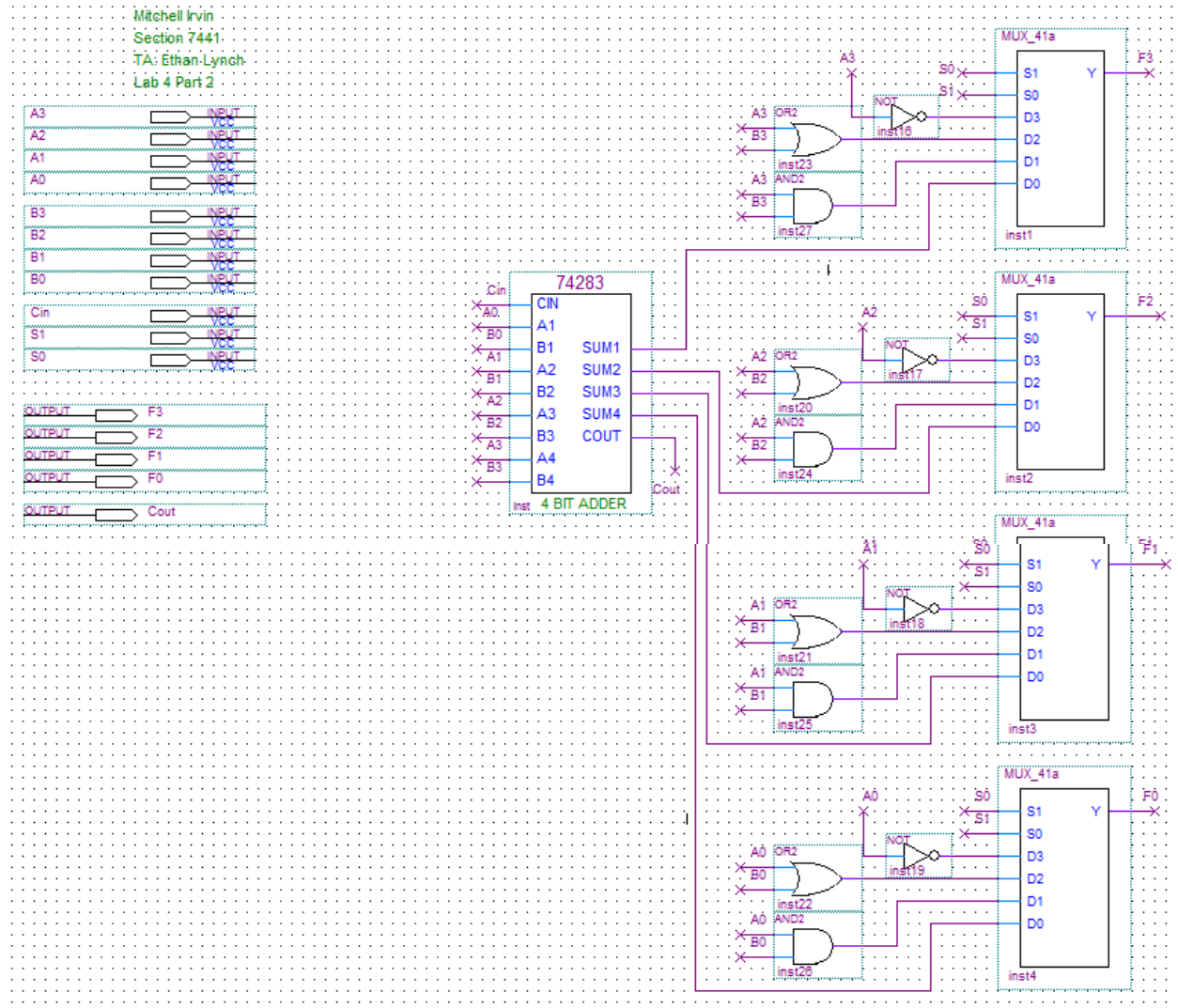
Part 1 BDF



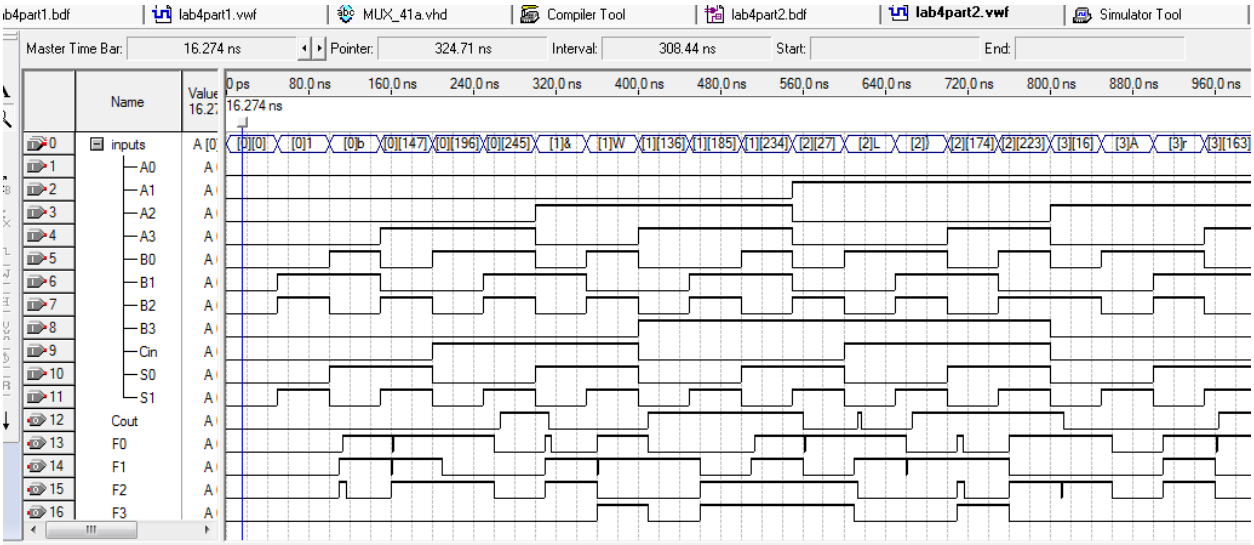
Part 1 VWF



Part 2 BDF



Part 2 VWF



4:1 MUX VHDL file

4part1.bdf | lab4part1.vwf | MUX_41a.vhd | Compile

```
1   library ieee; use ieee.std_logic_1164.all;
2   entity MUX_41a is port (
3       S1, S0: in bit;
4       D3, D2, D1, D0: in bit;
5       Y: out bit
6   );
7   end MUX_41a;
8   architecture logic OF MUX_41a IS
9   begin
10      Y <=    (D0 and (not S1) and (not S0)) or
11          (D1 and (not S1) and    S0 ) or
12          (D2 and     S1  and (not S0)) or
13          (D3 and     S1  and     S0 ) ;
14      end logic;
```