Lab 6 Summary
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Section 7441
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Prelab Part 1: VHDL of a 41MUX

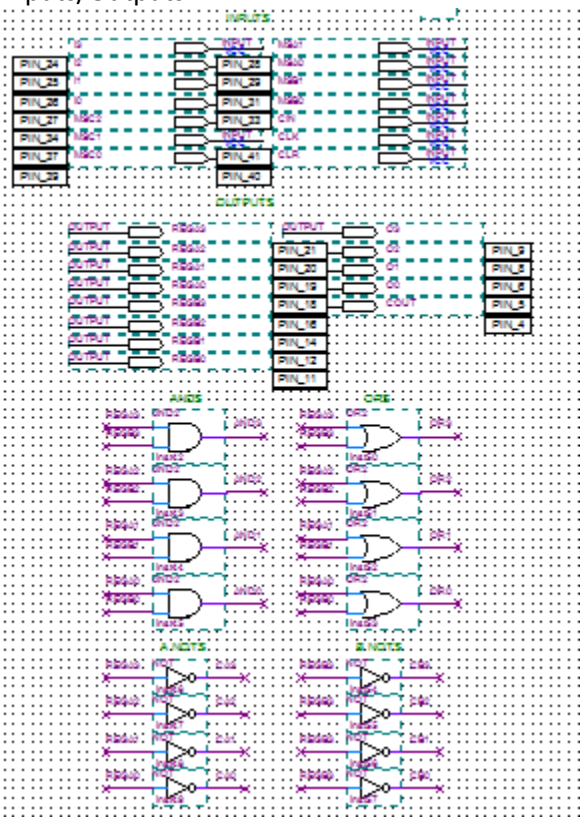
MUX41.vhd

```
1   library ieee; use ieee.std_logic_1164.all;
2   entity MUX_41a is port (
3       S1, S0: in bit;
4       D3, D2, D1, D0: in bit;
5       Y: out bit
6   );
7   end MUX_41a;
8   architecture logic OF MUX_41a IS
9   begin
10      Y <=    (D0 and (not S1) and (not S0)) or
11          (D1 and (not S1) and    S0 ) or
12          (D2 and     S1  and (not S0)) or
13          (D3 and     S1  and     S0 ) ;
14      end logic;
```

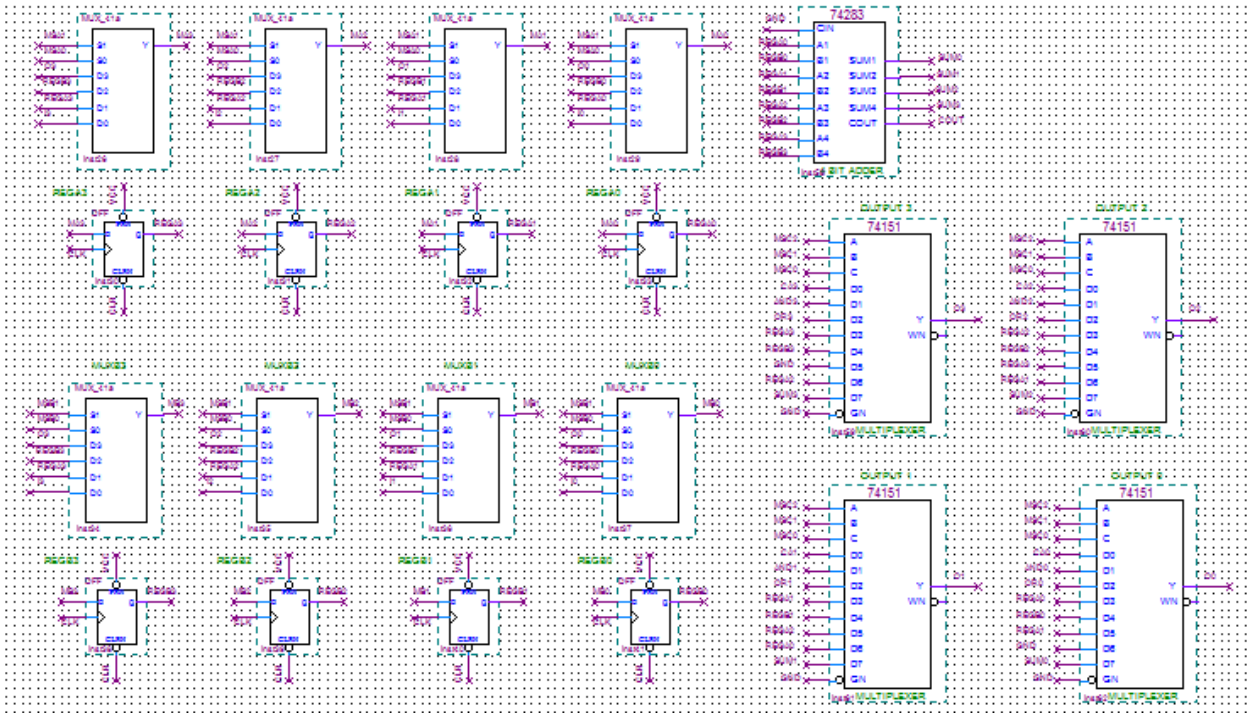
Verify that it works: if it didn't work the rest of my lab wouldn't work. I compiled it and created a VWF file to test it but that entire project folder got corrupted and I had to redo everything so please just let the rest of my lab be proof that it works

Part 2: ALU Design

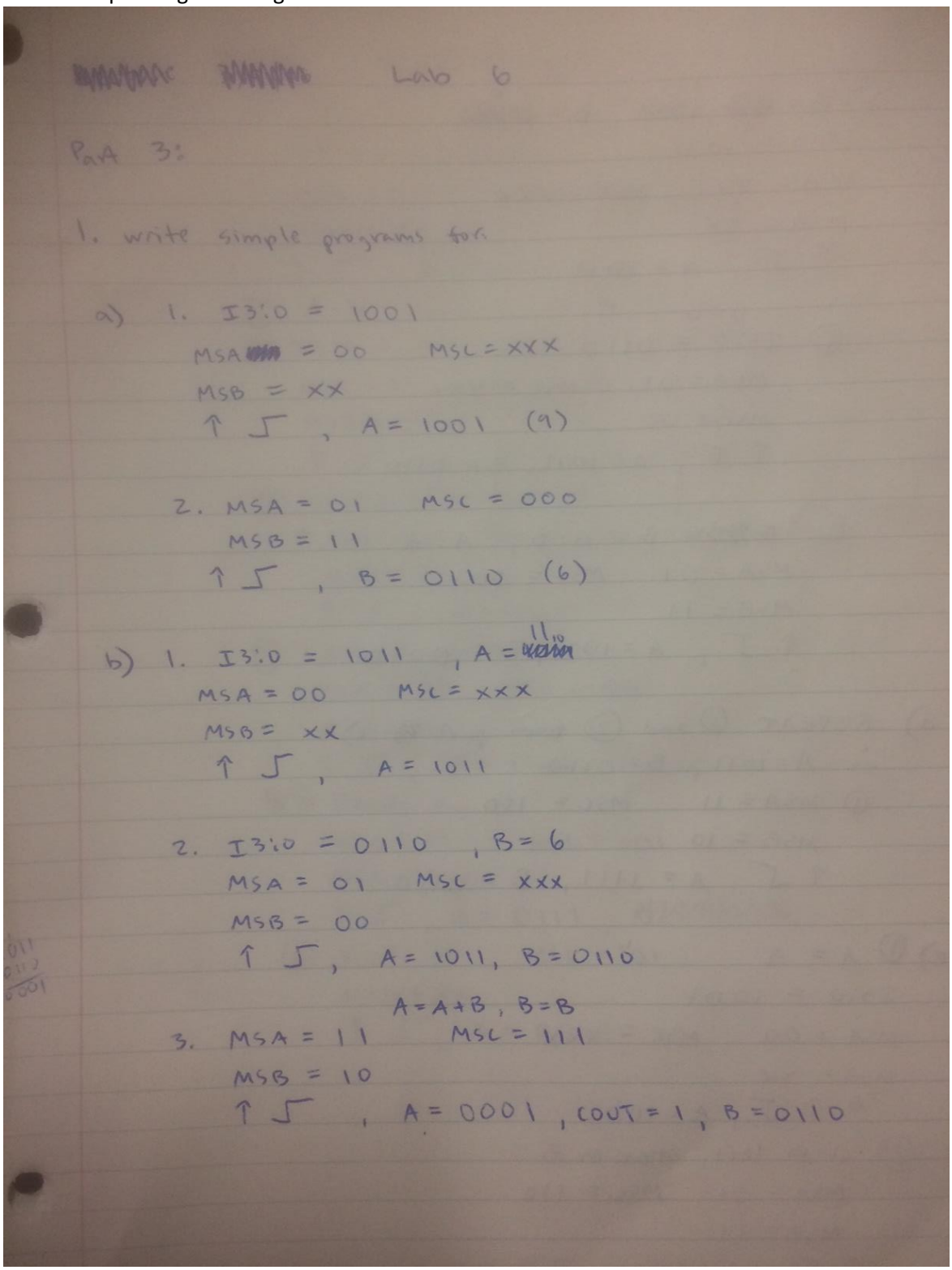
Inputs/Outputs



Logic Design



Part 3: Simple Program Design



Lab 6

Part 3:

1. write simple programs for

a) 1. I3:0 = 1001
MSA = 00 MSC = XXX
MSB = XX
↑ ⌐ , A = 1001 (9)

2. MSA = 01 MSC = 000
MSB = 11
↑ ⌐ , B = 0110 (6)

b) 1. I3:0 = 1011 , A = 11_{10}
MSA = 00 MSC = XXX
MSB = XX
↑ ⌐ , A = 1011

2. I3:0 = 0110 , B = 6
MSA = 01 MSC = XXX
MSB = 00
↑ ⌐ , A = 1011, B = 0110

A = A + B , B = B

3. MSA = 11 MSC = 111
MSB = 10
↑ ⌐ , A = 0001 , COUT = 1 , B = 0110

c) ① A = 11, B = 6

I3:0 = 1011

MSA = 00 MSC = XXX

MSB = XX

↑ ∫, A = 1011

B = 6

② I3:0 = 0110

MSA = 01 MSC = XXX

MSB = 00

↑ ∫, A = 1011, B = 0110

③ B = A · B, A = A

MSA = 01 MSC = 001

MSB = 11

↑ ∫, A = 1011, B = 0010

d) REPEAT ① and ② from part c)

∴ A = 1011, B = 0110

① MSA = 11 MSC = 110

MSB = 10

↑ ∫, A = 1111, B = 0110

e) ① A = 9

I3:0 = 1001

MSA = 00 MSC = XXX

MSB = XX

↑ ∫, A = 1001

② shift left, store in B

MSA = 01 MSC = 110

MSB = 11

↑ ∫, A = 1001, B = 0010

f) ① A = 3

I3:0 = 0011

MSA = 00 MSC = XXX

MSB = XX

↑ ⌐, A = 0011

② A · 4, load 2 into B

I3:0 = 0010

MSA = 11 MSC = 110

MSB = 00

↑ ⌐, A = 0110, B = 0010

③ second shift for A

MSA = 11 MSC = 110

MSB = 10

↑ ⌐, A = 1100, B = 0010

④ Add 2 to A

MSA = 11 MSC = 111

MSB = 10

↑ ⌐, A = 1110, B = 0010

⑤ Divide by 4

MSA = 11 MSC = 101

MSB = XX

↑ ⌐, A = 0111,

⑥ MSA = 11 MSC = 101

MSB = XX

↑ ⌐, A = 0011,

Verification of Prelab Part 3 in Quartus