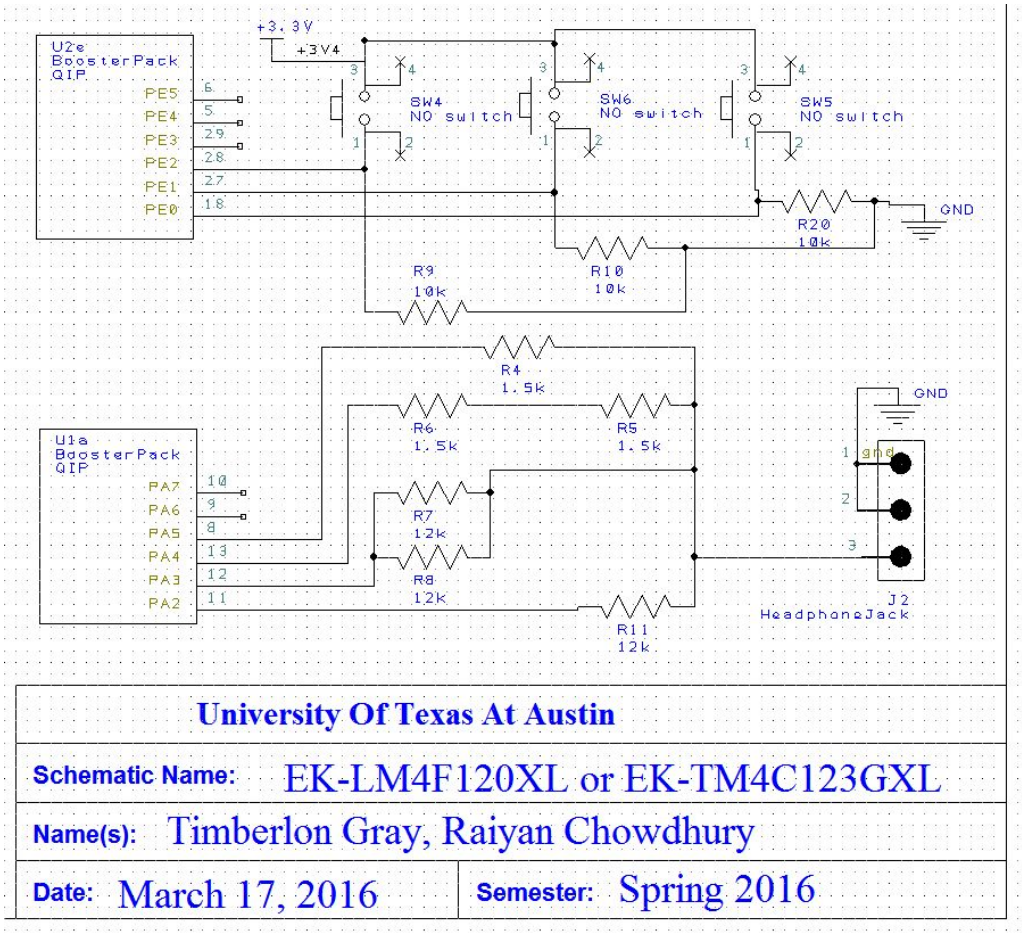


University Of Texas At Austin	
Schematic Name: EK-LM4F120XL or EK-TM4C123GXL	
Name(s): Timberlon Gray, Raiyan Chowdhury	
Date: March 17, 2016	**Semester:** Spring 2016

Software Design (next page):

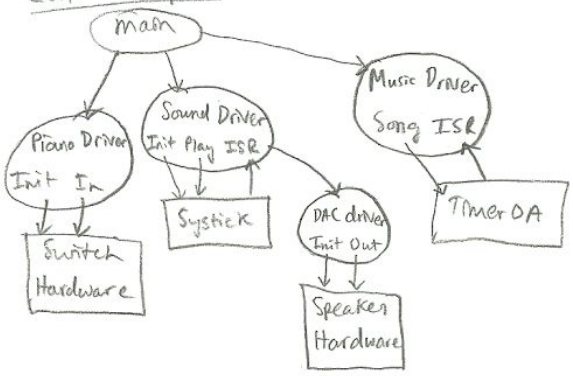
Sound data (sine wave)

8
10
13
14
15
14
13
10
8
5
2
1
0
1
2
5

Song Data

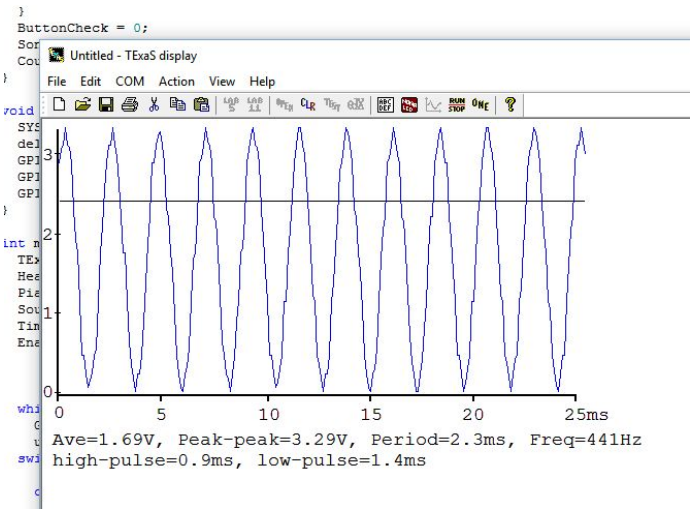
12755	G note
666	length of G note (for tempo)
15169	E note
666	
12755	
333	
15169	
333	
19111	C note
666	

Call Graph

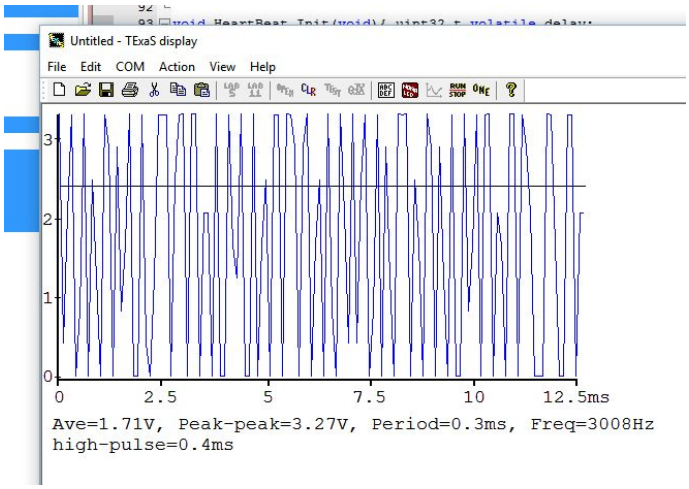


Data Flow is the same as Figure 6.6

Note A (440Hz):



Heartbeat:



Measurement Data:

Bits 3-0	Theoretical DAC voltage	Measured DAC voltage
0	0	0
1	.22	.22
2	.44	.44
3	.66	.65
4	.88	.87
5	1.10	1.09
6	1.32	1.31
7	1.54	1.53
8	1.76	1.74
9	1.98	1.96
10	2.2	2.18
11	2.42	2.40
12	2.64	2.62
13	2.86	2.83

14	3.08	3.05
15	3.3	3.27

Resolution: .22V ideal, or .21V actual
Range: 3.3V ideal, or 3.27V actual
Precision: 16
Accuracy: -.01 or -1%

Questions:

a. **When does the interrupt trigger occur?**
   When SysTick's CURRENT value is decremented from 1 to 0, the COUNT flag (bit 16 of NVIC_ST_CTRL_R) is set, triggering an interrupt provided that the INTEN bit was set prior.
b. **In which file is the interrupt vector?**
   In the startup.s file.
c. **List the steps that occur after the trigger occurs and before the processor executes the handler.**
   8 registers, with R0 on top, are pushed onto the stack. The PC is loaded with the vector address for the handler. The IPSR register is set to 15 and the top 24 bits of the LR are all set, which signifies that the processor is executing an interrupt service routine.
d. **It looks like *BX LR* instruction simply moves LR into PC, how does this return from interrupt?**
   Because the top 24 bits of the LR are all set to signify that an ISR was just being executed, it knows to return from the interrupt by popping eight registers off the stack again. The bottom 8 bits, depending on what they are, provide further specification on how to return from the interrupt.