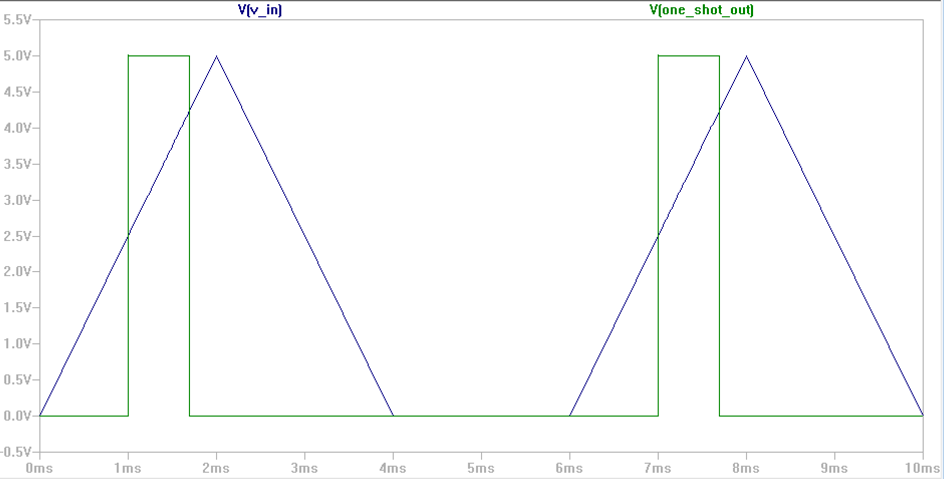
6.301 Final Project Deliverable 1

# One-shot circuit

This one-shot circuit simulates the edge triggered interrupt that would be implemented on the Arduino to capture the falling edge of the comparator output. In the given example, the flip-flop is positive edge triggered rather than negative edge triggered. The timing goes like this:

1. When the input voltage reaches the threshold (2.5V) for the flip-flop, the flip-flop clocks the D input to the Q output, making Q a logic high and ~Q a logic low.
2. While ~Q is low, the voltage controlled switch (a relay?) is de-energized and open, so the logic high on Q charges capacitor C1 through resistor R1 until eventually (when V\_CLR = 2.5), the CLR input to the flip-flop is asserted, causing Q to switch back low and ~Q to switch back high.
3. Now that ~Q is high, the voltage controlled switch is energized and closed, discharging the resistor and quickly de-asserting CLR to allow for the whole cycle to repeat.



The on time can be derived using simple time constants:



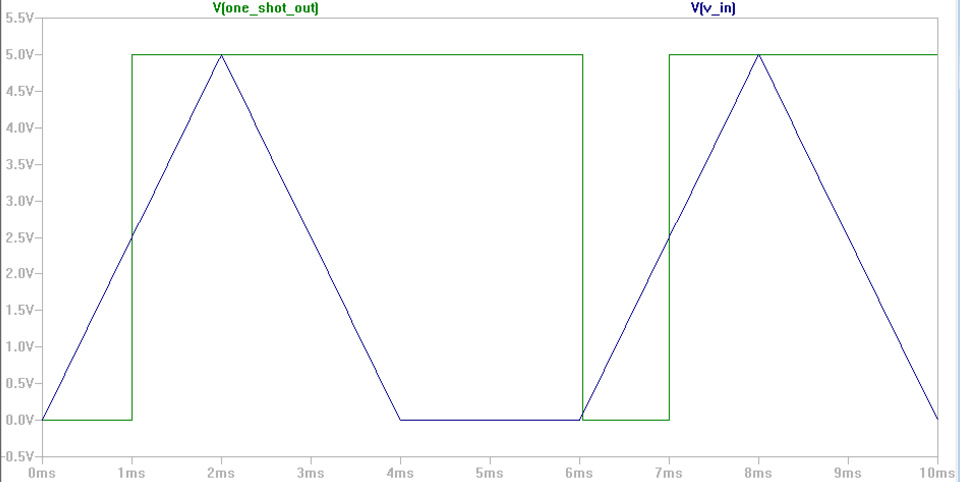
## 

In the sample code, the ramp up time is 5ms. To have an on time of 5ms, we find that



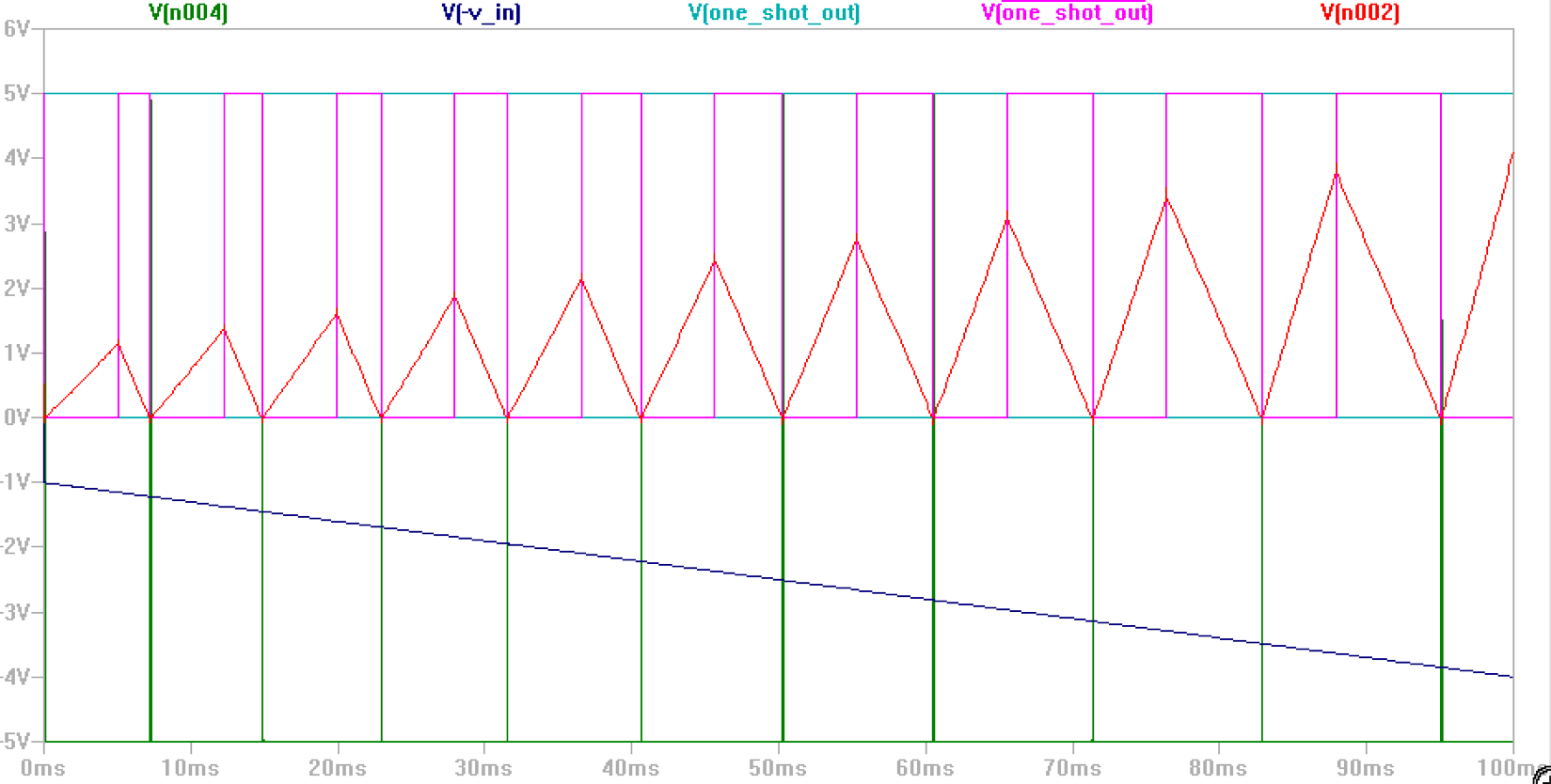
Choosing the E12 values of R1=33k and C1=0.22u, we get a time constant of 7.26ms.

After simulating with these values, we see the expected 5ms on time:



# Dual slope circuit

In this circuit, the outputs from the one-shot circuit are conveniently used to toggle the control switches for the dual-slope DAC. In the untriggered state, V\_REF is connected to the integrator and the voltage into the comparator is ramping down. Once it returns to 0V, the comparator output goes high since the integrator output is connected to the inverting input of the comparator output. The rising edge triggers the one-shot circuit, which is able to hold switch a closed for a known amount of time (5ms in my adjusted configuration), the ramp up period. Thus in this configuration the one-shot circuit simulates the entire Arduino ISR, except without a clock signal or counter to measure the period of the ramp down stage.



This screenshot shows how the input voltage changes the ramp down period while the ramp up period stays constant at 5ms due to the RC one-shot circuit. I changed the integrator capacitance so the integrator voltage wouldn’t hit the 5V and clip.