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DSP Based All-Digital Resolver-to-Digital Conversion Using DSRF-PLL

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***Abstract*—Nowadays all-digital resolver-to-digital conversion is popularly invested for space-limited applications. However time delay is inevitable in demodulation part when frequency shifting algorithm used. Furthermore, the angle calculation result is affected by time delay. So the synchronous demodulation is analyzed in this paper to void time delay. The demodulated sine and cosine signals always exist with amplitude and quadrature errors. In order to eliminate the influence of these two errors, the double synchronous reference frame–based phase-locked loop (DSRF-PLL) is investigated in the angle calculation part. DSRF-PLL removes the angular position error caused by the amplitude error and makes the position error caused by the quadrature error to be a constant value, which can be easily compensated in the software. So the angular position can be detected with no time delay and error. The presented all-digital resolver-to-digital conversion scheme is verified by the simulation and experimental results at the end of this paper.**

Keywords- resolver-to-digital conversion; synchronous demodulation; double synchronous reference frame; DSP

I. INTRODUCTION

Resolvers are very robust and cost-effective angular position sensors that are extensively used in many safety-critical applications like aircrafts, satellite antennas and robots [1]. They resemble small motors and have magnetically coupled rotor and stator windings. A resolver-to-digital converter (RDC) is used to obtain the angular position information from the analog output of the resolver. The accuracy of the shaft angular speed and position measurement is fundamentally based on the assumption that ideal analog resolver signals are supplied to the RDC and on the high resolution of RDCs. However, in reality, no resolver generates ideal signals, and high resolution RDCs are very expensive. So there is the necessity for cost effective realization, flexibility of operation, reduction of weight and size, and wide range of operation. This paper gives a different approach to achieve the same goal, namely, to implement the external resolver-to-digital converter IC as an all-digital R/D conversion.

Several methods for R/D conversion, e.g. [1]-[3] exist in the literature, focusing on ways to improve the measurement accuracy of the R/D converter, however, techniques that can reduce or eliminate the position error incurred due to the amplitude and quadrature errors, are rarely found. In [4] and [5], Hanselman presents a thorough investigation of the effects of common non-ideal resolver signal characteristics on position accuracy and discusses some techniques that reduce the position error. However, it is time consuming and labor intensive. And the quadrature error cannot be eliminated if the amplitude error already exists. In [6], Bergas-Jané *et al*. present a methodology to suppress gain and phase errors based on the DSRF-PLL, but the specific derivation process and implementation are not given.

In this paper, an alternative solution for a RDC, based on software approach is investigated. The presented conversion scheme integrates the synchronous demodulation's advantage and the error elimination of the DSRF-PLL. DSRF-PLL detects resolver positive direction's angular position and speed accurately even in the presence of the amplitude and quadrature errors. This all-digital resolver-to-digital conversion can be implemented in a commercial digital signal processor (DSP) which is commonly used for servo drive systems; the necessary hardware is reduced to a few low-cost amplifiers saving space on board. Experimental results obtained with a TMS320F2812 DSP are presented to show the reasonable accuracy and good performances.

II. PRICIPLE OF OPERATION OF A RESOLVER

The resolver is widely used for its fine resolution and accuracy, low output impedance, wide temperature range of operation, and simple and robust construction, operates on the principle of mutual induction, as in a transformer.

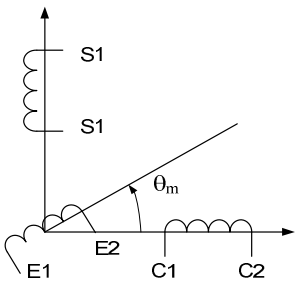

Figure 1. Simplified schematic of a resolver

Fig.1 shows the simplified schematic of a resolver. The excitation coil (E1-E2) resides in the rotor and is usually fed by means of brushes or magnetic coupling from the stator, with an

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excitation voltage of frequency ω_e in the range from 4 to 10 KHz as in Eq. (1). S1-S2 and C1-C2 are two quadrature stator coils, usually known as the sine and the cosine coils, respectively.

$$V_E = U_m \cos(\omega_e t) \tag{1}$$

Equations (2) and (3) show the voltages induced in both stator coils when the rotor coil is excited by the excitation signal. These two signals are the excitation signals modulated by the sine and cosine of the mechanical angle (θ_m) as follows:

$$V_S = kU_m \sin\theta_m \cos(\omega_e t) \tag{2}$$

$$V_C = kU_m \cos\theta_m \cos(\omega_e t) \tag{3}$$

where: k=resolver rotor-to-stator transformation ratio;

U_m =excitation signal amplitude;

θ_m =resolver shaft absolute angular position

ω_e =excitation signal angular frequency

Each of the signals expressed by Eq. (2) and Eq. (3) should be conditioned by a differential amplifier in order to refer them to a signal ground, to amplify them and to reject common mode noise. Then the conditioned signals are sent to the inputs of the RDC which demodulates and processes them outputting the angular position of the resolver shaft in a digital form.

The demodulated signals:

$$V_{S1} = \alpha k U_m \sin\theta_m \tag{4}$$

$$V_{C1} = \alpha k U_m \cos\theta_m \tag{5}$$

where α is a coefficient in the range between -1 and 1, depending on the sampling moment of the excitation period.

Once V_{S1} and V_{C1} are obtained, it is easy to obtain the mechanical angle θ_m with a four quadrant inverse tangent function:

$$\theta_m = \begin{cases} \arctan\dfrac{V_{S1}}{V_{C1}} & if\ V_{C1} >= 0 \\ \pi + \arctan\dfrac{V_{S1}}{V_{C1}} & if\ V_{C1} < 0 \end{cases} \tag{6}$$

III. SOFTWARE-BASED R/D CONVERSION

Fig. 2 depicts the general structure of the software-based R/D converter. In this R/D conversion scheme, the sinusoidal excitation signal for the resolver is generated with the PWM module of the DSP. To match resolver characteristics, the PWM signal has to be filtered and amplified. At the same time, the peak of the excitation signal is detected when the signal is generated. At the positive peak, the sample and hold unit is triggered and the resolver's amplitude-modulated output is synchronously demodulated. Certainly, before demodulated, the sine and cosine signals have to be adapted to the DSP ADCs inputs with instrumental amplifiers. Eventually, this synchronous demodulation extracts the resolver outputs' envelopes, which can be used to compute the shaft rotation θ_m by using various strategies, such as inverse tangent (including LUT), PLL and the synchronous rotating reference frame based-PLL (SRF-PLL).

There are some advantages of generating excitation signal inside the DSP:

- Flexibility of changing the resolver excitation frequency;
- Accessibility of detecting the peak of the excitation signal with very simple logic;
- Reduction of weight and size as the most work is done inside the DSP.

The following subsection briefly describes the method of synchronous demodulation and DSRF-PLL.

A. Synchronous Amplitude Demodulation

As the resolver's output signals are the excitation signal modulated by the sine and cosine of the mechanical angle. Before angle calculation, the signals should be demodulated. There are two main approaches to demodulate the resolver output signals. One is synchronous amplitude demodulation [7], the other one is frequency shifting algorithm [8]. Frequency shifting algorithm needs a low-pass filter which will introduce a time delay and affect the dynamics of system. While synchronous demodulation does not bring any time delay and is very simple, especially when the excitation signal is generated inside the DSP.

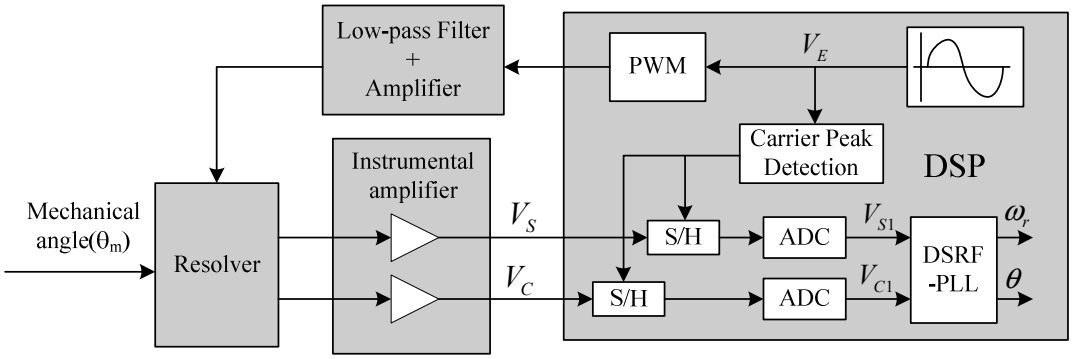


Figure 2. General structure of the complete system

In order to obtain maximum accuracy, the quadrature outputs should be simultaneously sampled at the positive peak of the excitation signal, as shown in Fig. 3. In the DSP, a lookup table (LUT) that contains sine values is stored in the memory. The corresponding PWM duty cycle is searched from the LUT regularly according to the excitation frequency. The excitation signal reaches peak value when the PWM duty cycle gets the maximum in the LUT. So the ADC module should be triggered once the PWM duty cycle equals to the maximum.

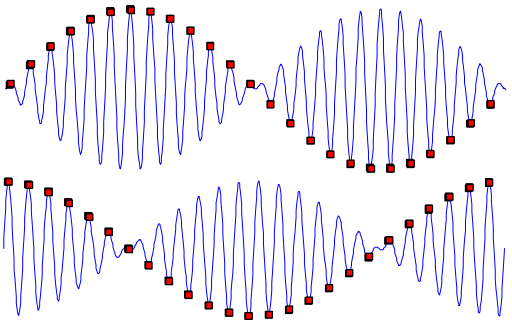


Figure 3. Sine and cosine signals are sampled at the peak of excitation signal

There are some drawbacks of the synchronous demodulation: it is not easy to get the exact maximum of the carrier because the real excitation signal suffers various delays in the analog hardware components, and further complicated by variation of temperature and age [8]. However, in fact, there is no need to make the samples taken at the exact peak of the carrier, as long as the quadrature signals are sampled at the same point of the carrier, and this point is far from the zero crossing point of the carrier. That is, the absolute value of in equations (4) and (5). And it is easy to implemented, due to the symmetrical structure of the analog circuit. In addition, when this condition is not fulfilled, that is the sine and cosine signals have different delays during the transmission, the errors induced are amplitude error and quadrature error (Fig. 4). These errors can be corrected by the angle calculation strategy which is introduced in the following subsection. So in order to avoid bringing time delay and improve the dynamics of system, here choose the synchronous demodulation method.

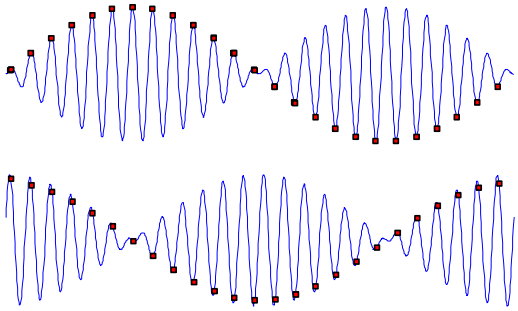


Figure 4. Non-ideal synchronous demodulation

B. Double synchronous reference frame based PLL

It is necessary to mention that resolvers are not ideal electrical machines [9]. It is common to find two kind errors in the sine and cosine signals:

- Amplitude errors, that is, the amplitudes of the sine and cosine signals are not the same;
- Quadrature errors, that is, the phase of the sine signal is not lag 90 degree with the cosine signal.

These two kind errors also can be introduced by the non-ideal synchronous demodulation stated previously. If not properly corrected, they will lead to position and speed errors. The estimated speed has a large fluctuation, and the calculated angle has a significant difference with the real position.

In order to eliminate the influence caused by amplitude and quadrature errors, a DSRF-PLL is applied to calculate the angle [6]. Supposing the resolver has both amplitude and quadrature errors, which without loss of generality, can be assumed to be all concentrated in the cosine signal. The sine and cosine signals are then rewritten as Eq. (7)

$$v_S = \begin{bmatrix} V_{C2} \\ V_{S2} \end{bmatrix} = \begin{bmatrix} aV\cos(\theta_m + b) \\ V\sin\theta_m \end{bmatrix} \tag{7}$$

If the SRF-PLL is used to solve these unbalanced resolver signals, the estimated speed accelerates and decelerates. The DSRF-PLL is similar to the SRF-PLL. But it is composed of two rotating reference axes: dq^{+1}, rotating with the positive direction with the angular position $\hat{\theta}$; and dq^{-1}, rotating with the negative direction with the angular positive $-\hat{\theta}$. As shown in Fig. 5.

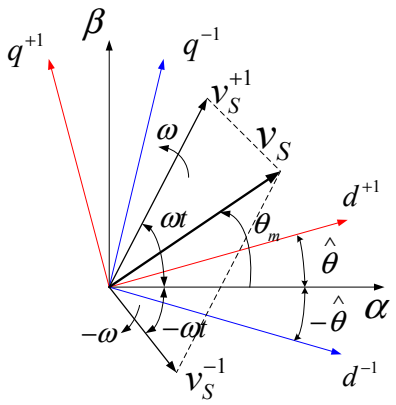


Figure 5. Vector v_S and axes of DSRF

Then the unbalanced vector v_S can be expressed on the DSRF yielding [10]:

$$\begin{aligned} v_{S(dq^{+1})} &= \begin{bmatrix} v_{Sd^{+1}} \\ v_{Sq^{+1}} \end{bmatrix} = \begin{bmatrix} T_{dq^{+1}} \end{bmatrix} \cdot v_S \\ &= V_S^{+1} \begin{bmatrix} \cos(\omega t - \hat{\theta}) \\ \sin(\omega t - \hat{\theta}) \end{bmatrix} + V_S^{-1} \begin{bmatrix} \cos(-\omega t - \hat{\theta}) \\ \sin(-\omega t - \hat{\theta}) \end{bmatrix} \end{aligned} \tag{8}$$

$$v_{S(dq^{-1})} = \begin{bmatrix} v_{Sd^{-1}} \\ v_{Sq^{-1}} \end{bmatrix} = \left[T_{dq^{-1}}\right] \cdot v_S = V_S^{+1} \begin{bmatrix} \cos(\omega t + \hat{\theta}) \\ \sin(\omega t + \hat{\theta}) \end{bmatrix} + V_S^{-1} \begin{bmatrix} \cos(-\omega t + \hat{\theta}) \\ \sin(-\omega t + \hat{\theta}) \end{bmatrix} \quad (9)$$

where $\left[T_{dq^{+1}}\right] = \left[T_{dq^{-1}}\right]^T = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix}$

ω is the angular speed of resolver. It is possible to achieve $\hat{\theta} \approx \omega t$ by using a PLL structure. If a perfect synchronization of the PLL is possible, that is if $\hat{\theta} \approx \omega t$, the vector v_S can be rewritten as follows:

$$v_{S(dq^{+1})} = \begin{bmatrix} v_{Sd^{+1}} \\ v_{Sq^{+1}} \end{bmatrix} = V_S^{+1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} + V_S^{-1} \begin{bmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{bmatrix} \quad (10)$$

$$v_{S(dq^{-1})} = \begin{bmatrix} v_{Sd^{-1}} \\ v_{Sq^{-1}} \end{bmatrix} = V_S^{-1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} + V_S^{+1} \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} \quad (11)$$

In equation (10), the amplitude of the signal in dq^{+1} axes contains a constant value and an oscillation with a frequency 2ω , and vice versa. In order to cancel the oscillations in the dq^{+1} axes signals, a decoupling unit is applied [10] shown in Fig. 6 according to Eq. (12a) and (12b).

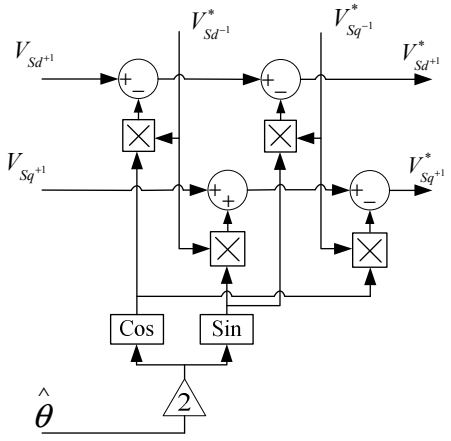


Figure 6. Decoupling unit for the dq^{+1} axes

The dq^{-1} axes signals can also be decoupled according to Eq. (12c) and (12d):

$$v^*_{Sd^{+1}} = v_{Sd^{+1}} - v^*_{Sd^{-1}} \cos 2\hat{\theta} - v^*_{Sq^{-1}} \sin 2\hat{\theta} \quad (12a)$$

$$v^*_{Sq^{+1}} = v_{Sq^{+1}} - v^*_{Sd^{-1}} \sin 2\hat{\theta} - v^*_{Sq^{-1}} \cos 2\hat{\theta} \quad (12b)$$

$$v^*_{Sd^{-1}} = v_{Sd^{-1}} - v^*_{Sd^{+1}} \cos 2\hat{\theta} + v^*_{Sq^{+1}} \sin 2\hat{\theta} \quad (12c)$$

$$v^*_{Sq^{-1}} = v_{Sq^{-1}} - v^*_{Sq^{+1}} \cos 2\hat{\theta} - v^*_{Sd^{+1}} \sin 2\hat{\theta} \quad (12d)$$

Eventually, the positive constant component is detected successfully. Once the amplitude of the positive-sequence is detected, it is sent to a PLL to get the angular speed and the angular position. The whole structure of DSRF-PLL is depicted in Fig. 7.

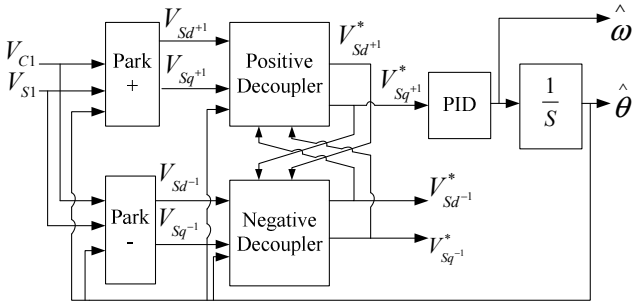


Figure 7. Structure diagram of DSRF-PLL

In addition, it is worth emphasizing that there is no constant error between the estimated angular position and the actual value if there is only an amplitude error. However, when the quadrature error exists, there is an initial phase difference between the positive rotation vector and the actual vector. That is to say, a constant error ε will appear in the estimated result. This error can be calculated as Eq. (13), and can be easily compensated in the software.

$$\varepsilon = act\tan\left(\frac{a\sin b}{1 + a\cos b}\right) \quad (13)$$

IV. SIMULATION RESULTS

In most resolver-to-digital conversion, SRF-PLL is the popular strategy of angle calculation. Fig. 8 depicts the traditional strategy SRF-PLL. The cosine and sine signals are sent into the Park transform as α and β components respectively. The V_q component is proportional to the sine of the position error. A second-order closed loop controller (formed by a PID plus a null pole integrator) is used to keep V_q component near null by locking to the angle.

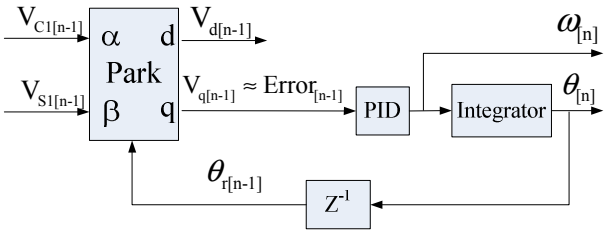


Figure 8. Syncronous rotating reference frame PLL

The SRF-PLL and DSRF-PLL strategies are simulated using the Simulink at the same time. Fig. 9 shows the general structure of simulation.

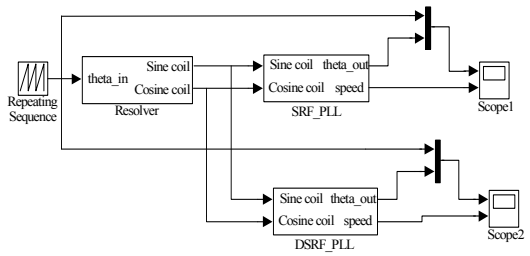


Figure 9. General block diagraph of simulation

The resolver block outputs the sine and cosine signals containing amplitude and quadrature errors. In specific, the sine signal is 20% larger than cosine one and lags 70° instead of 90° . The Lissajous curve of the sine and cosine signals is shown in Fig. 10. This curve is a perfect circle when there are no amplitude and quadrature errors, while it turns into an ellipse if the errors exist.

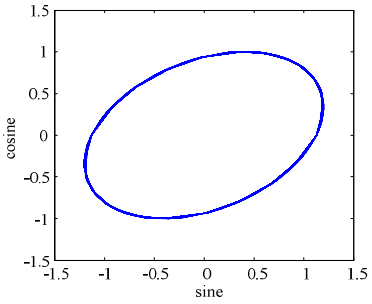


Figure 10. Lissajous curve of the sine and cosine signals

Fig. 11 gives the simulation results of the SRF-PLL. The estimated speed contains a large fluctuation around the true

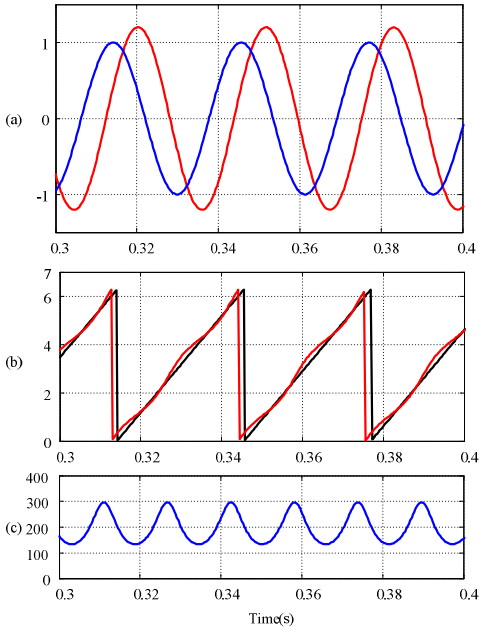


Figure 11. Simulation results of SRF-PLL.(a): sine and cosine signals(sine signal is 20% larger than cosine one and dephased 70°). (b): estimation of angular posion (red) and real position (black). (c): estimation of speed

speed 200 rad/s, and the estimated position result has a significant difference with the real position.

As stated in Section III, the decoupling unit is used to cancel the oscillations in the dq^{+1} axes signals. The simulation results of $V_{Sd^+}^*$ and $V_{Sd^-}^*$ is shown as Fig. 12, from which we can see the process of the elimination of the oscillations.

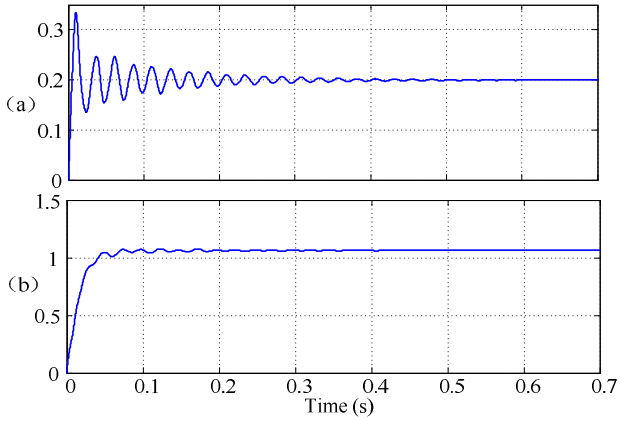


Figure 12. Decoupled dq^{+1} signals. (a): $V_{Sq^+}^*$ component. (b): $V_{Sd^+}^*$ component.

After decoupled, the positive constant component is sent to a PID controller to get the angular speed and position. Fig. 9 shows the simulation results for the resolver signals with amplitude and quadrature errors. It can be seen that the estimated speed is 200 rad/s, and the amplitude and quadrature errors have little influence on the speed and position results.

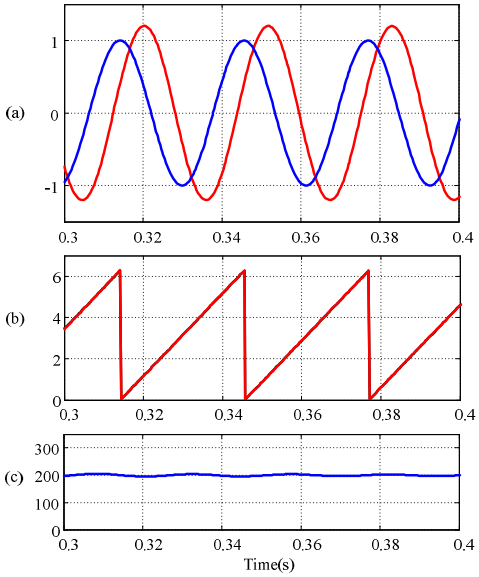
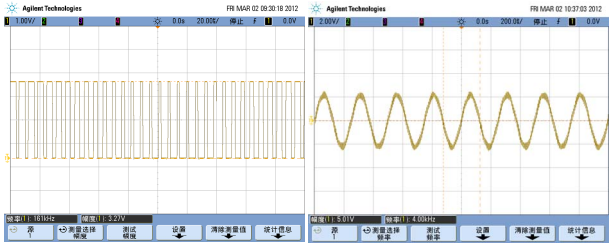


Figure 13. Simulation results of DSRF-PLL. (a): sine and cosine signals(sine signal is 20% larger than cosine one and dephased 70°). (b): estimation and real angular position. (c): estimation of speed

V. EXPERIMENTAL RESULTS

In order to evaluate the performance of the whole system, an experiment has been carried out using DSP (TMS320F2812). This 32-bit DSP has ADCs with 12-bit resolution and twelve PWMs, which is particularly designed for motor control. The control board includes a serial communication bus, which is used to transmit DSP's variable values to PC. Beside the control board, the experimental system contains a BLDC motor with a two-pole resolver.

The nominal excitation frequency of the resolver is 4 KHz, which is digitally generated with the PWM module of the DSP at an output frequency of 160 KHz. There are 40 points per period, which is quite enough due to the low-pass filter applied. Fig. 14 shows the SPWM generated by the DSP and the filtered signal.



(a) (b)

Figure 14. (a): SPWM output. (b): filtered carrier

After synchronous demodulation, the sine and cosine signals are calculated by both SRF-PLL and DSRF-PLL strategies, which give estimation to the mechanical velocity and angle. The obtained results are plotted with Matlab as Fig. 15, showing a good conformance with the simulation results.

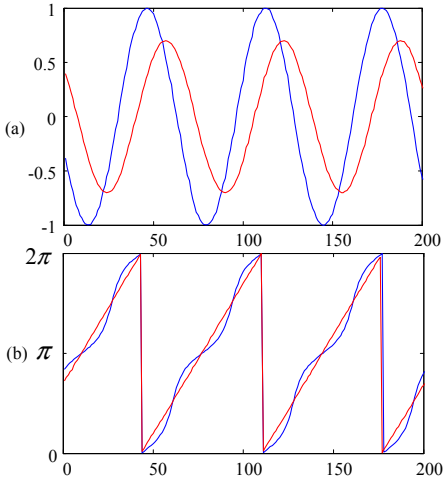


Figure 15. Experimental data plotted in Matlab. (a): Demodulated sine and cosine signals(sine signal is 30% lower than cosine one and dephased 60°). (b): angular position calculated by SRF-PLL (blue)and DSRF-PLL (red)

VI. CONCLUSION

All-digital RDC is a cost-economical and flexible resolver signals processing scheme, which is used in more and more ordinary occasions replacing commercial RDC IC. A scheme incorporates software-based generation of the excitation signal, synchronous demodulation and DSRF-PLL is investigated in this paper. The software-based generation of the excitation signal makes the synchronous demodulation feasible. And synchronous demodulation is utilized to avoid the time delay of the low-pass filter. On the other hand, DSRF-PLL is a suitable strategy to eliminate the influence caused by amplitude and quadrature errors exist in the resolver output signals. The whole system is low-cost and flexible. Simulations together with an experimental evaluation were presented to verify and validate the effectiveness of the all-digital resolver-to-digital conversion and the excellent results obtained by the DSRF-PLL.

VII. ACKNOWLEDGEMENT

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REFERENCES

[1] A. Murray, B. Hare, and A. Hirao, "Resolver position sensing system with integrated fault detection for automotive applications," in *Proc. IEEE Sensors,* vol. 2, pp. 864-869, Jun. 2002.

[2] C. H. Yim, I. J. Ha, and M. S. Ko, "A resolver-to-digital conversion method for fast tracking," *IEEE Trans, Ind. Electron*., vol. 39, no. 5, pp.369-378, Oct. 1992.

[3] M. Benammar, L. Ben-Brahim, and M. A. Alhamadi, "A high precision resolver-to-digital converter," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 6, pp. 2289-2296, Dec. 2005.

[4] Hanselman, D.C., "Resolver signal requirements for high accuracy resolver-to-digital conversion," *IEEE Trans. Ind. Electron*., vol.37, no.6, pp. 556-561, Dec 1990.

[5] D. Hanselman, "Techniques for improving resolver-to-digital conversion accuracy," *IEEE Trans. Ind. Electron.*, vol. 38, no. 6, pp. 501-504, Dec. 1991.

[6] Bergas-Jané, J.; Ferrater-Simón, C.; Gross, G.; Ramírez-Pisco, R.; Galceran-Arellano, S.; Rull-Duran, J.; , "High-Accuracy All-Digital Resolver-to-Digital Conversion," *IEEE Trans. Ind. Electron*., vol.59, no.1, pp.326-333, Jan. 2012.

[7] S. Sarma, V. K. Agrawal, and S. Udupa, "Software-based resolver-to-digital conversion using a DSP," *IEEE Trans. Ind. Electron*., vol. 55, no. 1, pp. 371-379, Jan. 2008.

[8] G. Gross, M. Teixido,.A. Sudria, and J. Bergas, "All-digital resolver-to-digital conversion," in *Proc. Eur. Conf. Power Electron. Appl*., Sep. 11-14, 2005, pp. 1-8.

[9] A. Bunte and S. Beineke, "High-performance speed measurement by suppression of systematic resolver and encoder errors," *IEEE Trans. Ind. Electron*., vol. 51, no. 1, pp. 49-53, Feb. 2004.

[10] P. Rodriguez, J. Pou, J. Bergas, J. Candela, R. Burgos, and D.Boroyevich, "Decoupled double synchronous reference frame PLL for Power converters control," *IEEE Trans. Power Electron*., vol. 22, no. 2, pp. 584-592, Mar. 2007.