

Efficient Execution of DG-FEM workloads on GPUs via CUDAGraphs

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Senior Thesis

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ABSTRACT

Array programming paradigm offers routines to express the computation cleanly for a wide variety of scientific computing applications (Finite Element Method, Stencil Codes, Image Processing, Machine Learning, etc.). While there's ongoing work to provide efficient data structures and fast library implementations for many common array operations, the performance benefits are tied to optimized method calls and vectorized array operations, both of which evaporate in larger scientific codes that do not adhere to these constraints. There have been a lot of efforts in scaling up n-d array applications through kernel and loop fusion, but little attention has been paid towards harnessing the concurrency across array operations. The dependency pattern between these array operations allow multiple array operations to be executed concurrently. This concurrency can be targeted to accelerate the application's performance. NVIDIA's `CUDA`Graphs offers a task programming model that can help realise this concurrency by overcoming kernel launch latencies and exploiting kernel overlap by scheduling multiple kernel executions in parallel. In this work we map the array operations onto a precise data-flow graph and expose that to a GPU via `CUDA`Graphs. To evaluate the soundness of this approach, we port a suite of DG-FEM operators that represent real life workloads to our framework and observe a speedup of upto 24x over a version where the array operations are executed one after the other.

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execution of a user-defined Directed Acyclic Graph (DAG). See Fig 2. for an example of a `CUDAGraph`. When one places a kernel into a stream, the host driver performs a sequence of operations in preparation for the execution of the kernel. These operations are what are typically called “kernel overhead”. To reduce this cost, CUDA graphs amortize the overheads of multiple kernel launches into one graph launch. However, since computing a graph is more expensive than running kernels directly[2], the performance gains only become apparent for large computations that *fill* the GPU.

One such class of discretizations that is able to scale up to modern GPU architectures is Discontinuous Galerkin Finite Element Method (DG-FEM). The characteristics of DG-FEM for PDE computations on GPUs have been investigated in [14], coming to the conclusion that speed-ups of factor 50 or more are possible. This makes DG-FEM an appealing application for `CUDAGraphs`. While our framework is generic, we evaluate the profitability of `CUDAGraphs` by targeting three end-to-end DG-FEM operators and observe a speedup of upto 24x.

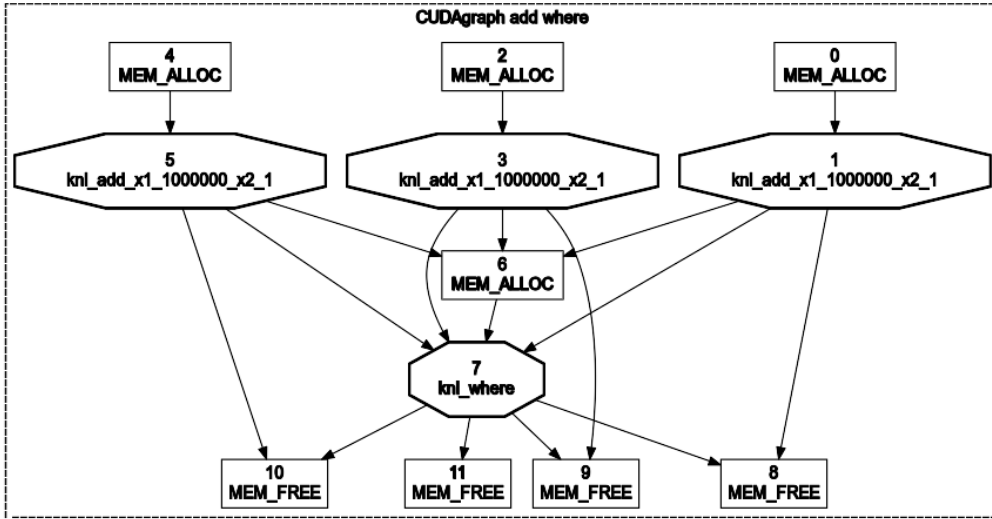


Figure 2. `CUDAGraph` API generated graph for `where(condition, if, else) + 1`

We formulate our system by building a `CUDAGraph`-based PyCUDA target for Pytato’s IR which captures the user-defined DAG. The process is *transparent*. The key technical contributions of our thesis involve:

1. Extending PyCUDA to allow calls to the `CUDAGraph` API
2. Mapping the array operations onto a DAG through Pytato’s IR to generate PyCUDA-`CUDAGraph` code.
3. Providing an evaluation for profitability of `CUDAGraphs` for DG-FEM workloads.

2. RELATED WORK

Castro et al [11] gives an overview of the current task-based Python computing landscape by mentioning PyCOMPs[26], Pygion[25], PyKoKKos[6] and Legion [7] that rely on *decorators*. A decorator is an instruction set before the definition of a function. The decorator function transforms the user function (if applicable) into a parallelization-friendly. PyCOMPs and Pygion both rely on `@task` decorator to dynamically add tasks to the data dependency graph. The scheduling policy is *locality-aware* where the runtime system computes a score

for all of the available resources and chooses the one with the highest score. The score is the number of task input parameters that are already present on that resource, thus minimizing delays between task executions. **Legion** uses a data-centric programming model which relies on *software out-of-order processor* (SOOP), for scheduling tasks which takes locality and independence properties captured by logical regions while making scheduling decisions.

In **Jug** [12] arguments take values or outputs of another tasks and parallelization is achieved by running more than one **Jug** processes for distributing the tasks. In **Pydron**[21], decorated functions are first translated into an intermediate representation and then analyzed by a scheduler which modifies the execution graph as each task is finished.

Since all of these frameworks rely on explicit tasks declarations, they are not yet able to realise the concurrency available across array operations.

CuPy serves as a drop-in replacement to **Numpy** and targets to **cuBLAS**, **cuDNN** and **cuSPARSE**. **Julia**[9] GPU programming models use **CUDA.jl** to provide high level mechanics to define multidimensional arrays (**CUArray**). Both **CuPy** and **Julia** offer interfaces for *implicit* graph construction which *captures* a **CUDAGraph** by recording all the operations on single or multiple streams. Although capturing all the operations on streams leads to terse application code, staging computations within a user-code with interleaving in-graph and out-of-graph operations cannot be expressed. This can lead to repeated computations of the same sub-graphs.

JAX[10] optimizes GPU performance by translating *high-level traces* into **XLA**[24] **HLO** and then performing vectorization/parallelization and **JIT** compilation. Deep learning (DL) symbolic mathematical libraries such as **TensorFlow**[4] and **PyTorch**[23] allow neural networks to be specified as DAGs along which data is transformed. Both of them follow a delayed execution model where the DAG is built at run time, not at compile-time or eagerly. Each kernel’s historical performance and scheduling is tracked to allow the creation of heuristics that guide future scheduling of the same kernel. The operators are then sequentially scheduled to a single computation stream in the GPU.

Both **StarPU**[5] and **ParSEC**[13] provide excellent support for heterogeneous hardware on distributed systems. Both of them share a number of common features: tasks appear to execute in program order, dependencies between tasks are determined by the arguments supplied to task calls along with the privileges requested by tasks, and tasks can be offloaded to available GPUs (with data movement managed by the system). **ParSEC** in particular uses a DSL compiler to read a program representation (a recursive, algebraic description of a task graph) and generate code to execute the tasks described in the program.

3. OVERVIEW

3.1. CUDA Graphs

CUDAGraphs provide a way to execute a partially ordered set of compute/memory operations on a GPU, compared to the fully ordered **CUDA** streams: a stream in **CUDA** is a queue of copy and compute commands. Within a stream, enqueued operations are executed on the GPU in the same order as they are placed into the stream by the programmer with a single active task at a given instant. Thus, two kernels in the same stream cannot execute in parallel, even without data dependencies. This can lead to underutilization of GPU resources as shown in Fig 1. The solution is to run different **CUDA** streams in parallel through the use of **CUDA** events, which allow streams to synchronize with each other without blocking the host execution. However, using **CUDA** events to efficiently synchronize multiple complex streams by hand can be cumbersome.

CUDAGraphs offer a means to efficiently schedule kernel launches on multiple streams through a user-defined DAG. A CUDAGraph is a set of nodes representing memory/compute operations, connected by edges representing run-after dependencies.

CUDA 10 introduced explicit APIs for creating graphs, e.g. *cuGraphCreate*, to create a graph; *cuGraphAddMemAllocNode*/*cuGraphAddKernelNode*/*cuGraphMemFreeNode*, to add a new node to the graph with the corresponding run-after dependencies with previous nodes to be executed on the GPU; *cuGraphInstantiate*, to create an executable graph in a stream; and a *cuGraphLaunch*, to launch an executable graph. We wrapped this API using PyCUDA which provided a high level Python scripting interface for GPU programming. Table 1. summarizes some of the operations offered by our PyCUDA-CUDAGraph interface.

Operations	PyCUDA routines
Memory Allocation	<code>add_memalloc_node</code>
Kernel Execution	<code>add_kernel_node</code>
Host to Device Copy	<code>add_memcpy_htod_node</code>
Device to Device Copy	<code>add_memcpy_dtod_node</code>
Device to Host Copy	<code>add_memcpy_dtoh_node</code>
Memory Free	<code>add_memfree_node</code>
Graph Creation	<code>Graph</code>
Graph Instantiation	<code>GraphExec</code>
Update ExecGraph arguments	<code>batched_set_kernel_node_arguments</code>
Graph Launch	<code>launch</code>

Table 1. PyCUDA wrapper functions around CUDAGraph API

3.2. Loopy

Loopy[15] is a Python-based transformation toolkit to generate transformed kernels. We make use of the following components in our pipeline to generate performance tuned CUDA kernels:

1. *Loop Domains*: The upper and lower bounds of the result array's memory access pattern in the OpenCL format sourced from the `shape` attribute within `IndexLambda` and expressed using the `isl` library.
2. *Statement*: A set of instructions specified in conjunction with an iteration domain which encodes an assignment to an entry of an array. The right-hand side of an assignment consists of an expression that may consist of arithmetic operations and calls to functions.
3. *Kernel Data*: A sorted list of arguments capturing all of the array node's dependencies.

Algorithm 1: Loopy kernel for doubling operation

```
lp.make_kernel(
    domains = "{[_0]:0<=_0<4}",
    instructions = "out[_0]=2*a[_0]",
    kernel_data = [lp.GlobalArg("out", shape=lp.auto, dtype="float64"),
                   lp.GlobalArg("a", shape=lp.auto, dtype="float64")])
```

3.3. Pytato

Pytato[18] is a lazy-evaluation programming based Python package that offers a Numpy-like frontend for recording array expressions.

Pytato offers an IR which encodes user defined array computations as a DAG where nodes correspond to array operations and edges represent dependencies between inputs/outputs of these operations. In this work, we are interested in the normalized form of Pytato IR, which is comprised of the following two node types:

1. *Placeholder*: A named abstract array whose shape and dtype is known with data supplied during runtime. This permits the automated gathering of a self-contained description of a piece of code without incurring the penalty faced by repeated memory transfers from the device's DRAM to lower levels of cache.
2. *IndexLambda*: Represents an array comprehension recording a scalar expression containing per index value of the array computation. This helps create a generalized

Here's a simple example demonstrating Pytato usage

Algorithm 2: Pytato expression building for doubling operation

```
# CreatePlaceholder node for storing array description
x = pt.make_placeholder(name="x", shape=(4,4), dtype="float64")

# Express array computation as a scalar expression using IndexLambda
result = 2*x
```

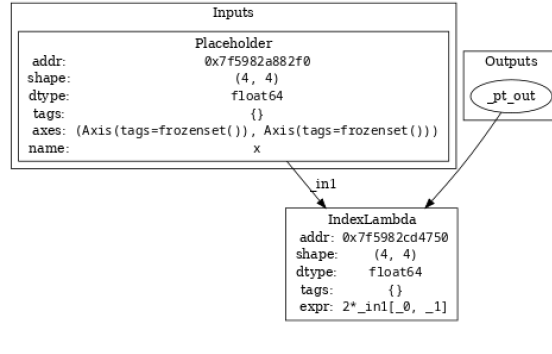


Figure 3. Pytato IR corresponding to doubling operation

4. LOWERING ARRAY OPERATIONS TO CUDAGRAPHS

We make use of lazy evaluation where the definition and submission of work are decoupled. CUDAGraphs follow a delayed execution model where no operations to the GPU are submitted during graph building. This allows the scheduler to be made aware of a defined dependency graph ahead of execution. Since Pytato's computation graph maps precisely onto CUDAGraphs, we implemented a Pytato-CUDAGraph visitor for rewriting Pytato IR expressions. Pytato code is lowered onto CUDAGraph through a two stage process triggered by the `pt.generate_cudagraph` function.

Algorithm 3: Pytato-PyCUDA Graph generated code

```

import pycuda.driver as _pt_drv
import numpy as np
from pycuda.driver import KernelNodeParams as _pt_KernelNodeParams
from pycuda.compiler import SourceModule as _pt_SourceModule
from pycuda import gpuarray as _pt_gpuarray
from functools import cache

# {{{ Create and load kernel module

_pt_mod_0 = _pt_SourceModule("

#define bIdx(N) ((int) blockIdx.N)\n#define tIdx(N) ((int)
threadIdx.N)\n\nextern \"C\" __global__ void __launch_bounds__(16)
knl_mult_x1_1_x2_16(double *__restrict__ out, double const *__restrict__
_in1)\n{\n    int const ibatch = 0;\n    out[4 * (tIdx(x) / 4) +
tIdx(x) + -4 * (tIdx(x) / 4)] = 21 * _in1[4 * (tIdx(x) / 4) + tIdx(x) +
-4 * (tIdx(x) / 4)];\n}\n}

")

# }}}
# {{{ Stage 1: Build and cache CUDAGraph

@cache
def exec_graph_builder():
    _pt_g = _pt_drv.Graph()
    _pt_buffer_acc = {}
    _pt_node_acc = {}
    _pt_memalloc, _pt_array = _pt_g.add_memalloc_node(size=128,
dependencies=[])
    _pt_kernel_0 = _pt_g.add_kernel_node(_pt_array, 139712027164672,
func=_pt_mod_0.get_function('knl_mult_x1_1_x2_16'), block=(16, 1, 1),
grid=(1, 1, 1), dependencies=[_pt_memalloc])
    _pt_buffer_acc['_pt_array'] = _pt_array
    _pt_node_acc['_pt_kernel_0'] = _pt_kernel_0
    _pt_g.add_memfree_node(_pt_array, [_pt_kernel_0])
    return (_pt_g.get_exec_graph(), _pt_g, _pt_node_acc, _pt_buffer_acc)

# }}}
# {{{ Stage 2: Update execution graph

def _pt_kernel(allocator=cuda_allocator, dev=cuda_dev, *, a):
    _pt_result = _pt_gpuarray.GPUArray((4, 4), dtype='float64',
allocator=allocator, dev=dev)
    _pt_exec_g, _pt_g, _pt_node_acc, _pt_buffer_acc =
exec_graph_builder()
    _pt_exec_g.batched_set_kernel_node_arguments(
{_pt_node_acc['_pt_kernel_0']}:
_pt_drv.KernelNodeParams(args=[_pt_result.gpudata, a.gpudata]))
    _pt_exec_g.launch()
    _pt_tmp = {'_pt_out': _pt_result}
    return _pt_tmp['_pt_out'].get()

# }}}

```

4.1. Stage 1: Build **CUDAGraph**

Since the **CUDAGraph** runtime scheduler takes in a fully defined dataflow graph, we use Alg 4 to explore all of the array dependencies in the computation graph. We cache the resultant executable graph since the topology stays constant throughout the computation. This ensures that Alg 4 only gets executed only once during compilation with a $\Theta(V+E)$ complexity for Alg 5.

Algorithm 4: DAG Discovery for building **CUDAGraph**

Input: Pytato array computation graph

Output: `pycuda.Graph` object

Step 1: Initialize a `pycuda.Graph` object.

Step 2:

Output \leftarrow nodes in array computation graph with no successors.

Code $\leftarrow \psi$

ArrayToBuffers $\leftarrow \psi$

for $n \in \textit{Output}$ **do**

 GRAPHTRAVERSE(n , *Code*, *ArrayToBuffers*)

done

Step 3: Instantiate `pycuda.Graph` object and cache the resultant `pycuda.GraphExec` object to avoid triggering graph traversals for subsequent launches.

Algorithm 5: Array computation graph traversal

```

function PLACEHOLDERMAPPER(n, ArrayToBuffers)
    ArrayToBuffers[n]  $\leftarrow$  User provided buffer OR allocate new buffer using GPUArrays
    return ArrayToBuffers
end function

function LOOPYKERNEL(n.expr, n.shape, n.dtype, n.bindings)
    {Returns the kernel string and launch configuration}
end function

function INDEXLAMBDA_MAPPER(n, Code, ArrayToBuffers)
    Insert CUDAGraph memalloc node code for result array
    ArrayToBuffers[n]  $\leftarrow$  Buffer corresponding to allocated result array
    kernelString, grid, block = LOOPYKERNEL(n.expr, n.shape, n.dtype, n.bindings)
    Insert CUDAGraph kernel node code with temporary buffers for bindings into Code
    return Code, ArrayToBuffers
end function

function GRAPHTRAVERSE(n, Code, ArrayToBuffers)
    if n  $\in$  {Placeholder, DataWrapper} {
        ArrayToBuffers  $\leftarrow$  PLACEHOLDERMAPPER(n, ArrayToBuffers)
        return {n}, Code, ArrayToBuffers
    }
    else {
        Code, ArrayToBuffers  $\leftarrow$  INDEXLAMBDA_MAPPER(n, Code, ArrayToBuffers)
        n_deps  $\leftarrow$   $\psi$ 
        bindings  $\leftarrow$  IndexLambda bindings for n
        for c  $\in$  bindings do
            c_deps, Code, ArrayToBuffers  $\leftarrow$  GRAPHTRAVERSE(c, Code, ArrayToBuffers)
            n_deps  $\leftarrow$  n_deps  $\cup$  c_deps
        done
        return n_deps, Code, ArrayToBuffers
    }
end function

```

The `exec_graph_builder` function in Alg. 3 describes the graph building phase. Since arrays are being lazily evaluated during the building phase, all placeholders are replaced with temporary array buffers which are then updated during the execution phase. For every kernel node, the resulting array is allocated using `add_memalloc_node` and array operation is expressed through `add_kernel_node`. Instead of manually searching the parameter space, we generate the kernel string and the launch configuration by passing the IndexLambda scalar expression to Loopy.

4.2. Stage 2: Update CUDAGraphExec

Since the input parameters of the computation graph change with every integration, the corresponding CUDAGraph also changes. To avoid triggering a graph compilation for every

iteration, we use PyCUDA wrappers around *cuGraphExecSetKernelParams* functionality.

Since the graph topology does not change over different iterations, we are able to update the cached executable graph with new kernel parameters. This helps us avoid the expensive instantiation of a new graph. Thus, instead of Alg 4, Alg 6. gets executed for every graph launch. In Alg. 3, this corresponds to the driver calls enclosed in `_pt_kernel`

Algorithm 6: Buffer update in CUDAGraphExec

```

for  $n \in$  kernel nodes in pycuda.GraphExec with temporary buffers do
    • Replace temporary buffers with allocated/linked buffers from corresponding
      Placeholder nodes.
done

```

5. RESULTS

5.1. Experimental Setup

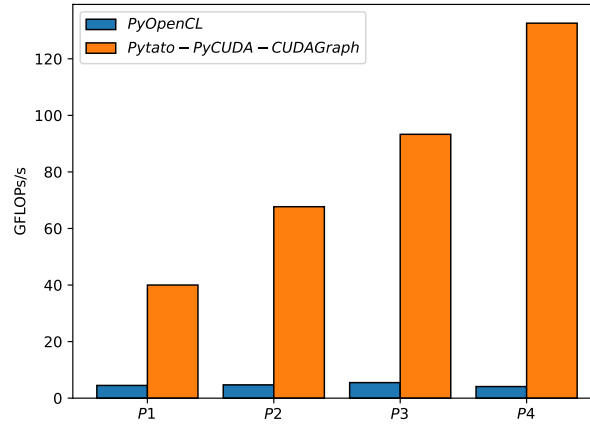
Applications: We demonstrate the performance of our framework on three end-to-end DG-FEM operators: Wave, Euler and Compressible Navier Stokes. We evaluated these operators on 3D meshes with tetrahedral cells. Our experimental parameters have been summarized in Table 2.

Tools: Two types of tools were used: (1) Compilers, NVCC V11 for CUDAGraphs and POCL-CUDA 3.1 for PyOpenCL, and (2) Analysis tools like `nvprof` and `nvvp`.

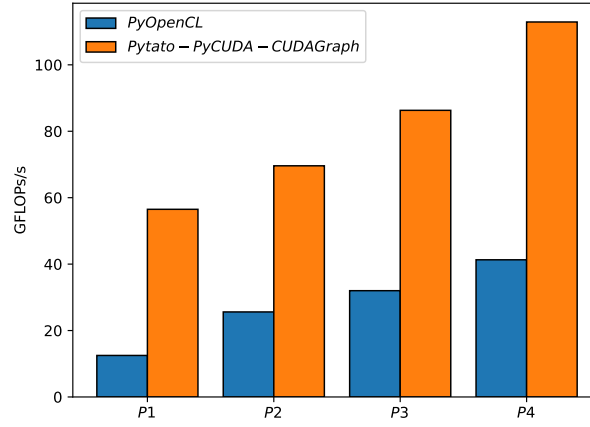
Platform: All of our experiments were performed on GPU NVIDIA TITAN V with 6144 GFLOPs/s peak double precision and 652.8 GB/s peak bandwidth.

Equation	Polynomial degrees	# of tetrahedrons in the mesh
<i>Wave</i>	1	1.25×10^5
	2	5.0×10^4
	3	2.5×10^4
	4	1.4×10^4
<i>Euler</i>	1	3.2768×10^4
	2	1.3284×10^4
	3	6.859×10^3
	4	4.913×10^3
<i>Compressible Navier Stokes</i>	1	8.2944×10^4
	2	4.8000×10^4
	3	2.4576×10^4
	4	1.0368×10^4

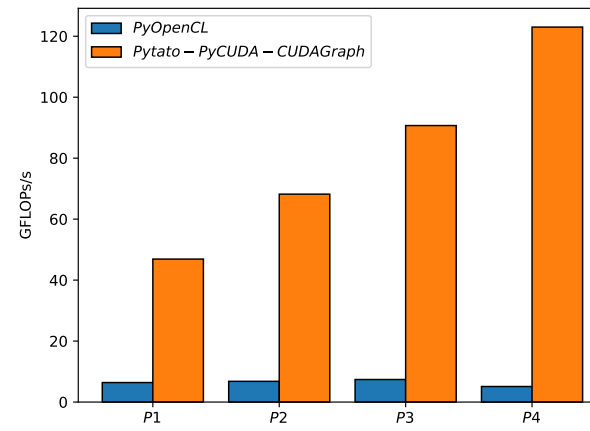
Table 2. Experimental parameters for DG-FEM operators



Wave



Euler



Compressible Navier Stokes

Figure 4. Performance of our framework (Pytato-PyCUDA-CUDAGraph) for DG-FEM operators over sequential stream execution (PyOpenCL).

5.2. Performance Evaluation

Methodology: We measure our speedup over PyOpenCL where the array operations are executed one after the other in a single stream. We used wall clock times for our measurement with 2 seconds being spent in the warmup loop and 5 seconds for the iteration loop.

We report speedups of upto 24x with the resulting performance being closely tied to the polynomial order as reported in [14]. We also note that the performance is largely limited by memory bandwidth. As observed in Fig. 2, the scheduler maximally parallelizes the given CUDAGraph without limiting the stream usage. Thus, in large graphs the GPU memory can explode which in this case prevented us from testing higher mesh discretizations.

6. CONCLUSION

In this work we realized the concurrency available across array operations through NVIDIA’s CUDAGraph task programming model. CUDAGraphs overcome the limitations of single stream execution through a user defined DAG that can be executed on GPUs using multiple streams and low kernel latencies. Firstly, we extended the PyCUDA GPU scripting framework to wrap around the CUDAGraph API. Next, we implemented a pipeline for lowering array operations onto CUDAGraph using Pytato which is a lazy evaluation-based array package. And finally we assessed the profitability of CUDAGraphs for DG-FEM workloads. We evaluated our framework on three end-to-end DG-FEM operators and observed a speedup of upto 24x for Navier Stokes operator over sequential stream execution.

For future work, we plan to come up with a performance model for the scheduling algorithm through a series of microbenchmarks. We will also leverage additional Pytato IR information to generate more optimized Loopy kernels.

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