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Open Core Protocol

The **Open Core Protocol** (**OCP**) is a protocol for on-chip subsystem communications. It is an openly licensed, core-centric protocol and defines a bus-independent, configurable interface. OCP International Partnership (OCP-IP) produces OCP specifications. OCP data transfer models range from simple request-grant handshaking through pipelined request-response to complex out-of-order operations.

Legacy IP cores can be adapted to OCP, while new implementations may take advantage of advanced features: designers select only those features and signals encompassing a core's specific data, control and test configuration.

The Open Core Protocol (OCP) is one of several FPGA processor interconnects used to connect soft FPGA peripherals to FPGA CPUs -- both soft microprocessor and hard-macro processor. Other such interconnects include Advanced eXtensible Interface (AXI), Avalon,[1] and the Wishbone bus.

FPGA vendor Altera joined the Open Core Protocol International Partnership in 2010.[2]

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Advantages

- Eliminates the ongoing task of interface protocol (re)definition, verification, documentation and support
- Readily adapts to support new core capabilities
- Test bench portability simplifies (re)verification
- Limits test suite modifications for core enhancements
- Interfaces to any bus structure or on-chip network
- Delivers industry-standard flexibility and reuse
- Point-to-point protocol can directly interface two cores

Disadvantages

- Neither Altera nor Xilinx, the two largest FPGA vendors, supports this protocol.

References

1. William G. Wong. "Understanding FPGA Processor Interconnects" (https://www.electronicde sign.com/technologies/fpgas/article/21795951/understanding-fpga-processor-interconnects).

2012.
2. "Altera, others join open core protocol group" (https://www.eetimes.com/altera-others-join-open-core-protocol-group/).

External links

- Official website (https://accellera.org/downloads/standards/ocp/) 🖊