WIKIPEDIA

PCI Express

PCI Express (**Peripheral Component Interconnect Express**), officially abbreviated as **PCIe** or **PCI-e**,[1] is a high-speed serial computer expansion bus standard, designed to replace the older PCI, PCI-X and AGP bus standards. It is the common motherboard interface for personal computers' graphics cards, hard disk drive host adapters, SSDs, Wi-Fi and Ethernet hardware connections.[2] PCIe has numerous improvements over the older standards, including higher maximum system bus throughput, lower I/O pin count and smaller physical footprint, better performance scaling for bus devices, a more detailed error detection and reporting mechanism (Advanced Error Reporting, AER),[3] and native hot-swap functionality. More recent revisions of the PCIe standard provide hardware support for I/O virtualization.

The PCI Express electrical interface is measured by the number of simultaneous lanes.[4] (A lane is a single send/receive line of data. The analogy is a highway with traffic in both directions.) The interface is also used in a variety of other standards — most notably the laptop expansion card interface called ExpressCard. It is also used in the storage interfaces of SATA Express, U.2 (SFF-8639) and M.2.

Format specifications are maintained and developed by the PCI-SIG (PCI Special Interest Group) — a group of more than 900 companies that also maintains the conventional PCI specifications.

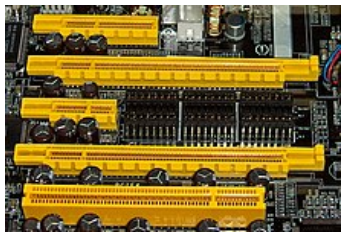
Contents

PCI Express

Peripheral Component Interconnect Express	
 PCI Express logo	
Year created	2003
Created by	Intel · Dell · HP · IBM
Supersedes	AGP · PCI · PCI-X
Width in bits	1 per lane (up to 16 lanes)
No. of devices	1 on each endpoint of each connection.[a]
Speed	Dual simplex (in each direction); examples in single-lane (x1) and 16-lane (x16): **Version 1.x:** 2.5 GT/s **x1:** 250 MB/s **x16:** 4 GB/s **Version 2.x:** 5 GT/s **x1:** 500 MB/s **x16:** 8 GB/s **Version 3.x:** 8 GT/s **x1:** 985 MB/s **x16:** 15.75 GB/s **Version 4.0:** 16 GT/s **x1:** 1.97 GB/s **x16:** 31.5 GB/s **Version 5.0:** 32 GT/s **x1:** 3.94 GB/s **x16:** 63 GB/s **Version 6.0:** 64 GT/s **x1:** 7.56 GB/s **x16:** 121 GB/s **Version 7.0:** 128 GT/s **x1:** 15.13 GB/s

	x16: 242 GB/s
Style	Serial
Hotplugging interface	Yes (with ExpressCard, OCuLink, CFexpress or U.2)
External interface	Yes (with OCuLink or PCI Express External Cabling)
Website	pcisig.com (https://pcisig.com/)

Two types of PCIe slot on an Asus H81M-K motherboard



Various slots on a computer motherboard, from top to bottom:

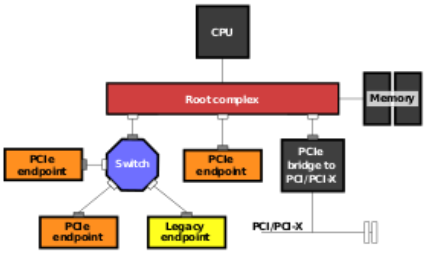
- PCI Express x4
- PCI Express x16
- PCI Express x1
- PCI Express X16
- Conventional PCI (32-bit, 5 V)

Architecture

Conceptually, the PCI Express bus is a high-speed serial replacement of the older PCI/PCI-X bus.[7] One of the key differences between the PCI Express bus and the older PCI is the bus topology; PCI uses a shared parallel bus architecture, in which the PCI host and all devices share a common set of address, data and control lines. In contrast, PCI Express is based on point-to-point topology, with separate serial links connecting every device to the root complex (host). Because of its shared bus topology, access to the older PCI bus is arbitrated (in the case of multiple masters), and limited to one master at a time, in a single direction. Furthermore, the older PCI clocking scheme limits the bus clock to the slowest peripheral on the bus (regardless of the devices involved in the bus transaction). In contrast, a PCI Express bus link supports full-duplex communication between any two endpoints, with no inherent limitation on concurrent access across multiple endpoints.

In terms of bus protocol, PCI Express communication is encapsulated in packets. The work of packetizing and de-packetizing data and status-message traffic is handled by the transaction layer of the PCI Express port (described later). Radical differences in electrical signaling and bus protocol require the use of a different mechanical form factor and expansion connectors (and thus, new motherboards and new adapter boards); PCI slots and PCI Express slots are not interchangeable. At the software level, PCI Express preserves backward compatibility with PCI; legacy PCI system software can detect and configure newer PCI Express devices without explicit support for the PCI Express standard, though new PCI Express features are inaccessible.

The PCI Express link between two devices can vary in size from one to 16 lanes. In a multi-lane link, the packet data is striped across lanes, and peak data throughput scales with the overall link width. The lane count is automatically negotiated during device initialization, and can be restricted by either endpoint. For example, a single-lane PCI Express (x1) card can be inserted into a multi-lane slot (x4, x8, etc.), and the initialization cycle auto-negotiates the highest mutually supported lane count. The link can dynamically down-configure itself to use fewer lanes, providing a failure tolerance in case bad or unreliable lanes are present. The PCI Express standard defines link widths of x1, x2, x4, x8 and x16. Up to and including PCIe 5.0, x12 and x32 links were defined as well but never used.[8] This allows the PCI Express bus to serve both cost-sensitive applications where high throughput is not needed, and performance-critical applications such as 3D graphics, networking (10 Gigabit Ethernet or multiport Gigabit Ethernet), and enterprise storage (SAS or Fibre Channel). Slots and connectors are only defined for a subset of these widths, with link widths in between using the next larger physical slot size.



Example of the PCI Express topology: white "junction boxes" represent PCI Express device downstream ports, while the gray ones represent upstream ports.[5]:7

As a point of reference, a PCI-X (133 MHz 64-bit) device and a PCI Express 1.0 device using four lanes (x4) have roughly the same peak single-direction transfer rate of 1064 MB/s. The PCI Express bus has the potential to perform better than the PCI-X bus in cases where multiple devices are transferring data simultaneously, or if communication with the PCI Express peripheral is bidirectional.

Interconnect

PCI Express devices communicate via a logical connection called an *interconnect*[9] or *link*. A link is a point-to-point communication channel between two PCI Express ports allowing both of them to send and receive ordinary PCI requests (configuration, I/O or memory read/write) and interrupts (INTx, MSI or MSI-X). At the physical level, a link is composed of one or more *lanes*.[9] Low-speed peripherals (such as an 802.11 Wi-Fi card) use a single-lane (x1) link, while a graphics adapter typically uses a much wider and therefore faster 16-lane (x16) link.

Lane

A lane is composed of two differential signaling pairs, with one pair for receiving data and the other for transmitting. Thus, each lane is composed of four wires or signal traces. Conceptually, each lane is used as a full-duplex byte stream, transporting data packets in eight-bit "byte" format simultaneously in both directions between endpoints of a link.[10] Physical PCI Express links may contain 1, 4, 8 or 16 lanes.[11][5]:4,5[9] Lane counts are written with an "x" prefix (for example, "x8" represents an eight-lane card or slot), with x16 being the largest size in common use.[12] Lane sizes are also referred to via the terms "width" or "by" e.g., an eight-lane slot could be referred to as a "by 8" or as "8 lanes wide."

For mechanical card sizes, see below.

PCI Express x1 card containing a PCI Express switch (covered by a small heat sink), which creates multiple endpoints out of one endpoint and lets multiple devices share it

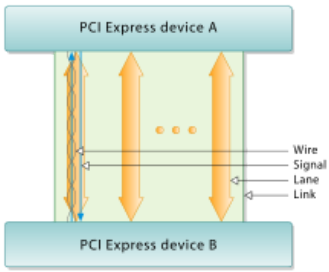
Serial bus

The bonded serial bus architecture was chosen over the traditional parallel bus because of inherent limitations of the latter, including half-duplex operation, excess signal count, and inherently lower bandwidth due to timing skew. Timing skew results from separate electrical signals within a parallel interface traveling through conductors of different lengths, on potentially different printed circuit board (PCB) layers, and at possibly different signal velocities. Despite being transmitted simultaneously as a single word, signals on a parallel interface have different travel duration and arrive at their destinations at different times. When the interface clock period is shorter than the largest time difference between signal arrivals, recovery of the transmitted word is no longer possible. Since timing skew over a parallel bus can amount to a few nanoseconds, the resulting bandwidth limitation is in the range of hundreds of megahertz.

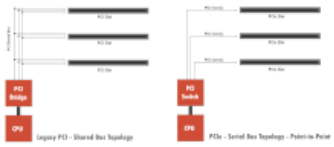
A serial interface does not exhibit timing skew because there is only one differential signal in each direction within each lane, and there is no external clock signal since clocking information is embedded within the serial signal itself. As such, typical bandwidth limitations on serial signals are in the multi-gigahertz range. PCI Express is one example of the general trend toward replacing parallel buses with serial interconnects; other examples include Serial ATA (SATA), USB, Serial Attached SCSI (SAS), FireWire (IEEE 1394), and RapidIO. In digital video, examples in common use are DVI, HDMI and DisplayPort.

Multichannel serial design increases flexibility with its ability to allocate fewer lanes for slower devices.

The PCIe slots on a motherboard are often labelled with the number of PCIe lanes they have. Sometimes what may seem like a large slot may only have a few lanes. For instance an x16 slot with only 4 PCIe lanes is quite common.[6]



A PCI Express link between two devices consists of one or more lanes, which are dual simplex channels using two differential signaling pairs.[5]:3



Highly simplified topologies of the Legacy PCI Shared (Parallel) Interface and the PCIe Serial Point-to-Point Interface[13]

Form factors

PCI Express (standard)

A PCI Express card fits into a slot of its physical size or larger (with x16 as the largest used), but may not fit into a smaller PCI Express slot; for example, a x16 card may not fit into a x4 or x8 slot. Some slots use open-ended sockets to permit physically longer cards and negotiate the best available electrical and logical connection.

The number of lanes actually connected to a slot may also be fewer than the number supported by the physical slot size. An example is a x16 slot that runs at x4, which accepts any x1, x2, x4, x8 or x16 card, but provides only four lanes. Its specification may read as "x16 (x4 mode)", while "mechanical @ electrical" notation (e.g. "x16 @ x4") is also common. The advantage is that such slots can accommodate a larger range of PCI Express cards without requiring motherboard hardware to support the full transfer rate. Standard mechanical sizes are x1, x4, x8, and x16. Cards with a differing number of lanes need to use the next larger mechanical size (i.e. a x2 card uses the x4 size, or a x12 card uses the x16 size).

The cards themselves are designed and manufactured in various sizes. For example, solid-state drives (SSDs) that come in the form of PCI Express cards often use HHHL (half height, half length) and FHHL (full height, half length) to describe the physical dimensions of the card.[14][15]

PCI card type	Dimensions height × length × width, maximum	
	(mm)	(in)
Full-Length	111.15 × 312.00 × 20.32	4.376 × 12.283 × 0.8
Half-Length	111.15 × 167.65 × 20.32	4.376 × 6.600 × 0.8
Low-Profile/Slim	68.90 × 167.65 × 20.32	2.731 × 6.600 × 0.8

Non-standard video card form factors

Intel P3608 NVMe flash SSD, PCI-E add-in card

Modern (since c.2012[16]) gaming video cards usually exceed the height as well as thickness specified in the PCI Express standard, due to the need for more capable and quieter cooling fans, as gaming video cards often emit hundreds of watts of heat.[17] Modern computer cases are often wider to accommodate these taller cards, but not always. Since full-length cards (312 mm) are uncommon, modern cases sometimes cannot fit those. The thickness of these cards also typically occupies the space of 2 PCIe slots. In fact, even the methodology of how to measure the cards varies between vendors, with some including the metal bracket size in dimensions and others not.

For instance, a 2020 Sapphire card measures 135 mm in height (excluding the metal bracket), which exceeds the PCIe standard height by 28 mm.[18] Another card by XFX measures 55 mm thick (i.e. 2.7 PCI slots at 20.32 mm), taking up 3 PCIe slots.[19] The Asus GeForce RTX 3080 10 GB STRIX GAMING OC video card is a two slot card that has dimensions of 318.5 mm × 140.1 mm × 57.8 mm, exceeding PCI Express' maximum length, height and thickness respectively.[20]

Pinout

The following table identifies the conductors on each side of the edge connector on a PCI Express card. The solder side of the printed circuit board (PCB) is the A side, and the component side is the B side.[21] PRSNT1# and PRSNT2# pins must be slightly shorter than the rest, to ensure that a hot-plugged card is fully inserted. The WAKE# pin uses full voltage to wake the computer, but must be pulled high from the standby power to indicate that the card is wake capable.[22]

PCI Express connector pinout (x1, x4, x8 and x16 variants)

Pin	Side B	Side A	Description
1	+12 V	PRSNT1#	Must connect to farthest PRSNT2# pin
2	+12 V	+12 V	Main power pins
3	+12 V	+12 V	
4	Ground	Ground	
5	SMCLK	TCK	SMBus and JTAG port pins
6	SMDAT	TDI	
7	Ground	TDO	
8	+3.3 V	TMS	
9	TRST#	+3.3 V	
10	+3.3 V aux	+3.3 V	Standby power
11	WAKE#	PERST#	Link reactivation; fundamental reset [23]
Key notch			
12	CLKREQ#[24]	Ground	Clock Request Signal
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK−	Lane 0 transmit data, + and −
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and −
17	PRSNT2#	HSIn(0)	
18	Ground	Ground	
PCI Express x1 cards end at pin 18			
19	HSOp(1)	Reserved	Lane 1 transmit data, + and −
20	HSOn(1)	Ground	
21	Ground	HSIp(1)	Lane 1 receive data, + and −
22	Ground	HSIn(1)	
23	HSOp(2)	Ground	Lane 2 transmit data, + and −
24	HSOn(2)	Ground	
25	Ground	HSIp(2)	Lane 2 receive data, + and −
26	Ground	HSIn(2)	
27	HSOp(3)	Ground	Lane 3 transmit data, + and −
28	HSOn(3)	Ground	
29	Ground	HSIp(3)	Lane 3 receive data, + and −
30	PWRBRK#[25]	HSIn(3)	
31	PRSNT2#	Ground	
32	Ground	Reserved	
PCI Express x4 cards end at pin 32			
33	HSOp(4)	Reserved	Lane 4 transmit data, + and −
34	HSOn(4)	Ground	
35	Ground	HSIp(4)	Lane 4 receive data, + and −
36	Ground	HSIn(4)	
37	HSOp(5)	Ground	Lane 5 transmit data, + and −
38	HSOn(5)	Ground	
39	Ground	HSIp(5)	Lane 5 receive data, + and −
40	Ground	HSIn(5)	
41	HSOp(6)	Ground	Lane 6 transmit data, + and −
42	HSOn(6)	Ground	
43	Ground	HSIp(6)	Lane 6 receive data, + and −
44	Ground	HSIn(6)	
45	HSOp(7)	Ground	Lane 7 transmit data, + and −

Pin	Side B	Side A	Description
50	HSOp(8)	Reserved	Lane 8 transmit data, + and −
51	HSOn(8)	Ground	
52	Ground	HSIp(8)	Lane 8 receive data, + and −
53	Ground	HSIn(8)	
54	HSOp(9)	Ground	Lane 9 transmit data, + and −
55	HSOn(9)	Ground	
56	Ground	HSIp(9)	Lane 9 receive data, + and −
57	Ground	HSIn(9)	
58	HSOp(10)	Ground	Lane 10 transmit data, + and −
59	HSOn(10)	Ground	
60	Ground	HSIp(10)	Lane 10 receive data, + and −
61	Ground	HSIn(10)	
62	HSOp(11)	Ground	Lane 11 transmit data, + and −
63	HSOn(11)	Ground	
64	Ground	HSIp(11)	Lane 11 receive data, + and −
65	Ground	HSIn(11)	
66	HSOp(12)	Ground	Lane 12 transmit data, + and −
67	HSOn(12)	Ground	
68	Ground	HSIp(12)	Lane 12 receive data, + and −
69	Ground	HSIn(12)	
70	HSOp(13)	Ground	Lane 13 transmit data, + and −
71	HSOn(13)	Ground	
72	Ground	HSIp(13)	Lane 13 receive data, + and −
73	Ground	HSIn(13)	
74	HSOp(14)	Ground	Lane 14 transmit data, + and −
75	HSOn(14)	Ground	
76	Ground	HSIp(14)	Lane 14 receive data, + and −
77	Ground	HSIn(14)	
78	HSOp(15)	Ground	Lane 15 transmit data, + and −
79	HSOn(15)	Ground	
80	Ground	HSIp(15)	Lane 15 receive data, + and −
81	PRSNT2#	HSIn(15)	
82	Reserved	Ground	

Legend	
Ground pin	Zero volt reference
Power pin	Supplies power to the PCIe card

46	HSOn(7)	Ground	
47	Ground	HSIp(7)	Lane 7 receive data, + and −
48	PRSNT2#	HSIn(7)	
49	Ground	Ground	
PCI Express x8 cards end at pin 49			

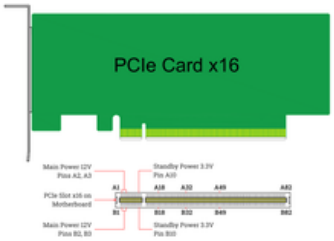
Card-to-host pin	Signal from the card to the motherboard
Host-to-card pin	Signal from the motherboard to the card
Open drain	May be pulled low or sensed by multiple cards
Sense pin	Tied together on card
Reserved	Not presently used, do not connect

Power

8-pin (left) and 6-pin (right) power connectors used on PCI Express cards

All PCI express cards may consume up to 3 A at +3.3 V (9.9 W). The amount of +12 V and total power they may consume depends on the type of card:[26]:35–36[27]

- x1 cards are limited to 0.5 A at +12 V (6 W) and 10 W combined.
- x4 and wider cards are limited to 2.1 A at +12 V (25 W) and 25 W combined.
- A full-sized x1 card may draw up to the 25 W limits after initialization and software configuration as a "high power device".
- A full-sized x16 graphics card[22] may draw up to 5.5 A at +12 V (66 W) and 75 W combined after initialization and software configuration as a "high power device".



The main 12V power supply for the PCIe slot is pins B2, B3 (side B) and pins A2, A3 (side A). Power standby 3.3V is pin B10 and A10. PCIe card x1 supplies up to 25W and x16 is 75W combined.[28]

Optional connectors add 75 W (6-pin) or 150 W (8-pin) of +12 V power for up to 300 W total (2 × 75 W + 1 × 150 W).

- Sense0 pin is connected to ground by the cable or power supply, or float on board if cable is not connected.
- Sense1 pin is connected to ground by the cable or power supply, or float on board if cable is not connected.

Some cards use two 8-pin connectors, but this has not been standardized yet as of 2018, therefore such cards must not carry the official PCI Express logo. This configuration allows 375 W total (1 × 75 W + 2 × 150 W) and will likely be standardized by PCI-SIG with the PCI Express 4.0 standard. The 8-pin PCI Express connector could be confused with the EPS12V connector, which is mainly used for powering SMP and multi-core systems. The power connectors are variants of the Molex Mini-Fit Jr. series connectors. [29]

Molex Mini-Fit Jr. part numbers[29]

Pins	Female/receptacle on PS cable	Male/right-angle header on PCB
6-pin	45559-0002	45558-0003
8-pin	45587-0004	45586-0005, 45586-0006

6-pin power connector (75 W)[30]	
Pin	**Description**
1	+12 V
2	Not connected (usually +12 V as well)
3	+12 V
4	Ground
5	Sense
6	Ground

8-pin power connector (150 W)[31][32][33]	
Pin	**Description**
1	+12 V
2	+12 V
3	+12 V
4	Sense1 (8-pin connected[A])
5	Ground
6	Sense0 (6-pin or 8-pin connected)
7	Ground
8	Ground

6 pin power connector pin map

8 pin power connector pin map

A. When a 6-pin connector is plugged into an 8-pin receptacle the card is notified by a missing *Sense1* that it may only use up to 75 W.

PCI Express Mini Card

PCI Express Mini Card (also known as **Mini PCI Express**, **Mini PCIe**, **Mini PCI-E**, **mPCIe**, and **PEM**), based on PCI Express, is a replacement for the Mini PCI form factor. It is developed by the PCI-SIG. The host device supports both PCI Express and USB 2.0 connectivity, and each card may use either standard. Most laptop computers built after 2005 use PCI Express for expansion cards; however, as of 2015, many vendors are moving toward using the newer M.2 form factor for this purpose.

Due to different dimensions, PCI Express Mini Cards are not physically compatible with standard full-size PCI Express slots; however, passive adapters exist that let them be used in full-size slots.[34]

A WLAN PCI Express Mini Card and its connector

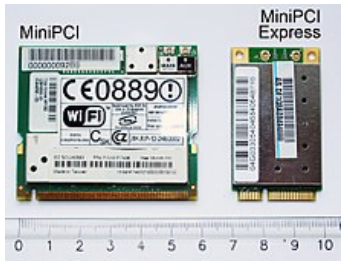
Physical dimensions

Dimensions of PCI Express Mini Cards are 30 mm × 50.95 mm (width × length) for a Full Mini Card. There is a 52-pin edge connector, consisting of two staggered rows on a 0.8 mm pitch. Each row has eight contacts, a gap equivalent to four contacts, then a further 18 contacts. Boards have a thickness of 1.0 mm, excluding the components. A "Half Mini Card" (sometimes abbreviated as HMC) is also specified, having approximately half the physical length of 26.8 mm.

Electrical interface

PCI Express Mini Card edge connectors provide multiple connections and buses:

- PCI Express x1 (with SMBus)
- USB 2.0
- Wires to diagnostics LEDs for wireless network (i.e., Wi-Fi) status on computer's chassis
- SIM card for GSM and WCDMA applications (UIM signals on spec.)
- Future extension for another PCIe lane
- 1.5 V and 3.3 V power



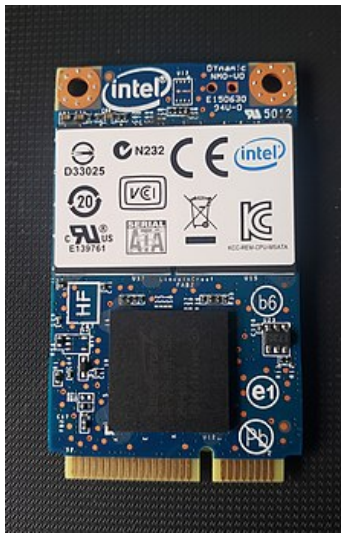
MiniPCI and MiniPCI Express cards in comparison

Mini-SATA (mSATA) variant

Despite sharing the Mini PCI Express form factor, an mSATA slot is not necessarily electrically compatible with Mini PCI Express. For this reason, only certain notebooks are compatible with mSATA drives. Most compatible systems are based on Intel's Sandy Bridge processor architecture, using the Huron River platform. Notebooks such as Lenovo's ThinkPad T, W and X series, released in March–April 2011, have support for an mSATA SSD card in their WWAN card slot. The ThinkPad Edge E220s/E420s, and the Lenovo IdeaPad Y460/Y560/Y570/Y580 also support mSATA.[35] On the contrary, the L-series among others can only support M.2 cards using the PCIe standard in the WWAN slot.

Some notebooks (notably the Asus Eee PC, the Apple MacBook Air, and the Dell mini9 and mini10) use a variant of the PCI Express Mini Card as an SSD. This variant uses the reserved and several non-reserved pins to implement SATA and IDE interface passthrough, keeping only USB, ground lines, and sometimes the core PCIe x1 bus intact.[36] This makes the "miniPCIe" flash and solid-state drives sold for netbooks largely incompatible with true PCI Express Mini implementations.

Also, the typical Asus miniPCIe SSD is 71 mm long, causing the Dell 51 mm model to often be (incorrectly) referred to as half length. A true 51 mm Mini PCIe SSD was announced in 2009, with two stacked PCB layers that allow for higher storage capacity. The announced design preserves the PCIe interface, making it compatible with the standard mini PCIe slot. No working product has yet been developed.



An Intel mSATA SSD

Intel has numerous desktop boards with the PCIe x1 Mini-Card slot that typically do not support mSATA SSD. A list of desktop boards that natively support mSATA in the PCIe x1 Mini-Card slot (typically multiplexed with a SATA port) is provided on the Intel Support site.[37]

PCI Express M.2

M.2 replaces the mSATA standard and Mini PCIe.[38] Computer bus interfaces provided through the M.2 connector are PCI Express 3.0 (up to four lanes), Serial ATA 3.0, and USB 3.0 (a single logical port for each of the latter two). It is up to the manufacturer of the M.2 host or device to choose which interfaces to support, depending on the desired level of host support and device type.

PCI Express External Cabling

PCI Express External Cabling (also known as *External PCI Express*, *Cabled PCI Express*, or *ePCIe*) specifications were released by the PCI-SIG in February 2007.[39][40]

Standard cables and connectors have been defined for x1, x4, x8, and x16 link widths, with a transfer rate of 250 MB/s per lane. The PCI-SIG also expects the norm to evolve to reach 500 MB/s, as in PCI Express 2.0. An example of the uses of Cabled PCI Express is a metal enclosure, containing a number of PCIe slots and PCIe-to-ePCIe adapter circuitry. This device would not be possible had it not been for the ePCIe specification.

PCI Express OCuLink

OCuLink (standing for "optical-copper link", since *Cu* is the chemical symbol for Copper) is an extension for the "cable version of PCI Express", acting as a competitor to version 3 of the Thunderbolt interface. Version 1.0 of OCuLink, released in Oct 2015, supports up to PCIe 3.0 x4 lanes (8 GT/s, 3.9 GB/s) over copper cabling; a fiber optic version may appear in the future.

In its latest version OCuLink-2, it supports up to 16 GB/s (PCIe 4.0 x8)[41] while the maximum bandwidth of a full speed Thunderbolt 4 cable is 5 GB/s. Some suppliers may design their connector product to be able to support next generation PCI Express 5.0 running at 32 GT/s per lane for future proofing and minimizing development costs over the next few years.[41] Initially, PCI-SIG expected to bring OCuLink into laptops for connection of powerful external GPU boxes. It turned out to be a rare use. Instead, OCuLink became popular for PCIe interconnections in servers.[42]

Derivative forms

Numerous other form factors use, or are able to use, PCIe. These include:

- Low-height card
- ExpressCard: Successor to the PC Card form factor (with x1 PCIe and USB 2.0; hot-pluggable)
- PCI Express ExpressModule: A hot-pluggable modular form factor defined for servers and workstations
- XQD card: A PCI Express-based flash card standard by the CompactFlash Association with x2 PCIe
- CFexpress card: A PCI Express-based flash card by the CompactFlash Association in three form factors supporting 1 to 4 PCIe lanes
- SD card: The SD Express bus, introduced in version 7.0 of the SD specification uses an x1 PCIe link
- XMC: Similar to the CMC/PMC form factor (VITA 42.3)
- AdvancedTCA: A complement to CompactPCI for larger applications; supports serial based backplane topologies
- AMC: A complement to the AdvancedTCA specification; supports processor and I/O modules on ATCA boards (x1, x2, x4 or x8 PCIe).
- FeaturePak: A tiny expansion card format (43 mm × 65 mm) for embedded and small-form-factor applications, which implements two x1 PCIe links on a high-density connector along with USB, I2C, and up to 100 points of I/O
- Universal IO: A variant from Super Micro Computer Inc designed for use in low-profile rack-mounted chassis.[43] It has the connector bracket reversed so it cannot fit in a normal PCI Express socket, but it is pin-compatible and may be inserted if the bracket is removed.
- M.2 (formerly known as NGFF)
- M-PCIe brings PCIe 3.0 to mobile devices (such as tablets and smartphones), over the M-PHY physical layer.[44][45]
- U.2 (formerly known as SFF-8639)

The PCIe slot connector can also carry protocols other than PCIe. Some 9xx series Intel chipsets support Serial Digital Video Out, a proprietary technology that uses a slot to transmit video signals from the host CPU's integrated graphics instead of PCIe, using a supported add-in.

The PCIe transaction-layer protocol can also be used over some other interconnects, which are not electrically PCIe:

- Thunderbolt: A royalty-free interconnect standard by Intel that combines DisplayPort and PCIe protocols in a form factor compatible with Mini DisplayPort. Thunderbolt 3.0 also combines USB 3.1 and uses the USB-C form factor as opposed to Mini DisplayPort.
- USB4

History and revisions

While in early development, PCIe was initially referred to as *HSI* (for *High Speed Interconnect*), and underwent a name change to *3GIO* (for *3rd Generation I/O*) before finally settling on its PCI-SIG name *PCI Express*. A technical working group named the *Arapaho Work Group* (AWG) drew up the standard. For initial drafts, the AWG consisted only of Intel engineers; subsequently, the AWG expanded to include industry partners.

Since, PCIe has undergone several large and smaller revisions, improving on performance and other features.

PCI Express link performance[46][47]

Version	Intro-duced	Line code		Transfer rate per lane[i][ii]	Throughput[i][iii]				
					x1	x2	x4	x8	x16
1.0	2003	NRZ	8b/10b	2.5 GT/s	0.250 GB/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s
2.0	2007			5.0 GT/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s	8.000 GB/s
3.0	2010		128b/130b	8.0 GT/s	0.985 GB/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s
4.0	2017			16.0 GT/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s
5.0	2019			32.0 GT/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s	63.015 GB/s
6.0	2022	PAM-4 FEC	242B/256B FLIT	64.0 GT/s 32.0 GBd	7.563 GB/s	15.125 GB/s	30.250 GB/s	60.500 GB/s	121.000 GB/s
7.0	2025 (planned)			128.0 GT/s 64.0 GBd	15.125 GB/s	30.250 GB/s	60.500 GB/s	121.000 GB/s	242.000 GB/s

Notes

i. In each direction (each lane is a dual simplex channel).
ii. Transfer rate refers to the encoded serial bit rate; 2.5 GT/s means 2.5 Gbit/s serial data rate.
iii. Throughput indicates the unencoded bandwidth (without 8b/10b, 128b/130b, or 242B/256B encoding overhead). The PCIe 1.0 transfer rate of 2.5 GT/s per lane means a 2.5 Gbit/s serial bit rate corresponding to a throughput of 2.0 Gbit/s or 250 MB/s prior to 8b/10b encoding.

PCI Express 1.0a

In 2003, PCI-SIG introduced PCIe 1.0a, with a per-lane data rate of 250 MB/s and a transfer rate of 2.5 gigatransfers per second (GT/s).

Transfer rate is expressed in transfers per second instead of bits per second because the number of transfers includes the overhead bits, which do not provide additional throughput;[48] PCIe 1.x uses an 8b/10b encoding scheme, resulting in a 20% (= 2/10) overhead on the raw channel bandwidth.[49] So in the PCIe terminology, transfer rate refers to the encoded bit rate: 2.5 GT/s is 2.5 Gbps on the encoded serial link. This corresponds to 2.0 Gbps of pre-coded data or 250 MB/s, which is referred to as throughput in PCIe.

PCI Express 1.1

In 2005, PCI-SIG[50] introduced PCIe 1.1. This updated specification includes clarifications and several improvements, but is fully compatible with PCI Express 1.0a. No changes were made to the data rate.

PCI Express 2.0

PCI-SIG announced the availability of the PCI Express Base 2.0 specification on 15 January 2007.[51] The PCIe 2.0 standard doubles the transfer rate compared with PCIe 1.0 to 5 GT/s and the per-lane throughput rises from 250 MB/s to 500 MB/s. Consequently, a 16-lane PCIe connector (x16) can support an aggregate throughput of up to 8 GB/s.

A PCI Express 2.0 expansion card that provides USB 3.0 connectivity.[b]

PCIe 2.0 motherboard slots are fully backward compatible with PCIe v1.x cards. PCIe 2.0 cards are also generally backward compatible with PCIe 1.x motherboards, using the available bandwidth of PCI Express 1.1. Overall, graphic cards or motherboards designed for v2.0 work, with the other being v1.1 or v1.0a.

The PCI-SIG also said that PCIe 2.0 features improvements to the point-to-point data transfer protocol and its software architecture.[52]

Intel's first PCIe 2.0 capable chipset was the X38 and boards began to ship from various vendors (Abit, Asus, Gigabyte) as of 21 October 2007.[53] AMD started supporting PCIe 2.0 with its AMD 700 chipset series and nVidia started with the MCP72.[54] All of Intel's prior chipsets, including the Intel P35 chipset, supported PCIe 1.1 or 1.0a.[55]

Like 1.x, PCIe 2.0 uses an 8b/10b encoding scheme, therefore delivering, per-lane, an effective 4 Gbit/s max. transfer rate from its 5 GT/s raw data rate.

PCI Express 2.1

PCI Express 2.1 (with its specification dated 4 March 2009) supports a large proportion of the management, support, and troubleshooting systems planned for full implementation in PCI Express 3.0. However, the speed is the same as PCI Express 2.0. The increase in power from the slot breaks backward compatibility between PCI Express 2.1 cards and some older motherboards with 1.0/1.0a, but most motherboards with PCI Express 1.1 connectors are provided with a BIOS update by their manufacturers through utilities to support backward compatibility of cards with PCIe 2.1.

PCI Express 3.0

PCI Express 3.0 Base specification revision 3.0 was made available in November 2010, after multiple delays. In August 2007, PCI-SIG announced that PCI Express 3.0 would carry a bit rate of 8 gigatransfers per second (GT/s), and that it would be backward compatible with existing PCI Express implementations. At that time, it was also announced that the final specification for PCI Express 3.0 would be delayed until Q2 2010.[56] New features for the PCI Express 3.0 specification included a number of optimizations for enhanced signaling and data integrity, including transmitter and receiver equalization, PLL improvements, clock data recovery, and channel enhancements of currently supported topologies.[57]

Following a six-month technical analysis of the feasibility of scaling the PCI Express interconnect bandwidth, PCI-SIG's analysis found that 8 gigatransfers per second could be manufactured in mainstream silicon process technology, and deployed with existing low-cost materials and infrastructure, while maintaining full compatibility (with negligible impact) with the PCI Express protocol stack.

PCI Express 3.0 upgraded the encoding scheme to 128b/130b from the previous 8b/10b encoding, reducing the bandwidth overhead from 20% of PCI Express 2.0 to approximately 1.54% (= 2/130). PCI Express 3.0's 8 GT/s bit rate effectively delivers 985 MB/s per lane, nearly doubling the lane bandwidth relative to PCI Express 2.0.[47]

On 18 November 2010, the PCI Special Interest Group officially published the finalized PCI Express 3.0 specification to its members to build devices based on this new version of PCI Express.[58]

PCI Express 3.1

In September 2013, PCI Express 3.1 specification was announced for release in late 2013 or early 2014, consolidating various improvements to the published PCI Express 3.0 specification in three areas: power management, performance and functionality.[45][59] It was released in November 2014.[60]

PCI Express 4.0

On 29 November 2011, PCI-SIG preliminarily announced PCI Express 4.0,[61] providing a 16 GT/s bit rate that doubles the bandwidth provided by PCI Express 3.0 to 31.5 GB/s in each direction for a 16-lane configuration, while maintaining backward and forward compatibility in both software support and used mechanical interface.[62] PCI Express 4.0 specs also bring OCuLink-2, an alternative to Thunderbolt. OCuLink version 2 has up to 16 GT/s (16 GB/s total for x8 lanes),[41] while the maximum bandwidth of a Thunderbolt 3 link is 5 GB/s.

In June 2016 Cadence, PLDA and Synopsys demoed PCIe 4.0 physical-layer, controller, switch and other IP blocks at the PCI SIG's annual developer's conference.[63]

Mellanox Technologies announced the first 100 Gbit/s network adapter with PCIe 4.0 on 15 June 2016,[64] and the first 200 Gbit/s network adapter with PCIe 4.0 on 10 November 2016.[65]

In August 2016, Synopsys presented a test setup with FPGA clocking a lane to PCIe 4.0 speeds at the Intel Developer Forum. Their IP has been licensed to several firms planning to present their chips and products at the end of 2016.[66]

On the IEEE Hot Chips Symposium in August 2016 IBM announced the first CPU with PCIe 4.0 support, POWER9.[67][68]

PCI-SIG officially announced the release of the final PCI Express 4.0 specification on 8 June 2017.[69] The spec includes improvements in flexibility, scalability, and lower-power.

On 5 December 2017 IBM announced the first system with PCIe 4.0 slots, Power AC922.[70][71]

NETINT Technologies introduced the first NVMe SSD based on PCIe 4.0 on 17 July 2018, ahead of Flash Memory Summit 2018[72]

AMD announced on 9 January 2019 its upcoming Zen 2-based processors and X570 chipset would support PCIe 4.0.[73] AMD had hoped to enable partial support for older chipsets, but instability caused by motherboard traces not conforming to PCIe 4.0 specifications made that impossible.[74][75]

Intel released their first mobile CPUs with PCI express 4.0 support in mid-2020, as a part of the Tiger Lake microarchitecture.[76]

PCI Express 5.0

In June 2017, PCI-SIG announced the PCI Express 5.0 preliminary specification.[69] Bandwidth was expected to increase to 32 GT/s, yielding 63 GB/s in each direction in a 16-lane configuration. The draft spec was expected to be standardized in 2019. Initially, 25.0 GT/s was also considered for technical feasibility.

On 7 June 2017 at PCI-SIG DevCon, Synopsys recorded the first demonstration of PCI Express 5.0 at 32 GT/s.[77]

On 31 May 2018, PLDA announced the availability of their XpressRICH5 PCIe 5.0 Controller IP based on draft 0.7 of the PCIe 5.0 specification on the same day.[78][79]

On 10 December 2018, the PCI SIG released version 0.9 of the PCIe 5.0 specification to its members,[80] and on 17 January 2019, PCI SIG announced the version 0.9 had been ratified, with version 1.0 targeted for release in the first quarter of 2019.[81]

On 29 May 2019, PCI-SIG officially announced the release of the final PCI Express 5.0 specification.[82]

On 20 November 2019, Jiangsu Huacun presented the first PCIe 5.0 Controller HC9001 in a 12 nm manufacturing process.[83] Production started in 2020.

On 17 August 2020, IBM announced the POWER10 processor with PCIe 5.0 and up to 32 lanes per single-chip module (SCM) and up to 64 lanes per double-chip module (DCM).[84]

On 9 September 2021, IBM announced the Power E1080 Enterprise server with planned availability date 17 September.[85] It can have up to 16 POWER10 SCMs with maximum of 32 slots per system which can act as PCIe 5.0 x8 or PCIe 4.0 x16.[86] Alternatively they can be used as PCIe 5.0 x16 slots for optional optical CXP converter adapters connecting to external PCIe expansion drawers.

On 27 October 2021, Intel announced the 12th Gen Intel Core CPU family, the world's first consumer x86-64 processors with PCIe 5.0 (up to 16 lanes) connectivity.[87]

On 22 March 2022, Nvidia announced Nvidia Hopper GH100 GPU, the world's first PCIe 5.0 GPU.[88]

On 23 May 2022, AMD announced its Zen 4 architecture with support for up to 24 lanes of PCIe 5.0 connectivity on consumer platforms.[89]

PCI Express 6.0

On 18 June 2019, PCI-SIG announced the development of PCI Express 6.0 specification. Bandwidth is expected to increase to 64 GT/s, yielding 128 GB/s in each direction in a 16-lane configuration, with a target release date of 2021.[90] The new standard uses 4-level pulse-amplitude modulation (PAM-4) with a low-latency forward error correction (FEC) in place of non-return-to-zero (NRZ) modulation.[91] Unlike previous PCI Express versions, forward error correction is used to increase data integrity and PAM-4 is used as line code so that two bits are transferred per transfer. With 64 GT/s data transfer rate (raw bit rate), up to 121 GB/s in each direction is possible in x16 configuration.[90]

On 24 February 2020, the PCI Express 6.0 revision 0.5 specification (a "first draft" with all architectural aspects and requirements defined) was released.[92]

On 5 November 2020, the PCI Express 6.0 revision 0.7 specification (a "complete draft" with electrical specifications validated via test chips) was released.[93]

On 6 October 2021, the PCI Express 6.0 revision 0.9 specification (a "final draft") was released.[94]

On 11 January 2022, PCI-SIG officially announced the release of the final PCI Express 6.0 specification.[95]

PAM-4 coding results in a vastly higher bit error rate (BER) of 10^{-6} (vs. 10^{-12} previously), so in place of 128b/130b encoding, a 3-way interlaced forward error correction (FEC) is used in addition to cyclic redundancy check (CRC). A fixed 256 byte Flow Control Unit (FLIT) block carries 242 bytes of data, which includes variable-sized transaction level packets (TLP) and data link layer payload (DLLP); remaining 14 bytes are reserved for 8-byte CRC and 6-byte FEC. [96][97] 3-way Gray code is used in PAM-4/FLIT mode to reduce error rate; the interface does not switch to NRZ and 128/130b encoding even when retraining to lower data rates.[98][99]

PCI Express 7.0

On 21 June 2022, PCI-SIG announced the development of PCI Express 7.0 specification.[100] It will deliver 128 GT/s raw bit rate and up to 242 GB/s per direction in x16 configuration, using the same PAM4 signaling as version 6.0. Doubling of the data rate will be achieved by fine-tuning channel parameters to decrease signal losses and improve power efficiency. The specification is expected to be finalised in 2025.

Extensions and future directions

Some vendors offer PCIe over fiber products,[101][102][103] with active optical cables (AOC) for PCIe switching at increased distance in PCIe expansion drawers,[104][86] or in specific cases where transparent PCIe bridging is preferable to using a more mainstream standard (such as InfiniBand or Ethernet) that may require additional software to support it.

Thunderbolt was co-developed by Intel and Apple as a general-purpose high speed interface combining a logical PCIe link with DisplayPort and was originally intended as an all-fiber interface, but due to early difficulties in creating a consumer-friendly fiber interconnect, nearly all implementations are copper systems. A notable exception, the Sony VAIO Z VPC-Z2, uses a nonstandard USB port with an optical component to connect to an outboard PCIe display adapter. Apple has been the primary driver of Thunderbolt adoption through 2011, though several other vendors[105] have announced new products and systems featuring Thunderbolt. Thunderbolt 3 forms the basis of the USB4 standard.

Mobile PCIe specification (abbreviated to *M-PCIe*) allows PCI Express architecture to operate over the MIPI Alliance's M-PHY physical layer technology. Building on top of already existing widespread adoption of M-PHY and its low-power design, Mobile PCIe lets mobile devices use PCI Express.[106]

Draft process

There are 5 primary releases/checkpoints in a PCI-SIG specification:[107]

- Draft 0.3 (Concept): this release may have few details, but outlines the general approach and goals.
- Draft 0.5 (First draft): this release has a complete set of architectural requirements and must fully address the goals set out in the 0.3 draft.
- Draft 0.7 (Complete draft): this release must have a complete set of functional requirements and methods defined, and no new functionality may be added to the specification after this release. Before the release of this draft, electrical specifications must have been validated via test silicon.
- Draft 0.9 (Final draft): this release allows PCI-SIG member companies to perform an internal review for intellectual property, and no functional changes are permitted after this draft.
- 1.0 (Final release): this is the final and definitive specification, and any changes or enhancements are through Errata documentation and Engineering Change Notices (ECNs) respectively.

Historically, the earliest adopters of a new PCIe specification generally begin designing with the Draft 0.5 as they can confidently build up their application logic around the new bandwidth definition and often even start developing for any new protocol features. At the Draft 0.5 stage, however, there is still a strong likelihood of changes in the actual PCIe protocol layer implementation, so designers responsible for developing these blocks internally may be more hesitant to begin work than those using interface IP from external sources.

Hardware protocol summary

The PCIe link is built around dedicated unidirectional couples of serial (1-bit), point-to-point connections known as *lanes*. This is in sharp contrast to the earlier PCI connection, which is a bus-based system where all the devices share the same bidirectional, 32-bit or 64-bit parallel bus.

PCI Express is a layered protocol, consisting of a *transaction layer*, a *data link layer*, and a *physical layer*. The Data Link Layer is subdivided to include a media access control (MAC) sublayer. The Physical Layer is subdivided into logical and electrical sublayers. The Physical logical-sublayer contains a physical coding sublayer (PCS). The terms are borrowed from the IEEE 802 networking protocol model.

Physical layer

The PCIe Physical Layer (*PHY*, *PCIEPHY*, *PCI Express PHY*, or *PCIe PHY*) specification is divided into two sub-layers, corresponding to electrical and logical specifications. The logical sublayer is sometimes further divided into a MAC sublayer and a PCS, although this division is not formally part of the PCIe specification. A specification published by Intel, the PHY Interface for PCI Express (PIPE),[109] defines the MAC/PCS functional partitioning and the interface between these two sub-layers. The PIPE specification also identifies the *physical media attachment* (PMA) layer, which includes the serializer/deserializer (SerDes) and other analog circuitry; however, since SerDes implementations vary greatly among ASIC vendors, PIPE does not specify an interface between the PCS and PMA.

Connector pins and lengths

Lanes	Pins		Length	
	Total	Variable	Total	Variable
x1	2×18 = 36[108]	2× 7 = 14	25 mm	7.65 mm
x4	2×32 = 64	2×21 = 42	39 mm	21.65 mm
x8	2×49 = 98	2×38 = 76	56 mm	38.65 mm
x16	2×82 = 164	2×71 = 142	89 mm	71.65 mm

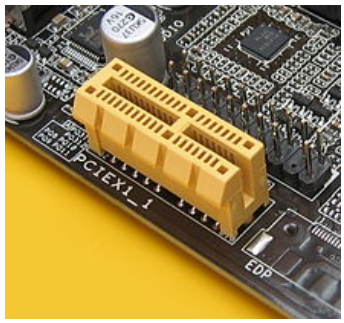
At the electrical level, each lane consists of two unidirectional differential pairs operating at 2.5, 5, 8, 16 or 32 Gbit/s, depending on the negotiated capabilities. Transmit and receive are separate differential pairs, for a total of four data wires per lane.

A connection between any two PCIe devices is known as a *link*, and is built up from a collection of one or more *lanes*. All devices must minimally support single-lane (x1) link. Devices may optionally support wider links composed of up to 32 lanes.[110][111] This allows for very good compatibility in two ways:

- A PCIe card physically fits (and works correctly) in any slot that is at least as large as it is (e.g., an x1 sized card works in any sized slot);
- A slot of a large physical size (e.g., x16) can be wired electrically with fewer lanes (e.g., x1, x4, x8, or x12) as long as it provides the ground connections required by the larger physical slot size.

In both cases, PCIe negotiates the highest mutually supported number of lanes. Many graphics cards, motherboards and BIOS versions are verified to support x1, x4, x8 and x16 connectivity on the same connection.

The width of a PCIe connector is 8.8 mm, while the height is 11.25 mm, and the length is variable. The fixed section of the connector is 11.65 mm in length and contains two rows of 11 pins each (22 pins total), while the length of the other section is variable depending on the number of lanes. The pins are spaced at 1 mm intervals, and the thickness of the card going into the connector is 1.6 mm.[112][113]



An open-end PCI Express x1 connector lets longer cards that use more lanes be plugged while operating at x1 speeds

Data transmission

PCIe sends all control messages, including interrupts, over the same links used for data. The serial protocol can never be blocked, so latency is still comparable to conventional PCI, which has dedicated interrupt lines. When the problem of IRQ sharing of pin based interrupts is taken into account and the fact that message signaled interrupts (MSI) can bypass an I/O APIC and be delivered to the CPU directly, MSI performance ends up being substantially better. [114]

Data transmitted on multiple-lane links is interleaved, meaning that each successive byte is sent down successive lanes. The PCIe specification refers to this interleaving as *data striping*. While requiring significant hardware complexity to synchronize (or deskew) the incoming striped data, striping can significantly reduce the latency of the n^{th} byte on a link. While the lanes are not tightly synchronized, there is a limit to the *lane to lane skew* of 20/8/6 ns for 2.5/5/8 GT/s so the hardware buffers can re-align the striped data.[115] Due to padding requirements, striping may not necessarily reduce the latency of small data packets on a link.

As with other high data rate serial transmission protocols, the clock is embedded in the signal. At the physical level, PCI Express 2.0 utilizes the 8b/10b encoding scheme[47] (line code) to ensure that strings of consecutive identical digits (zeros or ones) are limited in length. This coding was used to prevent the receiver from losing track of where the bit edges are. In this coding scheme every eight (uncoded) payload bits of data are replaced with 10 (encoded) bits of transmit data, causing a 20% overhead in the electrical bandwidth. To improve the available bandwidth, PCI Express version 3.0 instead uses 128b/130b encoding (1.54% overhead). Line encoding limits the run length of identical-digit strings in data streams and ensures the receiver stays synchronised to the transmitter via clock recovery.

A desirable balance (and therefore spectral density) of 0 and 1 bits in the data stream is achieved by XORing a known binary polynomial as a "scrambler" to the data stream in a feedback topology. Because the scrambling polynomial is known, the data can be recovered by applying the XOR a second time. Both the scrambling and descrambling steps are carried out in hardware.

Data link layer

The data link layer performs three vital services for the PCIe link:

1. sequence the transaction layer packets (TLPs) that are generated by the transaction layer,
2. ensure reliable delivery of TLPs between two endpoints via an acknowledgement protocol (ACK and NAK signaling) that explicitly requires replay of unacknowledged/bad TLPs,
3. initialize and manage flow control credits

On the transmit side, the data link layer generates an incrementing sequence number for each outgoing TLP. It serves as a unique identification tag for each transmitted TLP, and is inserted into the header of the outgoing TLP. A 32-bit cyclic redundancy check code (known in this context as Link CRC or LCRC) is also appended to the end of each outgoing TLP.

On the receive side, the received TLP's LCRC and sequence number are both validated in the link layer. If either the LCRC check fails (indicating a data error), or the sequence-number is out of range (non-consecutive from the last valid received TLP), then the bad TLP, as well as any TLPs received after the bad TLP, are considered invalid and discarded. The receiver sends a negative acknowledgement message (NAK) with the sequence-number of the invalid TLP, requesting re-transmission of all TLPs forward of that sequence-number. If the received TLP passes the LCRC check and has the correct sequence number, it is treated as valid. The link receiver increments the sequence-number (which tracks the last received good TLP), and forwards the valid TLP to the receiver's transaction layer. An ACK message is sent to remote transmitter, indicating the TLP was successfully received (and by extension, all TLPs with past sequence-numbers.)

If the transmitter receives a NAK message, or no acknowledgement (NAK or ACK) is received until a timeout period expires, the transmitter must retransmit all TLPs that lack a positive acknowledgement (ACK). Barring a persistent malfunction of the device or transmission medium, the link-layer presents a reliable connection to the transaction layer, since the transmission protocol ensures delivery of TLPs over an unreliable medium.

In addition to sending and receiving TLPs generated by the transaction layer, the data-link layer also generates and consumes data link layer packets (DLLPs). ACK and NAK signals are communicated via DLLPs, as are some power management messages and flow control credit information (on behalf of the transaction layer).

In practice, the number of in-flight, unacknowledged TLPs on the link is limited by two factors: the size of the transmitter's replay buffer (which must store a copy of all transmitted TLPs until the remote receiver ACKs them), and the flow control credits issued by the receiver to a transmitter. PCI Express requires all receivers to issue a minimum number of credits, to guarantee a link allows sending PCIConfig TLPs and

message TLPs.

Transaction layer

PCI Express implements split transactions (transactions with request and response separated by time), allowing the link to carry other traffic while the target device gathers data for the response.

PCI Express uses credit-based flow control. In this scheme, a device advertises an initial amount of credit for each received buffer in its transaction layer. The device at the opposite end of the link, when sending transactions to this device, counts the number of credits each TLP consumes from its account. The sending device may only transmit a TLP when doing so does not make its consumed credit count exceed its credit limit. When the receiving device finishes processing the TLP from its buffer, it signals a return of credits to the sending device, which increases the credit limit by the restored amount. The credit counters are modular counters, and the comparison of consumed credits to credit limit requires modular arithmetic. The advantage of this scheme (compared to other methods such as wait states or handshake-based transfer protocols) is that the latency of credit return does not affect performance, provided that the credit limit is not encountered. This assumption is generally met if each device is designed with adequate buffer sizes.

PCIe 1.x is often quoted to support a data rate of 250 MB/s in each direction, per lane. This figure is a calculation from the physical signaling rate (2.5 gigabaud) divided by the encoding overhead (10 bits per byte). This means a sixteen lane (x16) PCIe card would then be theoretically capable of 16x250 MB/s = 4 GB/s in each direction. While this is correct in terms of data bytes, more meaningful calculations are based on the usable data payload rate, which depends on the profile of the traffic, which is a function of the high-level (software) application and intermediate protocol levels.

Like other high data rate serial interconnect systems, PCIe has a protocol and processing overhead due to the additional transfer robustness (CRC and acknowledgements). Long continuous unidirectional transfers (such as those typical in high-performance storage controllers) can approach >95% of PCIe's raw (lane) data rate. These transfers also benefit the most from increased number of lanes (x2, x4, etc.) But in more typical applications (such as a USB or Ethernet controller), the traffic profile is characterized as short data packets with frequent enforced acknowledgements.[116] This type of traffic reduces the efficiency of the link, due to overhead from packet parsing and forced interrupts (either in the device's host interface or the PC's CPU). Being a protocol for devices connected to the same printed circuit board, it does not require the same tolerance for transmission errors as a protocol for communication over longer distances, and thus, this loss of efficiency is not particular to PCIe.

Efficiency of the link

As for any "network like" communication links, some of the "raw" bandwidth is consumed by protocol overhead:[117]

A PCIe 1.x lane for example offers a data rate on top of the physical layer of 250 MB/s (simplex). This isn't the payload bandwidth but the physical layer bandwidth – a PCIe lane has to carry additional information for full functionality.[117]

Gen 2 Transaction Layer Packet[117]:3

Layer	PHY	Data Link Layer	Transaction			Data Link Layer	PHY
Data	Start	Sequence	Header	Payload	ECRC	LCRC	End
Size (Bytes)	1	2	12 or 16	0 to 4096	4 (optional)	4	1

The Gen2 overhead is then 20, 24, or 28 bytes per transaction.

Gen 3 Transaction Layer Packet[117]:3

Layer	G3 PHY	Data Link Layer	Transaction Layer			Data Link Layer
Data	Start	Sequence	Header	Payload	ECRC	LCRC
Size (Bytes)	4	2	12 or 16	0 to 4096	4 (optional)	4

The Gen3 overhead is then 22, 26 or 30 bytes per transaction.

The $\textbf{Packet Efficiency} = \frac{\textbf{Payload}}{(\textbf{Payload} + \textbf{Overhead})}$ for a 128 byte payload is 86%, and 98% for a 1024 byte payload. For small accesses like register settings (4 bytes), the efficiency drops as low as 16%.

The maximum payload size (MPS) is set on all devices based on smallest maximum on any device in the chain. If one device has an MPS of 128 bytes, *all* devices of the tree must set their MPS to 128 bytes. In this case the bus will have a peak efficiency of 86% for writes.[117]:3

Applications

PCI Express operates in consumer, server, and industrial applications, as a motherboard-level interconnect (to link motherboard-mounted peripherals), a passive backplane interconnect and as an expansion card interface for add-in boards.

In virtually all modern (as of 2012) PCs, from consumer laptops and desktops to enterprise data servers, the PCIe bus serves as the primary motherboard-level interconnect, connecting the host system-processor with both integrated peripherals (surface-mounted ICs) and add-on peripherals (expansion cards). In most of these systems, the PCIe bus co-exists with one or more legacy PCI buses, for backward compatibility with the large body of legacy PCI peripherals.

Asus Nvidia GeForce GTX 650 Ti, a PCI Express 3.0 x16 graphics card

As of 2013, PCI Express has replaced AGP as the default interface for graphics cards on new systems. Almost all models of graphics cards released since 2010 by AMD (ATI) and Nvidia use PCI Express. Nvidia uses the high-bandwidth data transfer of PCIe for its Scalable Link Interface (SLI) technology, which allows multiple graphics cards of the same chipset and model number to run in tandem, allowing increased performance. AMD has also developed a multi-GPU system based on PCIe called CrossFire. AMD, Nvidia, and Intel have released motherboard chipsets that support as many as four PCIe x16 slots, allowing tri-GPU and quad-GPU card configurations.

External GPUs

The Nvidia GeForce GTX 1070, a PCI Express 3.0 x16 Graphics card

Theoretically, external PCIe could give a notebook the graphics power of a desktop, by connecting a notebook with any PCIe desktop video card (enclosed in its own external housing, with a power supply and cooling); this is possible with an ExpressCard or Thunderbolt interface. An ExpressCard interface provides bit rates of 5 Gbit/s (0.5 GB/s throughput), whereas a Thunderbolt interface provides bit rates of up to 40 Gbit/s (5 GB/s throughput).

In 2006, Nvidia developed the Quadro Plex external PCIe family of GPUs that can be used for advanced graphic applications for the professional market.[118] These video cards require a PCI Express x8 or x16 slot for the host-side card, which connects to the Plex via a VHDCI carrying eight PCIe lanes.[119]

Intel 82574L Gigabit Ethernet NIC, a PCI Express x1 card

In 2008, AMD announced the ATI XGP technology, based on a proprietary cabling system that is compatible with PCIe x8 signal transmissions.[120] This connector is available on the Fujitsu Amilo and the Acer Ferrari One notebooks. Fujitsu launched their AMILO GraphicBooster enclosure for XGP soon thereafter.[121] Around 2010 Acer launched the Dynavivid graphics dock for XGP.[122]

In 2010 external card hubs were introduced that can connect to a laptop or desktop through a PCI ExpressCard slot. These hubs can accept full-sized graphics cards. Examples include MSI GUS,[123] Village Instrument's ViDock,[124] the Asus XG Station, Bplus PE4H V3.2 adapter,[125] as well as more improvised DIY devices.[126] However such solutions are limited by the size (often only x1) and version of the available PCIe slot on a laptop.

A Marvell-based SATA 3.0 controller, as a PCI Express x1 card

The Intel Thunderbolt interface has provided a new option to connect with a PCIe card externally. Magma has released the ExpressBox 3T, which can hold up to three PCIe cards (two at x8 and one at x4).[127] MSI also released the Thunderbolt GUS II, a PCIe chassis dedicated for video cards.[128] Other products such as the Sonnet's Echo Express[129] and mLogic's mLink are Thunderbolt PCIe chassis in a smaller form factor.[130]

In 2017, more fully featured external card hubs were introduced, such as the Razer Core, which has a full-length PCIe x16 interface.[131]

Storage devices

An OCZ RevoDrive SSD, a full-height x4 PCI Express card

The PCI Express protocol can be used as data interface to flash memory devices, such as memory cards and solid-state drives (SSDs).

The XQD card is a memory card format utilizing PCI Express, developed by the CompactFlash Association, with transfer rates of up to 1GB/s.[132]

Many high-performance, enterprise-class SSDs are designed as PCI Express RAID controller cards. Before NVMe was standardized, many of these cards utilized proprietary interfaces and custom drivers to communicate with the operating system; they had much higher transfer rates (over 1 GB/s) and IOPS (over one million I/O operations per second) when compared to Serial ATA or SAS drives.[133][134] For example, in 2011 OCZ and Marvell co-developed a native PCI Express solid-state drive controller for a PCI Express 3.0 x16 slot with maximum capacity of 12 TB and a performance of to 7.2 GB/s sequential transfers and up to 2.52 million IOPS in random transfers.[135]

SATA Express was an interface for connecting SSDs through SATA-compatible ports, optionally providing multiple PCI Express lanes as a pure PCI Express connection to the attached storage device.[136] M.2 is a specification for internally mounted computer expansion cards and associated connectors, which also uses multiple PCI Express lanes.[137]

PCI Express storage devices can implement both AHCI logical interface for backward compatibility, and NVM Express logical interface for much faster I/O operations provided by utilizing internal parallelism offered by such devices. Enterprise-class SSDs can also implement SCSI over PCI Express.[138]

Cluster interconnect

Certain data-center applications (such as large computer clusters) require the use of fiber-optic interconnects due to the distance limitations inherent in copper cabling. Typically, a network-oriented standard such as Ethernet or Fibre Channel suffices for these applications, but in some cases the overhead introduced by routable protocols is undesirable and a lower-level interconnect, such as InfiniBand, RapidIO, or NUMAlink is needed. Local-bus standards such as PCIe and HyperTransport can in principle be used for this purpose,[139] but as of 2015, solutions are only available from niche vendors such as Dolphin ICS, and TTTech Auto.

Competing protocols

Other communications standards based on high bandwidth serial architectures include InfiniBand, RapidIO, HyperTransport, Intel QuickPath Interconnect, and the Mobile Industry Processor Interface (MIPI). The differences are based on the trade-offs between flexibility and extensibility vs latency and overhead. For example, making the system hot-pluggable, as with Infiniband but not PCI Express, requires that software track network topology changes.

Another example is making the packets shorter to decrease latency (as is required if a bus must operate as a memory interface). Smaller packets mean packet headers consume a higher percentage of the packet, thus decreasing the effective bandwidth. Examples of bus protocols designed for this purpose are RapidIO and HyperTransport.

PCI Express falls somewhere in the middle, targeted by design as a system interconnect (local bus) rather than a device interconnect or routed network protocol. Additionally, its design goal of software transparency constrains the protocol and raises its latency somewhat.

Delays in PCIe 4.0 implementations led to the Gen-Z consortium, the CCIX effort and an open Coherent Accelerator Processor Interface (CAPI) all being announced by the end of 2016.[140]

On 11 March 2019, Intel presented Compute Express Link (CXL), a new interconnect bus, based on the PCI Express 5.0 physical layer infrastructure. The initial promoters of the CXL specification included: Alibaba, Cisco, Dell EMC, Facebook, Google, HPE, Huawei, Intel and Microsoft.[141]

Integrators list

The PCI-SIG Integrators List lists products made by PCI-SIG member companies that have passed compliance testing. The list include switches, bridges, NICs, SSDs, etc.[142]

See also

- Active State Power Management (ASPM)
- Conventional PCI
- PCI configuration space
- PCI-X
- PCI/104-Express
- PCIe/104
- Root complex
- Serial Digital Video Out (SDVO)
- List of device bit rates § Main buses
- UCIe

Notes

a. Switches can create multiple endpoints out of one to allow sharing it with multiple devices.

b. The card's Serial ATA power connector is present because the USB 3.0 ports require more power than the PCI Express bus can supply. More often, a 4-pin Molex power connector is used.

References

1. Mayhew, D.; Krishnan, V. (August 2003). "PCI express and advanced switching: Evolutionary path to building next generation interconnects". *11th Symposium on High Performance Interconnects, 2003. Proceedings*. pp. 21–29. doi:10.1109/CONECT.2003.1231473 (https://doi.org/10.1109%2FCONECT.2003.1231473). ISBN 0-7695-2012-X. S2CID 7456382 (https://api.semanticscholar.org/CorpusID:7456382).
2. "Definition of PCI Express" (https://www.pcmag.com/encyclopedia/term/48998/pci-express). *PCMag*.
3. Zhang, Yanmin; Nguyen, T Long (June 2007). "Enable PCI Express Advanced Error Reporting in the Kernel" (https://web.archive.org/web/20160310074031/https://ols.fedoraproject.org/OLS/Reprints-2007/zhang-Reprint.pdf) (PDF). *Proceedings of the Linux Symposium*. Fedora project. Archived from the original (https://ols.fedoraproject.org/OLS/Reprints-2007/zhang-Reprint.pdf) (PDF) on 10 March 2016. Retrieved 8 May 2012.

4. https://www.hyperstone.com Flash Memory Form Factors – The Fundamentals of Reliable Flash Storage, Retrieved 19 April 2018
5. Ravi Budruk (21 August 2007). "PCI Express Basics" (https://web.archive.org/web/20140715120034/http://www.pcisig.com/developers/main/training_materials/get_document?doc_id=4e00a39acaa5c5a8ee44ebb07baba982e5972c67). PCI-SIG. Archived from the original (http://www.pcisig.com/developers/main/training_materials/get_document?doc_id=4e00a39acaa5c5a8ee44ebb07baba982e5972c67) (PDF) on 15 July 2014. Retrieved 15 July 2014.
6. "What are PCIe Slots and Their Uses" (https://pcguide101.com/motherboard/what-are-pcie-slots/). PC Guide 101. 18 May 2021. Retrieved 21 June 2021.
7. "How PCI Express Works" (http://computer.howstuffworks.com/pci-express.htm). *How Stuff Works*. 17 August 2005. Archived (https://web.archive.org/web/20091203053924/http://computer.howstuffworks.com/pci-express.htm) from the original on 3 December 2009. Retrieved 7 December 2009.
8. "4.2.4.9. Link Width and Lane Sequence Negotiation", *PCI Express Base Specification, Revision 2.1.*, 4 March 2009
9. "PCI Express Architecture Frequently Asked Questions" (https://web.archive.org/web/20081113163608/http://www.pcisig.com/news_room/faqs/faq_express/). PCI-SIG. Archived from the original (http://www.pcisig.com/news_room/faqs/faq_express/) on 13 November 2008. Retrieved 23 November 2008.
10. "PCI Express Bus" (https://web.archive.org/web/20071208162241/http://www.interfacebus.com/Design_Connector_PCI_Express.html). *Interface bus*. Archived from the original (http://www.interfacebus.com/Design_Connector_PCI_Express.html) on 8 December 2007. Retrieved 12 June 2010.
11. 32 lanes are defined by the *PCIe Base Specification* up to PCIe 5.0 but there's no card standard in the *PCIe Card Electromechanical Specification* and that lane number was never implemented.
12. "PCI Express – An Overview of the PCI Express Standard" (https://web.archive.org/web/20100105163040/http://zone.ni.com/devzone/cda/tut/p/id/3767). *Developer Zone*. National Instruments. 13 August 2009. Archived from the original (http://zone.ni.com/devzone/cda/tut/p/id/3767) on 5 January 2010. Retrieved 7 December 2009.
13. Qazi, Atif. "What are PCIe Slots?" (https://pcgearlab.com/motherboard/what-are-pcie-slots/). *PC Gear Lab*. Retrieved 8 April 2020.
14. "New PCIe Form Factor Enables Greater PCIe SSD Adoption" (http://www.nvmexpress.org/blog/new-pcie-form-factor-enables-greater-pcie-ssd-adoption/). *NVM Express*. 12 June 2012. Archived (https://web.archive.org/web/20150906180730/http://www.nvmexpress.org/blog/new-pcie-form-factor-enables-greater-pcie-ssd-adoption/) from the original on 6 September 2015.
15. "Memblaze PBlaze4 AIC NVMe SSD Review" (http://www.storagereview.com/memblaze_pblaze4_aic_nvme_ssd_review). *StorageReview*. 21 December 2015.
16. July 2015, Kane Fulton 20 (20 July 2015). "19 graphics cards that shaped the future of gaming" (https://www.techradar.com/news/gaming/19-graphics-cards-that-shaped-the-future-of-gaming-1289666). *TechRadar*.
17. Leadbetter, Richard (16 September 2020). "Nvidia GeForce RTX 3080 review: welcome to the next level" (https://www.eurogamer.net/articles/digitalfoundry-2020-nvidia-geforce-rtx-3080-review). *Eurogamer*.
18. "Sapphire Radeon RX 5700 XT Pulse Review | bit-tech.net" (https://bit-tech.net/reviews/tech/graphics/sapphire-radeon-rx-5700-xt-pulse-review/1/). *bit-tech.net*. Retrieved 26 August 2019.
19. "AMD Radeon™ RX 5700 XT 8GB GDDR6 THICC II – RX-57XT8DFD6" (http://xfxforce.com/en-gb/Products/product-category/amd-radeon-rx-5700xt-8gb-thicc-ii-rx-57xt8dfd6). *xfxforce.com*. Retrieved 25 August 2019.
20. "ROG Strix GeForce RTX 3080 OC Edition 10GB GDDR6X | Graphics Cards" (https://rog.asus.com/graphics-cards/graphics-cards/rog-strix/rog-strix-rtx3080-o10g-gaming-model/spec). *rog.asus.com*.
21. "What is the A side, B side configuration of PCI cards" (https://web.archive.org/web/20111102042843/http://www.adexelec.com/faq.htm#pcikeys). *Frequently Asked Questions*. Adex Electronics. 1998. Archived from the original (http://www.adexelec.com/faq.htm#pcikeys) on 2 November 2011. Retrieved 24 October 2011.
22. *PCI Express Card Electromechanical Specification Revision 2.0*
23. "PCI Express Card Electromechanical Specification Revision 4.0, Version 1.0 (Clean)" (https://members.pcisig.com/wg/PCI-SIG/document/13446).
24. "L1 PM Substates with CLKREQ, Revision 1.0a" (https://pcisig.com/sites/default/files/specification_documents/ECN_L1_PM_Substates_with_CLKREQ_31_May_2013_Rev10a.pdf) (PDF). PCI-SIG. Retrieved 8 November 2018.
25. "Emergency Power Reduction Mechanism with PWRBRK Signal ECN" (https://web.archive.org/web/20181109193739/https://pcisig.com/sites/default/files/specification_documents/Emergency%20Power%20Reduction%20Mechanism%20with%20PWRBRK%20Signal%20ECN.pdf) (PDF). PCI-SIG. Archived from the original (https://pcisig.com/sites/default/files/specification_documents/Emergency%20Power%20Reduction%20Mechanism%20with%20PWRBRK%20Signal%20ECN.pdf) (PDF) on 9 November 2018. Retrieved 8 November 2018.
26. *PCI Express Card Electromechanical Specification Revision 1.1*
27. Schoenborn, Zale (2004), *Board Design Guidelines for PCI Express Architecture* (http://e2e.ti.com/cfs-file/__key/communityserver-discussions-components-files/639/7851.PCIe_5F00_designGuides.pdf#page=19) (PDF), PCI-SIG, pp. 19–21, archived (https://web.archive.org/web/20160327185412/http://e2e.ti.com/cfs-file/__key/communityserver-discussions-components-files/639/7851.PCIe_5F00_designGuides.pdf#page=19) (PDF) from the original on 27 March 2016
28. "Where Does PCIe Cable Go?" (https://greatpcreview.com/guides/where-does-pcie-cables-go/). 16 January 2022. Retrieved 10 June 2022.
29. "Mini-Fit® PCI Express®* Wire to Board Connector System" (https://www.molex.com/pdm_docs/ps/PS-45558-001-001.pdf) (PDF). Retrieved 4 December 2020.
30. *PCI Express x16 Graphics 150W-ATX Specification Revision 1.0*

31. *PCI Express 225 W/300 W High Power Card Electromechanical Specification Revision 1.0*
32. *PCI Express Card Electromechanical Specification Revision 3.0*
33. Yun Ling (16 May 2008). "PCIe Electromechanical Updates" (https://web.archive.org/web/20151105083550/http://kavi.pcisig.com/developers/main/training_materials/get_document?doc_id=fa4ec3357012d69821baa0856011c665ac770768). Archived from the original (http://kavi.pcisig.com/developers/main/training_materials/get_document?doc_id=fa4ec3357012d69821baa0856011c665ac770768) on 5 November 2015. Retrieved 7 November 2015.
34. "MP1: Mini PCI Express / PCI Express Adapter" (http://www.hwtools.net/Adapter/MP1.html). *hwtools.net*. 18 July 2014. Archived (https://web.archive.org/web/20141003233055/http://www.hwtools.net/Adapter/MP1.html) from the original on 3 October 2014. Retrieved 28 September 2014.
35. "mSATA FAQ: A Basic Primer" (http://forum.notebookreview.com/lenovo-ibm/574993-msata-faq-basic-primer.html). Notebook review. Archived (https://web.archive.org/web/20120212164949/http://forum.notebookreview.com/lenovo-ibm/574993-msata-faq-basic-primer.html) from the original on 12 February 2012.
36. "Eee PC Research" (http://beta.ivancover.com/wiki/index.php/Eee_PC_Research). *ivc* (wiki). Archived (https://web.archive.org/web/20100330035948/http://beta.ivancover.com/wiki/index.php/Eee_PC_Research) from the original on 30 March 2010. Retrieved 26 October 2009.
37. "Desktop Board Solid-state drive (SSD) compatibility" (http://www.intel.com/support/motherboards/desktop/sb/CS-032415.htm?wapkw=032415). Intel. Archived (https://web.archive.org/web/20160102233130/http://www.intel.com/support/motherboards/desktop/sb/CS-032415.htm?wapkw=032415) from the original on 2 January 2016.
38. "How to distinguish the differences between M.2 cards | Dell US" (https://www.dell.com/support/article/en-us/sln301626/how-to-distinguish-the-differences-between-m-2-cards?lang=en). *www.dell.com*. Retrieved 24 March 2020.
39. "PCI Express External Cabling 1.0 Specification" (http://www.pcisig.com/specifications/pciexpress/pcie_cabling1.0/). Archived (https://web.archive.org/web/20070210055546/http://www.pcisig.com/specifications/pciexpress/pcie_cabling1.0/) from the original on 10 February 2007. Retrieved 9 February 2007.
40. "PCI Express External Cabling Specification Completed by PCI-SIG" (https://web.archive.org/web/20131126064157/http://www.pcisig.com/news_room/news/press_release/02_07_07). PCI SIG. 7 February 2007. Archived from the original (http://www.pcisig.com/news_room/news/press_release/02_07_07) on 26 November 2013. Retrieved 7 December 2012.
41. "OCuLink connectors and cables support new PCIe standard" (https://web.archive.org/web/20170313215047/http://www.connectortips.com/oculink-connectors-cables-support-new-pcie-standard/). *www.connectortips.com*. Archived from the original (https://www.connectortips.com/oculink-connectors-cables-support-new-pcie-standard/) on 13 March 2017.
42. Mokosiy, Vitaliy (9 October 2020). "Untangling terms: M.2, NVMe, USB-C, SAS, PCIe, U.2, OCuLink" (https://mokosiy.medium.com/untangling-terms-m-2-nvme-usb-c-sas-pcie-6599c044f38e). *Medium*. Retrieved 26 March 2021.
43. "Supermicro Universal I/O (UIO) Solutions" (http://www.supermicro.com/products/nfo/uio.cfm). Supermicro.com. Archived (https://web.archive.org/web/20140324184437/http://www.supermicro.com/products/nfo/uio.cfm) from the original on 24 March 2014. Retrieved 24 March 2014.
44. "Get ready for M-PCIe testing" (http://www.edn.com/design/pc-board/4423319/Get-ready-for-M-PCIe-testing), *PC board design*, EDN
45. "PCI SIG discusses M-PCIe oculink & 4th gen PCIe" (https://www.theregister.co.uk/Print/2013/09/13/pci_sig_discusses_m_pcie_oculink_and_fourth_gen_pcie/), *The Register*, UK, 13 September 2013, archived (https://web.archive.org/web/20170629201006/http://www.theregister.co.uk/Print/2013/09/13/pci_sig_discusses_m_pcie_oculink_and_fourth_gen_pcie/) from the original on 29 June 2017
46. "PCI Express 4.0 Frequently Asked Questions" (https://web.archive.org/web/20140518224913/http://www.pcisig.com/news_room/faqs/FAQ_PCI_Express_4.0/#EQ3). *pcisig.com*. PCI-SIG. Archived from the original (http://www.pcisig.com/news_room/faqs/FAQ_PCI_Express_4.0/#EQ3) on 18 May 2014. Retrieved 18 May 2014.
47. "PCI Express 3.0 Frequently Asked Questions" (https://web.archive.org/web/20140201172536/http://www.pcisig.com/news_room/faqs/pcie3.0_faq/#EQ2). *pcisig.com*. PCI-SIG. Archived from the original (http://www.pcisig.com/news_room/faqs/pcie3.0_faq/#EQ2) on 1 February 2014. Retrieved 1 May 2014.
48. "What does GT/s mean, anyway?" (http://www.tmworld.com/electronics-news/4380071/What-does-GT-s-mean-anyway-). *TM World*. Archived (https://web.archive.org/web/20120814002641/http://www.tmworld.com/electronics-news/4380071/What-does-GT-s-mean-anyway-) from the original on 14 August 2012. Retrieved 7 December 2012.
49. "Deliverable 12.2" (https://web.archive.org/web/20100817201815/http://www.eiscat.se/groups/EISCAT_3D_info/DeliverableWP12.2/preview_popup). SE: Eiscat. Archived from the original (http://www.eiscat.se/groups/EISCAT_3D_info/DeliverableWP12.2/preview_popup) on 17 August 2010. Retrieved 7 December 2012.
50. *PCI SIG* (http://www.pcisig.com/), archived (https://web.archive.org/web/20080706134414/http://pcisig.com/) from the original on 6 July 2008
51. "PCI Express Base 2.0 specification announced" (https://web.archive.org/web/20070304101327/http://www.pcisig.com/news_room/PCIe2_0_Spec_Release_FINAL2.pdf) (PDF) (Press release). PCI-SIG. 15 January 2007. Archived from the original (http://www.pcisig.com/news_room/PCIe2_0_Spec_Release_FINAL2.pdf) (PDF) on 4 March 2007. Retrieved 9 February 2007. — note that in this press release the term *aggregate bandwidth* refers to the sum of incoming and outgoing bandwidth; using this terminology the aggregate bandwidth of full duplex 100BASE-TX is 200 Mbit/s.
52. Smith, Tony (11 October 2006). "PCI Express 2.0 final draft spec published" (http://www.reghardware.co.uk/2006/10/11/pic-sig_posts_pcie_2_final_draft/). *The Register*. Archived (https://web.archive.org/web/20070129121731/http://www.reghardware.co.uk/2006/10/11/pic-sig_posts_pcie_2_final_draft/) from the original on 29 January 2007. Retrieved 9 February 2007.
53. Key, Gary; Fink, Wesley (21 May 2007). "Intel P35: Intel's Mainstream Chipset Grows Up" (http://www.anandtech.com/cpuchipsets/showdoc.aspx?i=2993). AnandTech. Archived (https://web.archive.org/web/20070523055011/http://www.anandtech.com/cpuchipsets/showdoc.aspx?i=2993) from the original on 23 May 2007. Retrieved 21 May 2007.

54. Huynh, Anh (8 February 2007). "NVIDIA "MCP72" Details Unveiled" (https://web.archive.org/web/20070210200616/http://www.dailytech.com/article.aspx?newsid=6021). AnandTech. Archived from the original (http://www.dailytech.com/article.aspx?newsid=6021) on 10 February 2007. Retrieved 9 February 2007.
55. "Intel P35 Express Chipset Product Brief" (http://download.intel.com/products/chipsets/P35/317304.pdf) (PDF). Intel. Archived (https://web.archive.org/web/20070926150158/http://download.intel.com/products/chipsets/P35/317304.pdf) (PDF) from the original on 26 September 2007. Retrieved 5 September 2007.
56. Hachman, Mark (5 August 2009). "PCI Express 3.0 Spec Pushed Out to 2010" (https://www.pcmag.com/article2/0,2817,2351266,00.asp). PC Mag. Archived (https://web.archive.org/web/20140107192535/http://www.pcmag.com/article2/0,2817,2351266,00.asp) from the original on 7 January 2014. Retrieved 7 December 2012.
57. "PCI Express 3.0 Bandwidth: 8.0 Gigatransfers/s" (http://www.extremetech.com/article2/0,1697,2169018,00.asp). ExtremeTech. 9 August 2007. Archived (https://web.archive.org/web/20071024140702/http://www.extremetech.com/article2/0,1697,2169018,00.asp) from the original on 24 October 2007. Retrieved 5 September 2007.
58. "PCI Special Interest Group Publishes PCI Express 3.0 Standard" (https://web.archive.org/web/20101121001048/http://www.xbitlabs.com/news/other/display/20101118151837_PCI_Special_Interest_Group_Publishes_PCI_Express_3_0_Standard.html). X bit labs. 18 November 2010. Archived from the original (http://www.xbitlabs.com/news/other/display/20101118151837_PCI_Special_Interest_Group_Publishes_PCI_Express_3_0_Standard.html) on 21 November 2010. Retrieved 18 November 2010.
59. "PCIe 3.1 and 4.0 Specifications Revealed" (http://www.eteknix.com/pcie-3-1-and-4-0-specifications-revealed/). *eteknix.com*. July 2013. Archived (https://web.archive.org/web/20160201102133/http://www.eteknix.com/pcie-3-1-and-4-0-specifications-revealed/) from the original on 1 February 2016.
60. "Trick or Treat… PCI Express 3.1 Released!" (http://blogs.synopsys.com/expressyourself/2014/11/12/trick-or-treat-pci-express-3-1-released/). *synopsys.com*. Archived (https://web.archive.org/web/20150323193106/https://blogs.synopsys.com/expressyourself/2014/11/12/trick-or-treat-pci-express-3-1-released/) from the original on 23 March 2015.
61. "PCI Express 4.0 evolution to 16 GT/s, twice the throughput of PCI Express 3.0 technology" (https://web.archive.org/web/20121223043627/http://www.pcisig.com/news_room/Press_Releases/November_29_2011_Press_Release_/) (press release). PCI-SIG. 29 November 2011. Archived from the original (http://www.pcisig.com/news_room/Press_Releases/November_29_2011_Press_Release_/) on 23 December 2012. Retrieved 7 December 2012.
62. "Frequently Asked Questions | PCI-SIG" (https://web.archive.org/web/20161020040106/https://pcisig.com/faq?field_category_value%5B%5D=pci_express_4.0). *pcisig.com*. Archived from the original (https://pcisig.com/faq?field_category_value%5B%5D=pci_express_4.0#4415) on 20 October 2016.
63. "PCIe 4.0 Heads to Fab, 5.0 to Lab" (http://www.eetimes.com/document.asp?doc_id=1330006). *EE Times*. 26 June 2016. Archived (https://web.archive.org/web/20160828221858/http://www.eetimes.com/document.asp?doc_id=1330006) from the original on 28 August 2016. Retrieved 27 August 2016.
64. "Mellanox Announces ConnectX-5, the Next Generation of 100G InfiniBand and Ethernet Smart Interconnect Adapter | NVIDIA" (https://www.mellanox.com/news/press_release/mellanox-announces-connectx-5-next-generation-100g-infiniband-and-ethernet-smart-interconnect). *www.mellanox.com*.
65. "Mellanox Announces 200Gb/s HDR InfiniBand Solutions Enabling Record Levels of Performance and Scalability | NVIDIA" (https://www.mellanox.com/news/press_release/mellanox-announces-200gbs-hdr-infiniband-solutions-enabling-record-levels-performance-and). *www.mellanox.com*.
66. "IDF: PCIe 4.0 läuft, PCIe 5.0 in Arbeit" (http://www.heise.de/newsticker/meldung/IDF-PCIe-4-0-laeuft-PCIe-5-0-in-Arbeit-3297114.html). *Heise Online* (in German). 18 August 2016. Archived (https://web.archive.org/web/20160819153631/http://www.heise.de/newsticker/meldung/IDF-PCIe-4-0-laeuft-PCIe-5-0-in-Arbeit-3297114.html) from the original on 19 August 2016. Retrieved 18 August 2016.
67. Brian Thompto, POWER9 Processor for the Cognitive Era (https://old.hotchips.org/wp-content/uploads/hc_archives/hc28/HC28.23-Tuesday-Epub/HC28.23.90-High-Perform-Epub/HC28.23.921-.POWER9-Thompto-IBM-final.pdf)
68. 2016 IEEE Hot Chips 28 Symposium (HCS), 21–23 Aug. 2016 (https://ieeexplore.ieee.org/xpl/conhome/7932734/proceeding)
69. Born, Eric (8 June 2017). "PCIe 4.0 specification finally out with 16 GT/s on tap" (https://techreport.com/news/32064/pcie-4-0-specification-finally-out-with-16-gt-s-on-tap). Tech Report. Archived (https://web.archive.org/web/20170608155216/http://techreport.com/news/32064/pcie-4-0-specification-finally-out-with-16-gt-s-on-tap) from the original on 8 June 2017. Retrieved 8 June 2017.
70. "IBM Unveils Most Advanced Server for AI" (https://www-03.ibm.com/press/us/en/pressrelease/53452.wss). *www-03.ibm.com*. 5 December 2017.
71. IBM Power System AC922 (8335-GTG) server helps you to harness breakthrough accelerated AI, HPDA, and HPC performance for faster time to insight, IBM Europe Hardware Announcement ZG17-0147 (https://www.ibm.com/common/ssi/ShowDoc.wss?docURL=/common/ssi/rep_ca/7/877/ENUSZG17-0147/index.html)
72. "NETINT Introduces Codensity with Support for PCIe 4.0 – NETINT Technologies" (https://www.netint.ca/blog/netint-introduces-codensity-with-support-for-pcie-4-0/). *NETINT Technologies*. 17 July 2018. Retrieved 28 September 2018.
73. Mujtaba, Hassan (9 January 2019). "AMD Ryzen 3000 Series CPUs Based on Zen 2 Launching in Mid of 2019" (https://wccftech.com/amd-ryzen-3000-zen-2-desktop-am4-processors-launching-mid-2019/).
74. Alcorn, Paul (3 June 2019). "AMD Nixes PCIe 4.0 Support on Older Socket AM4 Motherboards, Here's Why" (https://www.tomshardware.com/news/amd-pcie-4.0-socket-am4-motherboard,39559.html). *Tom's Hardware*. Archived (https://archive.today/20190610025155/https://www.tomshardware.com/news/amd-pcie-4.0-socket-am4-motherboard,39559.html) from the original on 10 June 2019. Retrieved 10 June 2019.

75. Alcorn, Paul (10 January 2019). "PCIe 4.0 May Come to all AMD Socket AM4 Motherboards (Updated)" (https://www.tomshardware.com/news/amd-ryzen-pcie-4.0-motherboard,38401.html). *Tom's Hardware*. Archived (https://archive.today/20190610025353/https://www.tomshardware.com/news/amd-ryzen-pcie-4.0-motherboard,38401.html) from the original on 10 June 2019. Retrieved 10 June 2019.
76. Cutress, Dr. Ian (13 August 2020). "Tiger Lake IO and Power" (https://www.anandtech.com/show/15971/intels-11th-gen-core-tiger-lake-soc-detailed-superfin-willow-cove-and-xelp/5). *Anandtech*.
77. "1,2,3,4,5... It's Official, PCIe 5.0 is Announced | synopsys.com" (https://blogs.synopsys.com/expressyourself/2017/08/15/1-2-3-4-5-its-official-pcie-5-0-is-announced). *www.synopsys.com*. Retrieved 7 June 2017.
78. "PLDA Announces Availability of XpressRICH5™ PCIe 5.0 Controller IP | PLDA.com" (https://www.plda.com/plda-announces-availability-xpressrich5tm-pcie-50-controller-ip). *www.plda.com*. Retrieved 28 June 2018.
79. "XpressRICH5 for ASIC | PLDA.com" (https://www.plda.com/products/pcie-solutions-asicsoc/pcie-controller-ip/pcie-soft-ip/pcie-40-soft-ip/xpressrich5-asic). *www.plda.com*. Retrieved 28 June 2018.
80. "Doubling Bandwidth in Under Two Years: PCI Express® Base Specification Revision 5.0, Version 0.9 is Now Available to Members" (http://pcisig.com/doubling-bandwidth-under-two-years-pci-express®-base-specification-revision-50-version-09-now). *pcisig.com*. Retrieved 12 December 2018.
81. "PCIe 5.0 Is Ready For Prime Time" (https://www.tomshardware.com/news/pcie-4.0-5.0-pci-sig-specification,38460.html). *tomshardware.com*. 17 January 2019. Retrieved 18 January 2019.
82. "PCI-SIG® Achieves 32GT/s with New PCI Express® 5.0 Specification" (https://www.businesswire.com/news/home/20190529005766/en/PCI-SIG%C2%AE-Achieves-32GTs-with-New-PCI-Express%C2%AE-5.0-Specification). *www.businesswire.com*. 29 May 2019.
83. "PCI-Express 5.0: China stellt ersten Controller vor" (https://www.pcgameshardware.de/Mainboard-Hardware-154107/News/PCI-Express50-China-stellt-ersten-Controller-vor-1337072/). *PC Games Hardware*. 18 November 2019.
84. IBM's POWER10 Processor, Hot Chips 32, August 16–18, 2020 (https://hc32.hotchips.org/assets/program/conference/day1/HotChips2020_Server_Processors_IBM_Starke_POWER10_v33.pdf)
85. Power E1080 Enterprise server delivers a uniquely architected platform to help securely and efficiently scale core operational and AI applications in a hybrid cloud, IBM Europe Hardware Announcement ZG21-0059 (https://www.ibm.com/common/ssi/rep_ca/9/877/ENUSZG21-0059/index.html)
86. IBM Power E1080 Technical Overview and Introduction (http://www.redbooks.ibm.com/redpapers/pdfs/redp5649.pdf)
87. "Intel Unveils 12th Gen Intel Core, Launches World's Best Gaming" (https://www.intel.com/content/www/us/en/newsroom/news/12th-gen-core-processors.html). Intel.com. Retrieved 16 February 2022.
88. "NVIDIA Announces Hopper Architecture, the Next Generation of Accelerated Computing" (https://nvidianews.nvidia.com/news/nvidia-announces-hopper-architecture-the-next-generation-of-accelerated-computing).
89. "AMD Showcases Industry-Leading Gaming, Commercial, and Mainstream PC Technologies at COMPUTEX 2022" (https://www.amd.com/en/press-releases/2022-05-23-amd-showcases-growth-gaming-commercial-and-mainstream-mobile-and-industry). AMD.com. Retrieved 23 May 2022.
90. "PCI-SIG® Announces Upcoming PCI Express® 6.0 Specification to Reach 64 GT/s" (https://www.businesswire.com/news/home/20190618005945/en/PCI-SIG%C2%AE-Announces-Upcoming-PCI-Express%C2%AE-6.0-Specification-to-Reach-64-GTs). *www.businesswire.com*. 18 June 2019.
91. Smith, Ryan. "PCI Express Bandwidth to Be Doubled Again: PCIe 6.0 Announced, Spec to Land in 2021" (https://www.anandtech.com/show/14559/pci-express-bandwidth-to-be-doubled-again-pcie-60-announced-spec-to-land-in-2021). *www.anandtech.com*.
92. "PCI Express 6.0 Reaches Version 0.5 Ahead Of Finalization Next Year – Phoronix" (https://www.phoronix.com/scan.php?page=news_item&px=PCI-Express-6.0-v0.5). *www.phoronix.com*.
93. Shilov, Anton (4 November 2020). "PCIe 6.0 Specification Hits Milestone: Complete Draft Is Ready" (https://www.tomshardware.com/news/pcie-6-specification-hits-milestone-complete-draft-is-ready). *Tom's Hardware*.
94. Yanes, Al. "PCIe® 6.0 Specification, Version 0.9: One Step Closer to Final Release | PCI-SIG" (https://pcisig.com/blog/pcie®-60-specification-version-09-one-step-closer-final-release). *pcisig.com*. Retrieved 6 October 2021.
95. "PCI-SIG® Releases PCIe® 6.0 Specification Delivering Record Performance to Power Big Data Applications" (https://www.businesswire.com/news/home/20220111005011/en/PCI-SIG%C2%AE-Releases-PCIe%C2%AE-6.0-Specification-Delivering-Record-Performance-to-Power-Big-Data-Applications). Business Wire. 11 January 2022. Retrieved 16 February 2022.
96. "The Evolution of the PCI Express Specification: On its Sixth Generation, Third Decade and Still Going Strong" (https://pcisig.com/blog/evolution-pci-express-specification-its-sixth-generation-third-decade-and-still-going-strong). Pci-Sig. 11 January 2022. Retrieved 16 February 2022.
97. Debendra Das Sharma. "PCIe 6.0 Specification: The Interconnect for I/O Needs of the Future" (https://ghostarchive.org/varchive/youtube/20211030/jhehXwnu0Ss). PCI-SIG. p. 8. Archived from the original (https://www.youtube.com/watch?v=jhehXwnu0Ss) on 30 October 2021.
98. "Pushing the Envelope with PCIe 6.0: Bringing PAM4 to PCIe" (https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/ip/design-ip/pushing-the-envelope-with-pcie-6-wp.pdf) (PDF). Retrieved 16 February 2022.
99. "PowerPoint Presentation" (https://pcisig.com/sites/default/files/files/PCIe%206.0%20Webinar_Final_.pdf) (PDF). Retrieved 16 February 2022.
100. "PCI-SIG® Announces PCI Express® 7.0 Specification to Reach 128 GT/s" (https://www.businesswire.com/news/home/20220621005137/en). Business Wire. 21 June 2022. Retrieved 25 June 2022.

101. "PLX demo shows PCIe over fiber as data center clustering interconnect" (http://www.cablinginstall.com/index/display/article-display/8876181966/articles/cabling-installation-maintenance/news/data-center/2011/6/plx-demo_shows_pcie.html). *Cabling install*. Penn Well. Retrieved 29 August 2012.
102. "Introduced second generation PCI Express Gen 2 over fiber optic systems" (http://www.adnaco.com/2011/09/03/new1). Adnaco. 22 April 2011. Archived (https://web.archive.org/web/20121004094357/http://www.adnaco.com/2011/09/03/new1/) from the original on 4 October 2012. Retrieved 29 August 2012.
103. "PCIe Active Optical Cable System" (http://www.samtec.com/cable-systems/active-optics/active-optical-cable/pcie.aspx). Archived (https://web.archive.org/web/20141230122105/http://www.samtec.com/cable-systems/active-optics/active-optical-cable/pcie.aspx) from the original on 30 December 2014. Retrieved 23 October 2015.
104. IBM Power Systems E870 and E880 Technical Overview and Introduction (http://www.redbooks.ibm.com/redpapers/pdfs/redp5137.pdf)
105. "Acer, Asus to Bring Intel's Thunderbolt Speed Technology to Windows PCs" (https://www.pcworld.com/article/240013/acer_asus_to_bring_intels_thunderbolt_speed_technology_to_windows_pcs.html). *PC World*. 14 September 2011. Archived (https://web.archive.org/web/20120118190546/http://www.pcworld.com/article/240013/acer_asus_to_bring_intels_thunderbolt_speed_technology_to_windows_pcs.html) from the original on 18 January 2012. Retrieved 7 December 2012.
106. Kevin Parrish (28 June 2013). "PCIe for Mobile Launched; PCIe 3.1, 4.0 Specs Revealed" (http://www.tomshardware.com/news/M-PCIe-M.2-PCIe-3.1-PCIe-4.0-OCuLink,23259.html). *Tom's Hardware*. Retrieved 10 July 2014.
107. "PCI Express 4.0 Draft 0.7 & PIPE 4.4 Specifications – What Do They Mean to Designers? — Synopsys Technical Article | ChipEstimate.com" (https://www.chipestimate.com/PCI-Express-40-Draft-07-and-PIPE-44-Specifications-What-Do-They-Mean-to-Designers/Synopsys/Technical-Article/2017/02/21). *www.chipestimate.com*. Retrieved 28 June 2018.
108. "PCI Express 1x, 4x, 8x, 16x bus pinout and wiring @" (http://pinouts.ru/Slots/pci_express_pinout.shtml). RU: Pinouts. Archived (https://web.archive.org/web/20091125025800/http://pinouts.ru/Slots/pci_express_pinout.shtml) from the original on 25 November 2009. Retrieved 7 December 2009.
109. "PHY Interface for the PCI Express Architecture" (https://web.archive.org/web/20080317171752/http://download.intel.com/technology/pciexpress/devnet/docs/pipe2_00.pdf) (PDF) (version 2.00 ed.). Intel. Archived from the original (http://download.intel.com/technology/pciexpress/devnet/docs/pipe2_00.pdf) (PDF) on 17 March 2008. Retrieved 21 May 2008.
110. PCI Express System Architecture (https://www.mindshare.com/files/ebooks/PCI%20Express%20System%20Architecture.pdf)
111. PCI Express Architecture, intel.com (https://www.intel.ru/content/www/ru/ru/io/pci-express/pci-express-architecture-general.html)
112. "Mechanical Drawing for PCI Express Connector" (http://www.interfacebus.com/PCI-Express-Bus-PCIe-Description.html#d). Interface bus. Retrieved 7 December 2007.
113. "FCi schematic for PCIe connectors" (http://portal.fciconnect.com/Comergent/fci/drawing/10018783.pdf) (PDF). FCI connect. Retrieved 7 December 2007.
114. Reducing Interrupt Latency Through the Use of Message Signaled Interrupts (https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/msg-signaled-interrupts-paper.pdf)
115. *PCI EXPRESS BASE SPECIFICATION, REV. 3.0* Table 4-24
116. "Computer Peripherals And Interfaces" (https://www.google.com/books?id=Xp7-NKsJ8_sC&pg=PA35&dq=frequent+enforced+acknowledgements/). Technical Publications Pune. Archived (https://web.archive.org/web/20140225203956/http://www.google.com/books?id=Xp7-NKsJ8_sC&pg=PA35&dq=frequent+enforced+acknowledgements%2F) from the original on 25 February 2014. Retrieved 23 July 2009.
117. Lawley, Jason (28 October 2014). "Understanding Performance of PCI Express Systems" (https://www.xilinx.com/support/documentation/white_papers/wp350.pdf) (PDF). 1.2. Xilinx.
118. "NVIDIA Introduces NVIDIA Quadro® Plex – A Quantum Leap in Visual Computing" (http://www.nvidia.com/object/IO_34527.html). *Nvidia*. 1 August 2006. Archived (https://web.archive.org/web/20060824225752/http://www.nvidia.com/object/IO_34527.html) from the original on 24 August 2006. Retrieved 14 July 2018.
119. "Quadro Plex VCS – Advanced visualization and remote graphics" (http://www.nvidia.com/page/quadroplex.html). nVidia. Archived (https://web.archive.org/web/20110428042937/http://www.nvidia.com/page/quadroplex.html) from the original on 28 April 2011. Retrieved 11 September 2010.
120. "XGP" (https://web.archive.org/web/20100129170434/http://ati.amd.com/technology/xgp/). *ATI*. AMD. Archived from the original (http://ati.amd.com/technology/xgp/) on 29 January 2010. Retrieved 11 September 2010.
121. *Fujitsu-Siemens Amilo GraphicBooster External Laptop GPU Released* (http://www.ubergizmo.com/2008/12/fujitsu-siemens-amilo-graphicbooster-external-laptop-gpu-released/), 3 December 2008, archived (https://web.archive.org/web/20151016192734/http://www.ubergizmo.com/2008/12/fujitsu-siemens-amilo-graphicbooster-external-laptop-gpu-released/) from the original on 16 October 2015, retrieved 9 August 2015
122. *DynaVivid Graphics Dock from Acer arrives in France, what about the US?* (http://www.ubergizmo.com/2010/08/dynavivid-graphics-dock-from-acer-arrives-in-france-what-about-the-us/), 11 August 2010, archived (https://web.archive.org/web/20151016192734/http://www.ubergizmo.com/2010/08/dynavivid-graphics-dock-from-acer-arrives-in-france-what-about-the-us/) from the original on 16 October 2015, retrieved 9 August 2015
123. Dougherty, Steve (22 May 2010), "MSI to showcase 'GUS' external graphics solution for laptops at Computex" (https://www.tweaktown.com/news/15382/msi_to_showcase_gus_external_graphics_solution_for_laptops_at_computex/), *TweakTown*
124. Hellstrom, Jerry (9 August 2011), "ExpressCard trying to pull a (not so) fast one?" (http://www.pcper.com/news/Editorial/ExpressCard-trying-pull-not-so-fast-one), *PC Perspective* (editorial), archived (https://web.archive.org/web/20160201160254/http://www.pcper.com/news/Editorial/ExpressCard-trying-pull-not-so-fast-one) from the original on 1 February 2016

125. "PE4H V3.2 (PCIe x16 Adapter)" (http://www.hwtools.net/Adapter/PE4H%20V3.2.html). Hwtools.net. Archived (https://web.archive.org/web/20140214012341/http://www.hwtools.net/Adapter/PE4H%20V3.2.html) from the original on 14 February 2014. Retrieved 5 February 2014.
126. O'Brien, Kevin (8 September 2010), "How to Upgrade Your Notebook Graphics Card Using DIY ViDOCK" (http://www.notebookreview.com/default.asp?newsID=5846&review=how+to+upgrade+laptop+graphics+notebook), *Notebook review*, archived (https://web.archive.org/web/20131213054647/http://www.notebookreview.com/default.asp?newsID=5846&review=how+to+upgrade+laptop+graphics+notebook) from the original on 13 December 2013
127. Lal Shimpi, Anand (7 September 2011), "The Thunderbolt Devices Trickle In: Magma's ExpressBox 3T" (http://www.anandtech.com/show/4743/the-thunderbolt-devices-trickle-in-magmas-expressbox-3t), *AnandTech*, archived (https://web.archive.org/web/20160304201352/http://www.anandtech.com/show/4743/the-thunderbolt-devices-trickle-in-magmas-expressbox-3t) from the original on 4 March 2016
128. "MSI GUS II external GPU enclosure with Thunderbolt" (https://www.theverge.com/2012/1/10/2698168/msi-GUS-II-external-thunderbolt-gpu-enclosure). *The Verge* (hands-on). 10 January 2012. Archived (https://web.archive.org/web/20120213123659/http://www.theverge.com/2012/1/10/2698168/msi-GUS-II-external-thunderbolt-gpu-enclosure) from the original on 13 February 2012. Retrieved 12 February 2012.
129. "PCI express graphics, Thunderbolt" (http://www.tomshardware.com/reviews/pci-express-graphics-thunderbolt,3263-2.html), *Tom's hardware*, 17 September 2012
130. "M logics M link Thunderbold chassis no shipping" (https://www.engadget.com/2012/12/13/mlogics-mlink-thunderbolt-chassis-now-shipping-399/), *Engadget*, 13 December 2012, archived (https://web.archive.org/web/20170625182008/https://www.engadget.com/2012/12/13/mlogics-mlink-thunderbolt-chassis-now-shipping-399/) from the original on 25 June 2017
131. Burns, Chris (17 October 2017), "2017 Razer Blade Stealth and Core V2 detailed" (https://www.slashgear.com/2017-razer-blade-stealth-and-core-v2-detailed-17504328/), *SlashGear*, archived (https://web.archive.org/web/20171017211631/https://www.slashgear.com/2017-razer-blade-stealth-and-core-v2-detailed-17504328/) from the original on 17 October 2017
132. "CompactFlash Association readies next-gen XQD format, promises write speeds of 125 MB/s and up" (https://www.engadget.com/2011/12/08/compactflash-association-readies-next-gen-xqd-format-promises-w/). Engadget. 8 December 2011. Archived (https://web.archive.org/web/20140519002107/http://www.engadget.com/2011/12/08/compactflash-association-readies-next-gen-xqd-format-promises-w/) from the original on 19 May 2014. Retrieved 18 May 2014.
133. Zsolt Kerekes (December 2011). "What's so very different about the design of Fusion-io's ioDrives / PCIe SSDs?" (http://www.storagesearch.com/ssd-29.html). storagesearch.com. Archived (https://web.archive.org/web/20130923065816/http://www.storagesearch.com/ssd-29.html) from the original on 23 September 2013. Retrieved 2 October 2013.
134. "Fusion-io ioDrive Duo Enterprise PCIe Review" (https://web.archive.org/web/20131004230049/http://www.storagereview.com/fusionio_iodrive_duo_enterprise_pcie_review). storagereview.com. 16 July 2012. Archived from the original (http://www.storagereview.com/fusionio_iodrive_duo_enterprise_pcie_review) on 4 October 2013. Retrieved 2 October 2013.
135. "OCZ Demos 4 TiB, 16 TiB Solid-State Drives for Enterprise" (https://web.archive.org/web/20130325121004/http://www.xbitlabs.com/news/storage/display/20120110180208_OCZ_Demos_4TB_16TB_Solid_State_Drives_for_Enterprise.html). X-bit labs. Archived from the original (http://www.xbitlabs.com/news/storage/display/20120110180208_OCZ_Demos_4TB_16TB_Solid_State_Drives_for_Enterprise.html) on 25 March 2013. Retrieved 7 December 2012.
136. "Enabling Higher Speed Storage Applications with SATA Express" (http://www.sata-io.org/technology/sataexpress.asp). SATA-IO. Archived (https://web.archive.org/web/20121127010238/http://www.sata-io.org/technology/sataexpress.asp) from the original on 27 November 2012. Retrieved 7 December 2012.
137. "SATA M.2 Card" (https://www.sata-io.org/sata-m2-card). SATA-IO. Archived (https://web.archive.org/web/20131003103042/https://www.sata-io.org/sata-m2-card) from the original on 3 October 2013. Retrieved 14 September 2013.
138. "SCSI Express" (https://web.archive.org/web/20130127094133/http://www.scsita.org/library/scsi-express/). SCSI Trade Association. Archived from the original (http://www.scsita.org/library/scsi-express/) on 27 January 2013. Retrieved 27 December 2012.
139. Meduri, Vijay (24 January 2011). "A Case for PCI Express as a High-Performance Cluster Interconnect" (http://www.hpcwire.com/hpcwire/2011-01-24/a_case_for_pci_express_as_a_high-performance_cluster_interconnect.html). HPCwire. Archived (https://web.archive.org/web/20130114041356/http://www.hpcwire.com/hpcwire/2011-01-24/a_case_for_pci_express_as_a_high-performance_cluster_interconnect.html) from the original on 14 January 2013. Retrieved 7 December 2012.
140. Evan Koblentz (3 February 2017). "New PCI Express 4.0 delay may empower next-gen alternatives" (https://www.techrepublic.com/article/new-pci-express-4-0-delay-may-empower-next-gen-alternatives/). *Tech Republic*. Archived (https://web.archive.org/web/20170401143837/http://www.techrepublic.com/article/new-pci-express-4-0-delay-may-empower-next-gen-alternatives/) from the original on 1 April 2017. Retrieved 31 March 2017.
141. Cutress, Ian. "CXL Specification 1.0 Released: New Industry High-Speed Interconnect From Intel" (https://www.anandtech.com/show/14068/cxl-specification-1-released-new-industry-high-speed-interconnect-from-intel). *www.anandtech.com*. Retrieved 9 August 2019.
142. "Integrators List | PCI-SIG" (http://pcisig.com/developers/integrators-list). *pcisig.com*. Retrieved 27 March 2019.

Further reading

- Budruk, Ravi; Anderson, Don; Shanley, Tom (2003), Winkles, Joseph 'Joe' (ed.), *PCI Express System Architecture*, Mind share PC system architecture, Addison-Wesley, ISBN 978-0-321-15630-3, 1120 pp.
- Solari, Edward; Congdon, Brad (2003), *Complete PCI Express Reference: Design Implications for Hardware and Software Developers*, Intel, ISBN 978-0-9717861-9-6, 1056 pp.

- Wilen, Adam; Schade, Justin P; Thornburg, Ron (April 2003), *Introduction to PCI Express: A Hardware and Software Developer's Guide*, Intel, ISBN 978-0-9702846-9-3, 325 pp.

External links

- Media related to PCIe at Wikimedia Commons
- PCI-SIG Specifications (https://pcisig.com/specifications)