Advanced Microcontroller Bus Architecture

The ARM **Advanced Microcontroller Bus Architecture** (**AMBA**) is an open-standard, on-chip interconnect specification for the connection and management of functional blocks in system-on-a-chip (SoC) designs. It facilitates development of multi-processor designs with large numbers of controllers and components with a bus architecture. Since its inception, the scope of AMBA has, despite its name, gone far beyond microcontroller devices. Today, AMBA is widely used on a range of ASIC and SoC parts including applications processors used in modern portable mobile devices like smartphones. AMBA is a registered trademark of ARM Ltd.[1]

AMBA was introduced by ARM in 1996. The first AMBA buses were the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). In its second version, AMBA 2 in 1999, ARM added AMBA High-performance Bus (AHB) that is a single clock-edge protocol. In 2003, ARM introduced the third generation, AMBA 3, including Advanced eXtensible Interface (AXI) to reach even higher performance interconnect and the Advanced Trace Bus (ATB) as part of the CoreSight on-chip debug and trace solution. In 2010 the AMBA 4 specifications were introduced starting with AMBA 4 AXI4, then in 2011[2] extending system-wide coherency with AMBA 4 AXI Coherency Extensions (ACE). In 2013[3] the AMBA 5 Coherent Hub Interface (CHI) specification was introduced, with a re-designed high-speed transport layer and features designed to reduce congestion. These protocols are today the de facto standard for embedded processor bus architectures because they are well documented and can be used without royalties.

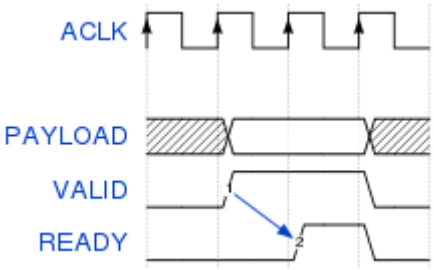
Contents

Design principles

An important aspect of an SoC is not only which components or blocks it houses, but also how they interconnect. AMBA is a solution for the blocks to interface with each other.

The objective of the AMBA specification is to:

- facilitate *right-first-time* development of embedded microcontroller products with one or more CPUs, GPUs or signal processors,
- be technology independent, to allow reuse of IP cores, peripheral and system macrocells across diverse IC processes,
- encourage modular system design to improve processor independence, and the development of reusable peripheral and system IP libraries
- minimize silicon infrastructure while supporting high performance and low power on-chip communication.



AMBA AXI handshake

AMBA protocol specifications

The AMBA specification defines an on-chip communications standard for designing high-performance embedded microcontrollers. It is supported by ARM Limited with wide cross-industry participation.

The *AMBA 5 specification* defines the following buses/interfaces:

- AXI5, AXI5-Lite and ACE5 Protocol Specification
- Advanced High-performance Bus (AHB5, AHB-Lite)
- Coherent Hub Interface (CHI) [3]
- Distributed Translation Interface (DTI)
- Generic Flash Bus (GFB)

The *AMBA 4 specification* defines following buses/interfaces:

- AXI Coherency Extensions (ACE) - widely used on the latest ARM Cortex-A processors including Cortex-A7 and Cortex-A15
- AXI Coherency Extensions Lite (ACE-Lite)
- Advanced Extensible Interface 4 (AXI4)
- Advanced Extensible Interface 4 Lite (AXI4-Lite)
- Advanced Extensible Interface 4 Stream (AXI4-Stream v1.0)
- Advanced Trace Bus (ATB v1.1)
- Advanced Peripheral Bus (APB4 v2.0)
- AMBA Low Power Interfaces (Q-Channel and P-Channel)

AMBA 3 specification defines four buses/interfaces:

- Advanced eXtensible Interface (AXI3 or AXI v1.0) - widely used on ARM Cortex-A processors including Cortex-A9
- Advanced High-performance Bus Lite (AHB-Lite v1.0)
- Advanced Peripheral Bus (APB3 v1.0)
- Advanced Trace Bus (ATB v1.0)

AMBA 2 specification defines three buses/interfaces:

- Advanced High-performance Bus (AHB) - widely used on ARM7, ARM9 and ARM Cortex-M based designs
- Advanced System Bus (ASB)

- Advanced Peripheral Bus (APB2 or APB)

AMBA specification (First version) defines two buses/interfaces:

- Advanced System Bus (ASB)
- Advanced Peripheral Bus (APB)

The timing aspects and the voltage levels on the bus are not dictated by the specifications.

AXI Coherency Extensions (ACE and ACE-Lite)

ACE, defined as part of the AMBA 4 specification, extends AXI with additional signalling introducing system wide coherency.[4] This system coherency allows multiple processors to share memory and enables technology like ARM's big.LITTLE processing. The **ACE-Lite** protocol enables one-way coherency, also known as I/O coherency; for example, a network interface that can read from the caches of a fully coherent ACE processor.

Advanced eXtensible Interface (AXI)

AXI, the third generation of AMBA interface defined in the AMBA 3 specification, is targeted at high performance, high clock frequency system designs and includes features that make it suitable for high speed sub-micrometer interconnect:

- separate address/control and data phases
- support for unaligned data transfers using byte strobes
- burst based transactions with only start address issued
- issuing of multiple outstanding addresses with out of order responses
- easy addition of register stages to provide timing closure.

Advanced High-performance Bus (AHB)

AHB is a bus protocol introduced in Advanced Microcontroller Bus Architecture version 2 published by ARM Ltd company.

In addition to previous release, it has the following features:

- large bus-widths (64/128/256/512/1024 bit).

A simple transaction on the AHB consists of an address phase and a subsequent data phase (without wait states: only two bus-cycles). Access to the target device is controlled through a MUX (non-tristate), thereby admitting bus-access to one bus-master at a time.

AHB-Lite is a subset of AHB formally defined in the AMBA 3 standard. This subset simplifies the design for a bus with a single master.

Advanced Peripheral Bus (APB)

APB is designed for low bandwidth control accesses, for example register interfaces on system peripherals. This bus has an address and data phase similar to AHB, but a much reduced, low complexity signal list (for example no bursts). Furthermore, it is an interface designed for a low frequency system with a low bit width (32 bits).

AMBA products

A family of synthesizable intellectual property (IP) cores *AMBA Products* is licensable from ARM Limited that implement a digital bus in an SoC for the efficient moving and storing of data using the AMBA protocol specifications. The AMBA family includes AMBA Network Interconnect (CoreLink NIC-400), Cache Coherent Interconnect (CoreLink CCI-500), SDRAM memory controllers (CoreLink DMC-400), DMA controllers (CoreLink DMA-230, DMA-330), level 2 cache controllers (L2C-310), etc.

A number of manufacturers utilize AMBA buses for non-ARM designs. As an example Infineon uses an AMBA bus for the ADM5120 SoC based on the MIPS architecture.

Competitors

- Wishbone from OpenCores – Free and open bus architecture (formerly from Silicore)
- CoreConnect bus technology from IBM, used in IBM's embedded PowerPC, but also in many other SoC-like systems with the Xilinx MicroBlaze or similar cores
- IPBus by IDT
- Avalon – proprietary bus system by Altera for use in their Nios II SoCs[5]
- Open Core Protocol (OCP) from Accellera
- HyperTransport (HT) from AMD (though this is an off-chip interface, not on-chip bus)
- QuickPath Interconnect (QPI) by Intel (though this is an off-chip interface, not on-chip bus)
- virtual share from PICC - free and open source
- TileLink - Free and open bus architecture from CHIPS Alliance[6]

See also

- Functional specification
- Master/slave (technology)
- Network on a chip, an alternative to bus-based architectures

References

1. AMBA Trademark License, http://arm.com/about/trademarks/arm-trademark-list/AMBA-trademark.php
2. New AMBA 4 Specification Optimizes Coherency for Heterogeneous Multicore SoCs, https://www.arm.com/new-amba-4-specification-optimizes-coherency-for-heterogeneous-multicore-socs.php
3. ARM Announces AMBA 5 CHI Specification to Enable High Performance, Highly Scalable System on Chip Technology, http://www.arm.com/about/newsroom/arm-announces-amba-5-chi-specification-to-enable-high-performance-highly-scalable-system-on-chip.php
4. Kriouile, A., & Serwe, W. (2013). Formal Analysis of the ACE Specification for Cache Coherent Systems-on-Chip. In Formal Methods for Industrial Critical Systems (pp. 108-122). Springer Berlin Heidelberg., ISBN 978-3-642-41010-9

5. Avalon (http://www.altera.com/literature/manual/mnl_avalon_spec.pdf)
6. "Chips Alliance" (https://chipsalliance.org/author/chipsalliance/). *Chips Alliance*. Retrieved 2020-06-21.

External links

- Arm Developer AMBA Homepage (https://developer.arm.com/architectures/system-architectures/amba) - from Arm
- AMBA Specification home page (http://www.arm.com/products/system-ip/amba/amba-open-specifications.php) - of ARM
- AMBA (https://web.archive.org/web/20130213024919/http://www.arm.com/products/system-ip/amba/index.php) of ARM
- AMBA Documentation (http://infocenter.arm.com/help/topic/com.arm.doc.set.amba/index.html) - from ARM
  - AMBA 2 Specification including AHB (http://infocenter.arm.com/help/topic/com.arm.doc.ihi0011a/index.html) - from ARM
  - AMBA AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite (http://infocenter.arm.com/help/topic/com.arm.doc.ihi0022d/index.html) - from ARM
  - AMBA APB Specification including APB4, APB3, APB2 (http://infocenter.arm.com/help/topic/com.arm.doc.ihi0024c/index.html) - from ARM
