

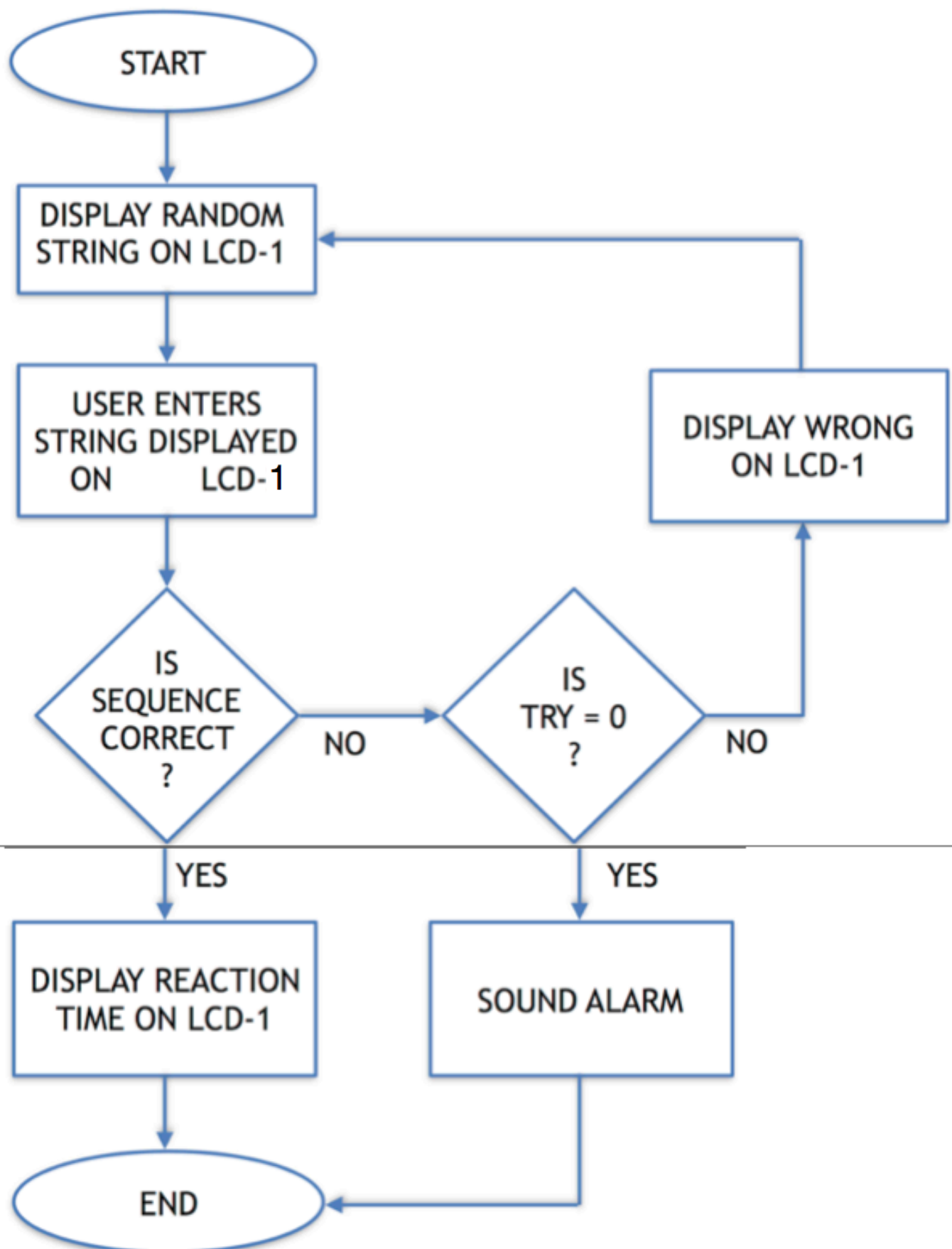
# **Microprocessors and Interfacing (EEE/INSTR/CS F241) Spirit Level Tester**

**Project Number — 22  
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**Saurav Narula — 2014B4A3814P  
Jai Agarwal — 2014B4A7428P  
Saniket More — 2014B4A7515P  
Govind Mittal — 2014B4A7530P**

## FLOW CHART



## **Hardware Used**

- 1 - 8086 - Microprocessor
- 2 - 6116 - 2 kB RAM
- 2 - 2732 - 4 kB ROM
- 1 - LCD
- 1 - 555(Timer/Oscillator)
- 1 - 74154 - 4:16 Decoder
- 2 - 74LS138 - 3:8 decoder for selecting memory(even/odd)
- 4 - 74LS373 - Octal Latch
- 4 - 74LS245 - Octal Bus Transceivers
- Matrix Hex Keyboard
- 2 - 8255 —To interface timer and the keypad
- 7 - OR gates
- 1 - Buzzer

## Memory mapping

The model uses 4k of RAM and 8k of ROM. Both the ROM and RAM are divided into even and odd banks, thus enabling copy of 16-bit of data in one cycle.

Read Only Memory(ROM):—

1. Even bank starting Address — 00000h
2. Even bank ending Address — 01FFEh
3. Odd bank starting address — 00001h
4. Odd bank ending address — 01FFFh

Random Access Memory(RAM):—

1. Even bank starting address — 02000h
2. Even bank ending address — 02FFEh
3. Odd bank starting address — 02001h
4. Odd bank ending address — 02FFFh

Chip	E/O	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	ADD
ROM	Even	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00000h
	Odd	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	01FFFh
RAM	Even	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	02000h
	Odd	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	02FFFh

## I/O Interfacing:

I/O Chip	A7	A6	A5	A4	A3	A2	A1	A0	Address
8255-1	0	0	0	1	0	0	0	0	10h
8255-1	0	0	0	1	0	1	1	0	16h
8255-2	0	0	1	0	0	0	0	0	20h
8255-2	0	0	1	0	0	1	1	0	26h

# Assumptions

- Pseudo random numbers are generated with a cycle of 19683 and hence, in this condition, supposed to be fairly random
- Software delays are producing the same amount of delay as hardware delay.
- Buzzer is turned on in the beginning to test whether it is functioning.
- The relay we use can be driven by any voltage output from the 8255A pins.
- Simulation time is not very slow as compared to real time.
- All the port driven i/o devices are working with any voltage output from the 8255A pins